Project Report: Design of 4-bit Array Multiplier in 45nm Technology

1. Introduction:

This report details the design and implementation of a 4-bit Array Multiplier using the Cadence Virtuoso custom integrated circuit (IC) design environment, targeting the 45nm Complementary Metal-Oxide-Semiconductor (CMOS) technology node. The primary objective was to design a functional, high-performance, and power-efficient digital arithmetic block suitable for inclusion in larger System-on-Chip (SoC) architectures.

1.1 Project Goal

To successfully design, simulate, and characterize a bit array multiplier, meeting functional specifications and achieving optimal power performance in the 45nm technology process.

1.2 Multiplier Architecture: The Array Multiplier

The Array Multiplier was chosen for its regular, structured layout, which is highly advantageous for custom VLSI design and synthesis. It performs multiplication by generating partial products and then summing them in a structured array of Full Adders (FA). For a multiplication, this results in an 8-bit product.

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2. Design Methodology and Implementation

The design was executed using a top-down approach within the Cadence Virtuoso environment.

2.1 Technology and Toolset

- Technology Node: 45nm CMOS Technology.
- Design Tool: Cadence Virtuoso Suite (Schematic Editor, Spectre Simulator)
- Design Level: Transistor-level and Gate-level implementation.

2.2 Design Flow

1. Cell Library Design: Fundamental cells (Inverter, OR gate, AND gate, XOR gate, Full Adder) were designed and characterized at the transistor level for optimized speed and area in the 45nm process.
2. Schematic Capture: The Array Multiplier was built hierarchically by instantiating the FA cells in the required array structure (typically a array of AND gates and a matrix of adders).
3. Simulation and Verification (Functional): Extensive functional verification was performed using the Spectre simulator to ensure correct operation across all possible 4-bit input combinations.
4. Power Analysis: Power simulations were conducted under worst-case switching scenarios to determine maximum power consumption.

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3. Implementation:

3.1 Designing of Blocks:

3.1.1 Inverter:

The inverter is the most fundamental logic gate, acting as a NOT function. It takes one input and produces the opposite logical output. The schematic of Inverter is given in Fig.1.

- Function: If the input (A) is logic 1 (High, VDD), the output (Y) is logic 0 (Low, Ground), and vice-versa.

- CMOS Implementation: It consists of a PMOS (Pull-Up Network) and an NMOS (Pull-Down Network) transistor connected in series between and Ground, with their gates tied together as the input.
- Sizing (120nm Width): Setting the width (W) for both the NMOS and PMOS to 120nm (with a minimum feature length, L, typically 45nm) dictates the drive strength. For a standard CMOS inverter, the PMOS width is often made 2-3 times larger than the NMOS width to equalize the pull-up and pull-down currents, as electrons (in NMOS) generally move faster than holes (in PMOS). A configuration usually results in a slower rise time.

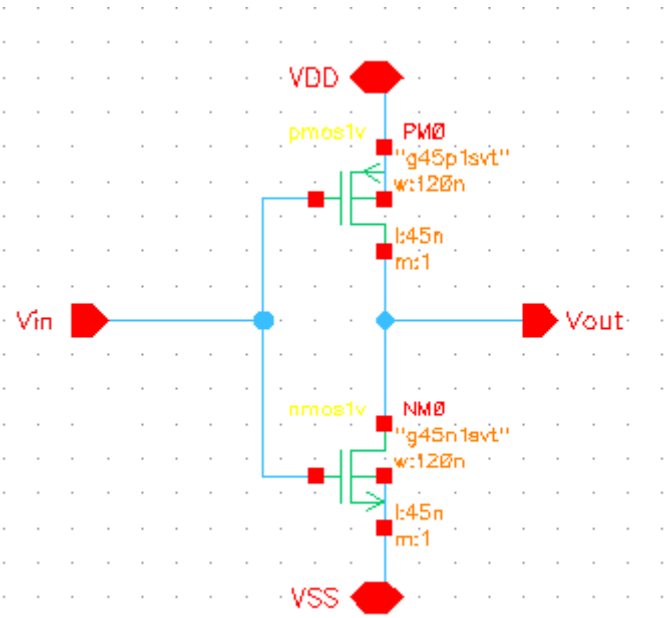

Fig. 1: Inverter Schematic

- Functional Simulation: Functional simulation for the designed block was successfully performed using the ADE L environment in Cadence Virtuoso to verify the circuit's logical correctness across all input combinations. The waveform is shown in Fig.2.

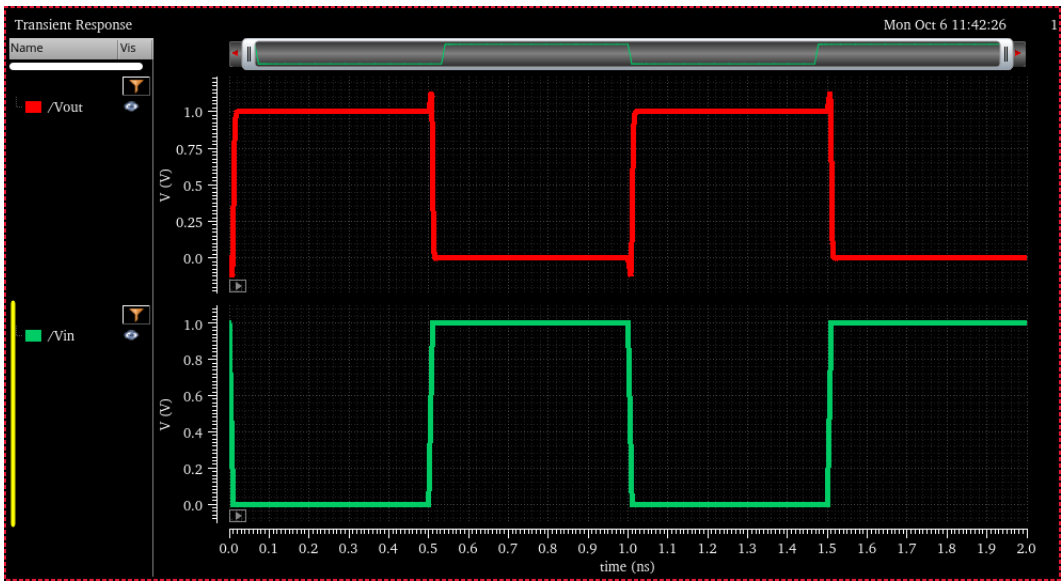

Fig. 2: Inverter Waveform

3.1.2 OR Gate:

The OR gate is a basic logic gate that performs logical disjunction. The Schematic of OR gate is given in Fig.3.

- Function: Y=A+B. The output (Y) is logic 1 (High) if at least one of the inputs (A or B) is logic 1. The output is 0 only if all inputs are 0.
- CMOS Implementation: It uses a series connection of PMOS transistors in the Pull-Up Network (PUN) and a parallel connection of NMOS transistors in the Pull-Down Network (PDN).
- Functional Simulation: Functional simulation for the designed block was successfully performed using the ADE L environment in Cadence Virtuoso to verify the circuit's logical correctness across all input combinations. The waveform is shown in Fig.4.

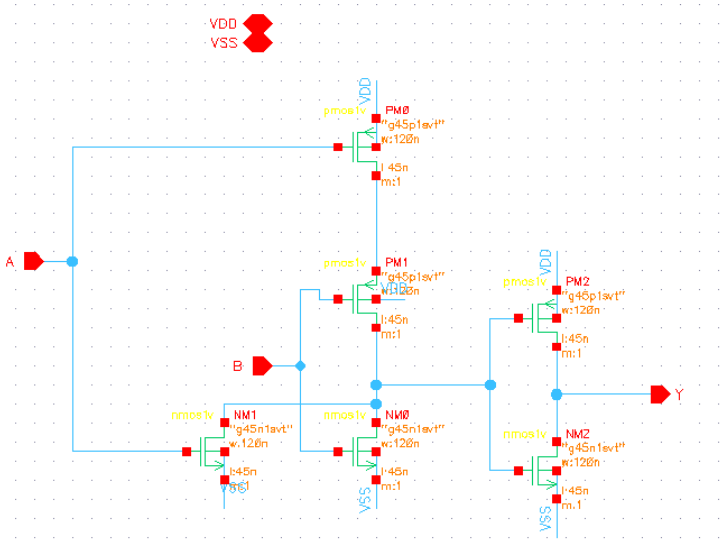

Fig. 3: OR Gate Schematic

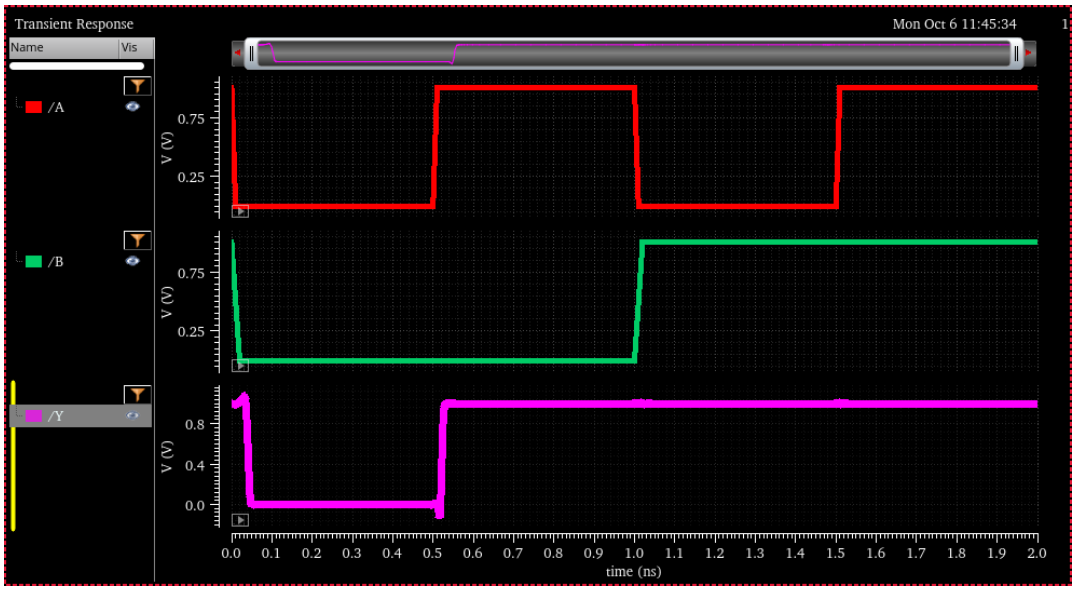

Fig. 4: OR Gate Waveform

3.1.3 AND Gate:

The AND gate is a basic logic gate that performs logical conjunction. The schematic is given in Fig.5.

- Function: Y=A·B. The output (Y) is logic 1 (High) only if all inputs (A and B) are logic 1. If any input is 0, the output is 0.
- CMOS Implementation: It uses a parallel connection of PMOS transistors in the Pull-Up Network (PUN) and a series connection of NMOS transistors in the Pull-Down Network (PDN).

- Functional Simulation: Functional simulation for the designed block was successfully performed using the ADE L environment in Cadence Virtuoso to verify the circuit's logical correctness across all input combinations. The waveform is shown in Fig.6.

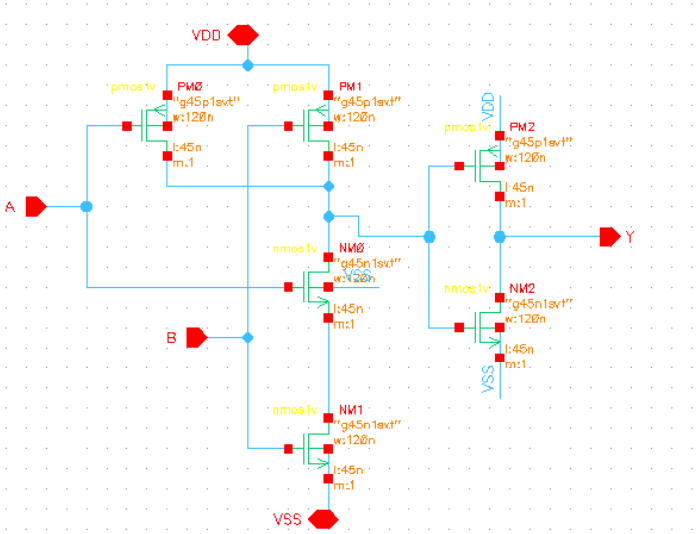

Fig. 5: AND Gate Schematic

Fig. 6: AND Gate Waveform

3.1.4 Full Adder:

The Full Adder is a fundamental arithmetic building block that adds three single-bit binary inputs, accounting for a carry-in from a less significant stage. The schematic is shown in Fig. 7.

- Inputs (3): Two data bits (**A** and **B**) and a Carry-In (**C**).
- Outputs (2): A Sum bit (**Sum**) and a Carry-Out bit (**Carry**).
- Equations:

  Sum = A^B^C;

  Carry = (A&B)+(C&(A^B));

- Functional Simulation: Functional simulation for the designed block was successfully performed using the ADE L environment in Cadence Virtuoso to verify the circuit's logical correctness across all input combinations. The waveform is shown in Fig.8.

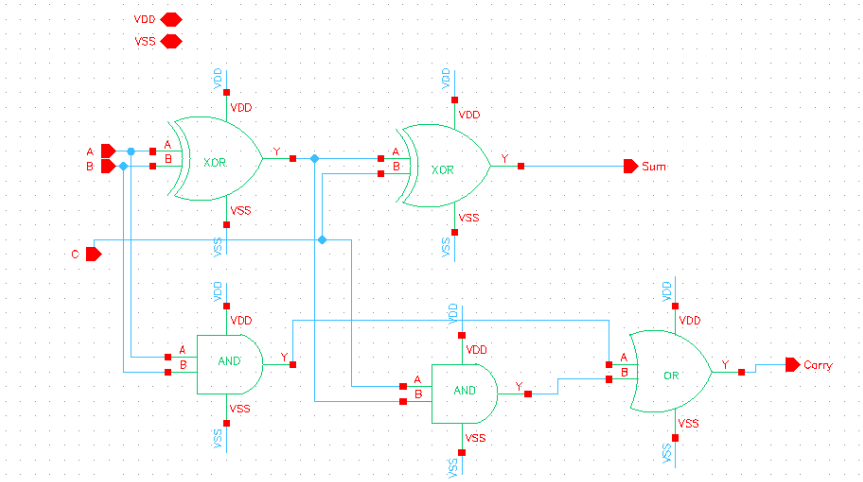

Fig. 7: Full Adder Schematic

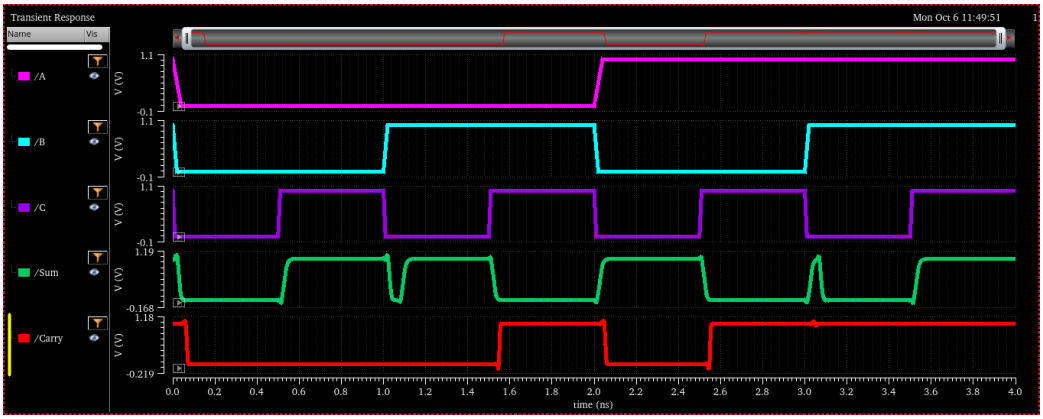

Fig. 8: Full Adder Waveform

3.2 Designing of 4-bit Array Multiplier:

The 4-bit array multiplier is a digital circuit designed to multiply two 4-bit binary numbers (**A3A2A1A0** and **B3B2B1B0**) to produce an 8-bit product (**S7…S0**).

- Architecture: It uses a highly regular, rectangular array structure of logic gates. The schematic is shown in Fig. 9.
    - Partial Product Generation: The first stage uses AND gates to calculate all partial products.
    - Partial Product Summation: The second stage uses an array of Full Adders (FA) arranged diagonally to sum the partial products.

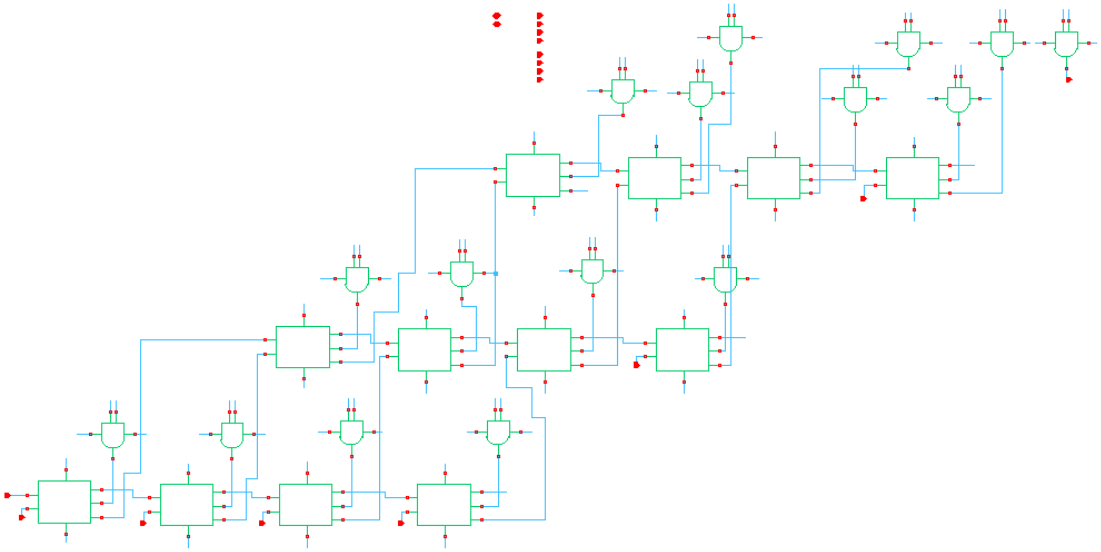

Fig. 9: Schematic of 4-bit Array Multiplier

3.3 Verifying the Multiplier block: Functional simulation for the designed block was successfully performed using the ADE L environment in Cadence Virtuoso to verify the circuit's logical correctness across all input combinations. The waveform is shown in Fig.10.

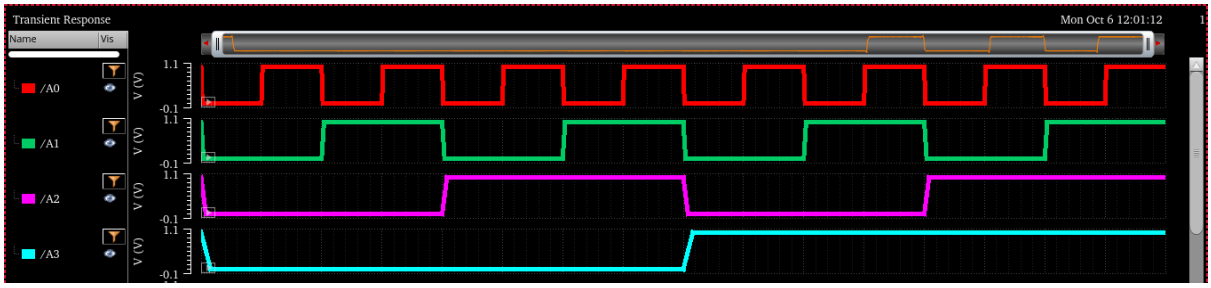

Fig. 10(a): A-input Waveform

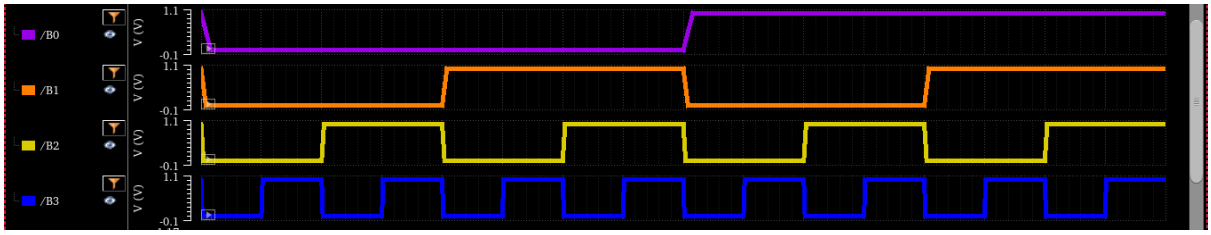

Fig. 10(b): B-input Waveform

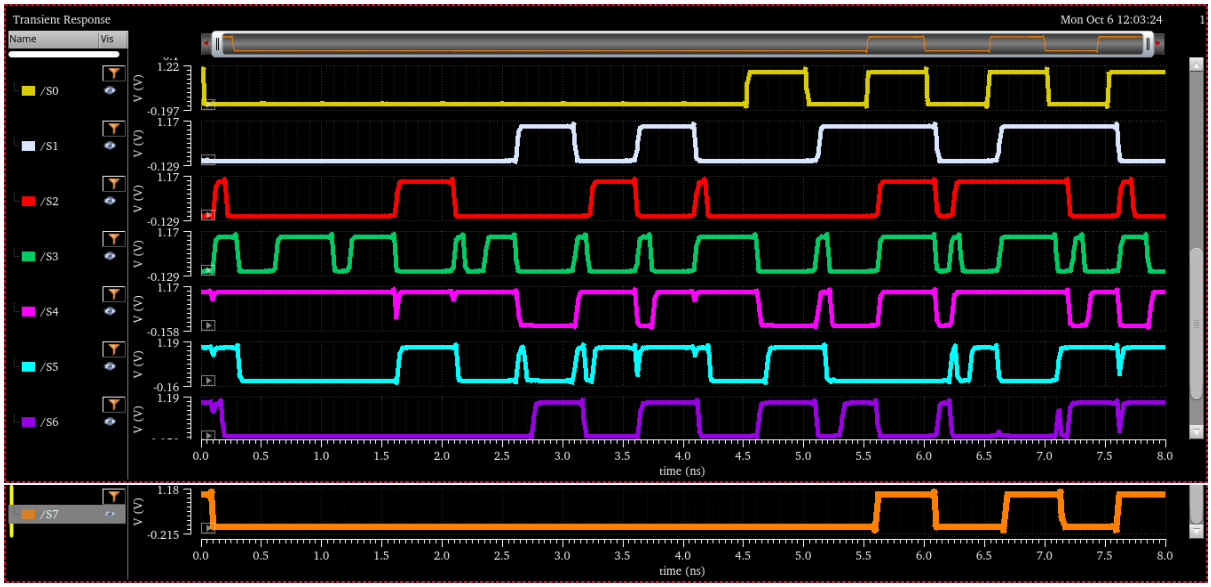

Fig. 10(c): Output Waveforms

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4. Results:

The final design met all functional requirements. Key performance metrics were extracted from the simulation results:

Parameter	Value
Maximum Power Consumption (Pmax)	8.893µW
Operating Voltage (VDD)	1V

The achieved maximum power consumption of 8.893µW demonstrates the efficiency gained from using the advanced 45nm technology, which is critical for mobile and battery-operated applications.

5. Conclusion:

The design and characterization of the 4-Bit Array Multiplier in 45nm CMOS technology using Cadence Virtuoso were successfully completed. The project confirmed the full functionality of the array architecture and achieved a highly competitive maximum power consumption of 8.893µW. This result validates the design methodology and demonstrates the feasibility of implementing low-power arithmetic blocks critical for modern deep submicron IC design.