BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT

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DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

Academic Year 2022-23

REPORT

On

"4 – BIT COMPARATOR"

Submitted By

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1BY20ET048	S VARSHA	
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Signature of faculty		

Course: Verilog HDL

Course Code: 18EC56

Under the guidance of

Prof. Saritha I G

Assistant Professor

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AIM:

Write Verilog code to simulate a 4 – bit comparator.

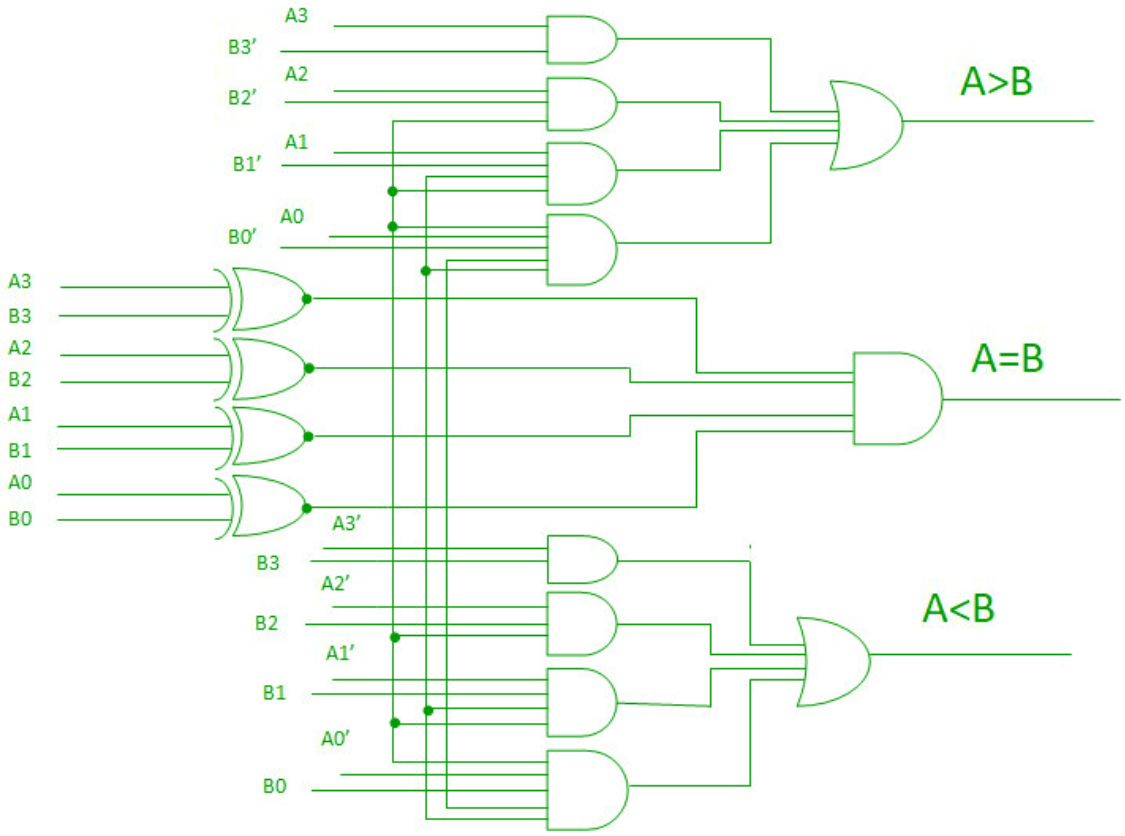
THEORY:

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers to find out whether one binary number is equal, less than, or greater than the other binary number.

A circuit is designed for which we will have two inputs one for A and the other for B and have three output terminals, one for A > B condition, one for A = B condition, and one for A < B condition.

A comparator used to compare two binary numbers each of four bits is called a 4-bit magnitude comparator. It consists of eight inputs each for two four-bit numbers and three outputs to generate less than, equal to, and greater than between two binary numbers.

LOGIC DIAGRAM:



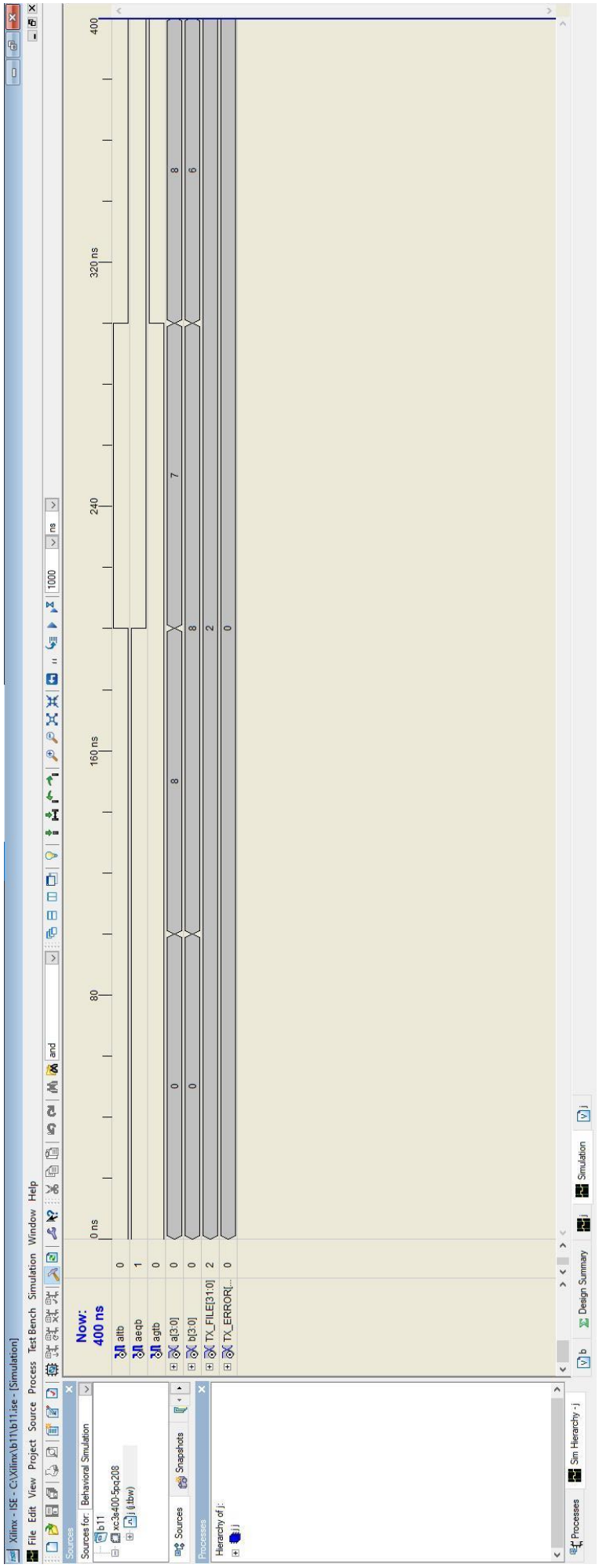
TRUTH TABLE:

Inputs		Comparator output		
a	**b**	**agtb**	**aeqb**	**altb**
1000	1000	0	1	0
0111	1000	0	0	1
1000	0110	1	0	0

VERILOG CODE:

```
module comp(a,b,aeqb,agtb,altb);
input [3:0] a,b;
output aeqb,agtb,altb;
reg aeqb,agtb,altb;
always @(a ,b)
begin
aeqb=0;
agtb=0;
altb=0;
if(a==b)   //checking for equality condition
aeqb=1;
else if (a>b) // checking greater than condition
agtb=1;
else
altb=1;
end
endmodule
```

OUTPUT:



RESULT:

4 – bit comparator is simulated and verified using Verilog.