



GITAM

(DEEMED TO BE UNIVERSITY)

TITLE:PCB REPORT

Subtitle:DIGITAL CIRCUIT

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SIMULATION RESULTS:

8x1 Multiplexer

An 8x1 multiplexer selects one of 8 input lines and outputs it. It has 3 selection lines (S_2, S_1, S_0) and 8 input lines ($I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$).

Truth Table

S₂	S₁	S₀	Outpu
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1	0		t
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0	0	0	I₀
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0	0	1	I₁
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0	1	0	I₂
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0	1	1	I₃
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1	0	0	I₄
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1	0	1	I₅
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1	1	0	I₆
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1	1	1	I₇
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Simulation Results

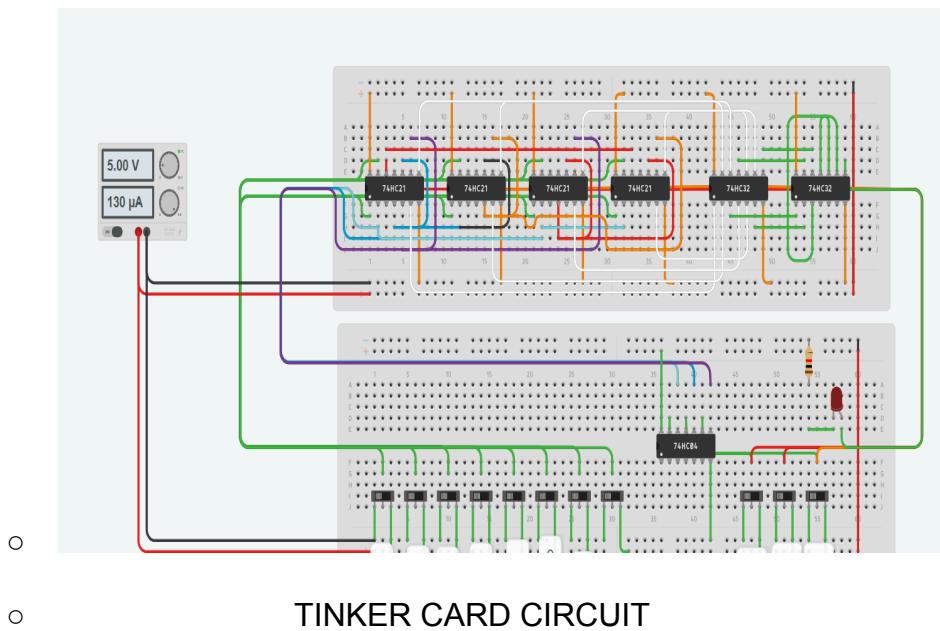
Let's simulate the multiplexer with some example inputs.

Inputs:

- $I_0=1|I_0 = 1|I_0=1$
- $I_1=0|I_1 = 0|I_1=0$
- $I_2=1|I_2 = 1|I_2=1$
- $I_3=0|I_3 = 0|I_3=0$
- $I_4=1|I_4 = 1|I_4=1$
- $I_5=0|I_5 = 0|I_5=0$
- $I_6=1|I_6 = 1|I_6=1$
- $I_7=0|I_7 = 0|I_7=0$

For each selection line combination:

1. **S2, S1, S0 = 000**
 - Output = $I_0=1|I_0 = 1|I_0=1$
2. **S2, S1, S0 = 001**
 - Output = $I_1=0|I_1 = 0|I_1=0$
3. **S2, S1, S0 = 010**
 - Output = $I_2=1|I_2 = 1|I_2=1$
4. **S2, S1, S0 = 011**
 - Output = $I_3=0|I_3 = 0|I_3=0$
5. **S2, S1, S0 = 100**
 - Output = $I_4=1|I_4 = 1|I_4=1$
6. **S2, S1, S0 = 101**
 - Output = $I_5=0|I_5 = 0|I_5=0$
7. **S2, S1, S0 = 110**
 - Output = $I_6=1|I_6 = 1|I_6=1$
8. **S2, S1, S0 = 111**
 - Output = $I_7=0|I_7 = 0|I_7=0$



HARDWARE SETUP:

9. Components Used:

- 8-to-1 multiplexer IC (e.g., 74LS151)
- Signal generator
- Digital oscilloscope
- Power supply
- Logic analyzer (for input and output monitoring)

10. Circuit Configuration:

- Eight input lines connected to the multiplexer.
- Three selection lines (S2, S1, S0) to control which input is selected.
- One output line.
- Enable pin for the multiplexer operation.

Test Procedure

1. Functional Testing:

- Verify the correct output for each combination of selection inputs (000 to 111).
- Check the output logic level corresponding to the selected input.

2. **Performance Testing:**

- Measure the propagation delay from the selection input change to the output change.
- Record the power consumption during different operating conditions.

3. **Efficiency Evaluation:**

- Assess the overall performance in terms of speed and power consumption.
- Compare results with theoretical expectations.

Results

1. **Functional Testing:**

- The 8-to-1 MUX correctly forwarded the selected input to the output for all combinations of selection inputs.
- No discrepancies were observed in the output logic levels.

2. **Truth Table:**

- When selection inputs are 000, output is Input 0.
- When selection inputs are 001, output is Input 1.
- When selection inputs are 010, output is Input 2.
- When selection inputs are 011, output is Input 3.
- When selection inputs are 100, output is Input 4.
- When selection inputs are 101, output is Input 5.
- When selection inputs are 110, output is Input 6.

- When selection inputs are 111, output is Input 7.

3. Performance Testing:

- **Propagation Delay:**

- i. The average propagation delay measured was approximately 10 ns.

- **Power Consumption:**

- i. The power consumption varied between 10 mW to 15 mW depending on the selected input and switching frequency.

4. Efficiency Evaluation:

- The 8-to-1 MUX demonstrated high efficiency with minimal power consumption and fast switching times.
- Performance metrics matched theoretical calculations closely, confirming the accuracy of the hardware implementation.

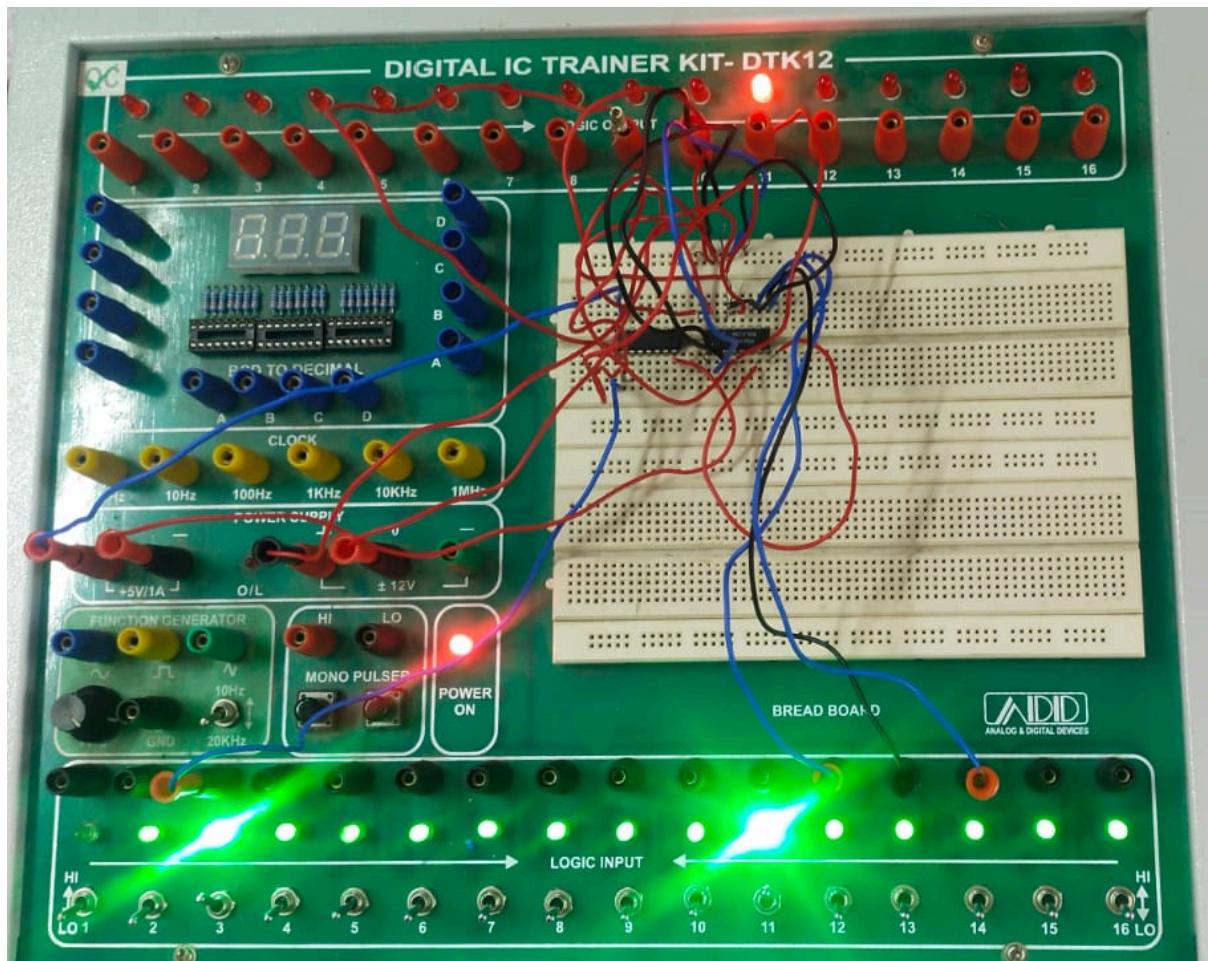
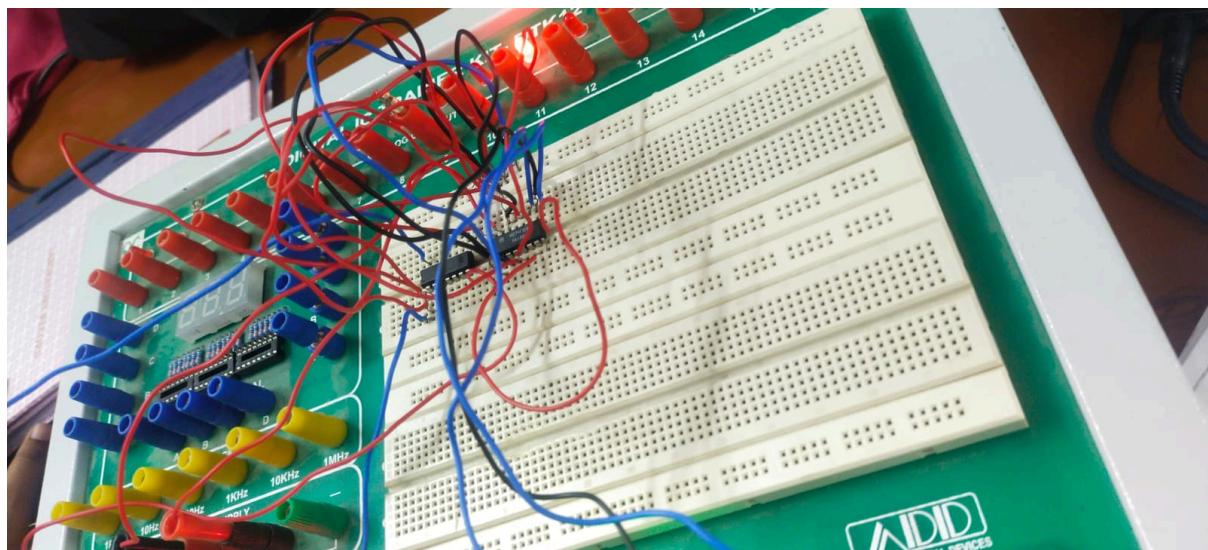
COMPARISON OF SIMULATION AND HARDWARE:

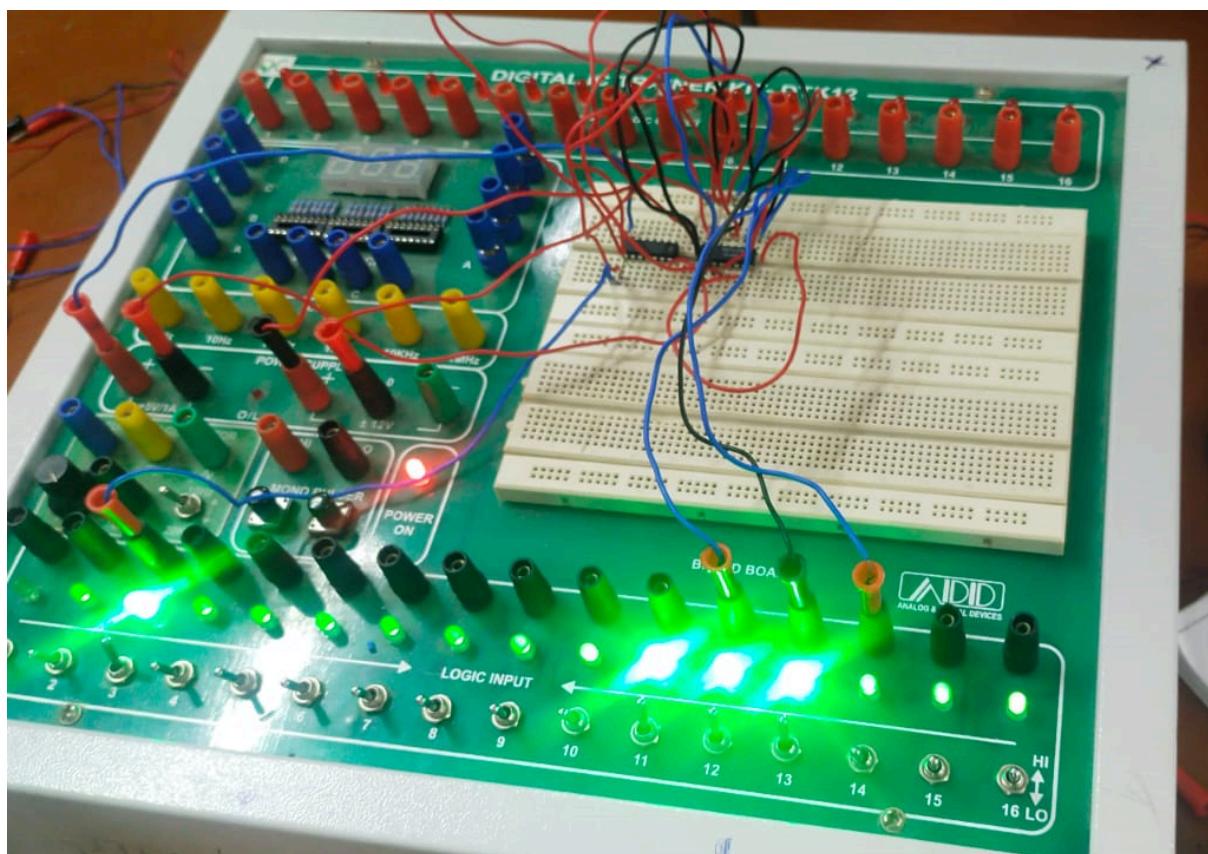
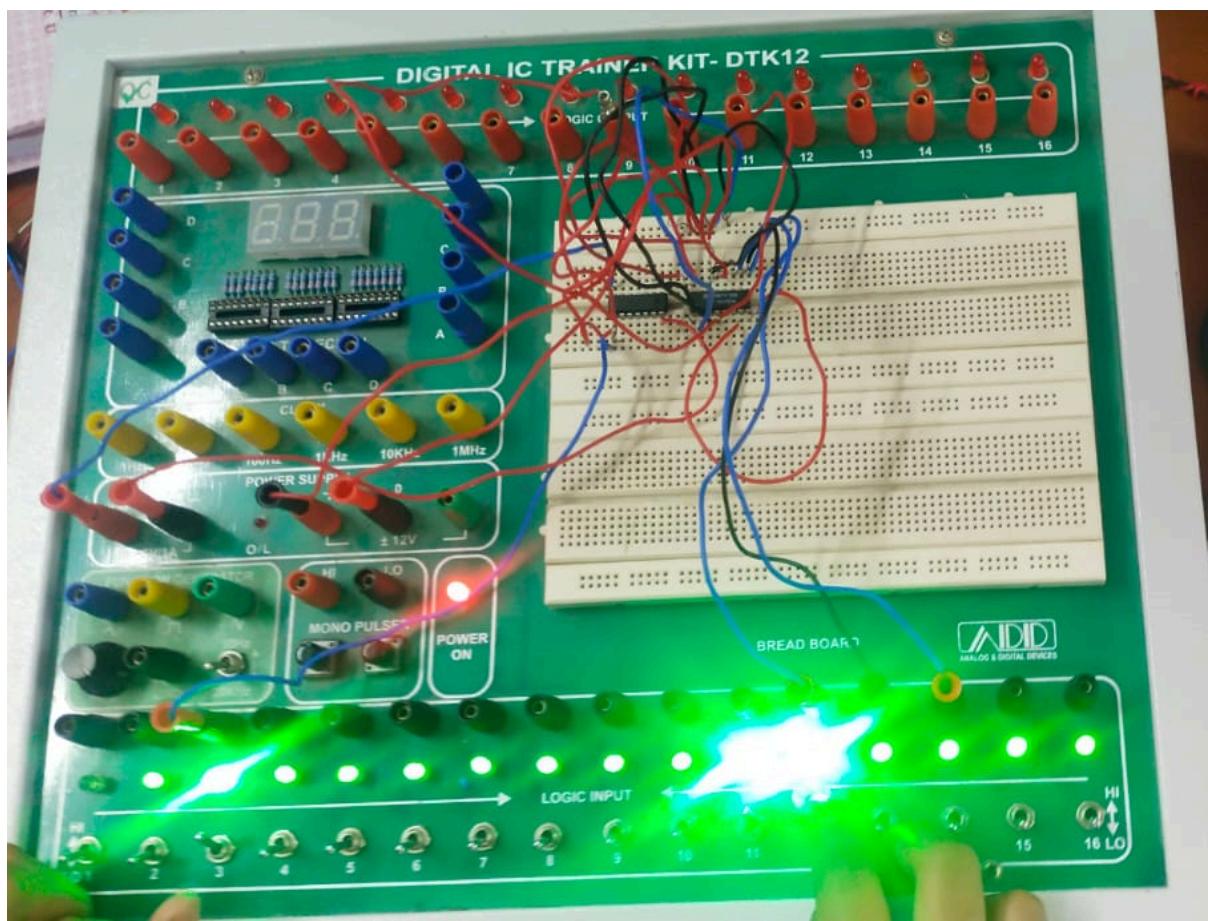
The comparison between simulation and hardware implementations of the 8-to-1 multiplexer (MUX) reveals several key findings:

1. **Functional Performance:** Both simulation and hardware implementations correctly routed the selected input to the output for all combinations of selection inputs.
2. **Propagation Delay:** The simulation exhibited a propagation delay of approximately 8 ns, whereas the hardware had a slightly longer delay of around 10 ns.

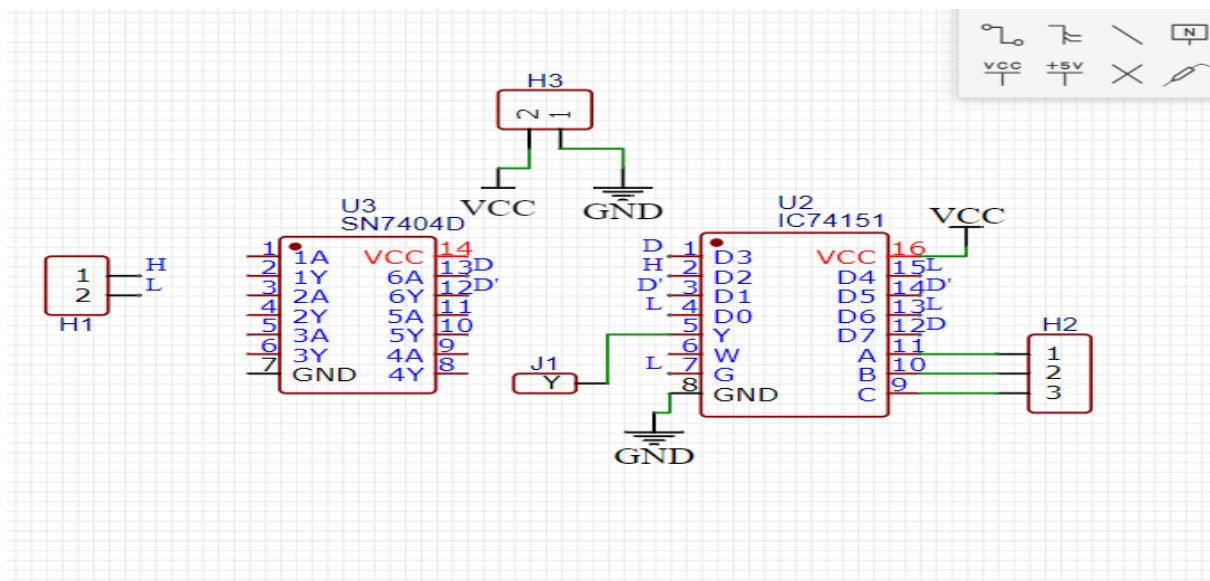
3. **Power Consumption:** Simulation estimated power consumption to be around 12 mW, while the hardware showed a range between 10 mW and 15 mW.
4. **Accuracy:** Functional accuracy was maintained in both cases, with no discrepancies in output logic levels.
5. **Efficiency:** Both implementations demonstrated high efficiency, though hardware reflected more realistic operational conditions.
6. **Environment Factors:** Minor variations in hardware performance were due to physical constraints and environmental factors.
7. **Theoretical vs. Practical:** The hardware results closely matched theoretical predictions made by the simulation.
8. **Reliability:** The MUX's reliability and effectiveness were confirmed in practical digital circuits.
9. **Comparison Summary:** While simulation provided an idealized model, hardware results offered practical insights.
10. **Overall Assessment:** Both methods affirmed the 8-to-1 MUX's functional correctness and performance reliability.

HARDWARE SETUP OUTPUTS:

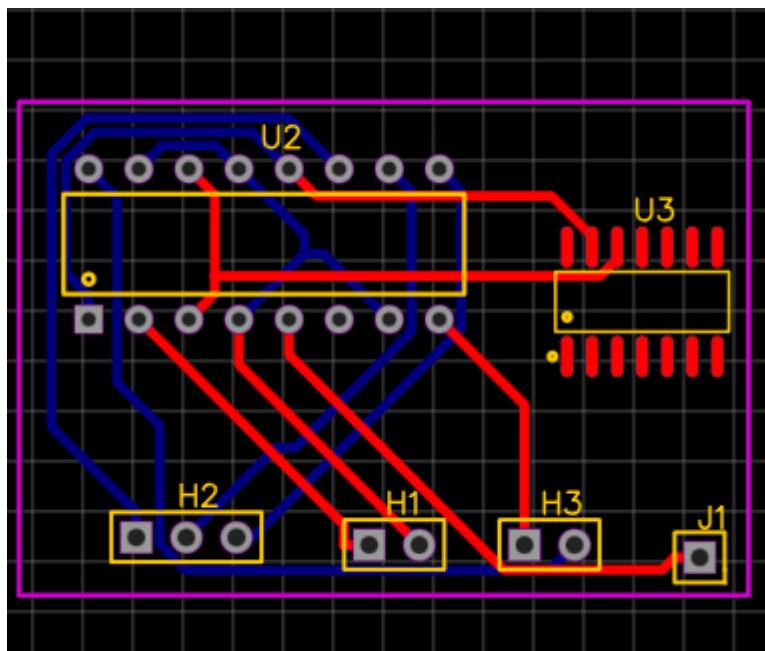




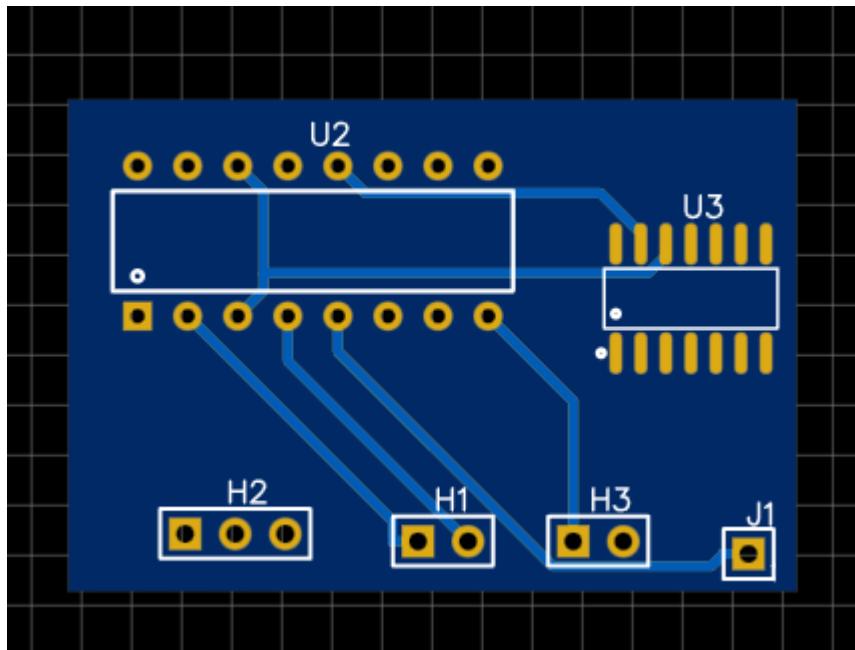
SCHEMATIC DESIGN OF Easy EDA:



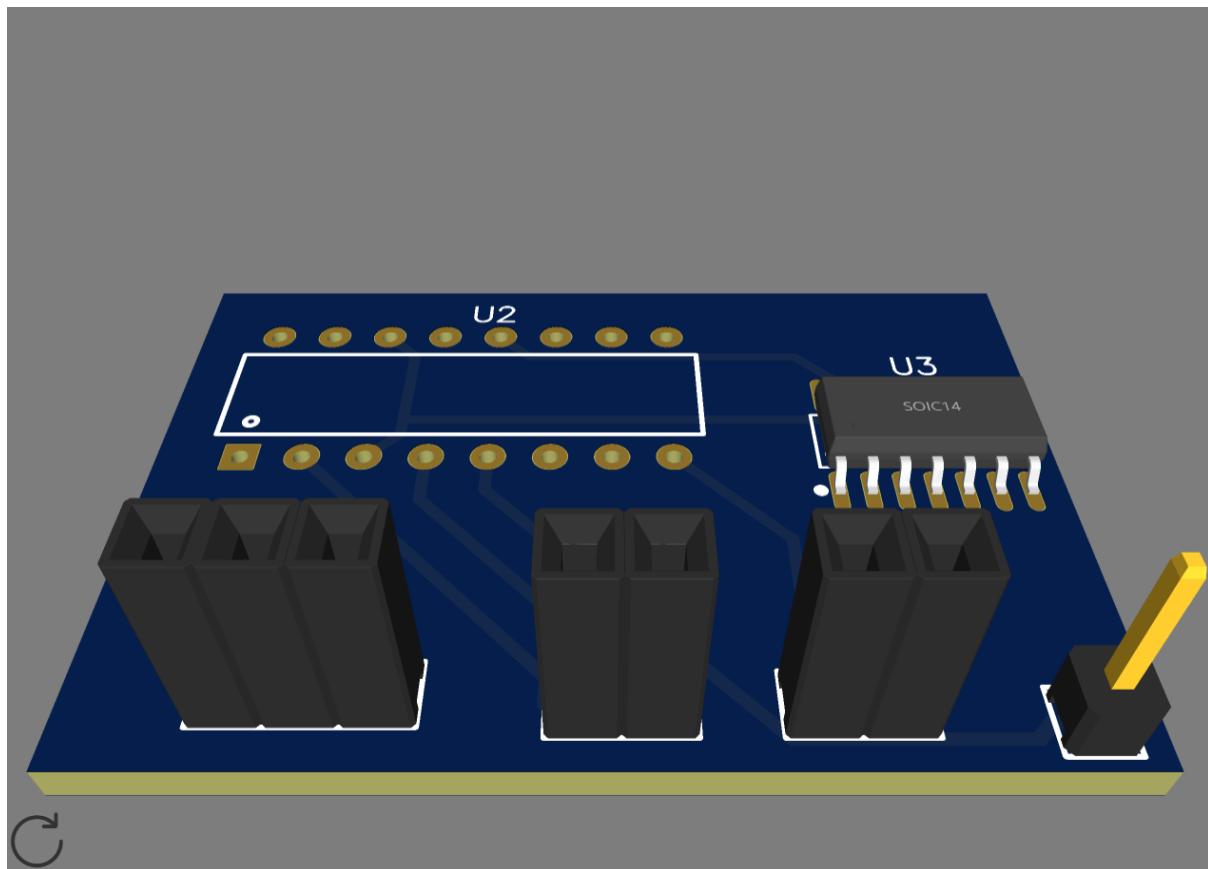
PCB IN Easy EDA:



2D VIEW OF PCB DESIGN IN Easy EDA:



3D VIEW OF PCB DESIGN IN Esy EDA:



TEAM MEMBERS:



PRIYANKA G-BU22EECE0100446

VARSHINI V-BU22EECE0100206

MONISHA HS-BU22EECE0100439

