**University of Central Florida**

**Department of Computer Science**

**CDA 5106: Fall 2023**

# Machine Problem 1: Cache Design, Memory Hierarchy Design

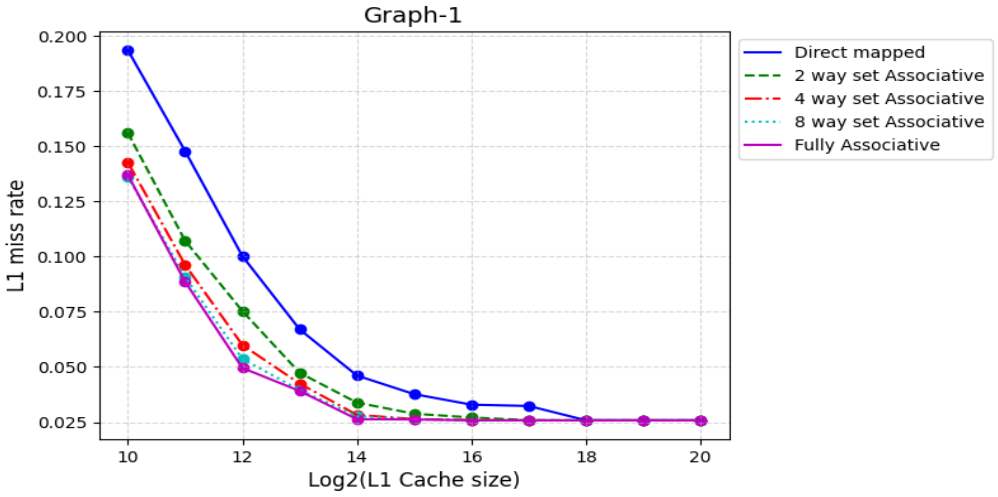
**by**

**Varshith Reddy Poreddy**

Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: Varshith Reddy Poreddy
(sign by typing your name)

**GRAPH-1:**




1. Discuss trends in the graph. For a given associativity, how does increasing cache size affect miss rate? For a given cache size, what is the effect of increasing associativity?

**Ans)** In the above graph, it is clear that as cache size increases, the miss rate decreases because larger cache has more storage capacity leading to a reduced miss rate and improved performance. And it is also evident that higher associativity with larger size has less miss rate because higher associativity reduces conflict misses, allowing the cache to store and retrieve data more efficiently, resulting in a lower miss rate.

2. Estimate the *compulsory miss rate* from the graph?

**Ans**) From the graph, compulsory miss rate is calculated by maximum cache size and for fully associativity mapping. Compulsory miss rate = 1.1% of total miss rate=> 1.1* (0.02582)/100 = **0.00028402** % of total misses.

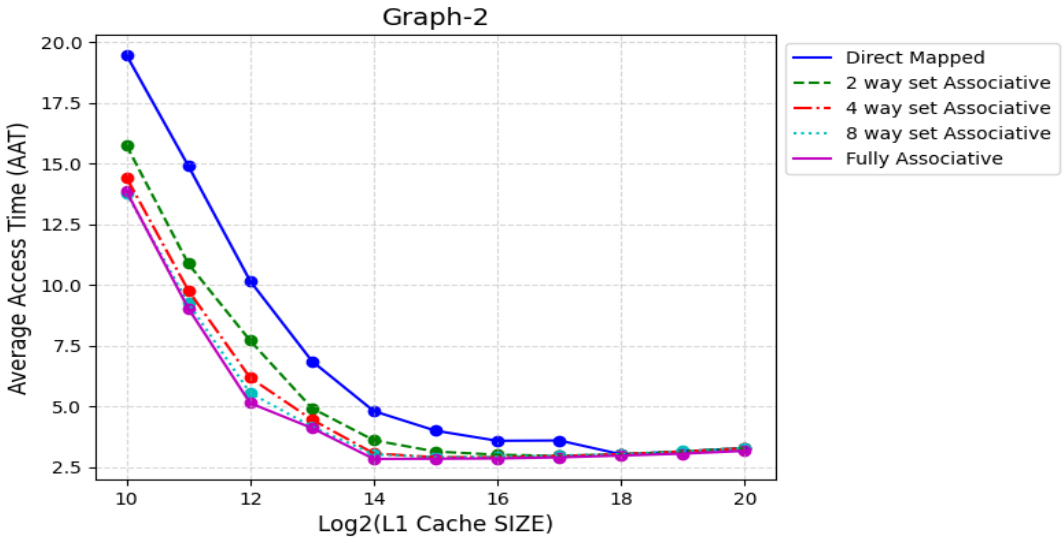
3. For each associativity, estimate the *conflict miss rate* from the graph?

**Ans)** The conflict miss rate is 4% of the average miss rate for each associativity.
For 1MB, the various associativity and conflict miss rate are given below:

**Associativity:** **Conflict miss rate:**

- 1 way associativity => 33% * 0.02582/100= **0.0085206**%
- 2 way associativity => 28% * 0.02582/100= **0.0072296**%
- 4 way associativity => 8% * 0.02582/100= **0.0020656**%
- 8 way associativity => 4% * 0.02582/100= **0.0010328**%

## GRAPH-2



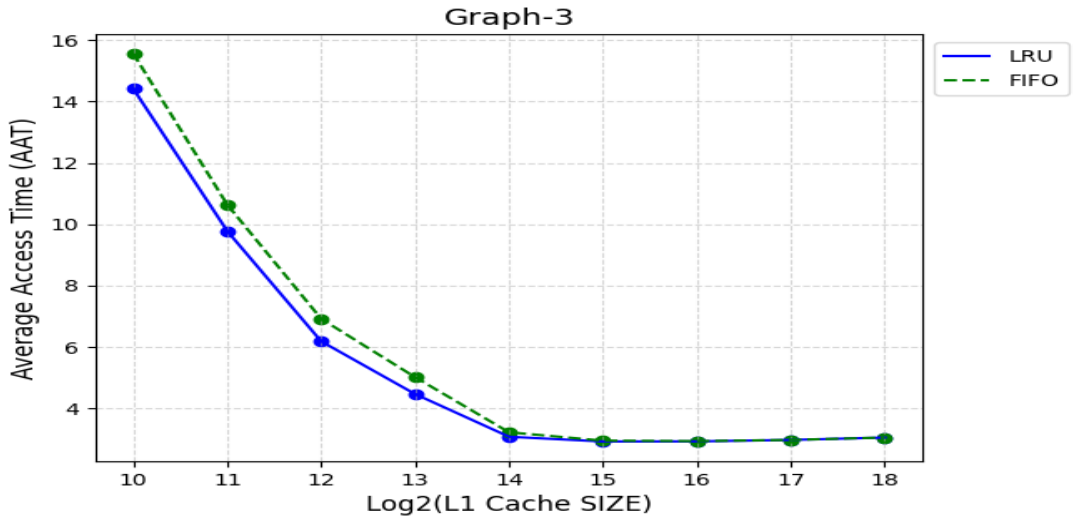

1. For a memory hierarchy with only an L1 cache and BLOCKSIZE = 32, which configuration yields the best (*i.e.*, lowest) AAT?

**Ans)** As per the graph, The configuration that yield lowest AAT is:

Cache size= 16 KB => 14

Fully Associativity=> AAT = **2.839608.**

## GRAPH-3:

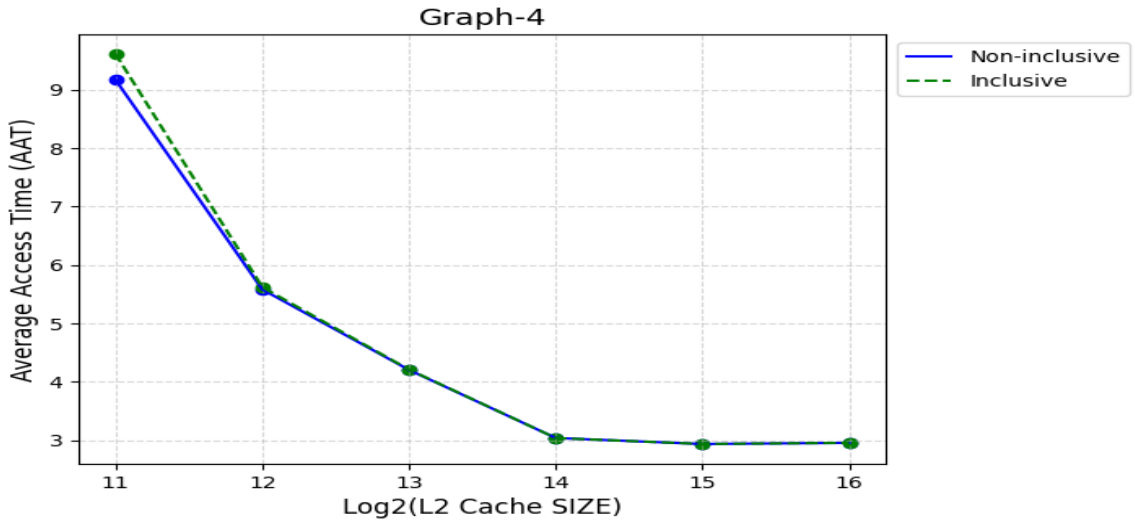


1. Discuss trends in the graph. Which replacement policy yields the best (*i.e.*, lowest) AAT?

Ans) In the graph-3, it is clear that LRU has lower AAT than FIFO because LRU replaces the least recently used block when a new block is added into the cache. However, the AAT of both replacement policies (LRU & FIFO) overlap with each other as the cache size increases indicating no use of replacement policies.

Lowest AAT:
Block size = 32
Replacement Policy = LRU
4- way set associativity
L1 Cache size = 32 KB=> 15
AAT = **2.91125**

**GRAPH-4:**




1. Discuss trends in the graph. Which inclusion property yields a better (i.e., lower) AAT?

Ans) In the above graph, it is evident that as cache size increases AAT decreases for both inclusion properties (Inclusive and Non- Inclusive) due to improved cache hit rates and a reduction in cache misses and both inclusive policies overlap with each other but non-inclusive have lower AAT initially.

The Configuration that yields lower AAT is Both Inclusive policies (Inclusive and Non-Inclusive) => L2 Cache size = 64KB => 16
Block size = 32
4- way Associativity
AAT = **2.7845110951**