Topic: 2:1 Mux with CPL

REPORT: VLSI Special assignment,

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ABSTRACT

This report explores the design and implementation of a 2:1 Mux via use of Complementary Pass Logic (CPL) topology, a significant advancement in digital circuit design. The Mux serves as a fundamental element/part in digital electronics also it's also a Universal logic (any circuit could be implemented by it). In contemporary digital systems, the demandfor efficient power consumption and high-speed operation has necessitated the exploration of alternative logic styles definitely CPL Suggest itself via this. CPL emerges as a compelling alternative to conventional CMOS logic due to itsunique architecture that leverages complementary transmission gates, comprised of both NMOS and PMOS transistors.

The primary advantages of CPL include is via enhanced power efficiency, reduced propagation delays, improved noise margins, and a more compact design footprint over CMOS. These attributes make CPL particularly suitable even for high-performance applications where speed and energy efficiency are critical. This report presents the design methodology for the CPL based 2:1 Mux, including the circuit architecture and thelogical arrangement of components how being done.

INTRODUCTION

The 2:1 Mux is a fundamental component in digital electronics, always servs as a fundamental necessity for designing out Complex circuits. In which there are 2 Inputs namely as A and B along with 1 select line namely as S. In general, if we see, Mux always uses to get designed via CMOS implementation but after which one will receive result as in form of more power consuming circuit less speed this difficulty rises along with as circuit complexity increases.

Complementary Pass Logic (CPL) has emerged as a powerful alternative to traditional static CMOS logic for implementing digital circuits having numerous advantages of itself compared to CMOS. CPL leverages a combination of complementary transmission gates to achieve lower power consumption, reduced delay, and improved noise margins which were not founded in CMOS. This topology allows for more compact designs while maintaining high-speed operation, making it especially suitable for applications in high-density integrated circuits.

In this report, we are providing design for 2:1 Mux via the help of CPL topology. We are going to discuss the circuit architecture and design methodology, emphasizing the advantages of CPL in terms of performance parameters which are mainly such as speed and power efficiency. Through detailed simulations, we evaluate the proposed 2:1 Mux behavior and performance under various conditions, demonstrating its effectiveness in modern digital applications how it turns out to be effective. This work aims to contribute to the ongoing efforts in optimizing arithmetic circuits and advancing the design of efficient digital systems.

WHY CPL OVER CMOS?

- **Power Efficiency**: Although CMOS is known for its low static power consumption, CPL can offer better dynamic power efficiency in certain applications. CPL circuits reduce the number of transistors required, which can minimize switching capacitance, thereby saving dynamic power. Therefore, in scenarios where dynamic power is more critical than static power—like in high-frequency operations—CPL proves out to be more efficient.

- **Speed and Delay**: The speed advantage comes from CPL's use of pass-transistor logic, which reduces the need for complex gate structures. CPL can directly pass signals with fewer intermediate stages, thereby reducing the overall propagation delay. In comparison, CMOS circuits often need additional transistors to invert signals or amplify weak ones, which can slow down the circuit. The reduced delay in CPL makes it ideal for high-speed applications like microprocessors and digital signal process

- **Reduced Area**: CPL can offer more compact designs by combining multiple functions into fewer transistors (since requires NMOS only). This reduction in transistor count not only saves silicon area (saving expenditure) but also enhances integration density, allowing for more complex circuits to fit within the same chip footprint.

• **Noise Immunity**: The complementary nature of CPL provides better noise margins compared to traditional CMOS designs. This is particularly important in environments with varying power supply levels and external noise is there present, ensuring reliable operation across different conditions making whole circuit thoroughly stable throughout.

• **Scalability**: As technology scales down to smaller nodes, CPL exhibits better performance characteristics than CMOS due to its inherent design advantages over CMOS. This makes it a more suitable option for next-generation integrated circuits where performance and power are increasingly critically.

BOOLEAN EXPRESSION

S	A	B	Y
0	0	0	0
0	0	1	0
1	1	0	0
1	1	1	1

From Truth table we can get output(Y).

Output (Y): The output is dependent primarily in select line, if select line(S) is logic 0, A will be transmitted and when select line(S) is logic 1, B will be transmitted.

$$Y = S' \cdot A + S \cdot B$$

GATE LEVEL DIAGRAM

Given below is a gate level diagram of 2:1 Mux having 2 inputs respectively as A and B along with one Select line as S, resulting output Y.

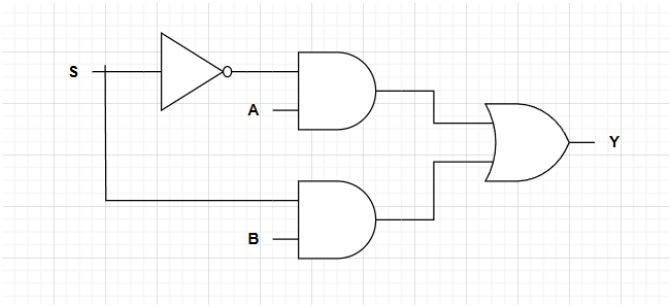


Figure 1. Gate level schematic diagram on 2:1 Mux.

STICK DIAGRAM

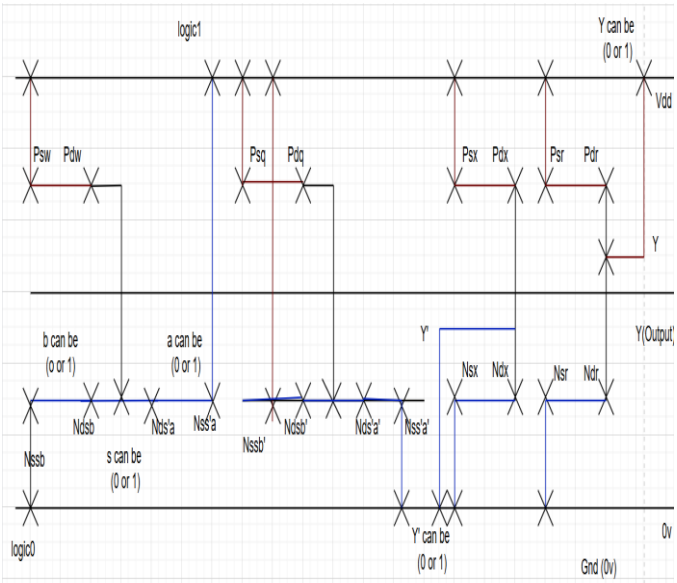


Figure 2. Stick diagram for CPL colours

1. Blue represents all NMOS connections.
2. Red represents all PMOS connections.

TRANSISTOR-LEVEL DIAGRAM

Given is a transistor level schematic for 2:1 Mux CPL. This includes providing complementary signals (S and S') as the driving inputs for the gates, thereby giving full swing outputs. The section will tell us why we find Y' instead of getting directly Y we will receive actually in order to receive full swing voltage we do so same for Y' we will first find Y.

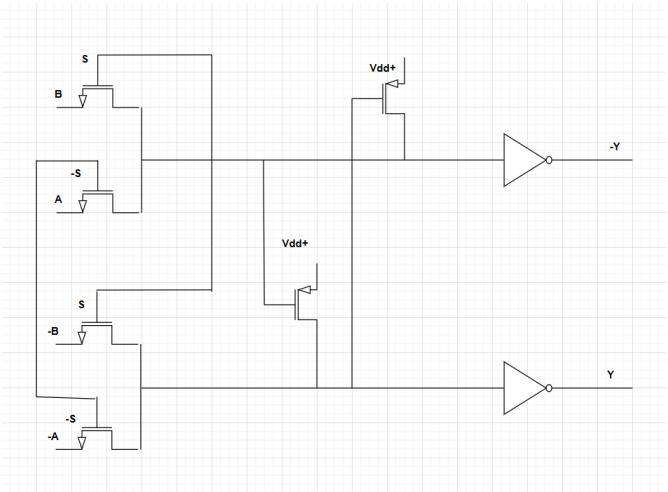


Figure 3. Transistor level schematic for 2:1 Mux with its appropriate inputs and complements is provided above. The normal and complemented values of literal A, B and S are implemented at NMOS with respect to CPL topology, answer of first above two NMOS will serve as an input for below PMOS similarly for above PMOS, answer of lower 2 NMOS will serve as input, along with that in their respective lines itself Inverter is there which helps us to get -Y(Y') and Y .

LAYOUT IN MICROWIND

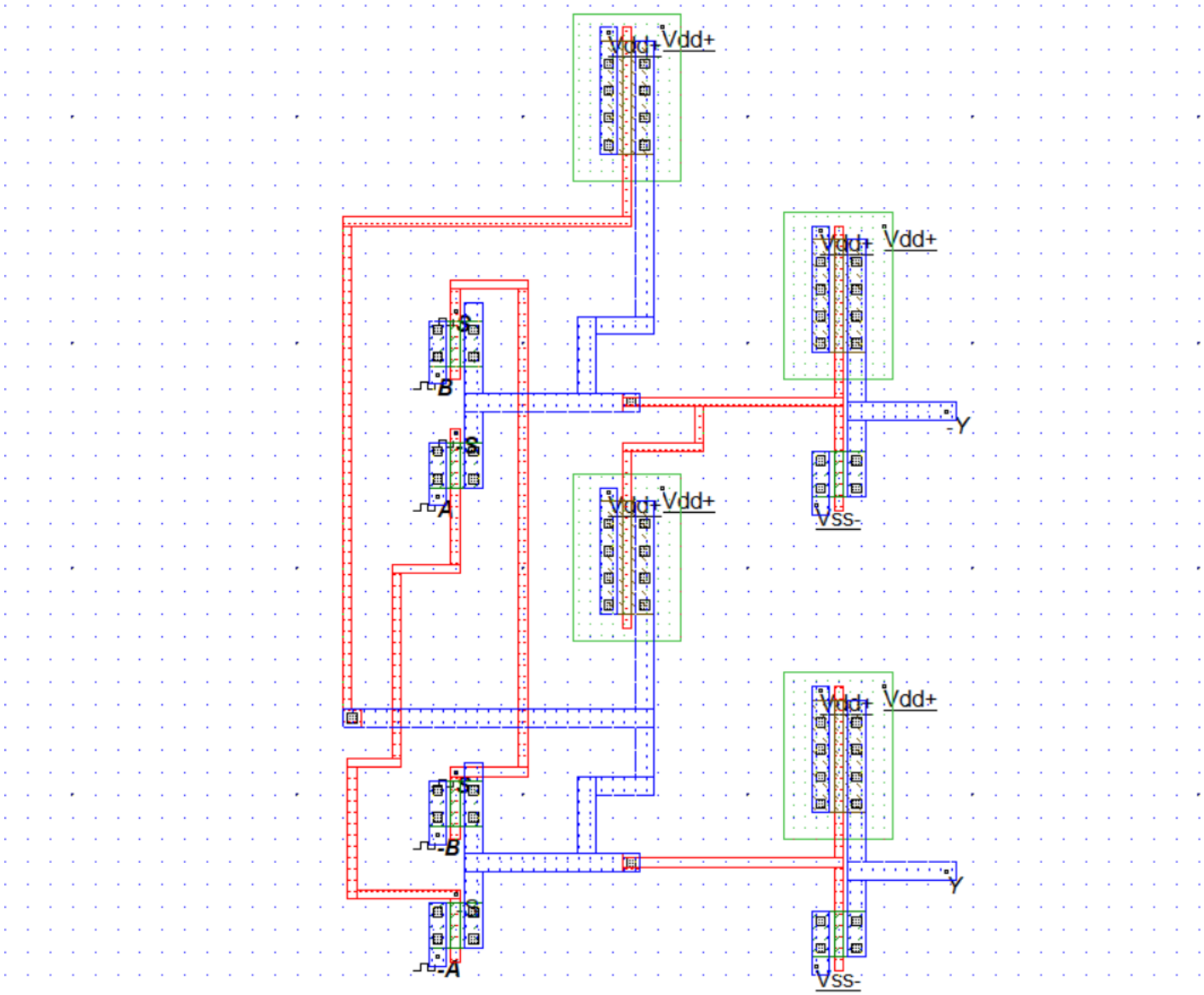


Figure 4. Establishing connections between components and preparing the Final layout.

In total, this CPL topology uses 4 PMOS + 6 NMOS, whereas if it was to be created via CMOS, it would have utilized 6 PMOS + 6 NMOS, making circuit more costly, so if we see that at a more complex circuitry level more NMOS and PMOS collectively would be there required via CMOS topology due to which cost will be lot and also complexity would increase, as a result of which we prefer CPL topology.

SIMULATING THE OUTPUT

As we can see below that our truth table does verify from simulations received as mentioned below from graphs also same for inverted output.

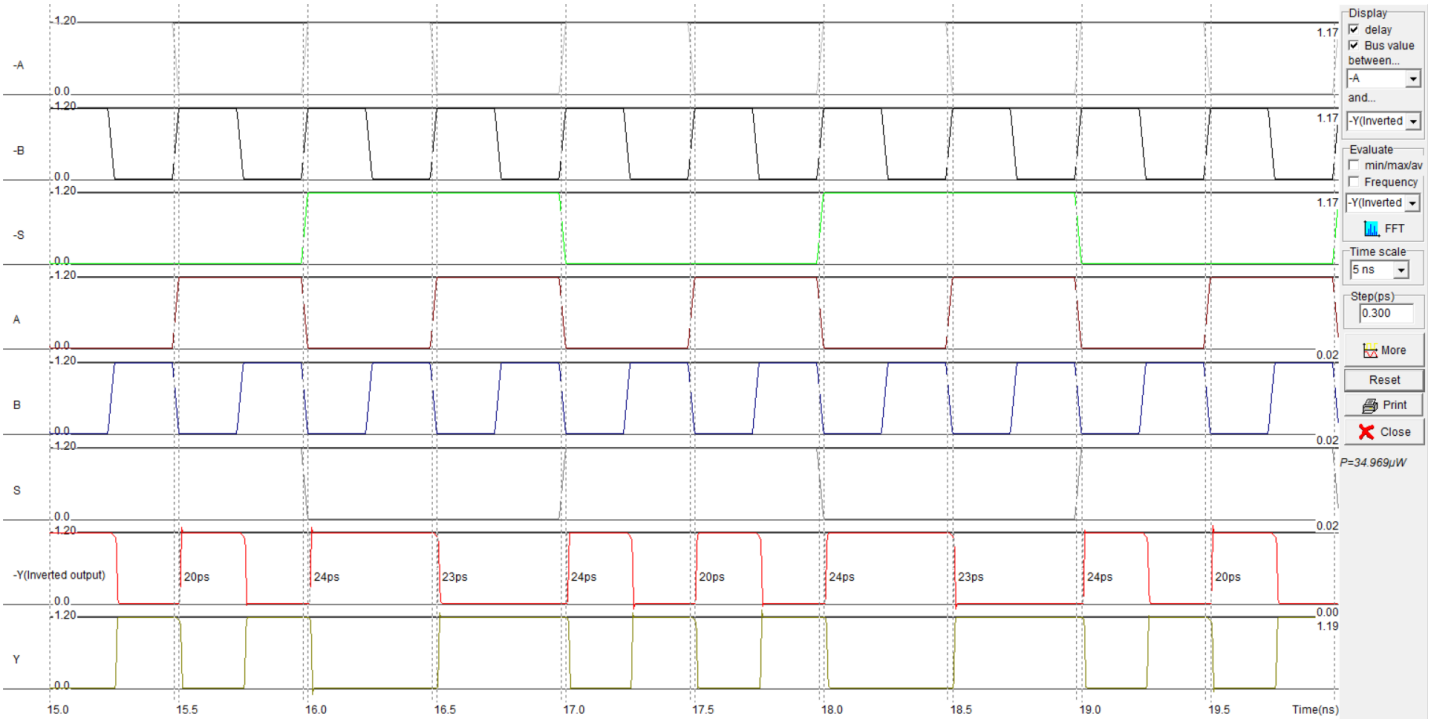


Figure 5. Transient response of the generated layout, implying the functionality of a 2:1 Mux with a, Time-scale at 20 ns and Amplitude of (0-1.2) v.

VTC FOR THE INVERTER MODULES USED

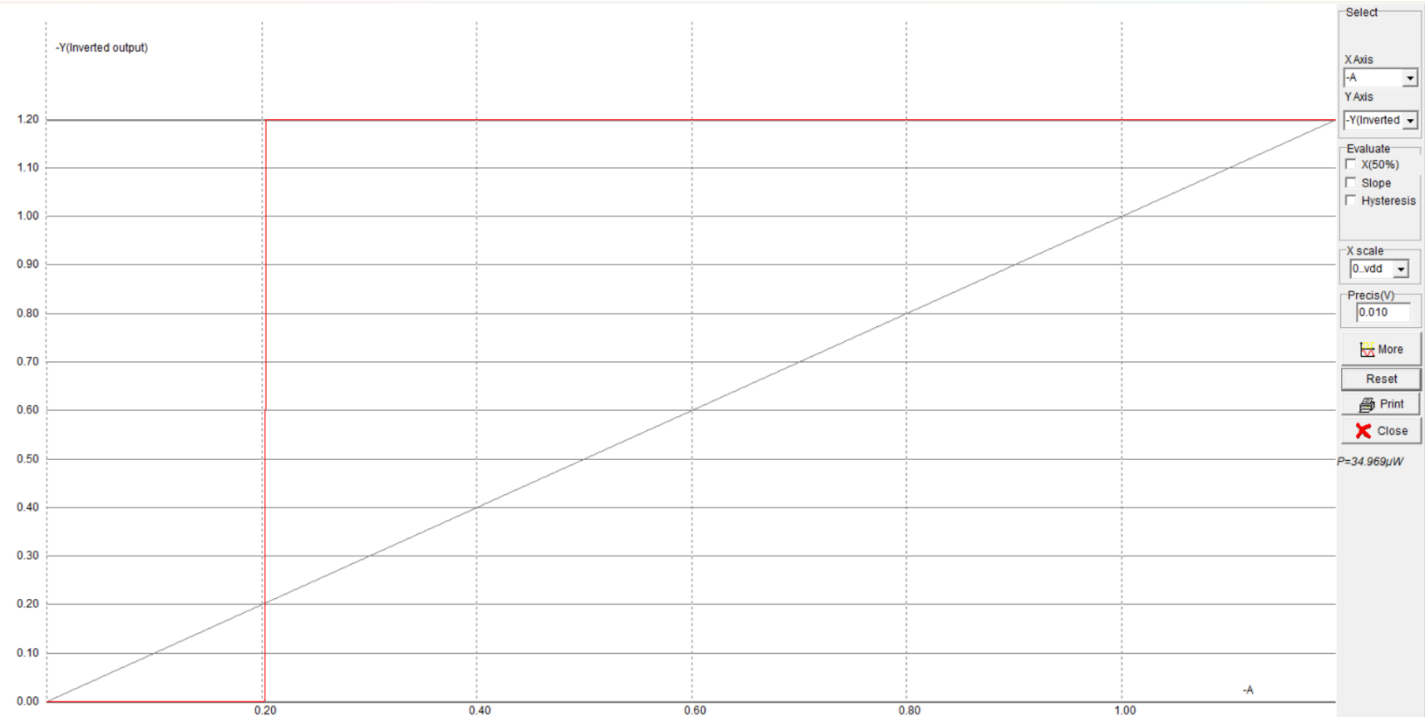
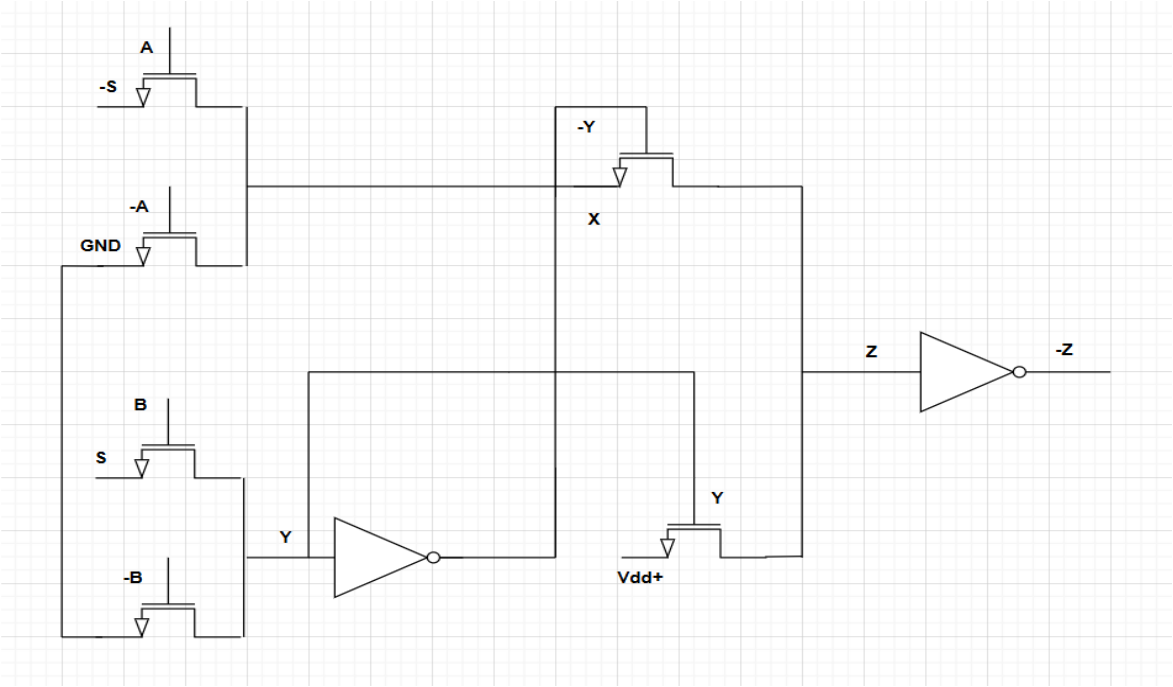
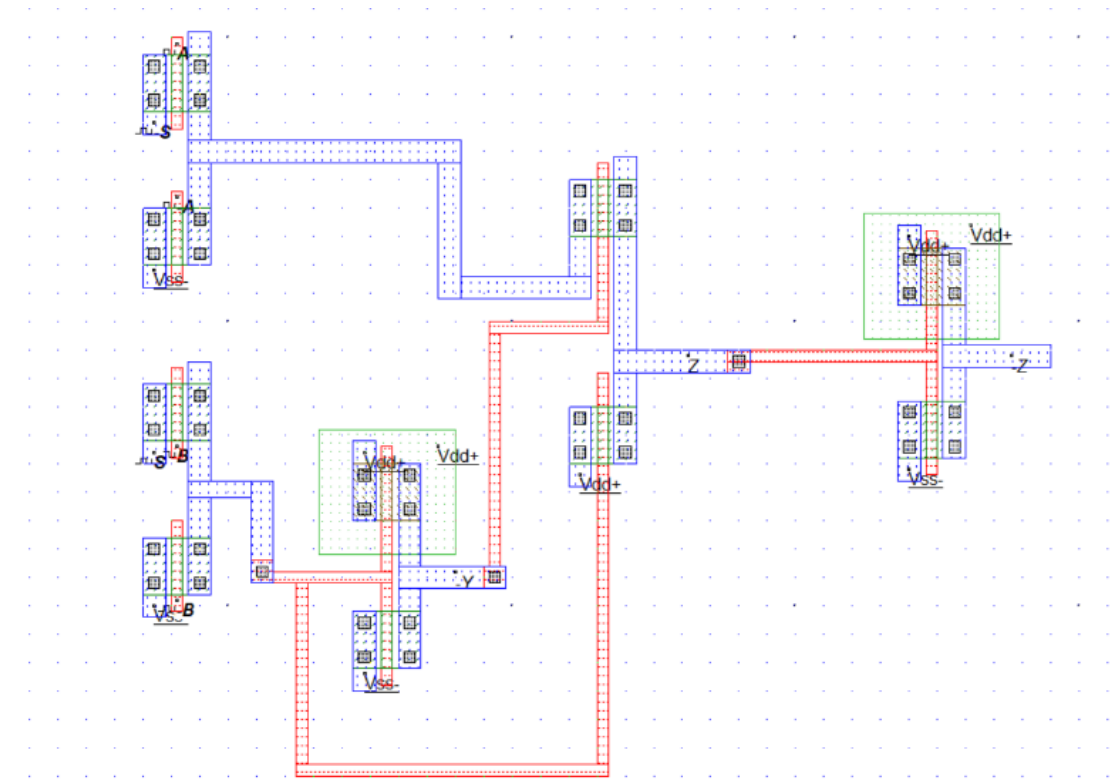


Figure 6. Voltage Transfer characteristics with respect to inverted output (Y') provided A' an input.

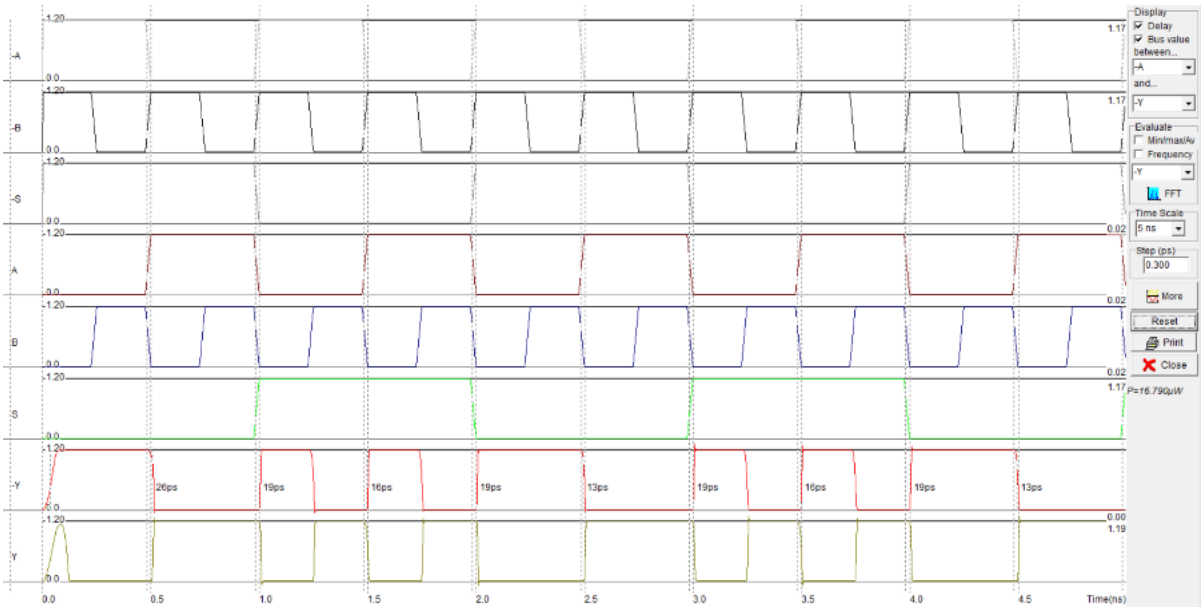
DISCREPANCIES IN DIRECT FORMATION



7a figure. Transistor level schematic diagram



7b figure. Micro wind layout



7c figure. Transient response for 2nd method

Figure 7. Three figures associated for the 2nd case.

One may think regarding why not we should go for conventional method of CPL topology simpler method to not go with that because it would require 8NMOS and 2PMOS whereas here we took 4NMOS and 6PMOS in which Cross coupled pull up PMOS transistors we took as a result of which speed of the overall output enhances. Along with that problem arises in terms of overall output we can clearly see here that overall output isn't refined as it is in cross-coupled case full swing voltage we do receive via placing inverter in front still not getting logic1 and logic0 when necessary, such as in staring case if we see that both output at initial stage is turning out to be same for staring phase which is not true.

PARAMETERS

We know that, for a CMOS Inverter, the $\boldsymbol{V_{OH} \approx V_{DD}}$ & $\boldsymbol{V_{OL} \approx 0}$. Thereby we proceed to calculate V_{IL} *and* V_{IH}.

Calculating V_{IL} :

By definition, the slope of the VTC is equal to (-1), i.e., $\frac{dVout}{dV_{in}} = -1$ when the input voltage is $V_{in} = V_{IL}$. Note that in this case, the NMOS transistor operates in saturation while the PMOS transistor operates in the linear region. From $I_{D,n} = I_{D,p}$ we obtain the following current equation

$$\frac{\boldsymbol{k_n}}{\boldsymbol{2}}\left(\boldsymbol{V_{GS,n} - V_{T0,n}}\right)^{\boldsymbol{2}} = \frac{\boldsymbol{k_p}}{\boldsymbol{2}}\left[\boldsymbol{2\left(V_{GS,p} - V_{T0,p}\right).V_{DS,p} - V_{DS,p}^2}\right]$$

Upon performing further substitutions such as, $V_{GS,n} = V_{in}, V_{GS,p} = V_{in} - V_{DD}$ & $V_{DS,p} = V_{out} - V_{DD}$ and satisfying the derivative conditions, we get:

$$\boldsymbol{V_{IL}} = \frac{\boldsymbol{2V_{out} + V_{T0,p} - V_{DD} + k_R.V_{t0,n}}}{\boldsymbol{1 + k_R}} \qquad \textit{where,} \qquad \boldsymbol{k_R = \frac{k_n}{k_p}}$$

Calculating V_{IH} :

When the input voltage is equal to $\boldsymbol{V_{IH}}$, the NMOS transistor operates in the linear region, and the PMOS transistor operates in saturation. Applying KCL to the output node, we obtain:

$$\frac{\boldsymbol{k_n}}{\boldsymbol{2}}\left[\boldsymbol{2\left(V_{GS,n} - V_{T0,n}\right).V_{DS,n} - V_{DS,n}^2}\right] = \frac{\boldsymbol{k_p}}{\boldsymbol{2}}\left(\boldsymbol{V_{GS,p} - V_{T0,p}}\right)^{\boldsymbol{2}}$$

Again substituting, $V_{GS,n} = V_{in}, V_{GS,p} = V_{in} - V_{DD}$ & $V_{DS,n} = V_{out}$ and solving by satisfying the derivatives, we get:

$$\boldsymbol{V_{IH}} = \frac{\boldsymbol{V_{DD} + V_{T0,p} + k_R(2V_{out} + V_{T0,n})}}{\boldsymbol{1 + k_R}} \qquad \textit{where,} \qquad \boldsymbol{k_R = \frac{k_n}{k_p}}$$

The inverter threshold voltage V_{th} was identified as one of the most important parameters that characterize the steady-state input-output behavior of the CMOS inverter circuit. The CMOS inverter can, by virtue of its complementary push-pull operating mode, provide a full output voltage swing between 0 and V_{DD}, and therefore, the noise margins are relatively wide. Thus, the problem of designing a CMOS inverter can be reduced to setting the inverter threshold to a desired voltage value. This is diagrammatically represented in Fig. 8 (a).

It was also observed that,

$$\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\boldsymbol{p}} \approx 2.5\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\boldsymbol{n}}$$

It should be noted that the numerical values used in the above equation for electron and hole mobilities are typical values, and that exact μ_n & μ_p values will vary with surface doping concentration of the substrate and the tub. Here , width and length PMOS and NMOS are (*1.5um & 0.12um*) and (*0.6um and 0.12um*).

PARAMETERS, RECORDED

Following parameters were observed via simulating the circuit.

The units are mentioned respectively for mentioned parameters:

V_{OH}	1.2	In Volts
V_{OL}	0	
V_{IH}	0.24	
V_{IL}	0.21	
$T_{p_{HL},INV}$	19	In ps $10^{-9}s$
$T_{p_{LH},INV}$	12	
$T_{p_{HL},O/P}$	14	
$T_{p_{LH},O/P}$	11.5	

SUMMARY

So, finally we implemented 2:1 Mux via the help of CPL topology using almost wherever possible for enhancement of speed for output we went for Cross coupled PMOS inverter both present at output side (Y AND Y') in order to receive full swing output from 0 to Vdd (here is 1.2)v.

This CPL configuration provides advantages such as lower power consumption, reduced propagation delays, and improved noise margins compared to traditional CMOS designs. On an overall basis, the CPL-based 2:1 Mux is more reliable in digital electronics if compared with traditional CMOS.

By choosing suitable length and width values we have satisfied the relation of PMOS and NMOS of (2.5:1) of (Width/Length) of PMOS/NMOS.

REFERENCES

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated circuits Analysis and design, Third edition.
2. https://www.ijareeie.com/upload/2015/march/16_Design.pdf.

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