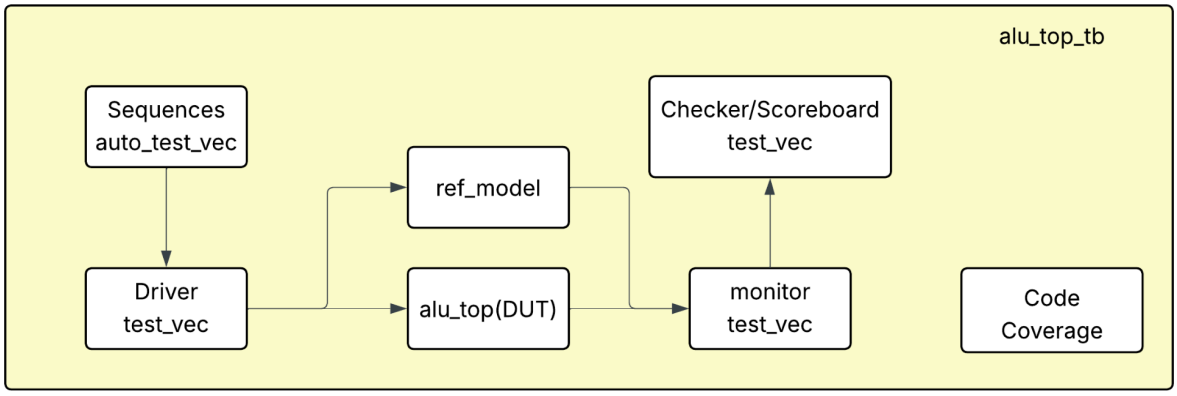
Test Plan: ALU_Test_plan



Test bench Architecture:

Testbench instantiates the DUT, generates the clock, manages stimulus, reference modeling, and checks correctness.

🔹 Sequences
Call auto_test_vec with different test scenarios, including valid, error, corner and random cases.
Example:
auto_test_vec("ADD", 0, 1, 2'b11, 1, `ADD, 8'd10, 8'd20, 0);
auto_test_vec("INC_A", 0, 1, 2'b01, 1, `INC_A, 8'd8, 0, 0);
...

🔹 auto_test_vec Task:
Accepts test vector parameters and computes the required delay using get_delay_cycles. Calls test_vec.

🔹 Reference Model (ref_model task):
Mirrors the ALU logic at a high level.

🔹 test_vec Task:(Driver,Monitor,Checker)

- Drives stimulus to DUT.(Driver)
- Waits for output to stabilise.(Monitor)
- Handles CE/rst hold logic (latching expected values if CE=0/rst=1).
- Calls the reference model to get expected values.(Monitor)
- Compares DUT outputs to reference model and prints [PASS] or [FAIL].(Checker)

🔹 Statistics and Logging (Scoreboard)
pass, fail, testnum keep track of test status.At the end, prints total passed/failed test count.

- Coverage Report:

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
alu_top_tb	84.75%	82.97%
is_two_op	90.90%	97.05%
get_delay_cycles	100.00%	100.00%
auto_test_vec	100.00%	100.00%
ref_model	81.65%	75.32%
test_vec	80.00%	58.24%
dut	100.00%	100.00%

Coverage Summary by Type:

Total Coverage:					84.75%	82.97%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Statements	358	353	5	1	98.60%	**98.60%**
Branches	121	115	6	1	95.04%	**95.04%**
FEC Expressions	104	95	9	1	91.34%	**91.34%**
FEC Conditions	48	25	23	1	52.08%	**52.08%**
Toggles	766	596	170	1	77.80%	**77.80%**

Report generated by Questa (ver. 10.7c) on Tuesday 27 May 2025 22:46:56 with command line:
vcover report -html alu.ucdb -htmldir covReport -details

- test_vec misses - all tests cases passed,so fail display branch is not hit
- ref_model misses - error cases satisfied in dut,but because of coding style some misses in ref model

Scope: /alu_top_tb/dut

Instance Path:
/alu_top_tb/dut
Design Unit Name:
work.alu_top
Language:
Verilog
Source File:
test_bench.v

Coverage Summary By Instance:

Scope	TOTAL	Statement	Branch	FEC Expression	FEC Condition	Toggle
TOTAL	100.00	100.00	100.00	100.00	100.00	100.00
dut	100.00	100.00	100.00	100.00	100.00	100.00
is_opA_only	100.00	100.00	100.00	100.00	100.00	--
is_opB_only	100.00	100.00	100.00	100.00	100.00	--
is_two_op	100.00	100.00	100.00	100.00	100.00	--
aluA	100.00	100.00	100.00	100.00	--	100.00
aluB	100.00	100.00	100.00	100.00	--	100.00
alu2	100.00	100.00	100.00	100.00	100.00	100.00

Local Instance Coverage Details:

Total Coverage:					100.00%	100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Statements	90	90	0	1	100.00%	100.00%
Branches	21	21	0	1	100.00%	100.00%
FEC Expressions	45	45	0	1	100.00%	100.00%
FEC Conditions	5	5	0	1	100.00%	100.00%
Toggles	284	284	0	1	100.00%	100.00%

Recursive Hierarchical Coverage Details:

Total Coverage:					100.00%	100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Statements	168	168	0	1	100.00%	100.00%
Branches	68	68	0	1	100.00%	100.00%
FEC Expressions	60	60	0	1	100.00%	100.00%
FEC Conditions	9	9	0	1	100.00%	100.00%
Toggles	476	476	0	1	100.00%	100.00%

- DUT Coverage ✅