10-BIT RING COUNTER

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Introduction

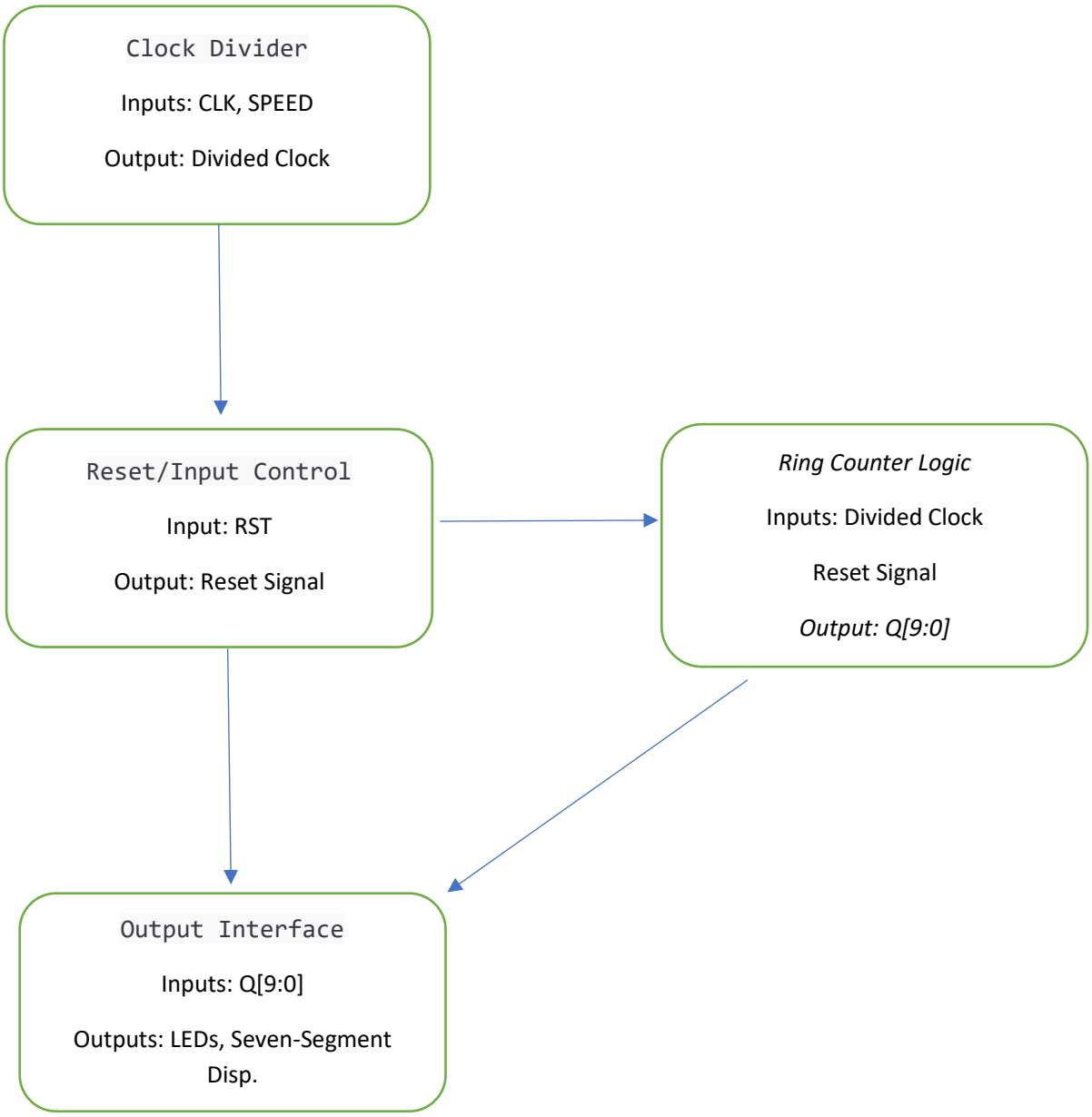
This project involves the implementation of a 10-bit ring counter on the DE10-Lite FPGA board using VHDL. A ring counter is a sequential circuit where a single '1' circulates through the flip-flops, ensuring predictable cyclic behavior. Our design incorporates an adjustable clock speed feature, allowing for configurable counter operation.

This project demonstrates modular digital design and FPGA implementation, showcasing practical applications in sequential logic systems.

System Overview

The 10-bit counter system comprises the following components:

1. **Clock Divider:**
   Adjusts the operational clock frequency to control counter speed.
2. **10-Bit Ring Counter Logic:**
   Implements cyclic behavior by propagating a single high logic state across ten stages.
3. **Control and Reset Logic:**
   Includes inputs for initializing the counter and managing its state transitions.
4. **Output Interface:**
   Displays the counter output on LEDs and optionally on a seven-segment display for clarity.



Implementation Details

1. **VHDL Design:**
    - **Clock Divider:** Generates a divided clock signal based on the configurable SPEED input.
    - **Ring Counter Logic:** Designed with 10 D flip-flops, each propagating the high state to the next stage on every clock pulse.

- **Reset and Initialization:** Ensures the counter starts with a '1' in the least significant bit (LSB).

2. **Simulation:**
   Verified using **ModelSim** to ensure correct operation under various clock speeds and initialization conditions.
3. **Hardware Implementation:**
   - Synthesized the design in **Quartus Prime**.
   - Pin assignments made for DE10-Lite FPGA for inputs (CLK, RST, SPEED) and outputs (Q[9:0]).

Results

1. Simulated Output: The counter successfully propagates the '1' through all stages with cyclic behavior. Clock speeds were validated for various configurations.

2. Hardware Testing: Output observed on LEDs; adjustable speed verified through visual inspection.

3. Challenges and Solutions:

- Clock Division Accuracy: Resolved using a counter-based clock divider.
- Reset Issues: Addressed by implementing an asynchronous reset mechanism.
- Output Visualization: Seven-segment displays used to mitigate rapid toggling on LEDs.

Conclusion

The project successfully demonstrates the implementation of a **10-bit ring counter** with a configurable clock. The system is modular, reliable, and demonstrates practical digital design techniques. Future enhancements could include integration with external sensors or further optimization of the clock divider.

References

1.EE232 lecture notes

2.EE232 YouTube lectures

3.Stephen Brown and Zvonko Vranesic, **“**Fundamentals of Digital Logic with VHDL Design,**”** Tata McGraw Hill