EE301 ANALOG CIRCUITS
COURSE PROJECT

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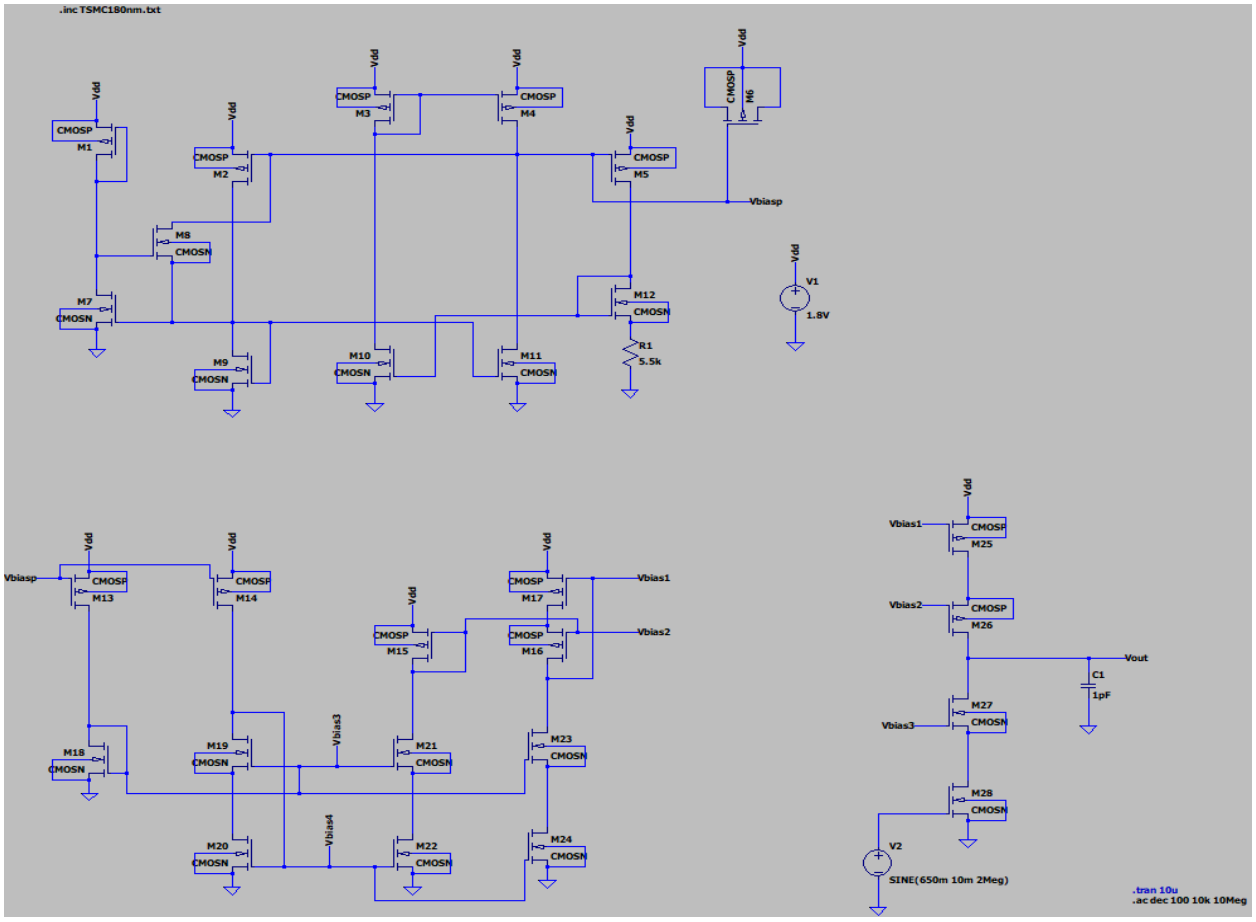
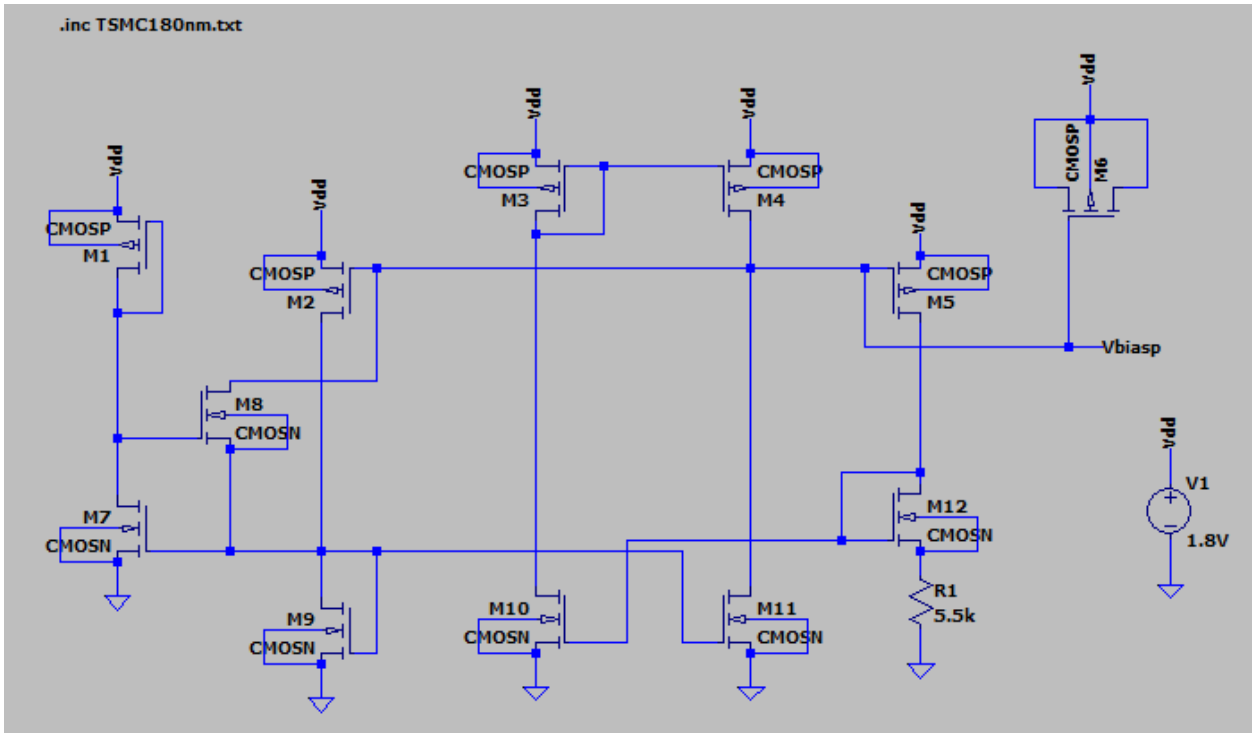
Objective: Design of cascode amplifier and cascode current mirror in schematic and layout using LTspiceand Magic in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

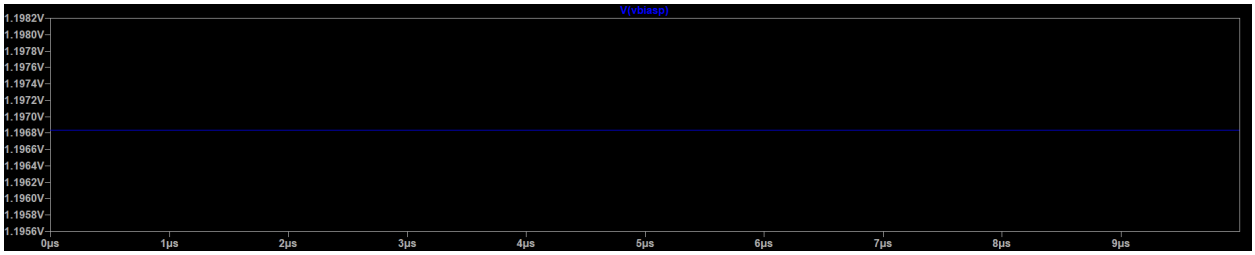
LTSpice Schematic:
For 180 nm:



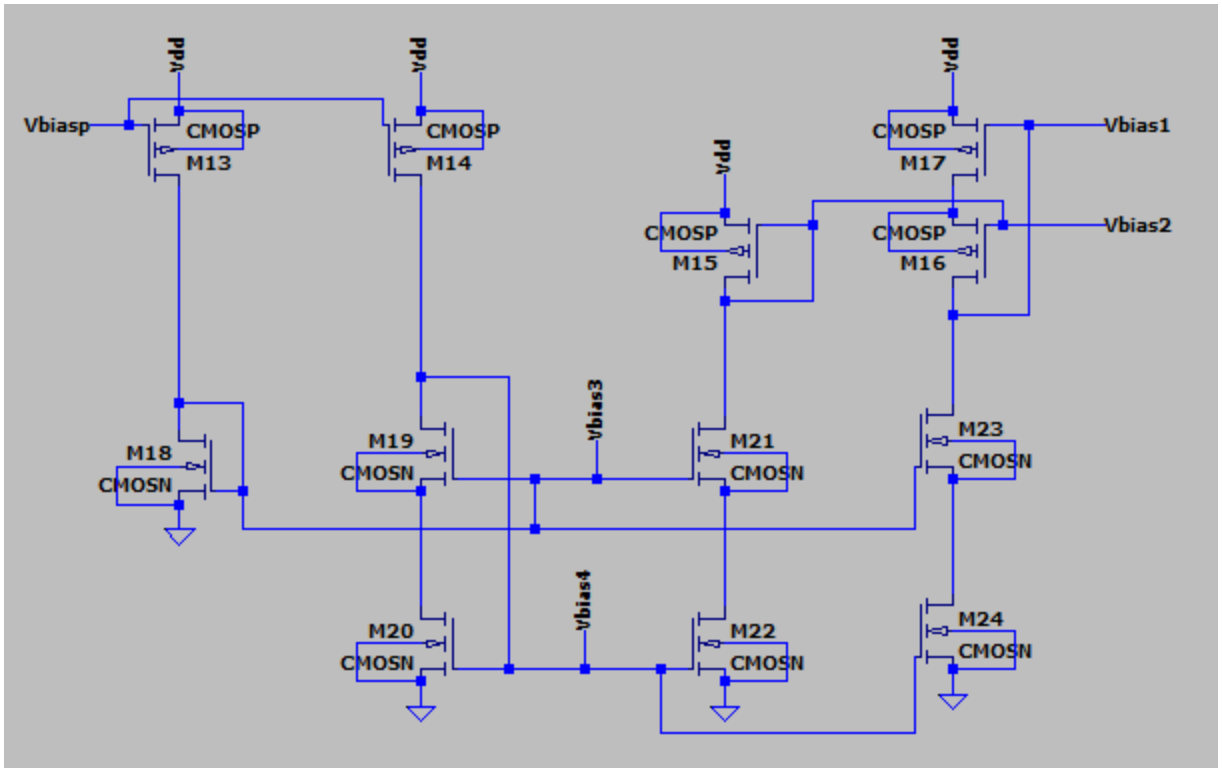
1. Beta Multiplier:



Vbiasp obtained = 1.1968V

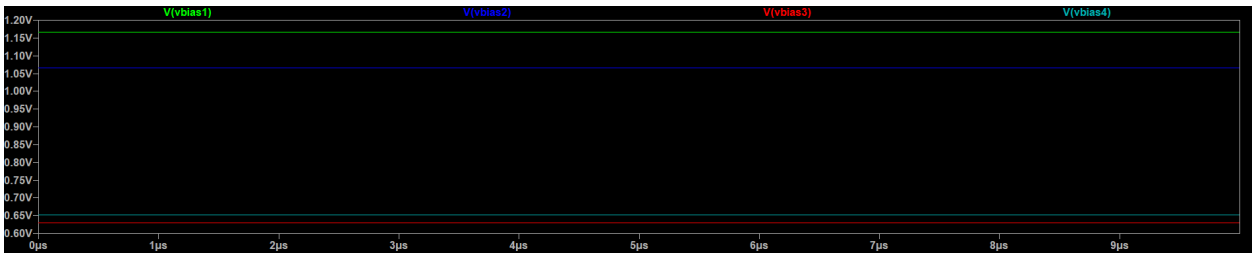


2. Cascode Current Mirror:

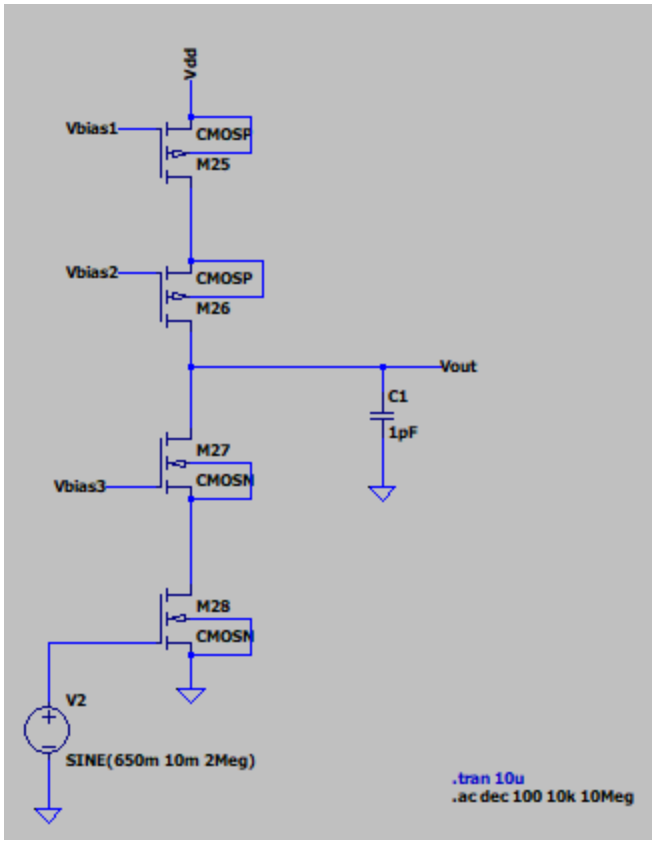


Vbias1, Vbias2, Vbias3, Vbias4 obtained are:

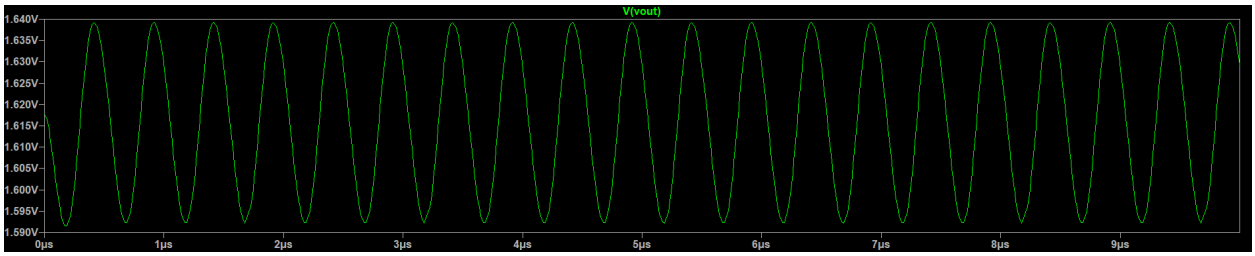
Vbias1 = 1.166V
Vbias2 = 1.063V
Vbias3 = 0.63V
Vbias4 = 0.653V



3. Cascode Amplifier:

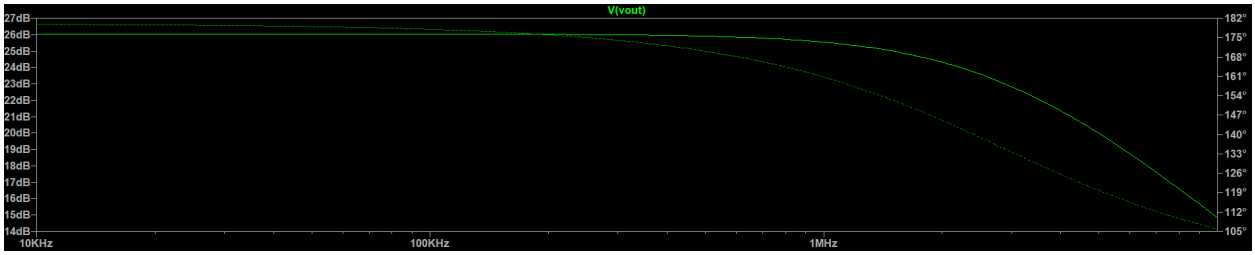


Output obtained:



Bode plot obtained:

Gain = 26.02 Db



Theoretical Calculations:

For 180nm :-

Target specifications :-

$A_V = 20 V/V$

Power dissipation $< 5mW$

Unity Gain BW $> 500 kHz$

$V_{DD} = 1.8V$, $\lambda = 0.09$

$V_{thN} = 0.5V$, $V_{thP} = -0.51V$

$\frac{1}{2}\mu_n C_{ox} = 175.4 \mu A/V^2$, $\frac{1}{2}\mu_p C_{ox} = -35.6 \mu A/V^2$

Calculations :-

Taking freq. pole location at $f_p = 2MHz$ (B.W > 500KHz)

$\therefore R_o = \frac{1}{2\pi f_p C_L} = \frac{1}{2\pi (2\times10^6) \times (10^{-12})} = 79,617.83 \Omega$

Now, $|g_m R_o| = \text{gain} = 20$

$g_m = \frac{20}{R_o} = 0.0002512 S$

$\therefore$ All MOSFET's are in sat. region & same current flows through all of them (in cascode amp.)

we know $V_{DS} = V_{GS} - V_{th} = V_{ov}$

→ from industrial std, drop across each MOSFET $= 0.2V$

For M_4, $V_{DS} = V_D - V_S = 0.2 \rightarrow V_D = 0.2V$

$V_S = 0$ ↙ Also, $V_{ov} = V_{GS} - V_{th} \rightarrow V_G = 0.2 + 0.5 = 0.7V$

hence $\boxed{V_{biasp} \leq V_G = 0.7V}$

For M_3, $V_{DS} = 0.2V = V_D - V_S$ ($V_S = 0.2V$) $= V_{ov}$

$$V_D = 0.4V$$

$$V_{GS} = V_{ov} + V_{th}$$

$$\Rightarrow V_G - 0.2 = 0.4 + 0.5 = 0.9V$$

$$\therefore \boxed{V_{bias3} < V_G = 0.9V}$$

For M_3, M_4; calculating $\left(\frac{W}{L}\right)$

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{th})$$

$$\left(\frac{W}{L}\right)_n = \frac{2.5 \times 10^{-4}}{2 \times 175.4 \times 0.2 \times 10^{-6}} = 3.563$$

& now, I_D, which is same for all MOSFET is given by,

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_n (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

$$= (175.4 \times 10^{-6})(3.563)(0.2)^2 (1 + 0.09 \times 0.2)$$

$$= 25.448\ \mu A$$

Now, For M_1 & M_2;

$$\left(\frac{W}{L}\right)_p = \frac{I_D}{\frac{\mu_p C_{ox}}{2} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})} = \frac{25.448 \times 10^{-6}}{(35.6 \times 10^{-6})(0.2)^2 (1 + 0.2 \times 0.09)}$$

$$\left(\frac{W}{L}\right)_p = 17.55$$

∴ For M_2,

$V_S = 1.6V$, $V_D = 1.4V$ $\longrightarrow$ $V_{SD} = 0.2V$

$V_{SG} = V_{SD} + |V_{thp}|$

$V_S - V_{SD} - |V_{thp}| = V_G$ (V_{bias2})

$V_{bias2} = 1.6 - 0.2 - 0.51 = \underline{0.89V}$

$V_{bias2} > 0.9V$

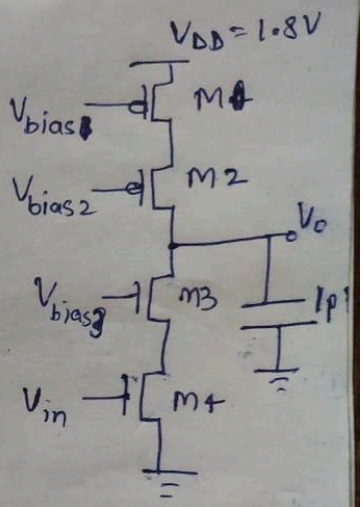
For $M1$,

$V_D = 1.6V$, $V_S = 1.8V$

$V_{bias1} = 1.8 - 0.2 - 0.5$

$= 1.1V$

in sat; for $\underline{V_{bias1} > 1.1V}$



Power dissipation = $V_{DD} \times I_D$

$= 1.8 \times 25.448\,\mu$

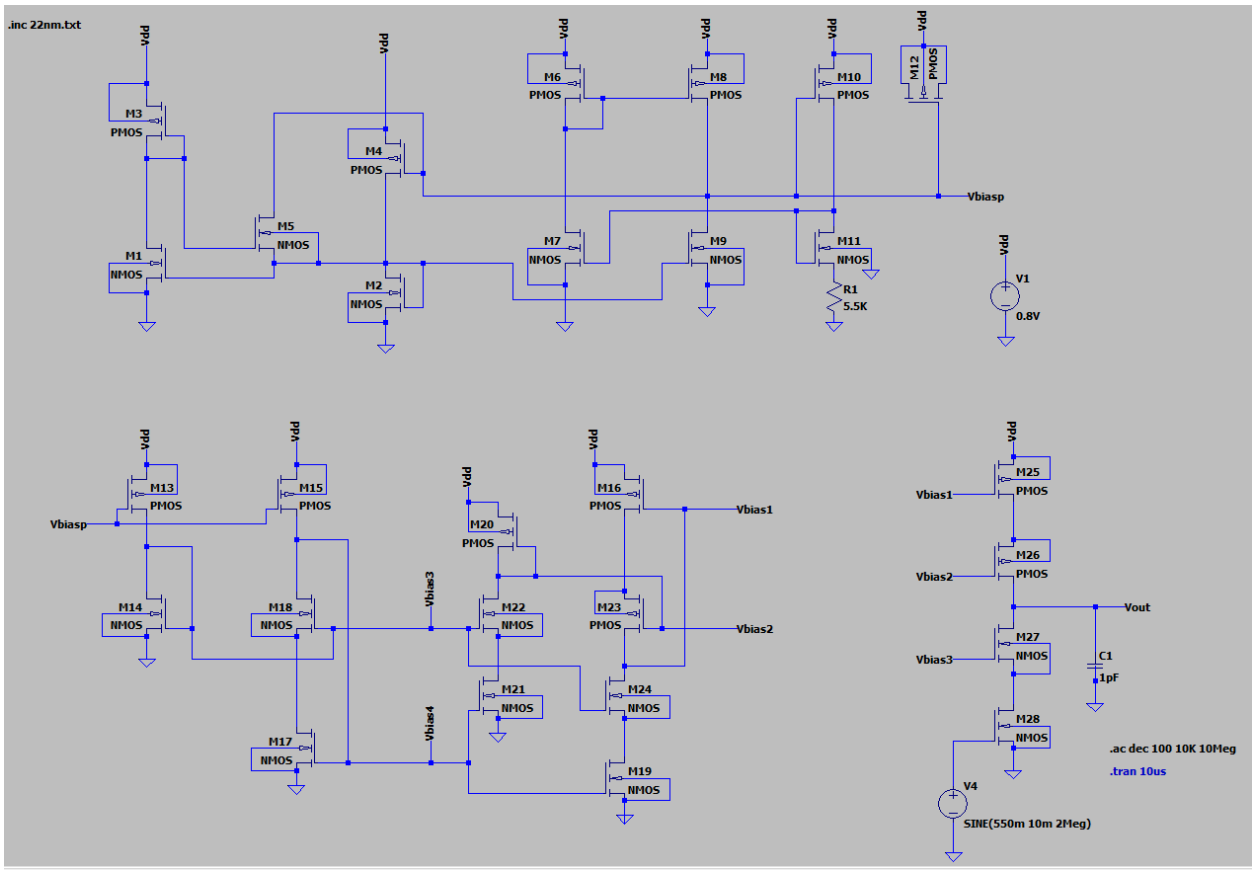
$= 45.80\,\mu W$

$= 0.045mw$ ($< 5mw$)

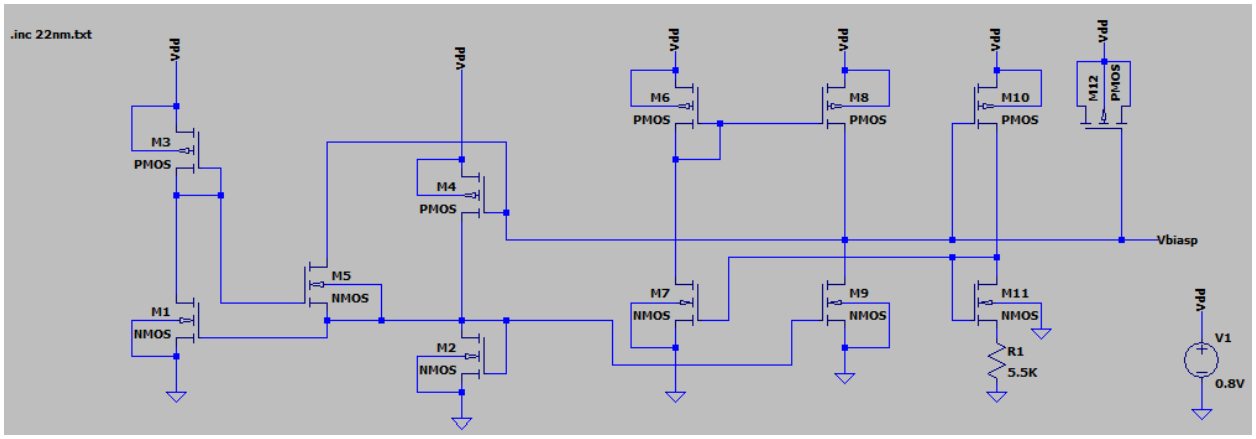
Comparision :-

	Theo.	Practical.
V_{biasp}	~~[illegible]~~	1.196V
V_{bias1}	$> 1.1V$	1.16V
V_{bias2}	$> 0.9V$	1.063V
V_{bias3}	$< 0.9V$	0.63V
V_S (offset)	0.7	0.640V
A_V	$\simeq 26$	26.02
P.D	$< 5mw$	0.045 mw

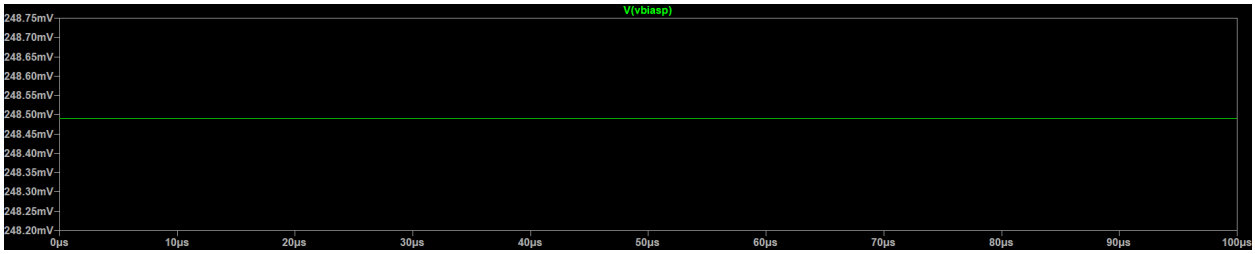
For 22nm:



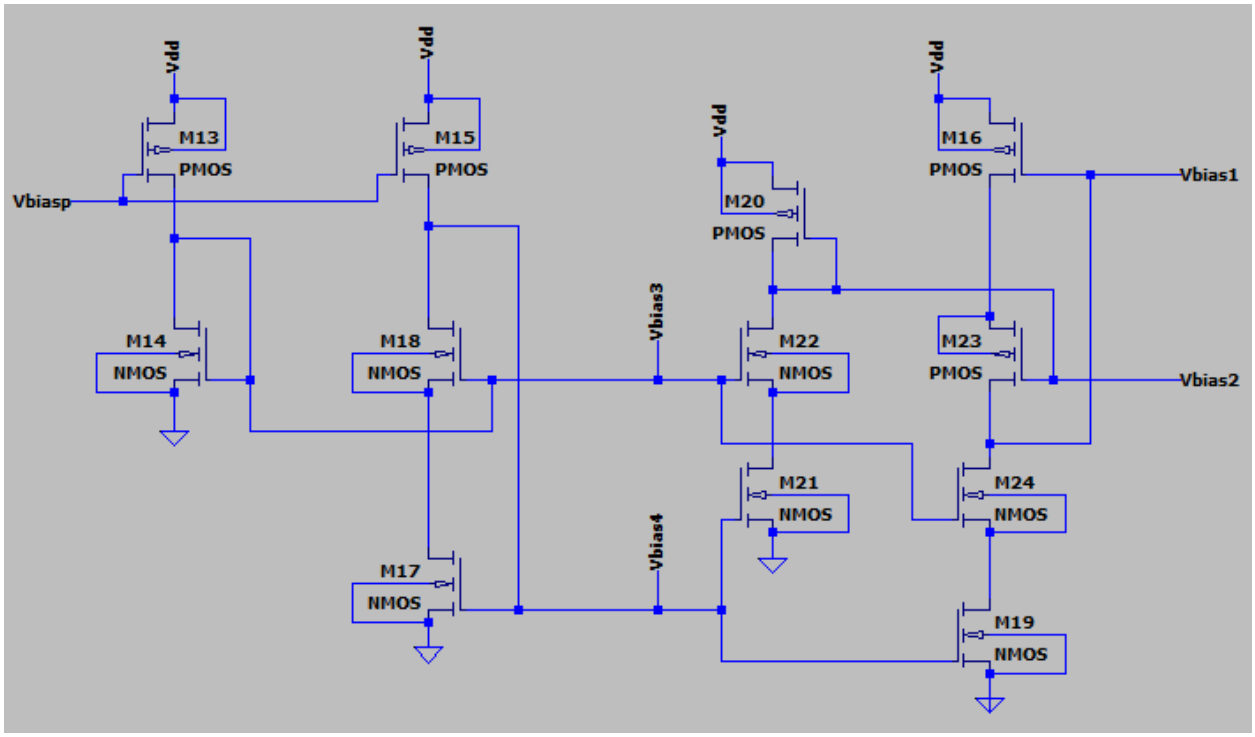
1. Beta Multiplier:



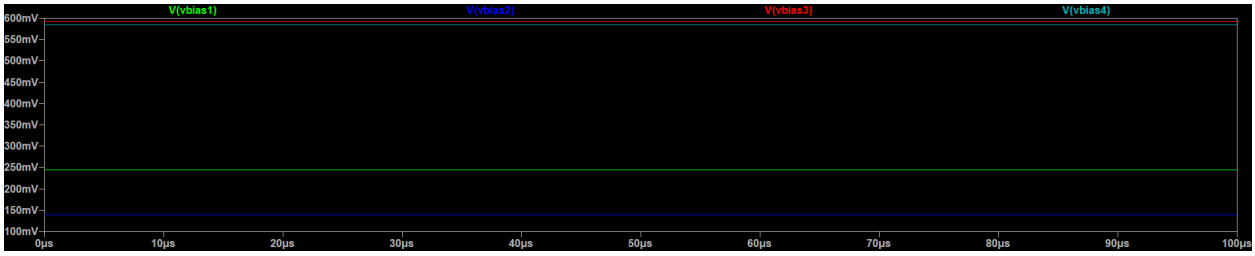
Vbiasp obtained = 248.5 mV



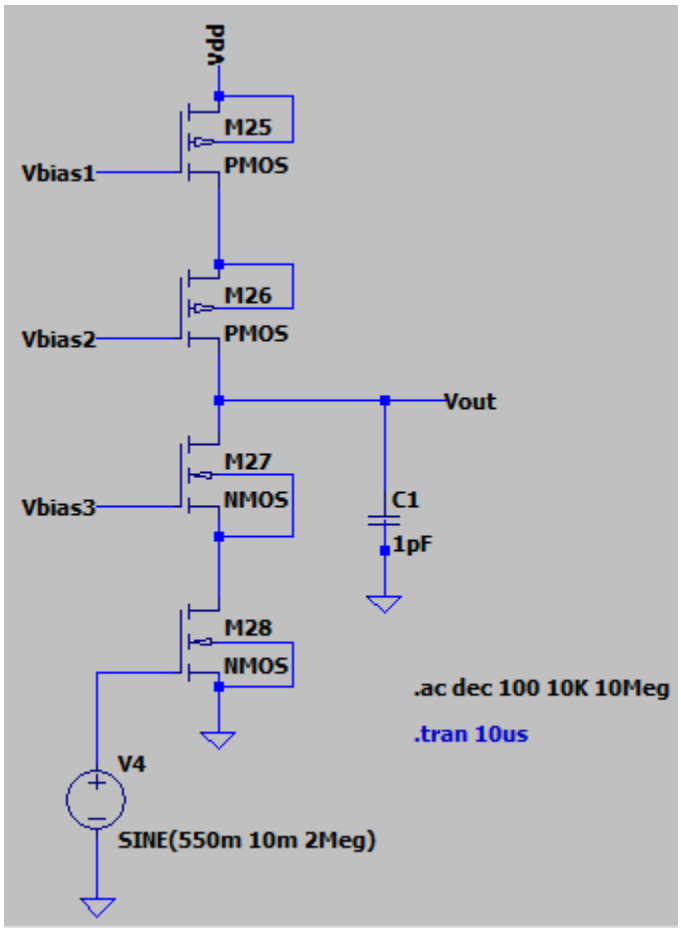
2. Cascode Current Mirror:



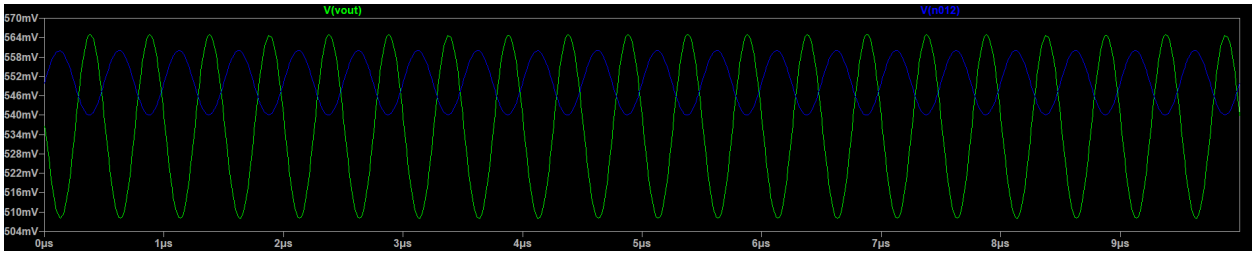
Vbias1, Vbias2, Vbias3, Vbias4 obtained are:
Vbias1 = 244.4mV
Vbias2 = 137.2mV
Vbias3 = 593.8mV
Vbias4 = 584.4mV



3. Cascode Amplifier:

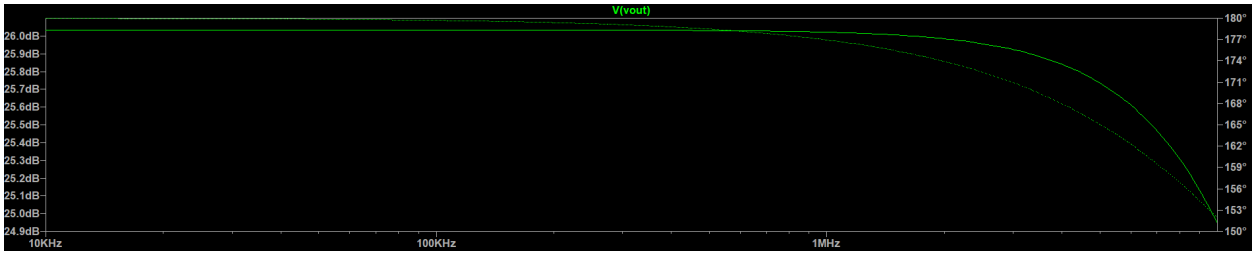


Output obtained:



Bode Plot:

Gain = 26.01 Db



Theoretical Calculations:

For 22nm :-

Target Specification :

$A_V = 20\ V/V$
$V_{DD} = 0.8V$
$C_L = 1pF$
$V_{thn} = 0.503\ V$
$V_{thp} = -0.3606$

Power dissipation < 5mw
Unity Gain BW > 500 kHz
$\lambda = 0.09$
$\mu_n C_{ox} = 100\ \mu A/V^2$
$\mu_p C_{ox} = 50\ \mu A/V^2$

Calculations :-

Taking freq. pole location $f_p = 2\ MHz$

$$R_{out} = \frac{1}{2\pi f_p C_L} = \frac{1}{2\pi (2\times10^6)(10^{-12})} = 79617.83$$

$$|g_m R_o| = 20 \rightarrow g_m = \frac{20}{R_{out}} = 2.5\times10^{-4}\ S$$

$V_{DS} = 0.2V$ (by industry standards)

$\rightarrow V_{DS} = V_{GS} - V_{th} = V_{ov} = 0.2V$

$$\rightarrow I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_N (V_{ov})^2(1+\lambda V_{DS}) \text{ or } g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_{ov})$$

$$2.5\times10^{-4} = 100\times10^{-6}\left(\frac{W}{L}\right)_N (0.2)$$

$$\left(\frac{W}{L}\right)_N = 12.5$$

$$\therefore I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right) V_{ov}^2 (1+\lambda V_{DS})$$

$$= \frac{1}{2}\times100\times10^{-6}\times12.5\times(0.2)^2\times(1+0.09\times0.2)$$

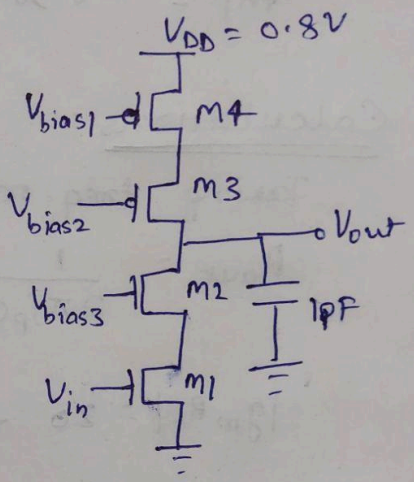
$$= 25.45\ \mu A$$

∵ cascode connection is in saturation region. Hence same current flows through all PMOS also.

$$\therefore I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{ov})^2 (1+\lambda V_{DS})$$

$$25.45 \times 10^{-6} = \frac{1}{2}(50\times 10^{-6})\left(\frac{W}{L}\right)_p (0.2)^2 (1+0.09\times 0.2)$$

$$\left(\frac{W}{L}\right)_p = 25$$



Now, for M1

$V_{DS} = 0.2 = V_D - 0V$

$V_{GS} = V_{ov} + V_{th} = 0.2 + 0.3$

$V_G = 0.5V$

For M2,

$V_D = 0.4V$

$\therefore V_{DS} = 0.2V \quad (\because V_S = 0.2V)$

$V_{DS} \geq V_{ov}$ or $V_{GS} = V_{ov} + V_{th}$

$\therefore V_{bias3} = 0.2 + 0.3 + 0.2 = \underline{0.7V}$

For M3,

$V_{SD} = 0.2V = V_S - V_D$.

$\therefore V_S = 0.2 + 0.4 = 0.6V$

$V_{SD} = V_{SG} - |V_{thP}| = V_{ov}$

$\therefore V_S - V_G - |V_{thP}| = V_{ov}$

$V_G = V_S - |V_{thP}| - V_{ov} = 0.6 - 0.2 = 0.36 - 0.2 = 0.04V$

$\underline{V_{bias2} \geq 0.04V}$

For M4, $V_{SD} = 0.2V$

$V_S = 0.2 + 0.6 = 0.8V$

$V_S - V_G - |V_{thP}| = V_{ov}$

$V_G = V_S - |V_{thP}| - V_{ov} = 0.8 - 0.36 - 0.2$

$V_G = 0.24V$

$V_{bias1} \geq 0.24V$

Power dissipation $= V_{DD} \times I_D$

$= 0.8 \times 25.45\mu$

$= 20.36\mu w$

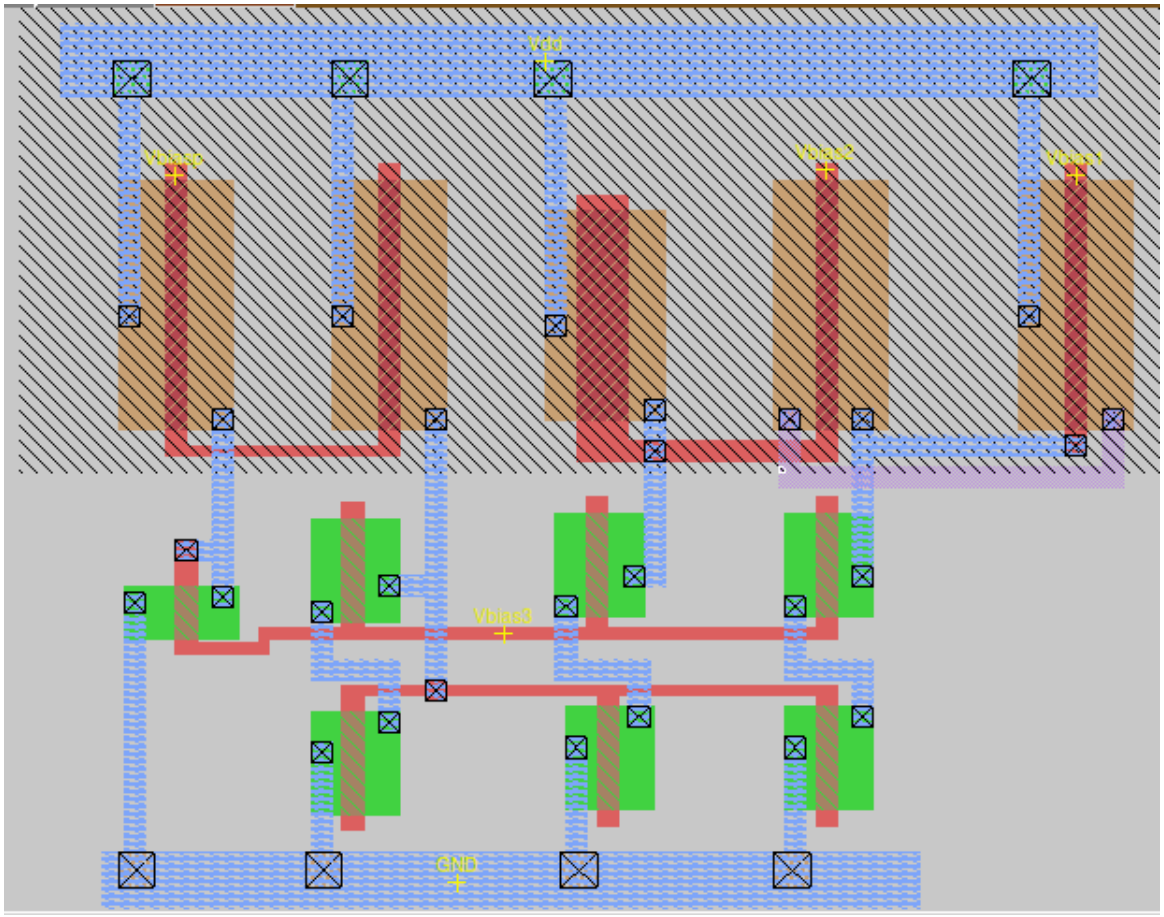
$= 0.02036\,mw < 5mw$

Comparision :-

	Theo.	Practical:
V_{biasp}	–	248.5mV
V_{bias1}	$\geq 0.24V$	0.2444 V
V_{bias2}	$\geq 0.04V$	0.137 V
V_{bias3}	$\leq 0.7V$	0.5938 V
V_S (offset)	0.5 V	0.55V
A_v	26dB	26.01 dB
p.D.	$< 5mw$	0.0203 mw

Magic Layouts:

1. Current Mirror:




```
varun@varun: ~/Desktop/magic/CurrentMirror
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model nfet
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model pfet
Warning: Ps = 0 is less than W.

Initial Transient Solution
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Node                                   Voltage
----                                   -------
vbias1                             1.86975e-08
vdd                                        1.8
vbias2                             1.07207
vbias3                             0.658032
vbiasp                                 1.196
v2#branch                                  0
v1#branch                          -3.21041e-05
```
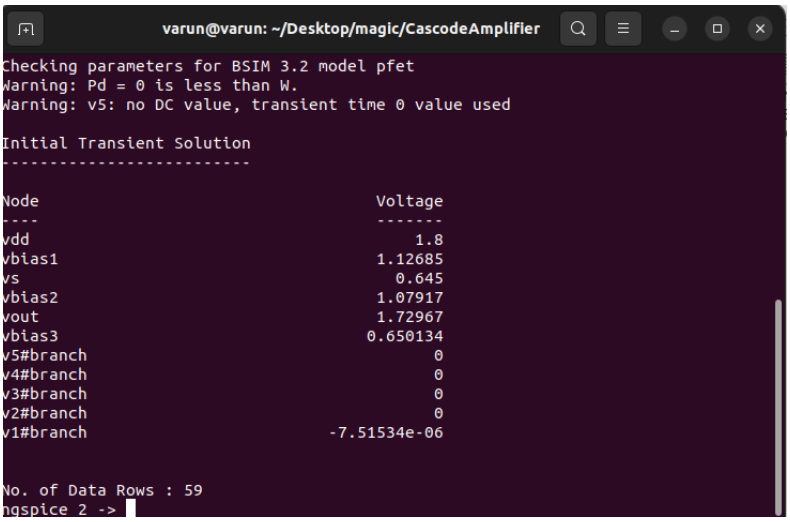
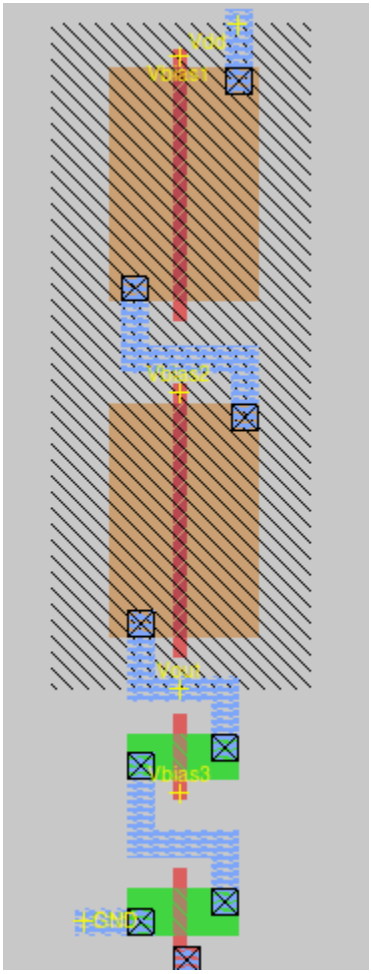

2. Cascode Amplifier:





Conclusion:

- The target specifications were obtained for both the 180nm and 22nm technologies.
- A gain of near about 26db was obtained in both the cases.
- DC offset value was chosen such that to obtain the desired expectations.
- Unity gain bandwidth greater than 500kHz was achieved both the cases.
- The frequency pole was taken to be 2MHz in both the cases.
- Gain was affected by the input frequency as well.