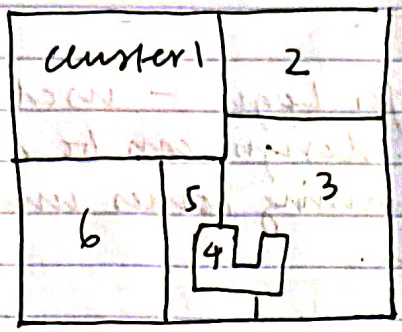
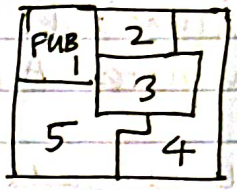
Chip Design – Notes #1

- RTL - Register Transfer Logic – used to define logic of the chip components. The design can be done only after logic is finalised. Logic forming comes under domain of Computer Architecture.
- RTL is coded using Verilog – translates logic to simple syntactical statements.
- RTL is verified by checking edge cases – extreme situations in which logic could fail.
- After Verilog code is written, there are two ways to proceed: hand drawn circuits, and synthesis based circuits.
- 80 – 90% of chips are designed using synthesis (currently)
- Hand drawn designs are better in most cases, especially when there is structure to the chip. However, they are time consuming.
- During design, different factors need to be considered such as AREA, POWER, TIMING, NOISE etc.
- Chip is divided into CLUSTERS, and clusters are divided into FUB's.
- Each FUB usually is designed by a separate team.



ZOOMED IN CLUSTER 1



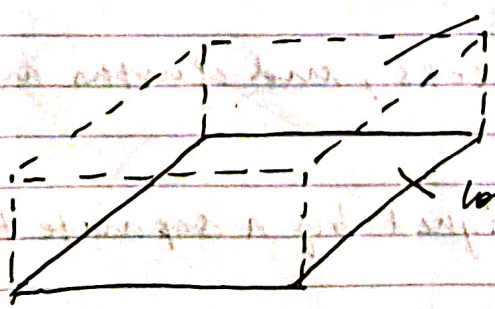
PLACEMENT

- In placement, area, power, time, noise should be considered.

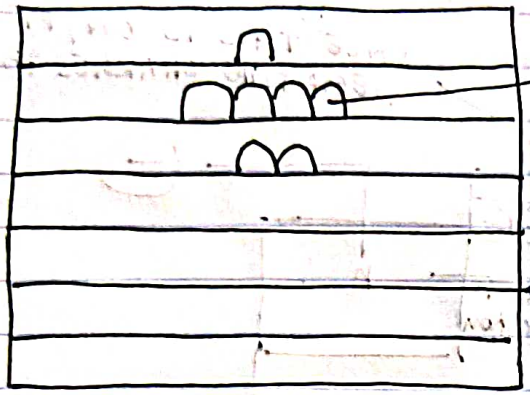
1. Area – smaller the area of PUB's, the better.
2. Power – lower the power consumption the better.
3. Time – External specs given to product should align with the time it takes for signal to flow through chip
4. Noise – should be minimum. Happens when signals get changed.

NOTE: Time from source of power to destination should be considered, not just within chip boundary.

STRUCTURE OF CHIP



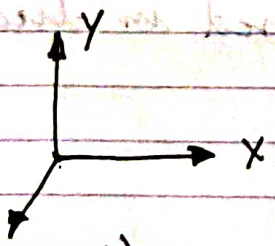
- ENLARGED LOWER SURFACE



- The logic of how current should flow through the chip is provided by the library team. The placement of the chip is optimized taking into account this

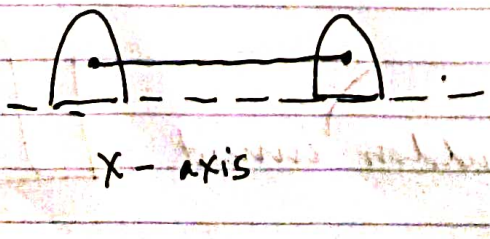
- Library teams group logic into units and provide those units to the placement teams.

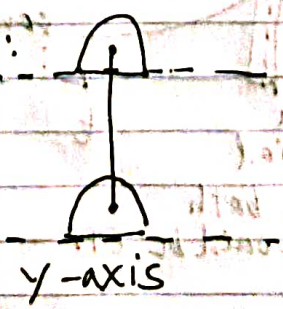
- These units are placed in such a way that wiring between them can be done with the least strain. i.e. taking into account wire path length, congestion etc.



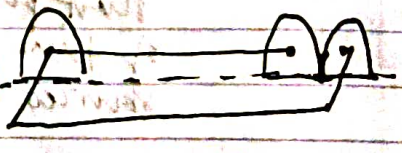
wires can be arranged in X, Y and Z axes.

- When different axes wires are used:



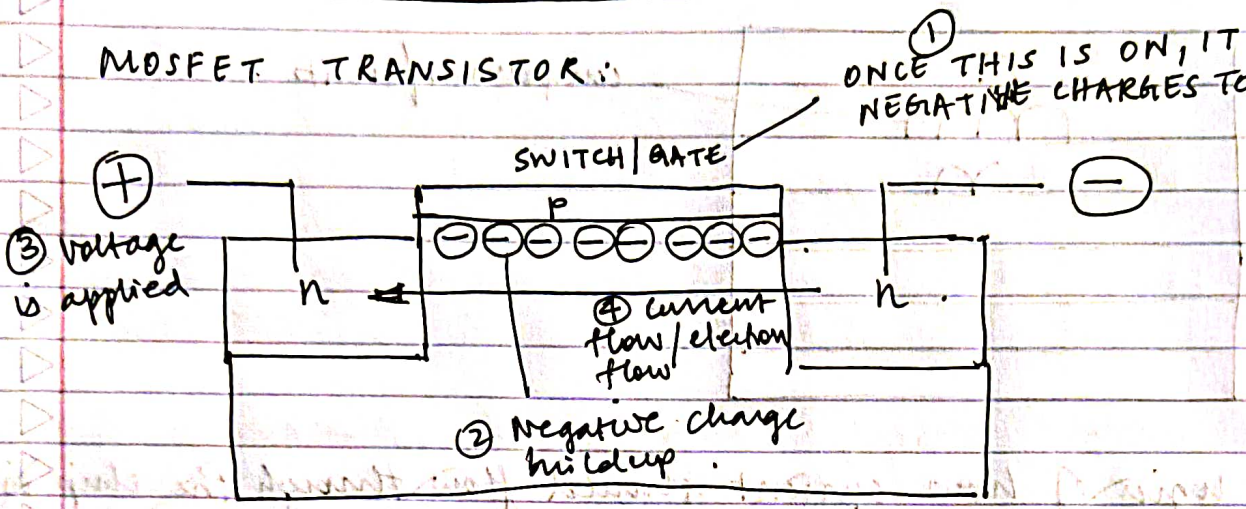


Z-AXIS, IS ONLY USED WHEN NON ADJACENT UNITS NEED TO TALK.



HOW LOGIC IS TRANSFORMED INTO CURRENTS

MOSFET TRANSISTOR:

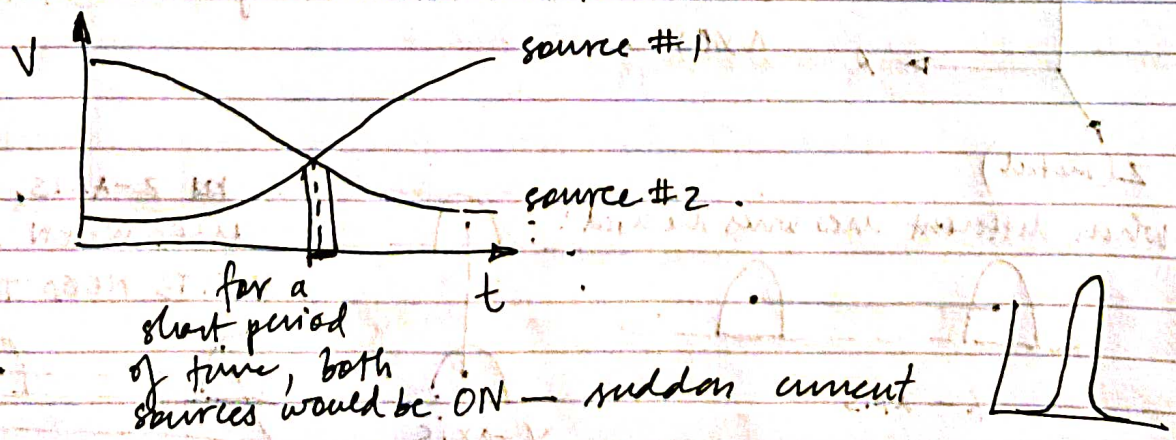


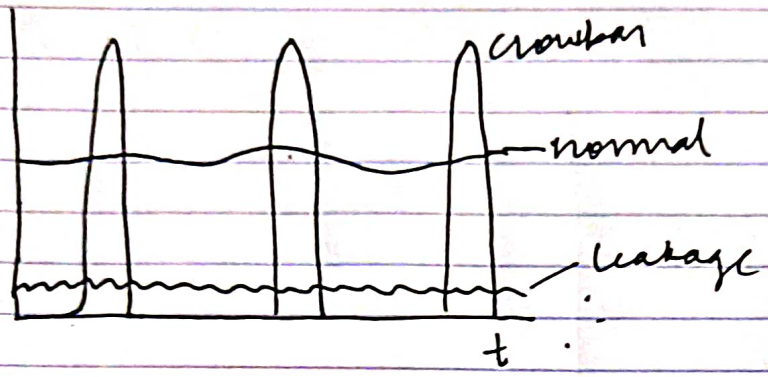
Steps ① – ④ are involved in acting as a switch/gate for current to flow.

Leakage and Crowbar currents

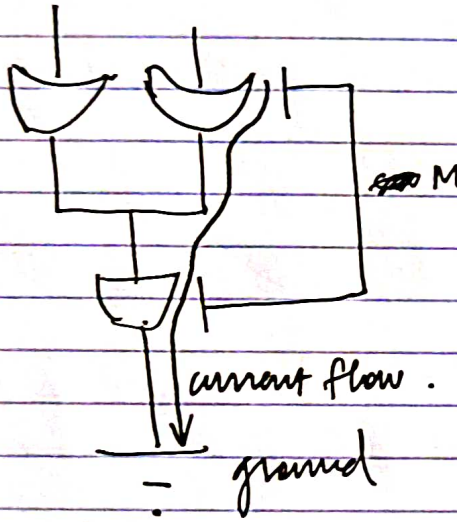
Leakage current – due to drift / reverse movement of electrons to expected flow direction. Small effect.

Crowbar currents – if voltages are reversed in direction, currents would look like this:





The area under the curve is proportional to total power consumption.



The MOSFETS between logic units can trigger / stop currents.

Potential areas where AI can be used:

1. Routing (Cadence) on motherboards – if RL / Deep learning can help find a single solution, all solutions can be found.
2. Optimization in P&R (already active research area)
3. Verilog code generation