2-Bit Arithmetic Logic Unit (ALU)

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1 Abstract

This report presents the design and analysis of a 2-Bit Arithmetic Logic Unit (ALU) implemented using basic logic gates (AND, OR, NAND, NOT) and simulated using Cadence Virtuoso at a 90 nm CMOS technology node. The ALU is designed to perform basic arithmetic and logical operations, including addition, subtraction, AND, OR, NAND, and NOT operations. The design is verified through simulation, and the results are analyzed for performance metrics such as delay, power consumption, and area. The project demonstrates the successful implementation of a 2-bit ALU, which can be extended to higher-bit ALUs for more complex applications.

2 Introduction:

An Arithmetic Logic Unit (ALU) is a fundamental component of a computer's central processing unit (CPU) that performs arithmetic and logical operations. This project focuses on designing a 2-bit ALU using basic logic gates (AND, OR, NAND, NOT) and simulating it using Cadence Virtuoso at a 90 nm CMOS technology node. The ALU is designed to perform basic operations such as addition, subtraction, AND, OR, NAND, and NOT. The design is verified through simulation, and the results are analyzed for performance metrics such as delay, power consumption, and area.

3 Applications:

The 2-bit ALU has a wide range of applications, including:

- Microprocessors: Used in CPUs to perform arithmetic and logical operations.
- Embedded Systems: Used in microcontrollers for control and data processing.
- Signal Processing: Used in digital signal processing (DSP) systems for arithmetic operations.
- Industrial Automation: Used in control systems for logic-based decision-making.
- Educational Purposes: Used as a teaching tool to demonstrate the working of ALUs in computer architecture.

4 State of the Art

Below is a table summarizing the evolution of ALUs, including their types, technology nodes, and performance metrics.

Year	**Type**	**Technology Node**	**Performance Metrics**	**Cost (Approx.)**	**Use Case**
1980s	4-bit ALU	1 μm	Low speed, high power	100–200	Early microprocessors
1990s	8-bit ALU	500 nm	Moderate speed, power	50–100	Embedded systems
2000s	16-bit ALU	180 nm	High speed, low power	20–50	DSP and industrial automation
2010s	32-bit ALU	90 nm	Very high speed, low power	10–20	Modern CPUs and microcontrollers
2020s	64-bit ALU	7 nm	Ultra-high speed, ultra-low power	5–10	High-performance computing

Table 1: Evolution of ALU Technologies with Technology Nodes, Performance, Cost, and Use Cases

5 Design Requirements:

The design requirements for the 2-bit ALU are as follows:

Component	**Component Value**	**Quantity**
AND Gate	2-input	2
OR Gate	2-input	2
NAND Gate	2-input	2
NOT Gate	1-input	2
CMOS Transistors	90 nm	20
Power Supply (Vdd)	3.8 V	1
Ground (GND)	0 V	1

Table 2: Design Requirements for the 2-bit ALU

6 Working Principle:

- The 2-bit ALU performs the following operations based on the
- control signals:
- Arithmetic Operations: Addition and subtraction.
- Logical Operations: AND, OR, NAND, and NOT.
- Control Signals: S1, S0: Control signals that determine the operation to be performed.

  A, B: 2-bit input operands.

Y: 2-bit output result.

S1	S0	Operation	Output (Y)
0	0	AND	Y = A AND B
0	1	OR	Y = A OR B
1	0	NAND	Y = A NAND B
1	1	NOT	Y = NOT A

Table 3: Truth Table for Logic Operations

7 Software Implementation:

The software implementation involves simulating the 2-bit ALU using Cadence Virtuoso. The simulation helps in verifying the circuit's functionality before hardware implementation. Key steps include:

8 AND GATE

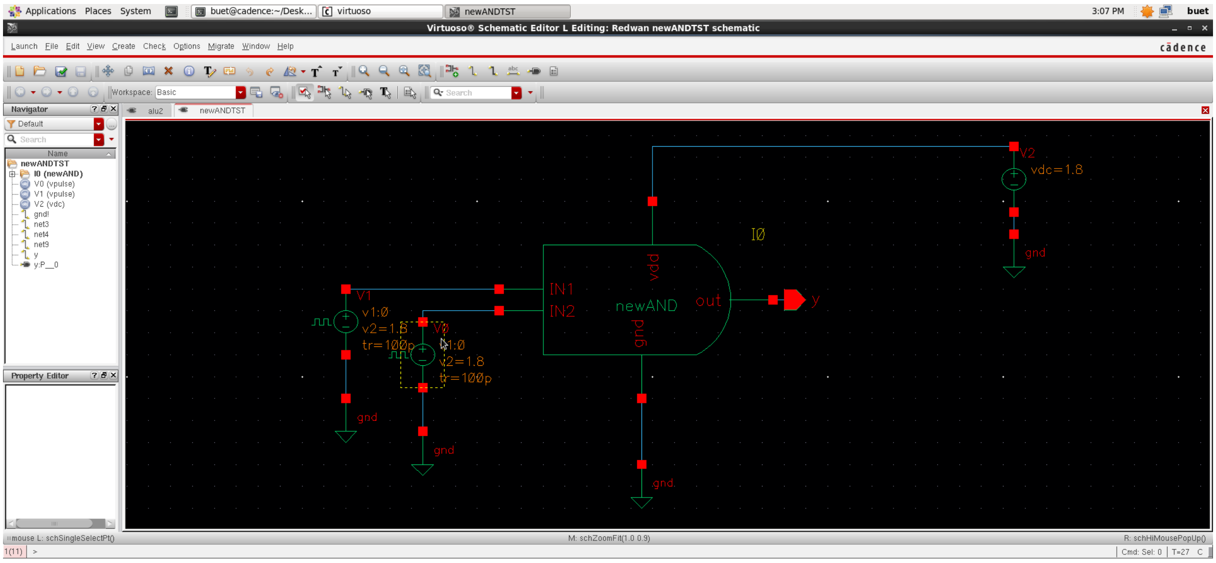

Fig1: AND Gate implementation

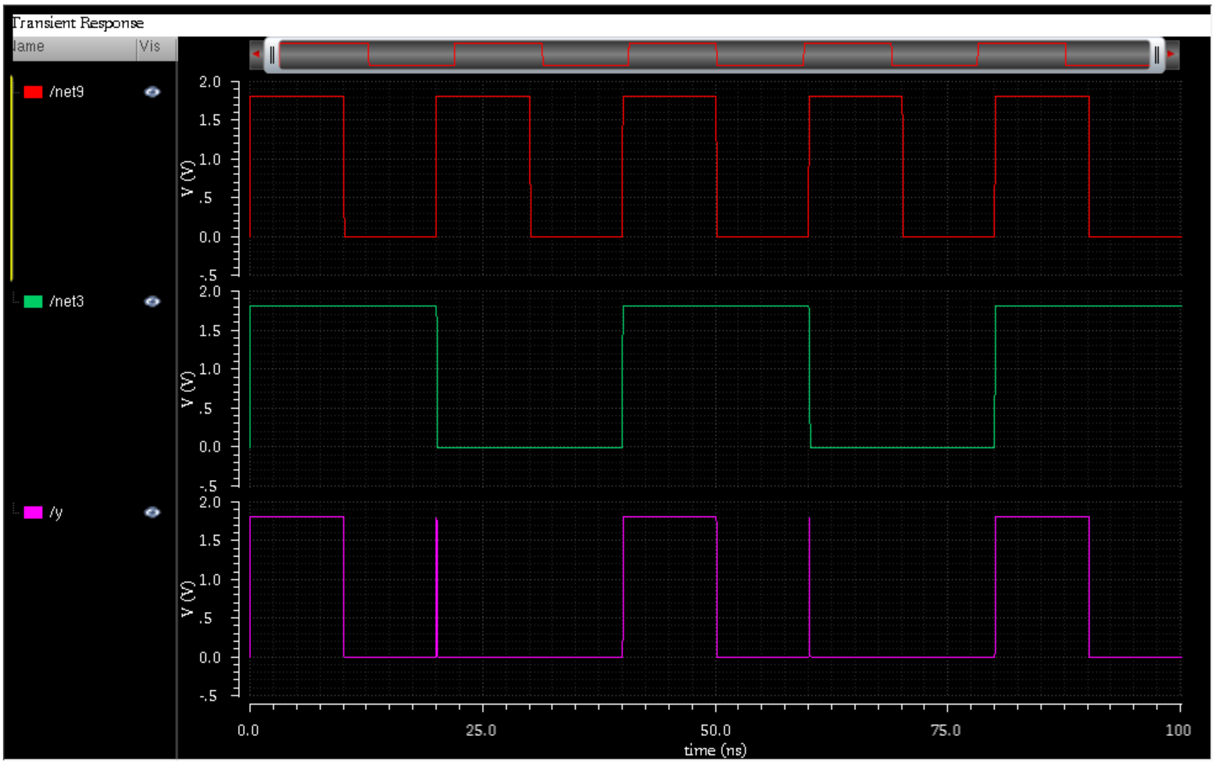

Fig1: AND Gate Output

9 OR GATE

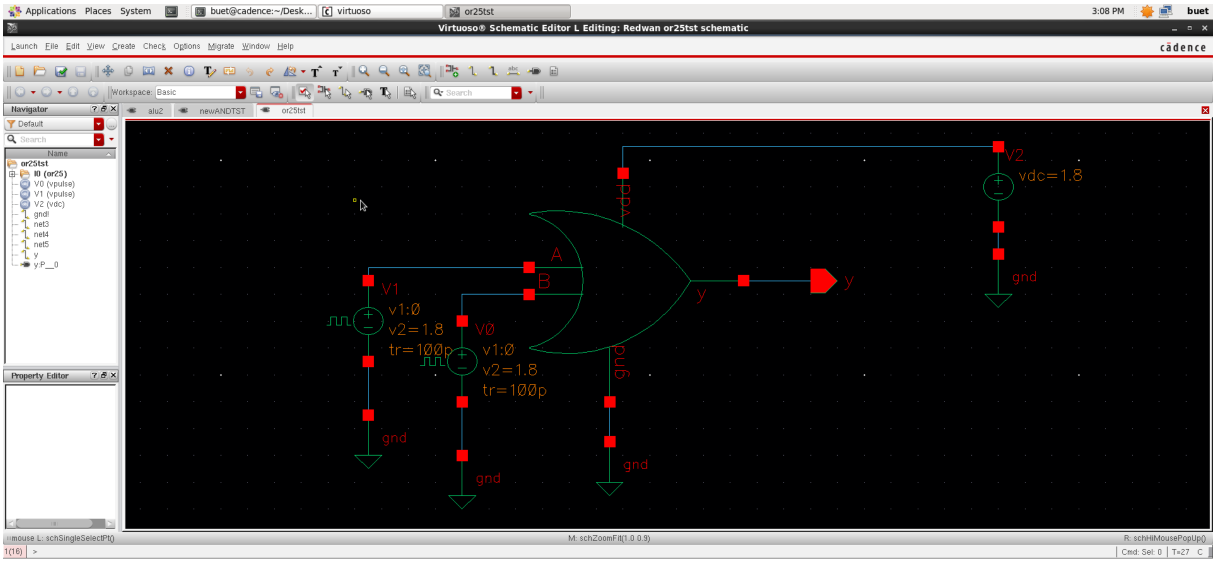

Fig1: OR Gate implementation

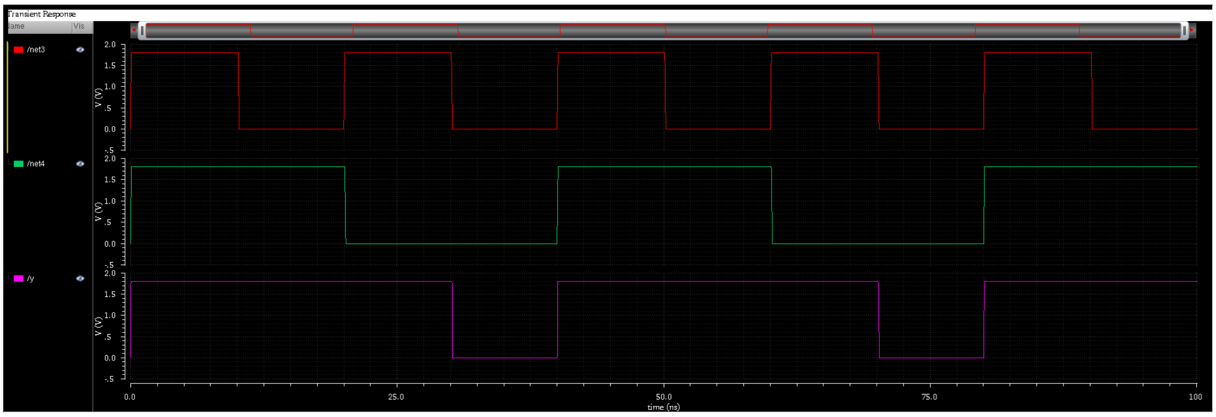

Fig1: OR Gate Output

10 NAND GATE

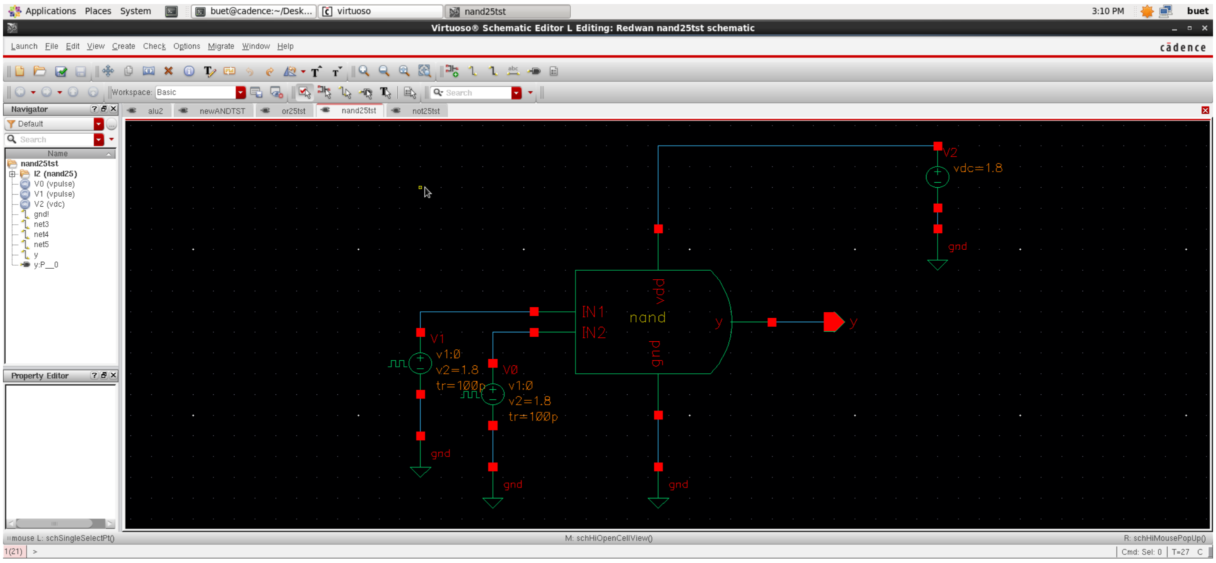

Fig1: NAND Gate implementation

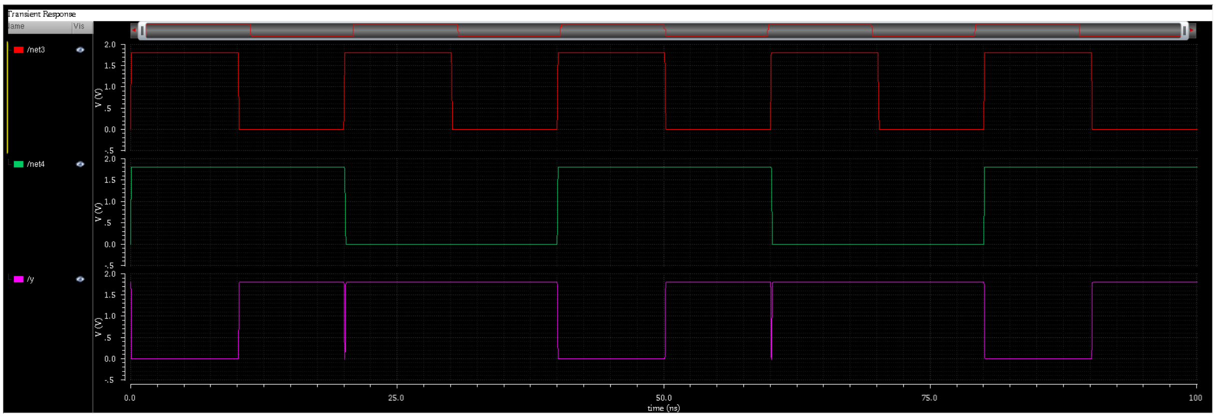

Fig1: nand Gate output

11 NOT GATE

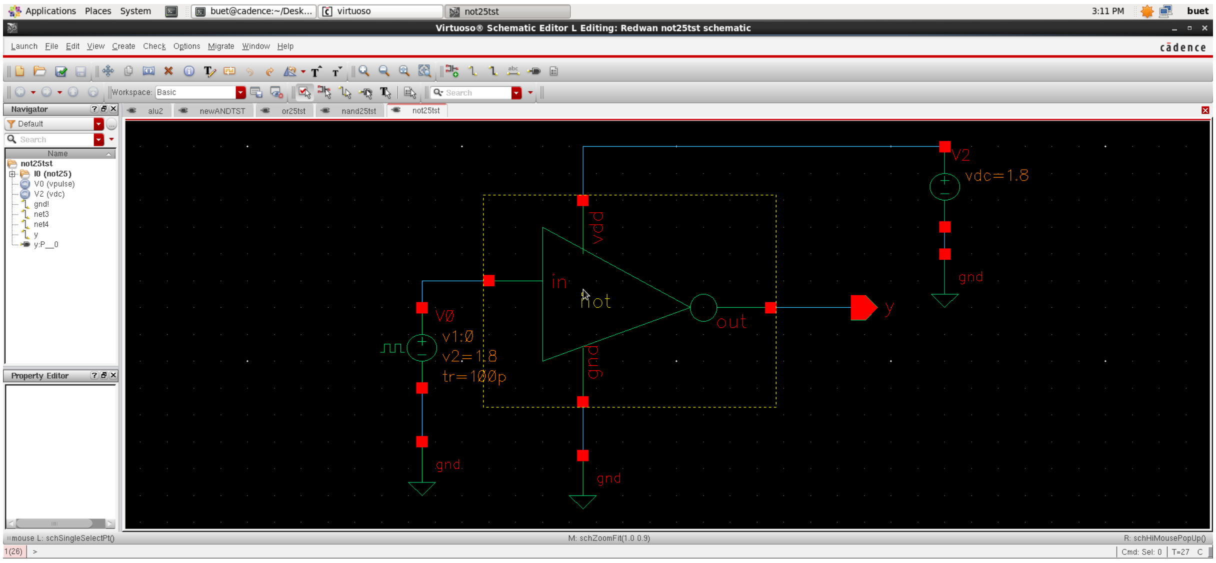

Fig1: NOT Gate implementation

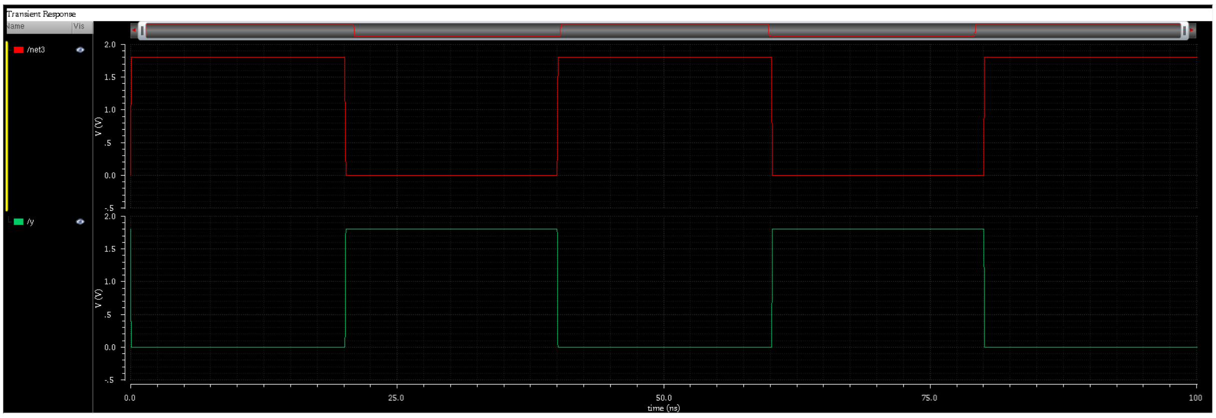

Fig1: NOT Gate Output

12 ALU

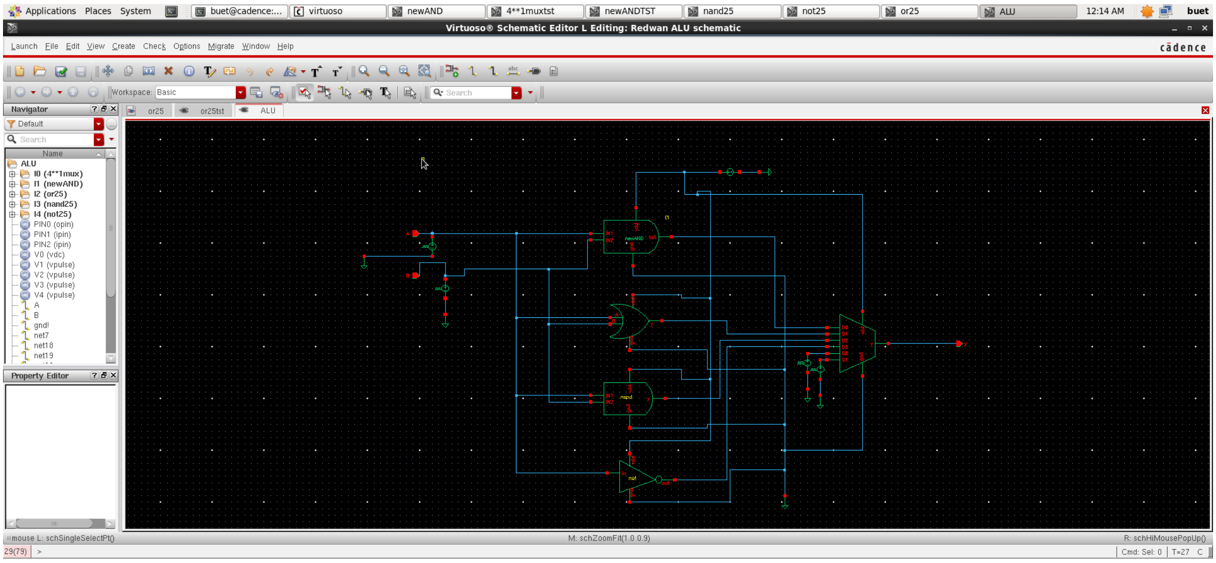

Fig1: ALU implementation

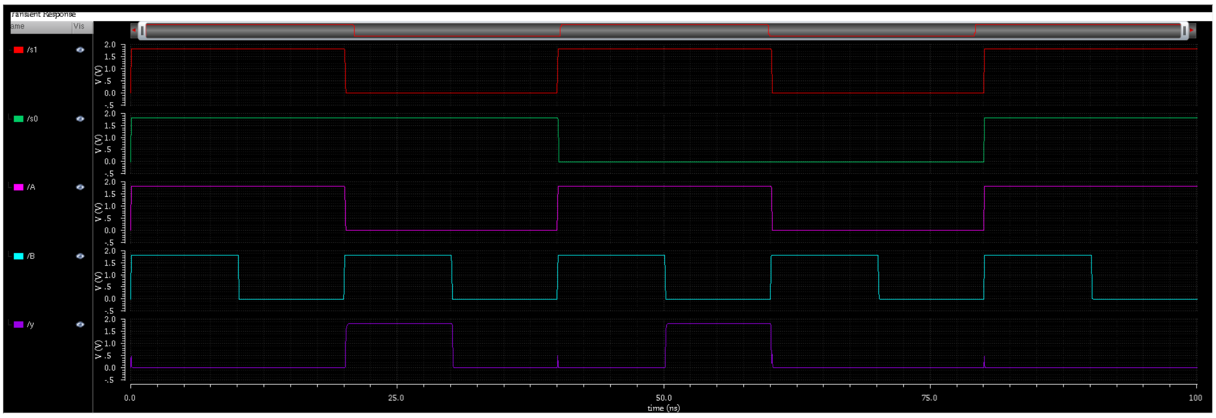

Fig1: ALU Output

13 Video Link :

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14 Conclusion:

The 2-bit ALU was successfully designed and implemented using basic logic gates (AND, OR, NAND, NOT) and simulated using Cadence Virtuoso at a 90 nm CMOS technology node. The design was verified through simulation, and the results were analyzed for performance metrics such as delay, power consumption, and area. The project demonstrates the successful implementation of a 2-bit ALU, which can be extended to higher-bit ALUs for more complex applications.

15 References

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