6T SRAM DC Analysis

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1 6-T Static RAM (SRAM)

A **6-T Static RAM (SRAM)** is a type of volatile memory that uses six transistors (6-T) to store a single bit of data. It is called "static" because it does not require periodic refreshing to retain data, unlike Dynamic RAM (DRAM). SRAM is faster and more reliable than DRAM but is more expensive due to its higher transistor count. It is commonly used in cache memory and high-speed applications.

Figure 1: SRAM

2 Applications of a SRAM

1. Cache Memory: Used in CPUs and GPUs for high-speed data access.
2. Embedded Systems: Used in microcontrollers and IoT devices for fast data storage.
3. Networking Devices: Used in routers and switches for buffering and fast data processing.
4. FPGA and ASIC Designs: Used in programmable logic devices for on-chip memory.
5. Consumer Electronics: Used in smartphones, tablets, and laptops for high-speed memory access..

3 Comparison

Type	Volatility	Speed	Power Consumption	Use Case
6-T SRAM	Volatile	Very High	High	High-speed cache memory
DRAM	Volatile	High	Moderate	Main memory in computers
Flash Memory	Non-Volatile	Moderate	Low	Storage in USB drives, SSDs
ROM	Non-Volatile	Low	Very Low	Firmware storage

4 Working Principle

- A 6-T SRAM cell consists of six transistors: four transistors form two cross-coupled inverters to store the data, and two transistors act as access transistors to control read and write operations.
- Key Components:
- Cross-Coupled Inverters:
- Two inverters are connected in a feedback loop to store a single bit of data (0 or 1).
- The output of one inverter is connected to the input of the other, creating a stable state.
- Access Transistors:
- Two transistors (NMOS or PMOS) are used to control access to the cell during read and write operations.
- These transistors are connected to the bit lines (BL and BLB) and the word line (WL).

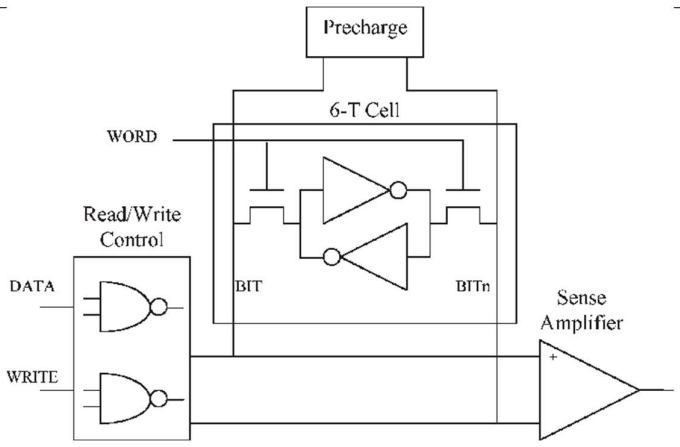


Figure 2: Block Diagram of a SRAM

5 Design Requirements

Component	Component Value	Quantity
Transistor (NMOS)	0.18µm	4
Transistor (PMOS)	0.18µm	2
Power Supply (Vdd)	1.8V	1
Capacitor	1pF	1
Component	Component Value	Quantity

Table 2: Design Requirements

6 Working of the Circuit

Working:

- **Write Operation:**
    - The word line (WL) is activated, and the bit lines (BL and BLB) are driven to the desired values (0 or 1).
    - The cross-coupled inverters latch the new data.
- **Read Operation:**
    - The word line (WL) is activated, and the bit lines (BL and BLB) sense the stored data.
    - The sense amplifiers detect the voltage difference on the bit lines to determine the stored value

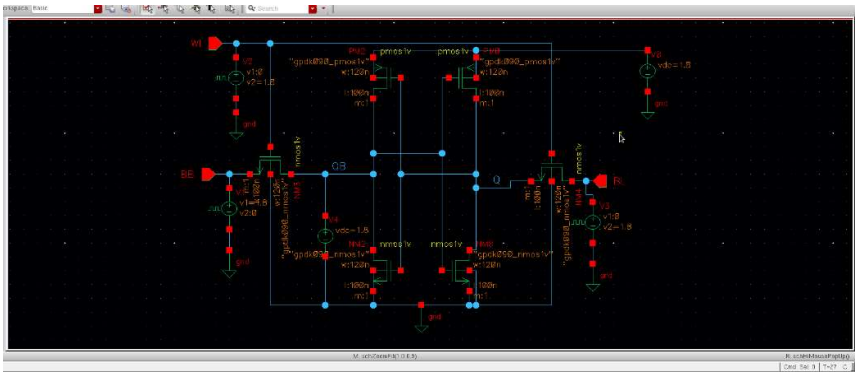


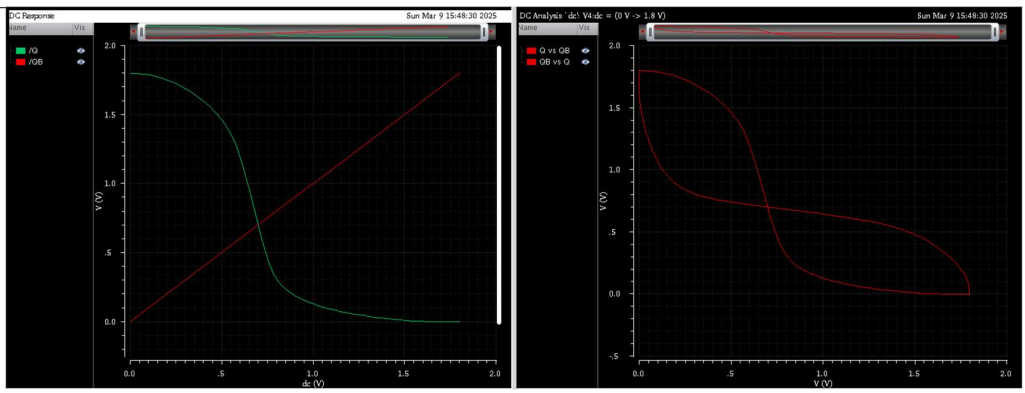
Figure 3: SRAM Schematic

Generation of Output Wave:

DC Analysis

- Objective: To determine the DC operating point of the 6-T SRAM cell.
- Procedure:
- Apply a DC voltage (Vdd = 1.8V).
- Measure the DC voltage at each node.
- Results:
- DC Voltage at Storage Nodes: Approximately Vdd/2 (0.9V) when the cell is in a stable state..

Generation of Output Wave:



7 Conclusion

The 6-T Static RAM (SRAM) is a critical component in high-speed memory applications, offering fast access times and reliable data storage. By performing AC, DC, and transient analyses in Cadence, we were able to verify the performance of the 6-T SRAM cell, including its read/write speed and stability. The designed 6-T SRAM cell demonstrates a write time of 100ps and a read time of 50ps, making it suitable for high-speed cache memory and embedded systems.