# IMPLEMENTATION OF A POWER FACTOR COMPENSATOR

A Report submitted to

MSRIT

Bangalore

for partial requirement of award of degree of

*Bachelor of Engineering in Electrical and Electronics Engineering*

by


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M S RAMAIAH INSTITUTE OF TECHNOLOGY

(Autonomous Institute, Affiliated to VTU)

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Department of Electrical and Electronics Engineering

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Bangalore – 54

# CERTIFICATE

This is to certify that the following students, who were working under our guidance, have completed their work as per our satisfaction with the topic "**IMPLEMENTATION OF A POWER FACTOR COMPENSATOR**". To the best of our understanding the work to be submitted in this report does not contain any work, which has been previously carried out by others and submitted by the candidates for themselves for the award of any degree anywhere.

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# DECLARATION

We hereby declare that the entire work embodied in this report has been carried out by us at M S Ramaiah Institute of Technology under the supervision of Sri. KODEESWARA KUMARAN G, Assistant Professor, MSRIT. This report has not been submitted in part or full for the award of any diploma or degree of this or any other University.

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# ABSTRACT

Power factor correction (PFC) is a technique of counteracting the undesirable effects of electric loads that create a power factor that is less than one. 95 % of industrial loads bear a dominantly lagging power factor. Generally Power factor correction is applied by an electrical power transmission utility to improve the stability and efficiency of the transmission network. Power factor correction setup can also be installed by individual electrical customers to reduce the costs charged to them by their electricity supplier. Many control methods for the Power Factor Correction (PFC) have been proposed. This work describes the design and development of a power factor corrector using PIC (Programmable Interface Controller) microcontroller chip. Measuring of power factor from load is achieved by using PIC Microcontroller-based developed algorithm. This algorithm determines the power factor and includes appropriate capacitors in order to compensate demand of excessive reactive power locally, thus bringing power factor near to unity. This setup has been tested using a 2 HP induction motor having a full load power factor of 0.55 lag, which led to actuation of a 1KVAR capacitor, improving the power factor to unity. The setup is found to be working satisfactorily.

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