CONTROL SIGNALS

	s1	s2	s3	s4	s40	s5	s6	s7	s8	s9	s10	s11	s12	s13	s14
carry_en	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Z_mux_ctrl	X	X	0	X	1	X	X	X	X	X	X	X	X	X	X
zero_en	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
mem_read_en	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0
mem_write_en	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
mem_address_mux_ctrl	1	X	X	X	0	X	0	X	X	X	X	0	X	X	X
IR_en	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rpe_mux_ctrl	X	X	X	X	X	X	0	X	X	X	1	X	0	1	X
Rpe_en	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0
D3_mux_ctrl	XX	XX	XX	01	XX	00	XX	XX	XX	01	XX	XX	10	XX	XX
A1_mux_ctrl	XX	0,I(14)	01	XX	XX	XX	XX	XX	XX	XX	01	XX	XX	01	10
A3_mux_ctrl	X	X	X	1	X	1	X	X	X	1	X	X	0	X	X
R7_mux_ctrl	X	1	X	X	X	1	X	1	X	~I(12)	1	X	X	X	X
RegFile_write	0	0	0	1	0	1	0	0	0	1	0	0	1	0	0
PC_write	0	1	0	0	0	1	0	1	0	1	1	0	0	0	0
T1_mux_ctrl	XX	0,I(12)+I(14).(~I(15))	00	XX	XX	XX	XX	XX	XX	XX	XX	10	XX	XX	00
T1_en	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1
T2_mux_ctrl	X	1	X	X	X	X	X	X	0	X	X	X	X	X	X
T2_en	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
Alu_uppermux_ctrl	XX	00	01	XX	XX	00	10	00	00	00	00	XX	10	XX	XX
Alu_lowermux_ctrl	XX	00	10	XX	XX	00	00	0,~I(13)	00	10	00	XX	00	XX	XX
T3_mux_ctrl	XX	XX	01	00	00	XX		XX	01	XX	10	XX	01	10	XX
T3_en	0	0	1	1	1	0	1	0	1	0	1	0	1	1	0
next_state	S1_decoder	S2_decoder	S3_decoder	S1	S4	S1	S6_decoder	S1	S9	S1	S11	S12	S12_decoder	S14	S6
Alu_signal_mux_ctrl	:=Alu_lowermux_ctrl(0).(~Alu_lowermux_ctrl(1))														

**** 'I' Stands for Instruction op code**