STATES

State Number	Description	Encoding
S1 (instruction_fetch)	$R7 \rightarrow mem_{address}$ $edb \rightarrow IR$	0001
S2	$I_{3-5}\ or\ I_{9-11} \rightarrow A1_{RF}$ $I_{6-8} \rightarrow A2_{RF}$ $D1\ or\ I_{0-5 \rightarrow SE6} \rightarrow T1$ $D2 \rightarrow T2$ $R7 \rightarrow alu$ $+1 \rightarrow alu$ $alu \rightarrow R7$	0010
S3	$T1 \rightarrow alu$ $T2 \rightarrow alu$ $alu \rightarrow T3$ $I_{9-11} \rightarrow A1_{RF}$ $D1 \rightarrow T1$	0011
S4	$T3 \rightarrow D3$ $I_{9-11} \rightarrow A3_{RF}$	0100
S5	$I_{0-8} \rightarrow DE \rightarrow D3$ $I_{9-11} \rightarrow A3_{RF}$ $R7 \rightarrow alu$ $+1 \rightarrow alu$ $alu \rightarrow R7$	0101
S6	$T3 \rightarrow mem_{address}, alu$ $T1 \rightarrow mem_{data}$ $+1 \rightarrow alu$ $alu \rightarrow t3$ $Logic \rightarrow R_{PE}$	0110
S7	$R7 \rightarrow alu$ $I_{0-5 \rightarrow SE6}\ or\ (+1) \rightarrow alu$ $alu \rightarrow R7$	0111
S8	$R7 \rightarrow alu$ $+1 \rightarrow alu$ $alu \rightarrow T3$ $I_{0-8} \rightarrow SE9 \rightarrow T2$	1000

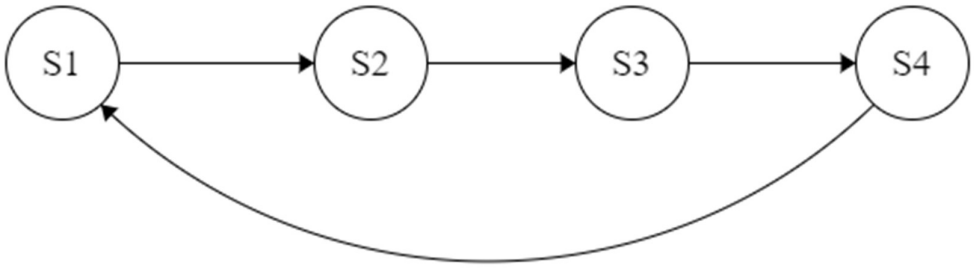
STATES

S9	$T3 \rightarrow D3$ $I_{9-11} \rightarrow A3_{RF}$ $R7 \rightarrow alu$ $T2 \rightarrow alu$ $alu\ or\ T2 \rightarrow R7$	1001
S10	$I_{9-11} \rightarrow A1_{RF}$ $D1 \rightarrow T3$ $I_{0-7} \rightarrow R_{PE}$ $R7 \rightarrow alu$ $+1 \rightarrow alu$ $alu \rightarrow R7$	1010
S11	$T3 \rightarrow mem_{address}$ $edb \rightarrow T1$	1011
S12	$R_{PE} \rightarrow PE \rightarrow A3$ $T1 \rightarrow D3$ $T3 \rightarrow alu$ $+1 \rightarrow alu$ $alu \rightarrow T3$ $Logic \rightarrow R_{PE}$	1100
S13	$I_{9-11} \rightarrow A1_{RF}$ $D1 \rightarrow T3$ $I_{0-7} \rightarrow R_{PE}$	1101
S14	$R_{PE} \rightarrow PE \rightarrow A1_{RF}$ $D1 \rightarrow T1$	1110
S40	$T3 \rightarrow mem_{address}$ $edb \rightarrow T3$	1111
Reset	----------	0000

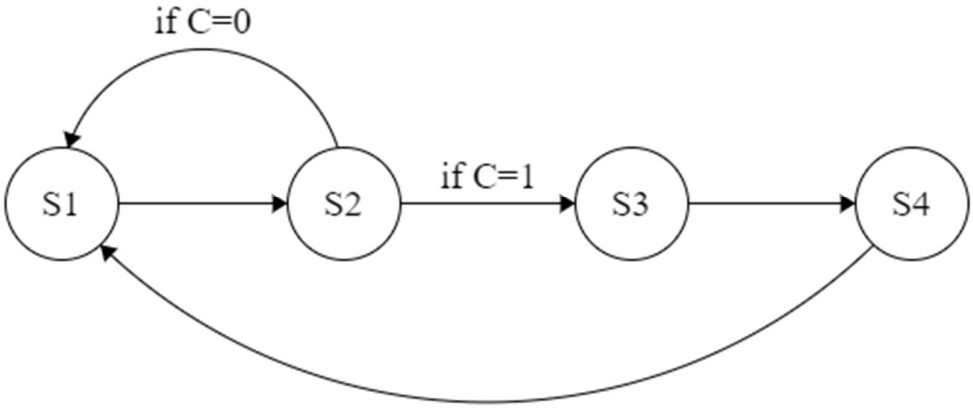
STATES

FLOWGRAPH FOR VARIOUS INSTRUCTIONS

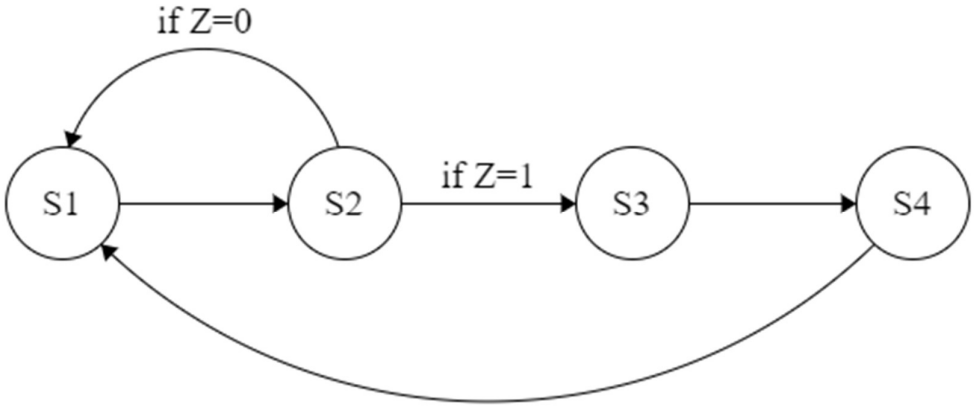
- **ADD**



- **ADC**

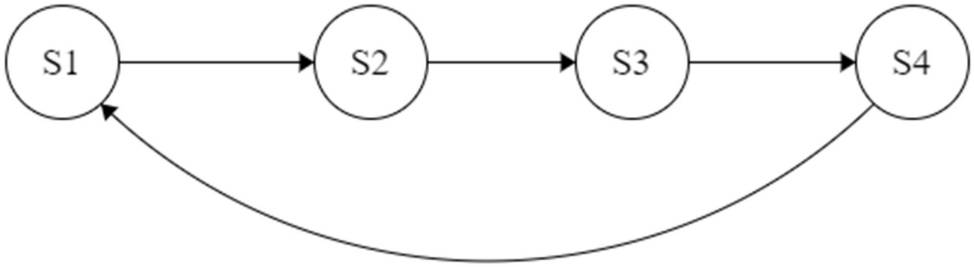


- **ADZ**

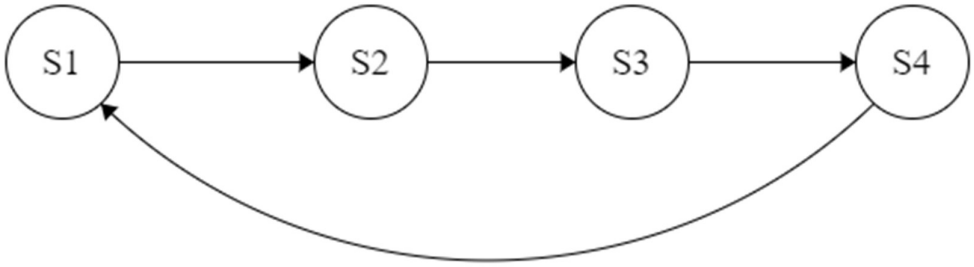


STATES

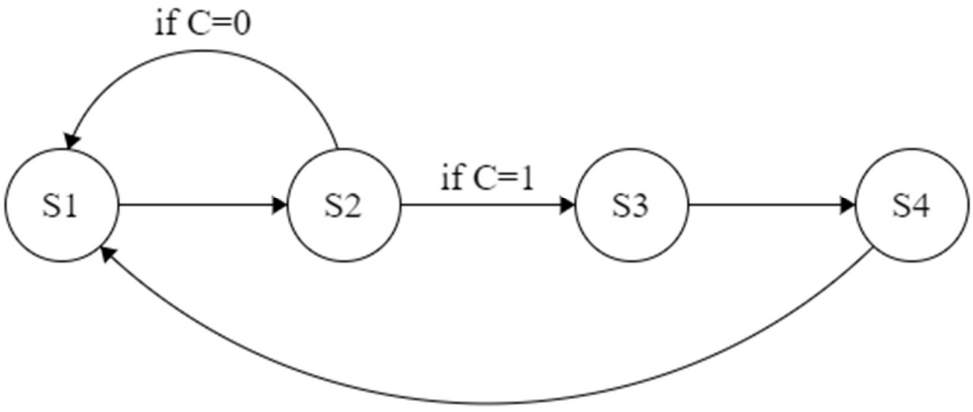
- **ADI**



- **NDU**

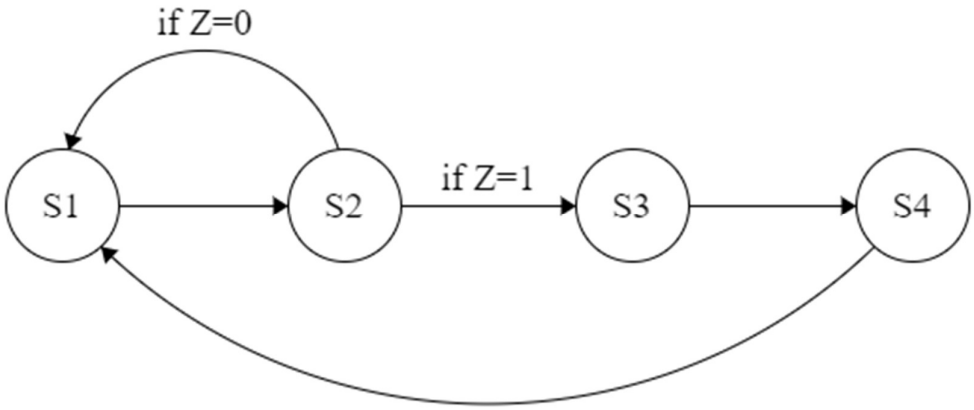


- **NDC**

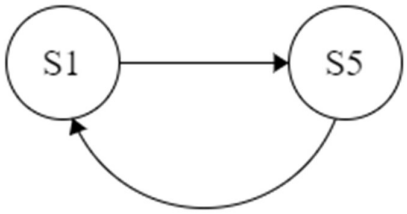


STATES

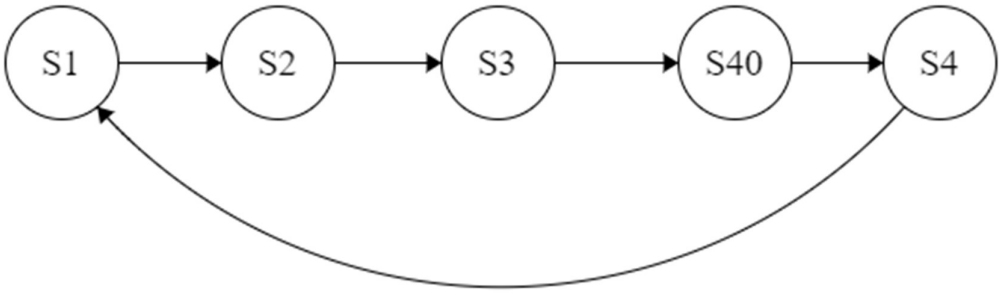
- **NDZ**



- **LHI**

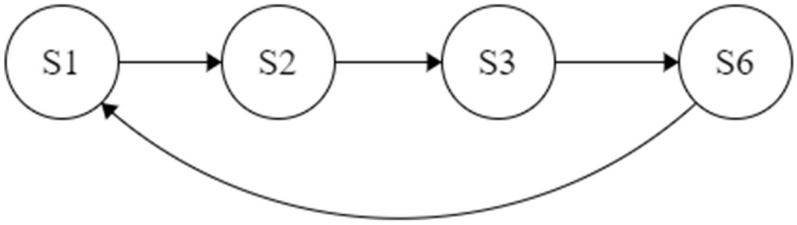


- **LW**

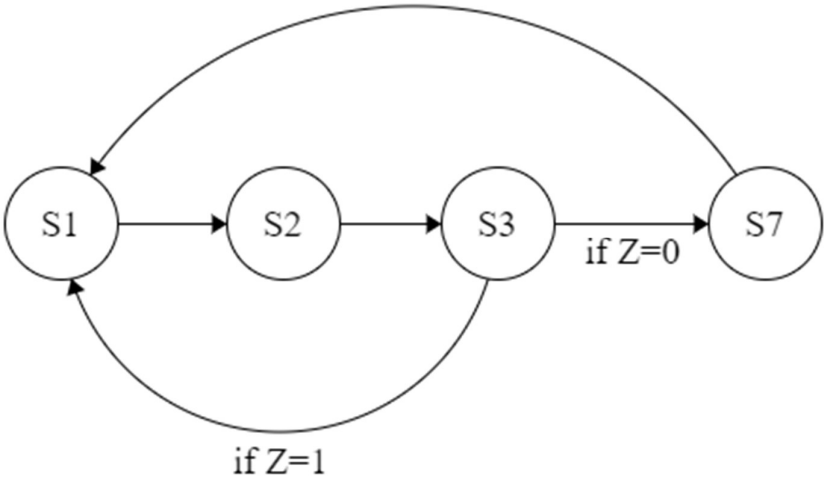


STATES

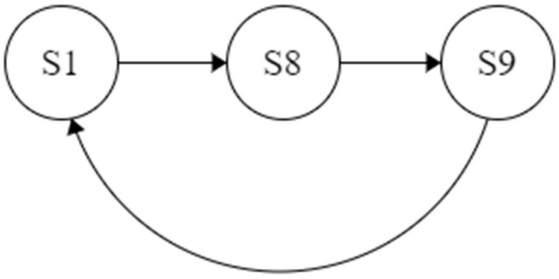
- **SW**



- **BEQ**

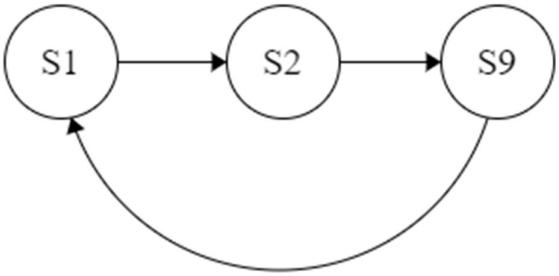


- **JAL**

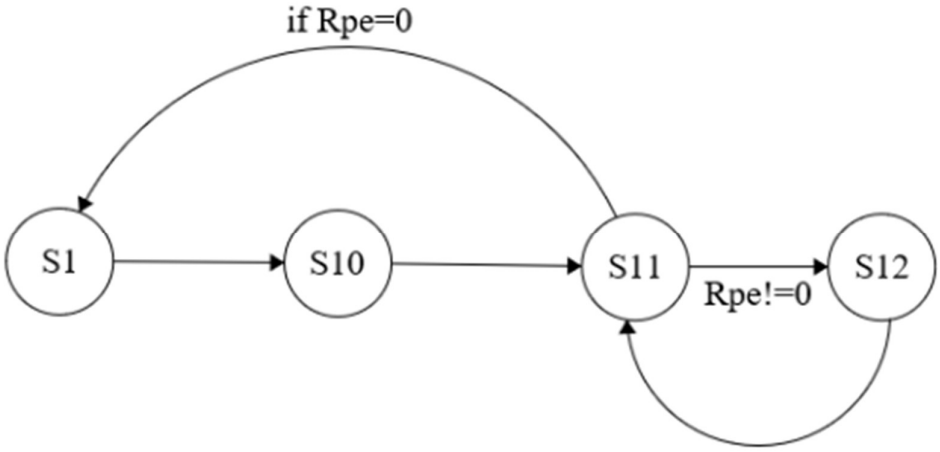


STATES

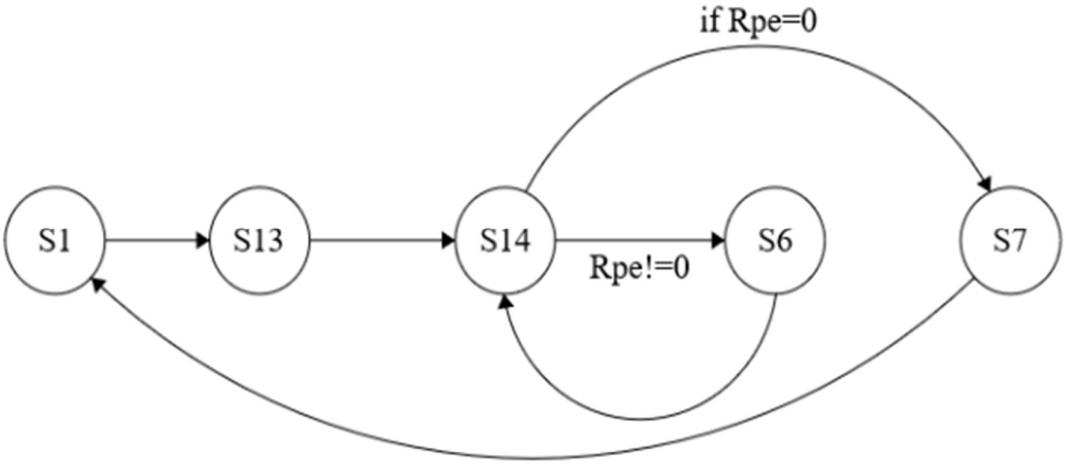
- **JLR**



- **LM**

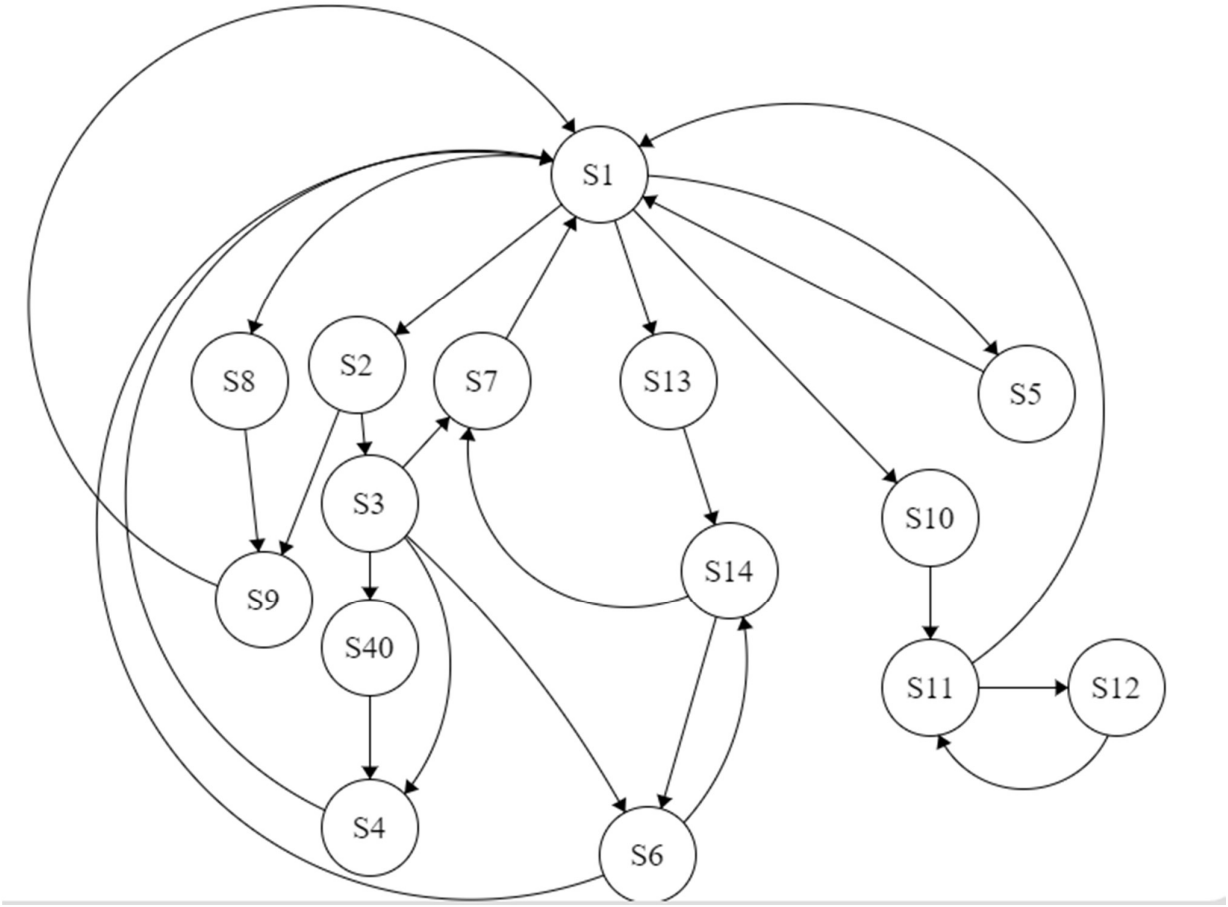


- **SM**



STATES

FSM for the System:



Decoders are used after states S1, S2, S3, S6, S12 to decide what next state will be by taking into consideration the op-code given in the instruction.