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"La Técnica al Servicio de la Patria"

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Tarea 4:

04_ CONTROL POR ANCHO DE PULSO(CCP/ECCP)

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CONTROL POR ANCHO DE PULSO(CCP/ECCP)

INTRODUCCION

Este dispositivo contiene un modulo de mejora de Captura/Comparación/PWM de CCP1 y de Captura/Comparación/PWM de CCP2. Ambos módulos son idénticos en operación, con la excepción de que las características de mejora de PWM solo están disponibles en el módulo CCP1.

MODULO DE MEJORA DE CAPTURA/COMPARACION/PWM DE CCP1

Este modulo de mejora es un periférico que permite al usuario medir y controlar diferentes eventos. En el modo captura, el periférico permite al usuario disparar una señal externa cuando la cantidad de tiempo establecida ha expirado. El modo PWM permite generar una señal de ancho de pulso moderado de la variación de frecuencia y el ciclo de trabajo. Podemos apreciar los módulos en las siguientes tablas:

REGISTER DEFINITIONS: CCP CONTROL

REGISTER 11-1: CCP1CON: ENHANCED CCP1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **P1M<1:0>:** PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A assigned as Capture/Compare input; P1B, P1C, P1D assigned as port pins

If CCP1M<3:2> = 11:

00 = Single output; P1A modulated; P1B, P1C, P1D assigned as port pins
01 = Full-Bridge output forward; P1D modulated; P1A active; P1B, P1C inactive
10 = Half-Bridge output; P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins
11 = Full-Bridge output reverse; P1B modulated; P1C active; P1A, P1D inactive

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** ECCP Mode Select bits

0000 = Capture/Compare/PWM off (resets ECCP module)
0001 = Unused (reserved)
0010 = Compare mode, toggle output on match (CCP1IF bit is set)
0011 = Unused (reserved)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP1IF bit is set)
1001 = Compare mode, clear output on match (CCP1IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 or TMR2
1100 = PWM mode; P1A, P1C active-high; P1B, P1D active-high
1101 = PWM mode; P1A, P1C active-high; P1B, P1D active-low
1110 = PWM mode; P1A, P1C active-low; P1B, P1D active-high
1111 = PWM mode; P1A, P1C active-low; P1B, P1D active-low

Además de las configuraciones de los Timer en la tabla siguiente:

TABLE 11-1: ECCP MODE – TIMER RESOURCES REQUIRED

ECCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

MODULO DE MEJORA DE CAPTURA/COMPARACION/PWM DE CCP2

El módulo de Captura/Comparación/PWM es un periférico que permite al usuario medir y controlar diferentes eventos. En el modo captura el periférico permite medir la duración de un evento. El modo comparador permite al usuario disparar un evento externo cuando una cantidad predeterminada de tiempo ha expirado. El modo PWM puede generar una señal modulada de ancho de pulso de frecuencia variable y ciclo de trabajo.

REGISTER 11-2: CCP2CON: CCP2 CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DC2B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR2L.

bit 3-0 **CCP2M<3:0>:** CCP2 Mode Select bits

0000 = Capture/Compare/PWM off (resets CCP2 module)
0001 = Unused (reserved)
0010 = Unused (reserved)
0011 = Unused (reserved)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP2IF bit is set)
1001 = Compare mode, clear output on match (CCP2IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP2IF bit is set, CCP2 pin is unaffected)
1011 = Compare mode, trigger special event (CCP2IF bit is set, TMR1 is reset and A/D conversion is started if the ADC module is enabled. CCP2 pin is unaffected.)
11xx = PWM mode.

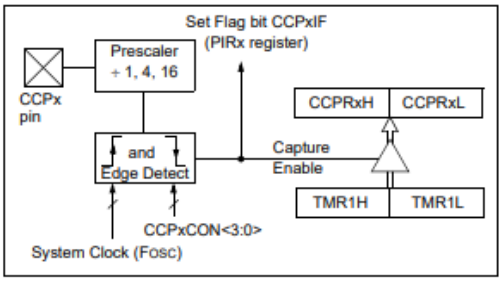
Además de las configuraciones de los Timer en la tabla siguiente:

TABLE 11-2: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

MODO DE CAPTURA

En el modo de captura, el CCPRRxH, CCPRxL captura valores de 16 bits del registro TMR1 cuando un evento ocurre en el pin CCPx. Un evento esta definido al seguir ciertas configuraciones. Para configurar el pin en modo captura, el CCPx debe de ser establecido como una salida al estar asociado con el bit de control TRIS. Además de que en Timer1 debe de estar funcionando en el modo Timer o como contador sincronizado para el módulo CCP. Se muestra el siguiente diagrama de operación:

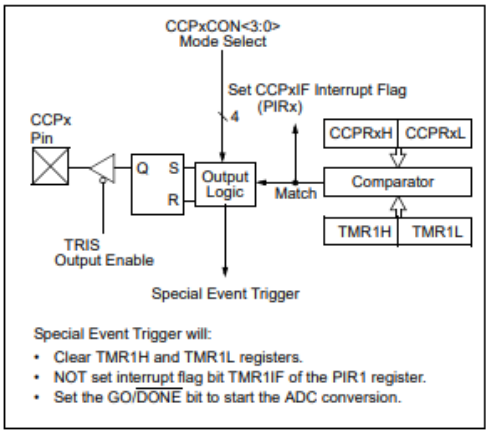



```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS;Load the W reg with
                    ; the new prescaler
                    ; move value and CCP ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ; value
```

MODO DE COMPARACION

En el modo comparación, el registro CCPRx de 18 bits es constantemente comparado con el registro TMR1. La igualdad puede ocurrir tras ciertas circunstancias con el módulo CCPx. La acción del pin está basada en el valor del CCPxM y CCPx1CON. Si selección se hace al momento de que el Timer1 se encuentra funcionando en el modo Timer o como contador sincronizado.

FIGURE 11-2: COMPARE MODE OPERATION BLOCK DIAGRAM



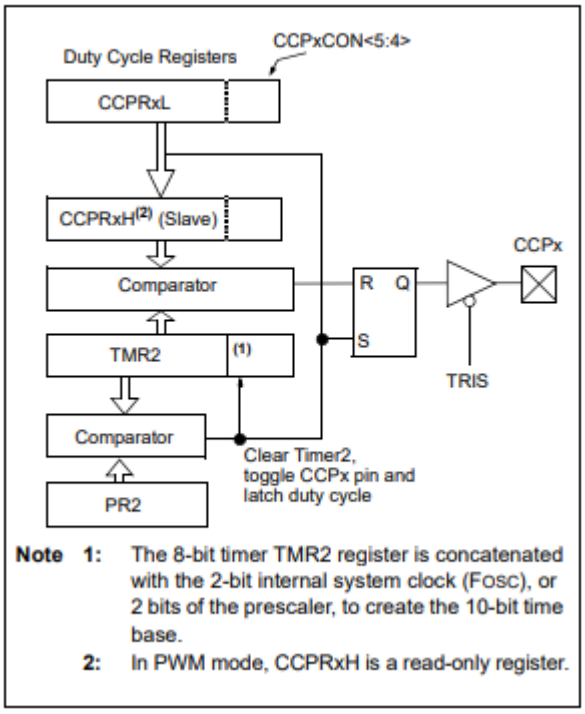
MODO PWM

El modo PWM genera una señal modulada de ancho de pulso en el pin CCPx. El ciclo de trabajo, periodo y resolución son determinados por los siguientes registros:

- PR2
- T2CON
- SSPRxL
- CCPxCON

En el modo de la modulación del ancho de pulso, el CCP produce una resolución de salida de 10 bits en el pin CCPx. Desde que el pin CCPx es multiplexada con el puerto, así que el TRIS de ese pin debe ser limpiado para activar el pin CCPx de salida.

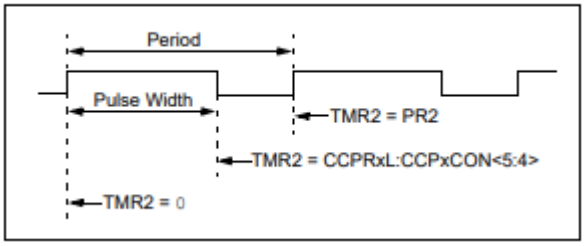
FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPRxH is a read-only register.

FIGURE 11-4: CCP PWM OUTPUT



Para calcular el periodo de PWM:

EQUATION 11-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

Note: TOSC = 1/FOSC

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Para calcular el ciclo de trabajo del PWM:

EQUATION 11-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxL:CCPxCON<5:4>) \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

EQUATION 11-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PR2 + 1)}$$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 11-3).

La resolución del PWM se calcula:

EQUATION 11-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 11-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

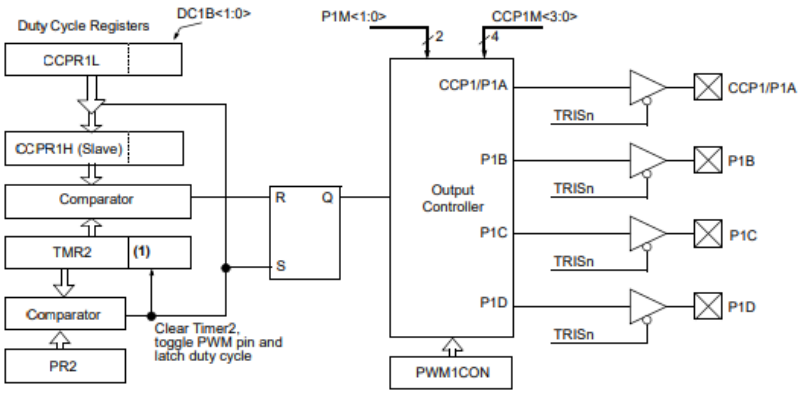
PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 11-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

Diagrama de PWM (Modo Mejorado):

FIGURE 11-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE



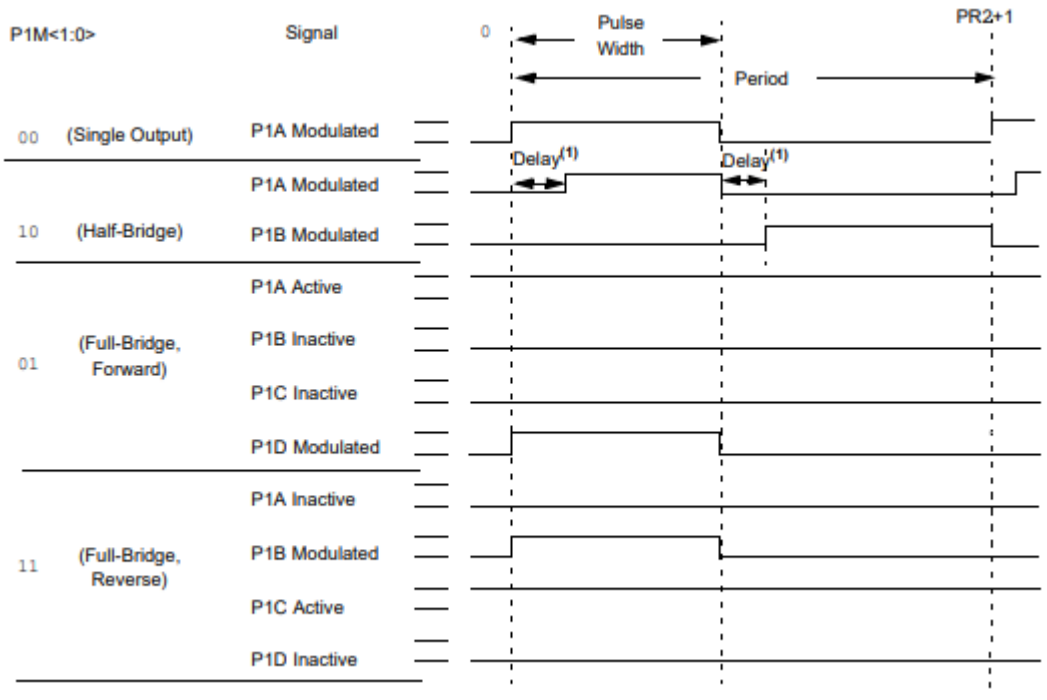
Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler to create the 10-bit time base.

Note 1: The TRIS register value for each PWM output must be configured appropriately.
2: Clearing the CCPxCON register will relinquish ECCP control of all PWM output pins.
3: Any pin not used by an Enhanced PWM mode is available for alternate pin functions.

TABLE 11-5: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	P1M<1:0>	CCP1/P1A	P1B	P1C	P1D
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

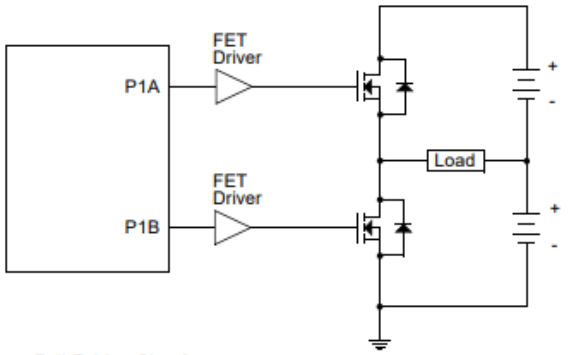
Note 1: Pulse Steering enables outputs in Single mode.



Relationships:

Diagrama de PWM (Modo de Puente Medio):

Standard Half-Bridge Circuit ("Push-Pull")



Half-Bridge Output Driving a Full-Bridge Circuit

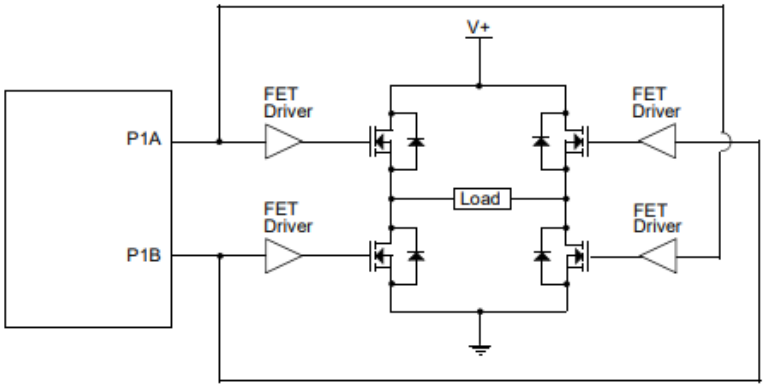


Diagrama de PWM (Modo de Puente Completo):