

1. Projekt: *Přístupový terminál*

Vstupní signály:

Výstupní signály:

Mealyho výstupy: FSM_LCD_WR, FSM_LCD_CLR

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graph TD
    TEST1([TEST1/000]) -- "0;K=8/10" --> TEST2([TEST2/000])
    TEST2 -- "0;K=6/10" --> TEST3([TEST3/000])
    TEST3 -- "0;K=3/10" --> TEST4([TEST4/000])
    TEST4 -- "0;K=1/10" --> TEST5([TEST5/000])
    TEST5 -- "0;K=3/10" --> TEST6([TEST6/000])
    TEST6 -- "0;K=6/10" --> TEST7([TEST7/000])
    TEST7 -- "0;K=5/10" --> TEST8A([TEST8A/000])
    TEST7 -- "0;K=3/10" --> TEST8B([TEST8B/000])
    TEST8A -- "0;K=3/10" --> TEST9A([TEST9A/000])
    TEST8B -- "0;K=9/10" --> TEST9B([TEST9B/000])
    TEST9A -- "0;K=7/10" --> PASS_OK[PASS_OK/000]
    TEST9B -- "0;K=5/10" --> TEST10B([TEST10B/000])
    TEST10B -- "0;K=4/10" --> PASS_OK
    TEST4 -- "0;K!=1,#/10" --> BAD_INPUT[BAD_INPUT/000]
    BAD_INPUT -- "0;K!=#/10" --> BAD_INPUT
    BAD_INPUT -- "0;K=#/10" --> PRINT_KO[PRINT_KO/110]
    PRINT_KO -- "1;X/10" --> FINISH{{FINISH/000}}
    FINISH -- "0;K!=#/10" --> FINISH
    FINISH -- "1;X/10" --> PRINT_OK[PRINT_OK/111]
    PRINT_OK -- "0;K=#/10" --> PASS_OK
    FINISH -- "0;K=#/01" --> PASS_OK
    
```