Operational NMOS amplifier with NMOS differential pair

February 11, 2024

1 current bias generation

Fig.1 represents the minimum voltage allowed for the current reference to work as supposed.

Corner	Minimum VOUT
Nominal	0.43
Worst corner	0.51
Best corner	0.37

Figure 1: minimum voltage

Fig.2 represent the output current characteristic fo nominal, worst and best case scenario.

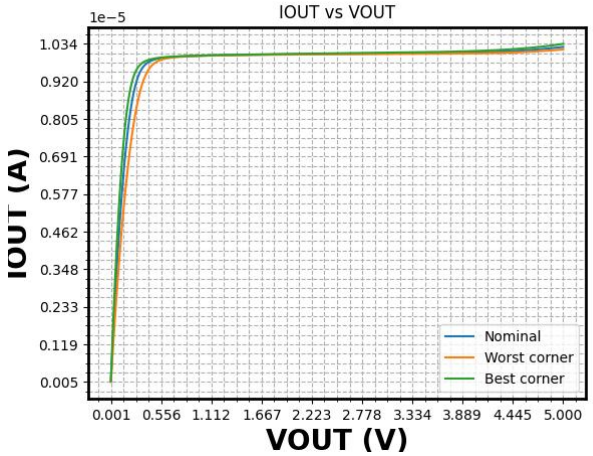

Figure 2: IOUT vs VOUT

Fig.3 represent the output impedance characteristic fo nominal, worst and best case scenario.

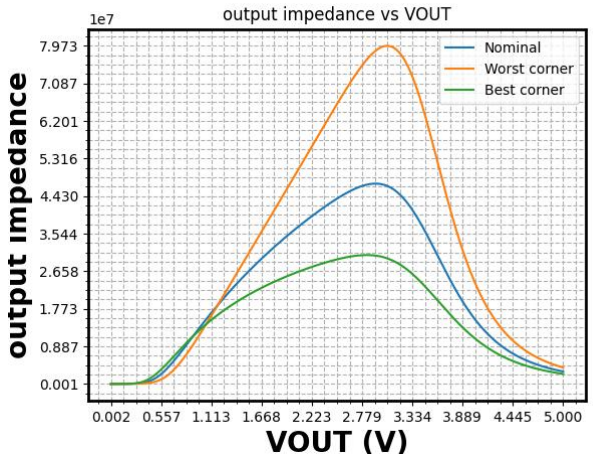

Figure 3: output impedance

Fig.**??** represent the current variation face an ac signal fo nominal, worst and best case scenario.

Corner	Maximum IOUT variation
Nominal	3.529843528582433e-08
Worst corner	2.929382780791912e-08
Best corner	4.521654961564536e-08

Figure 4: ac variation

Fig.5 represent the current variation at vout = VDD/2 with 200 runs.

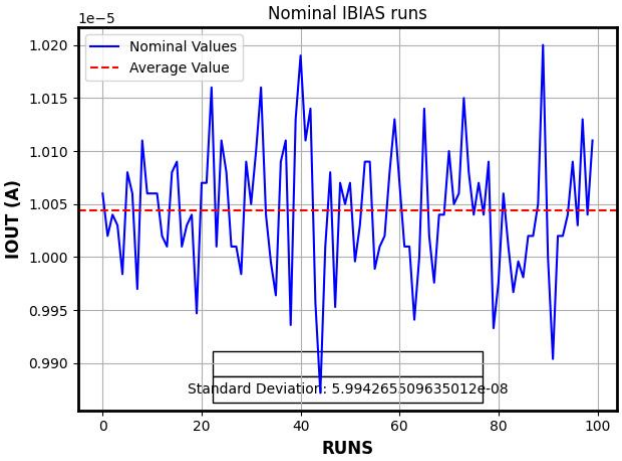

Figure 5: Monte carclo variations

Fig.6 represent the histogram.

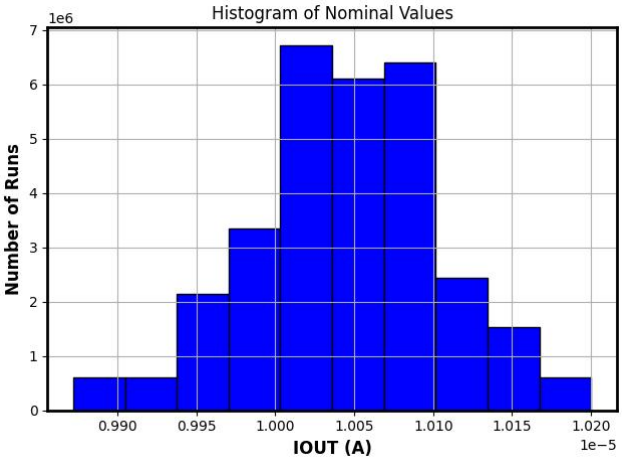

Figure 6: Monte carclo variations