5-BIT FLASH ADC

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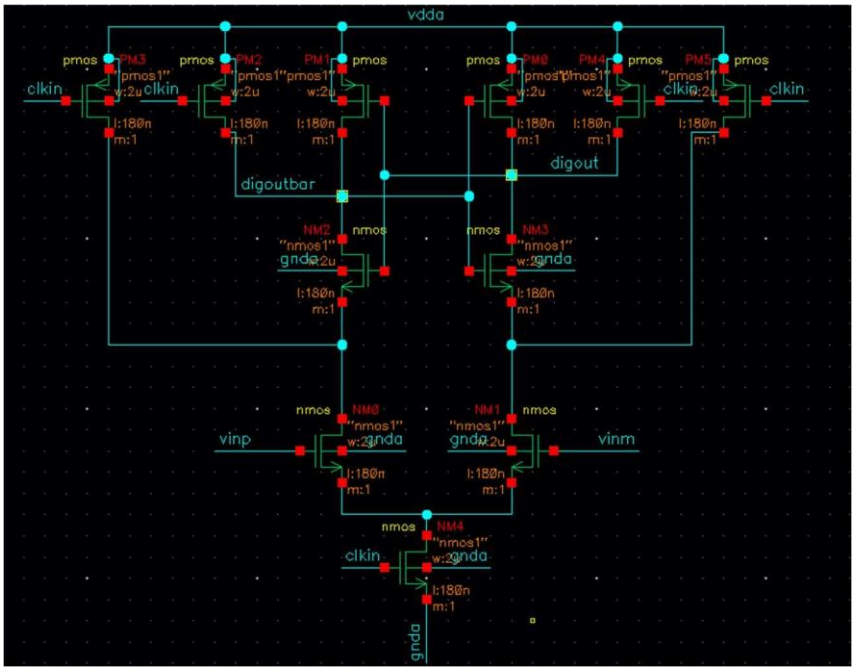
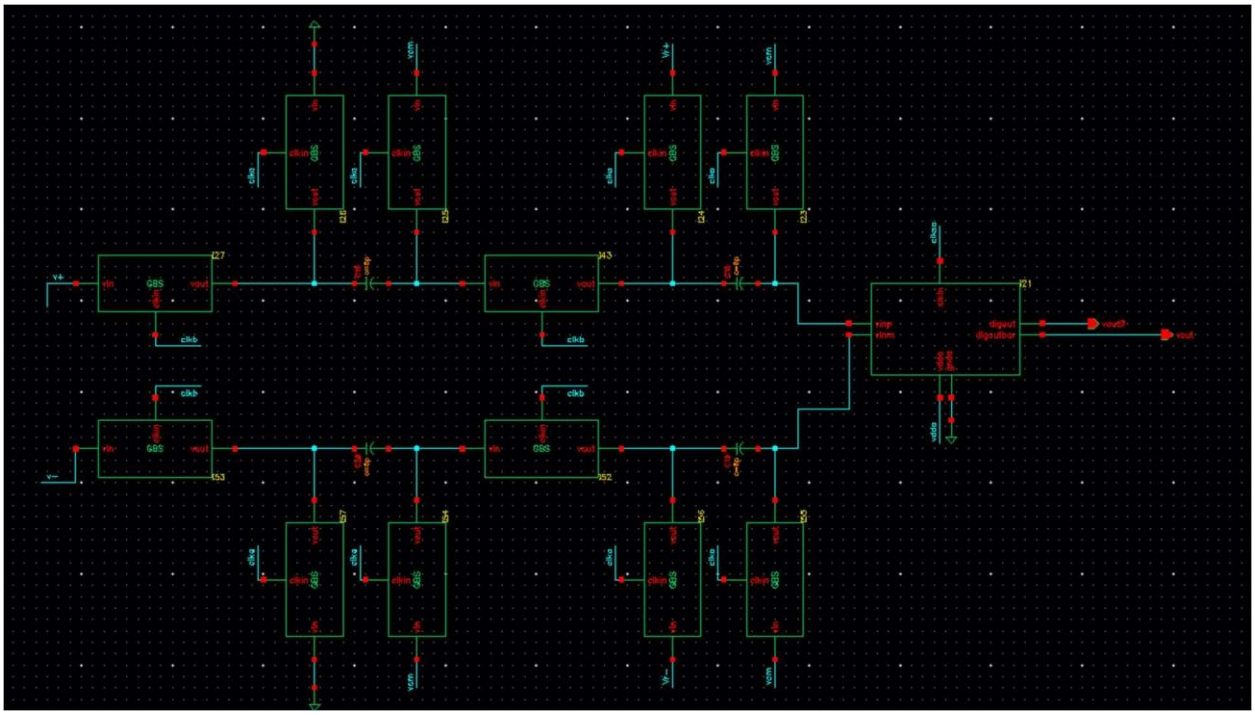
Schematic of Latch

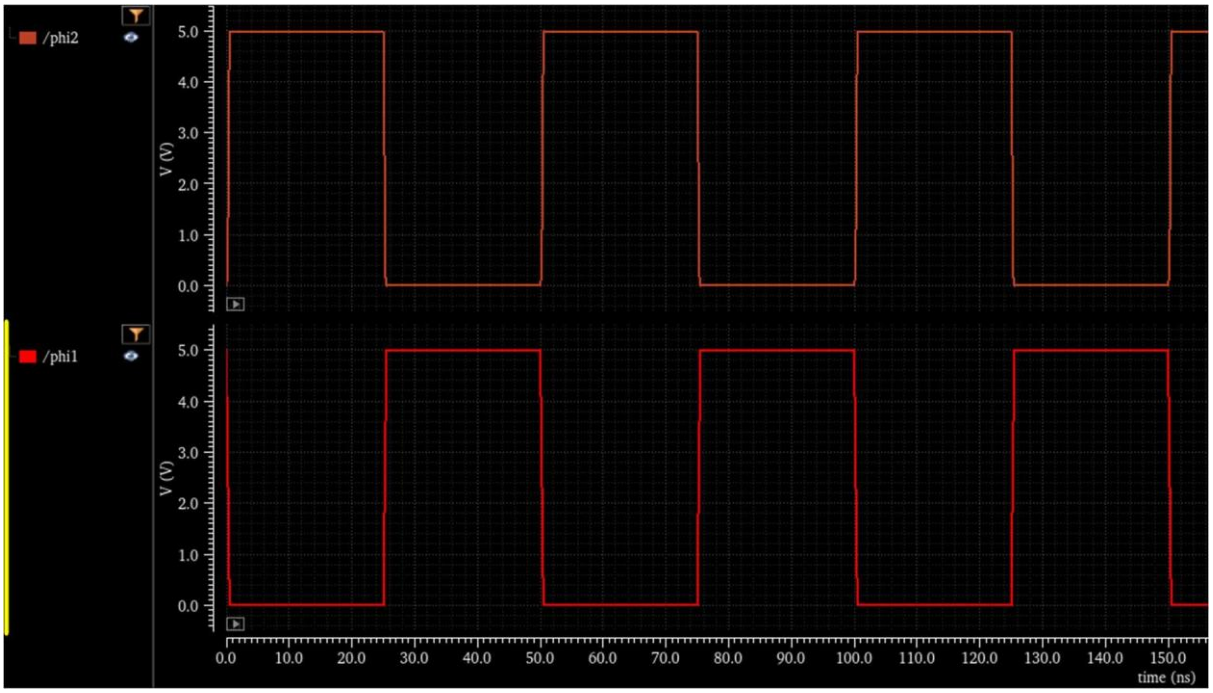
Strong arm latch is used as comparator



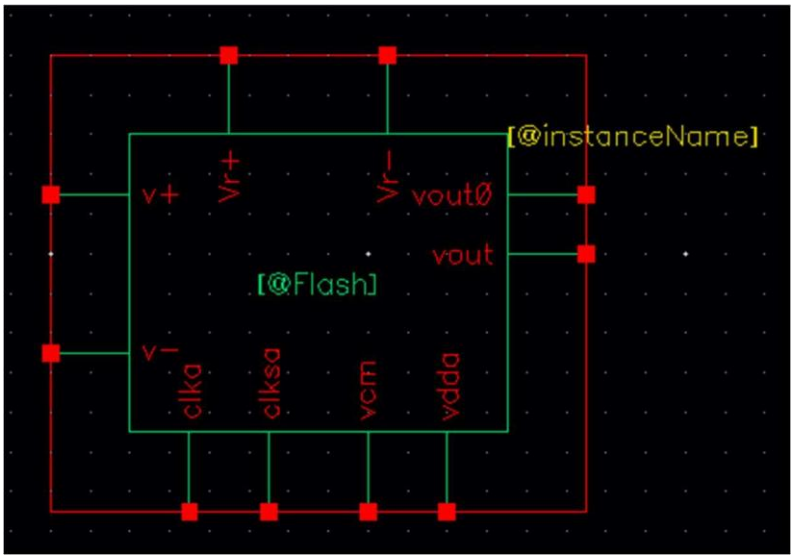
Reference subtraction is done using capacitor methods in 2 phases of one clock cycle as shown below.



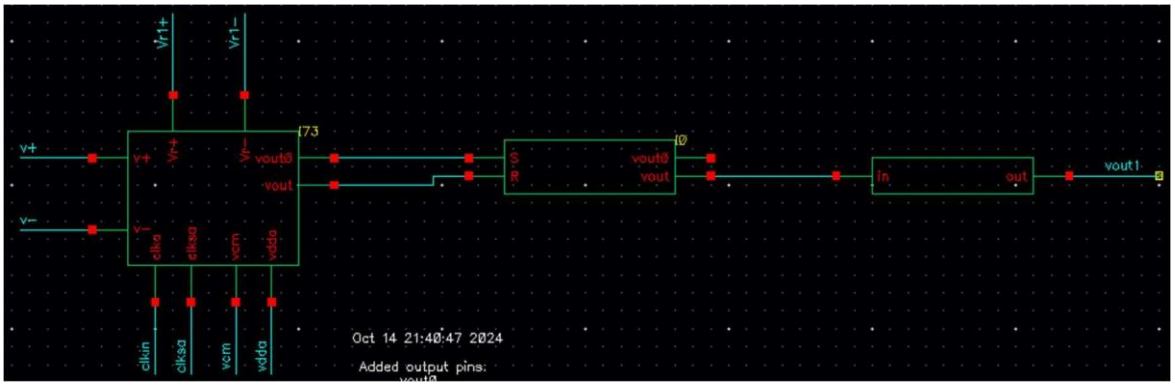
Switch Clocking scheme to Bootstrapped switch for reference subtraction



Total Flash comparator



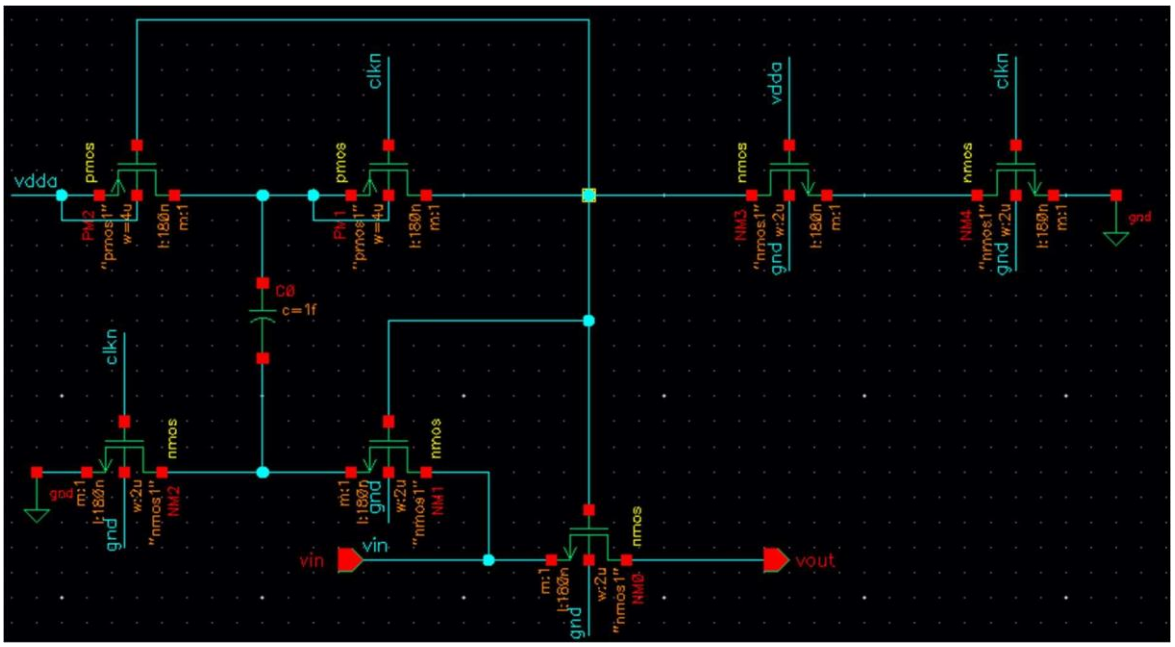
Comparator connected to SR latch and 2 inverters in series for stable output as shown below.



Switches

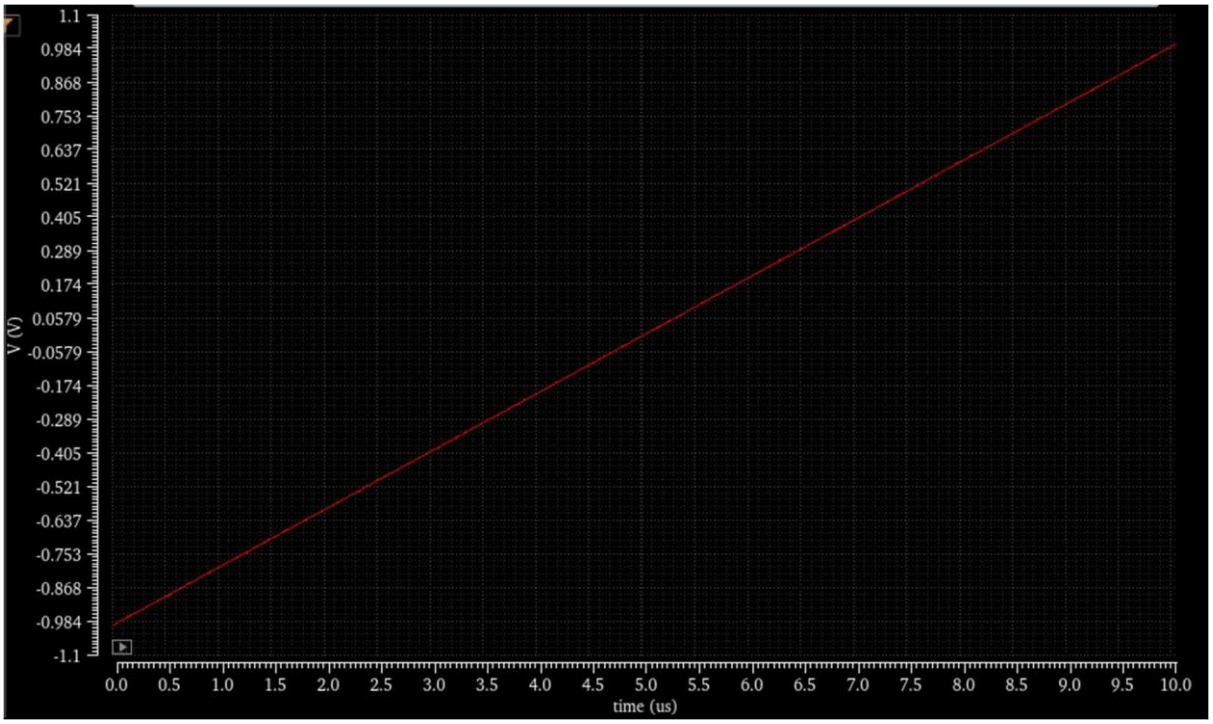
Choice of switch:

All the switches used including the ones used in reference subtraction are **Gate Bootstrapped switch**. To maintain a relatively constant on resistance for a switch, we wish to fix its gate-source voltage as the input varies. When the switch is off, the capacitor is charged to required gate source voltage such that resistance remains constant when the switch is ON.

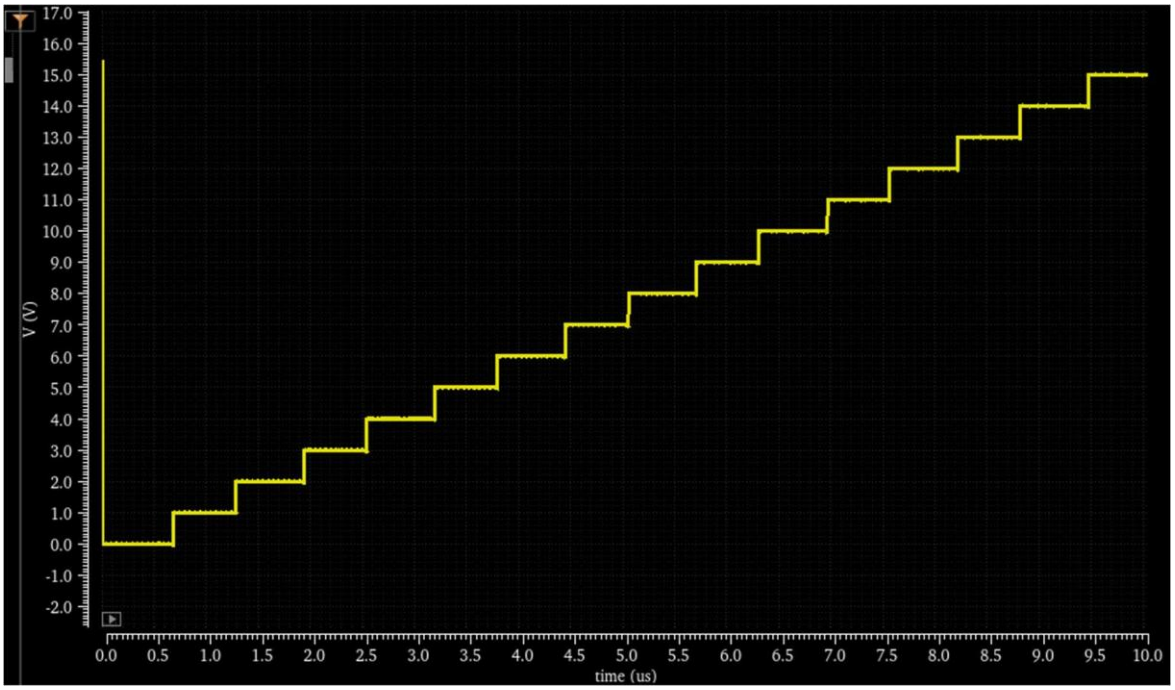


Input – Output Characteristic of ADC

Input Ramp signal



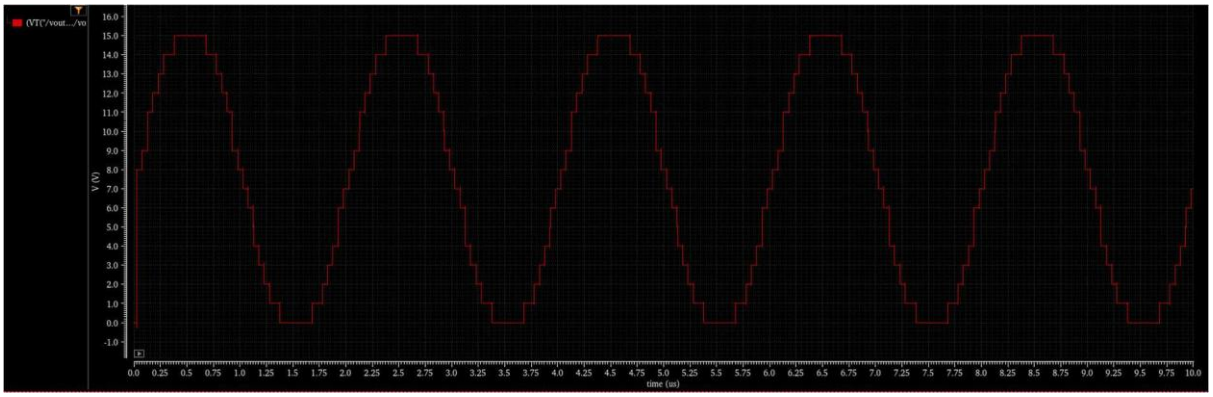
Output Step signal

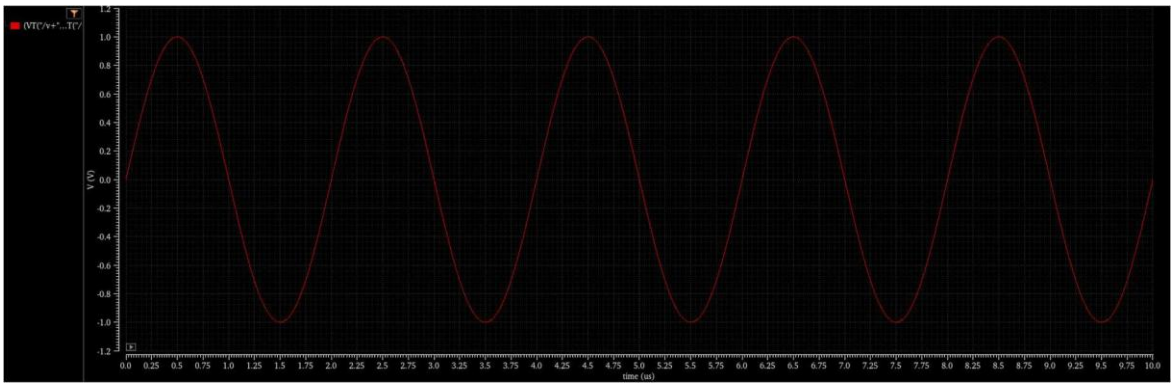


Time Domain Waveforms

Input frequency = 500kHz

Sampling frequency = 20MHz



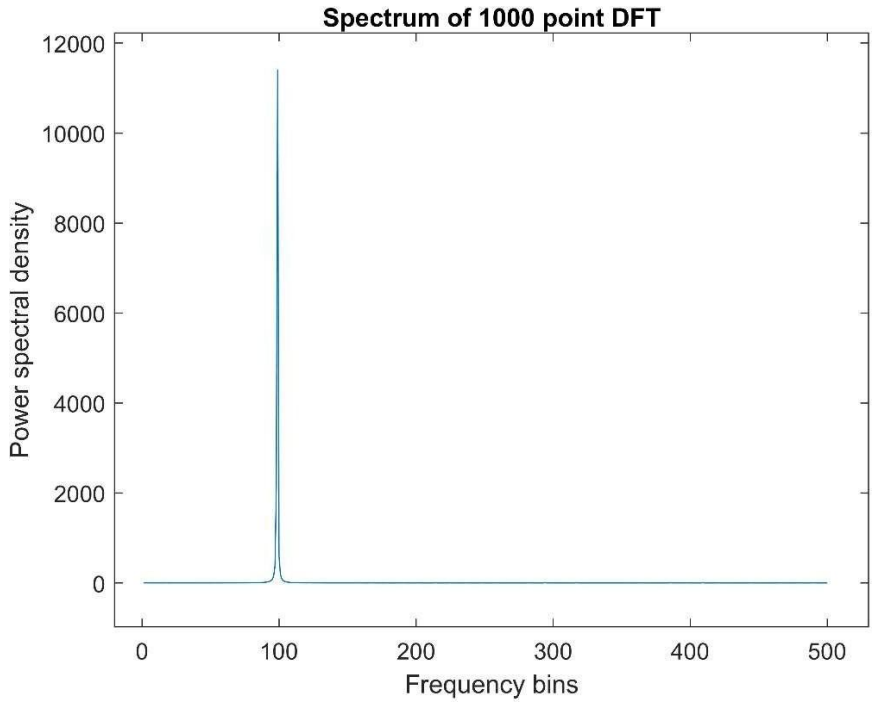


Spectrum

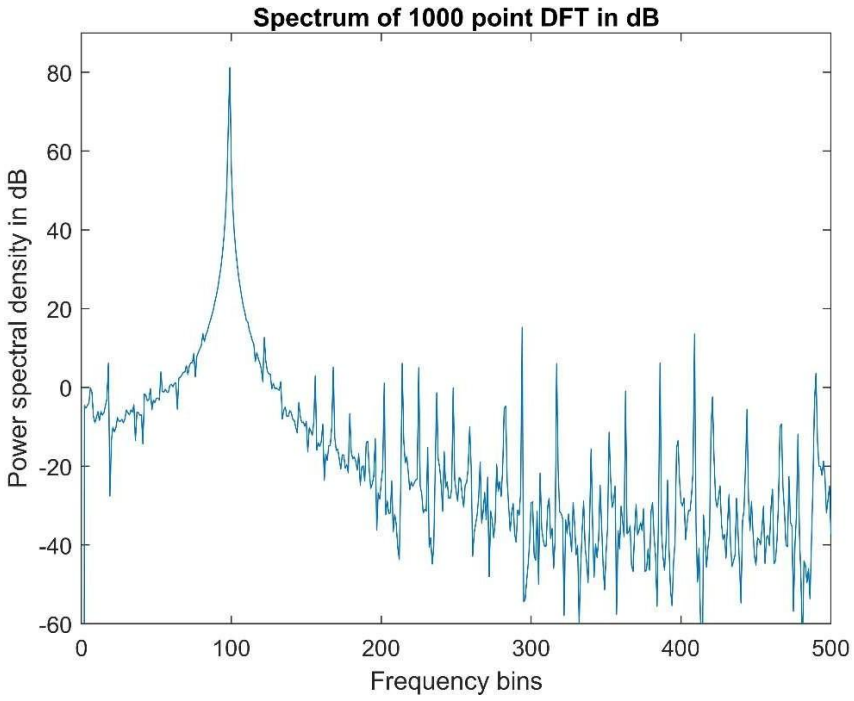
1. For low frequency tone

i. f0 = (97.7/1000)* fs

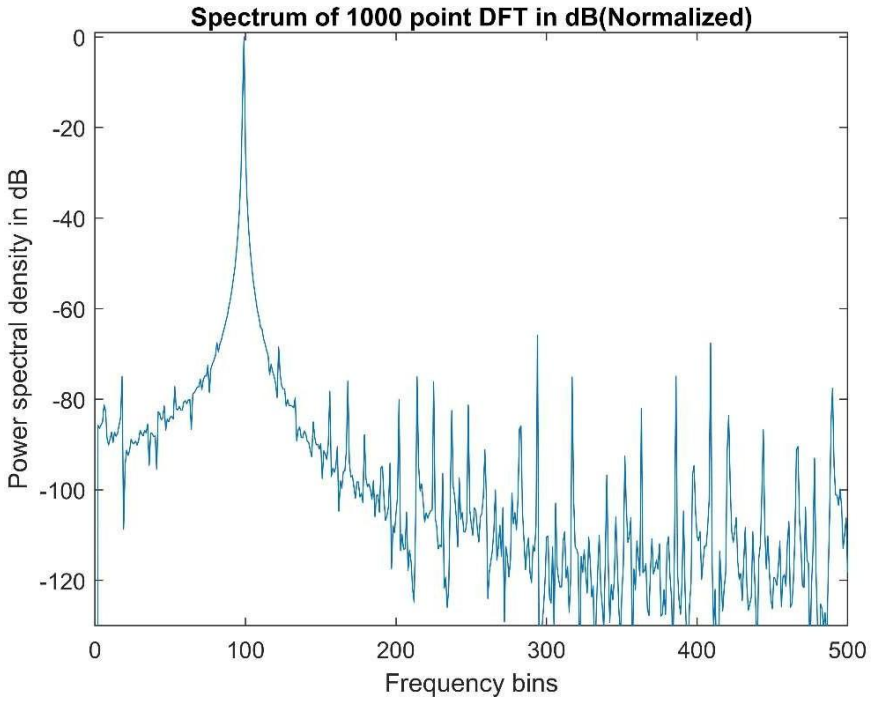
Signal not falling on bin,



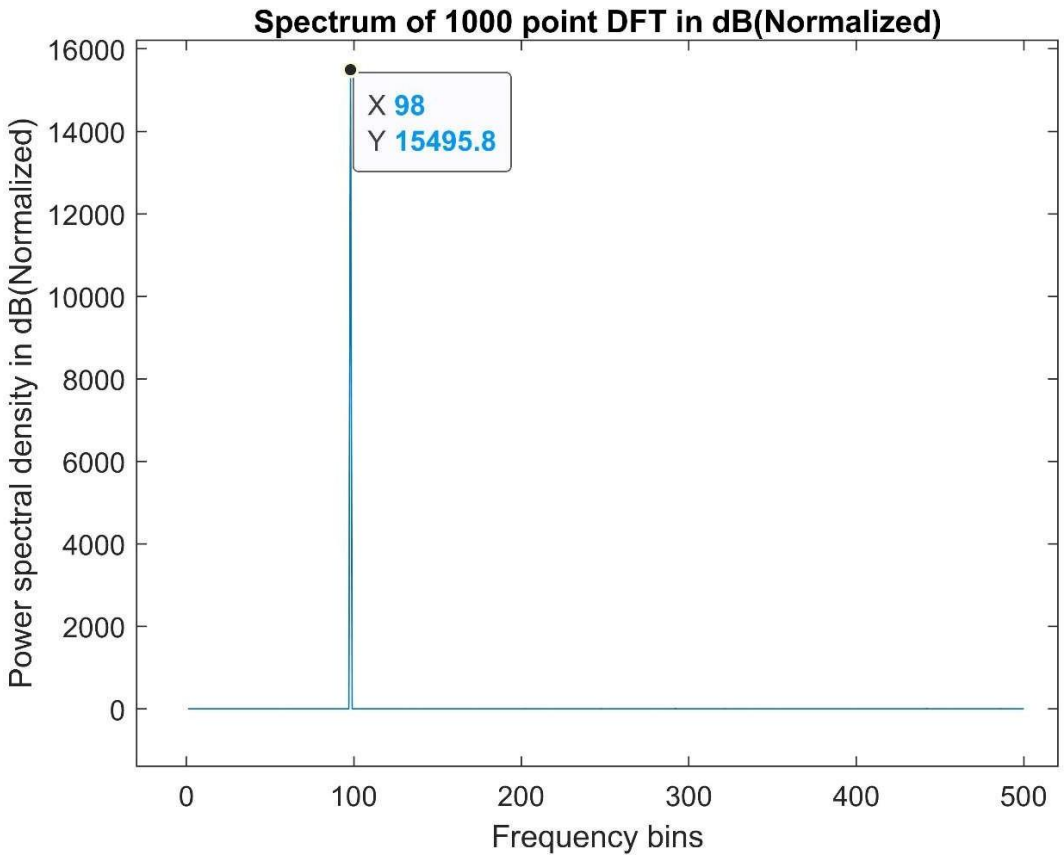
In dB,



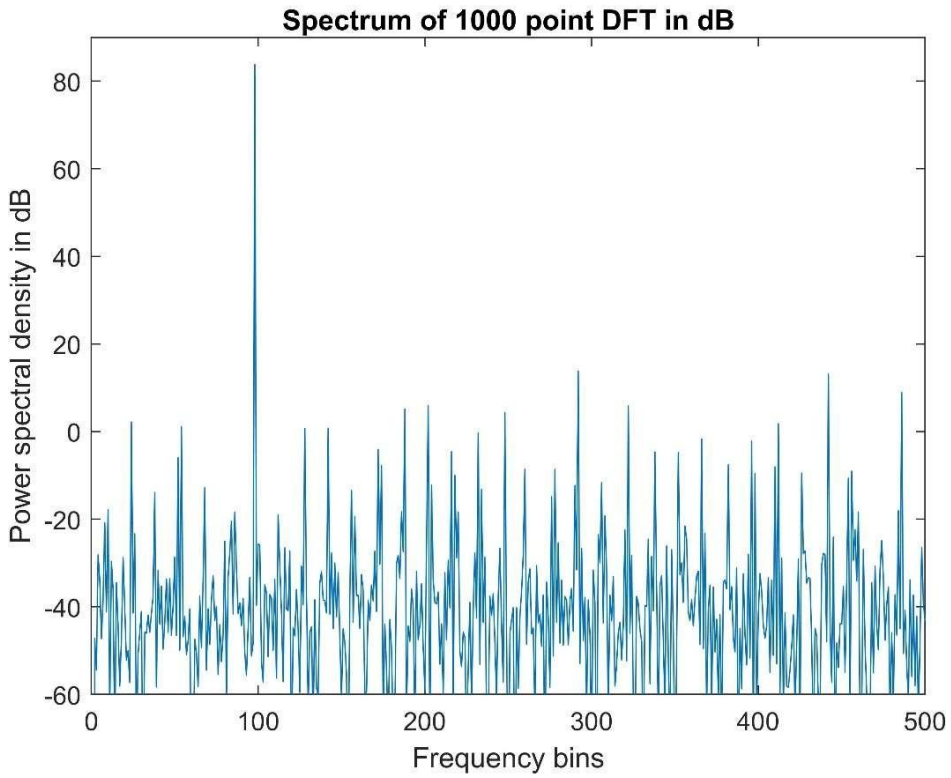
In dB with spectral powers normalized to signal strength,



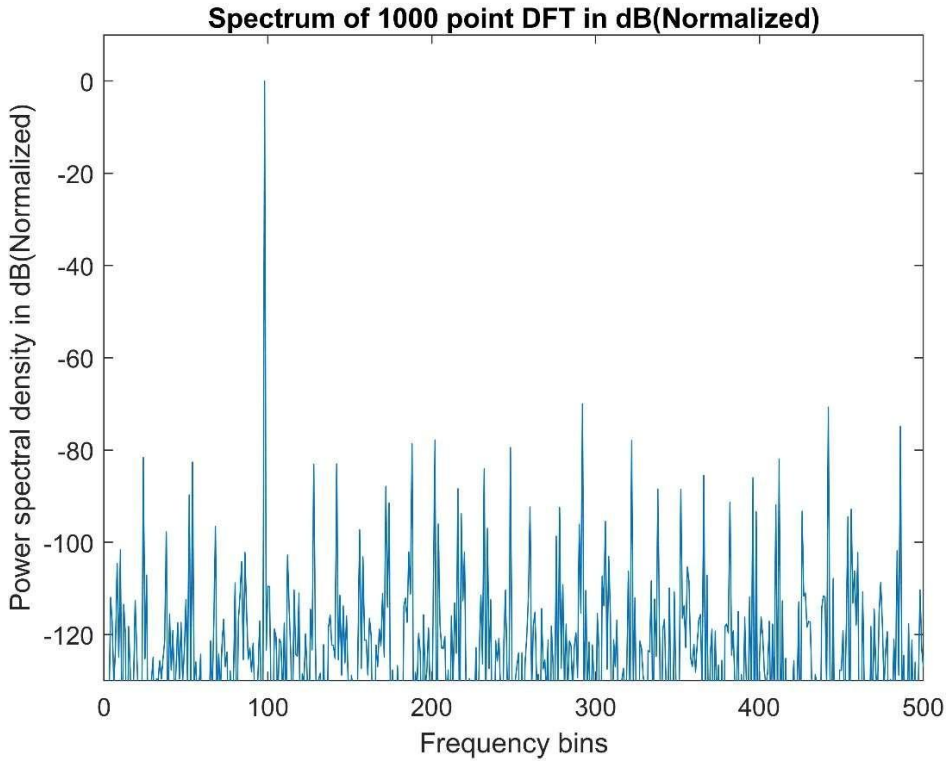
ii. Signal on bin with f = (98/1000)fs



In dB,

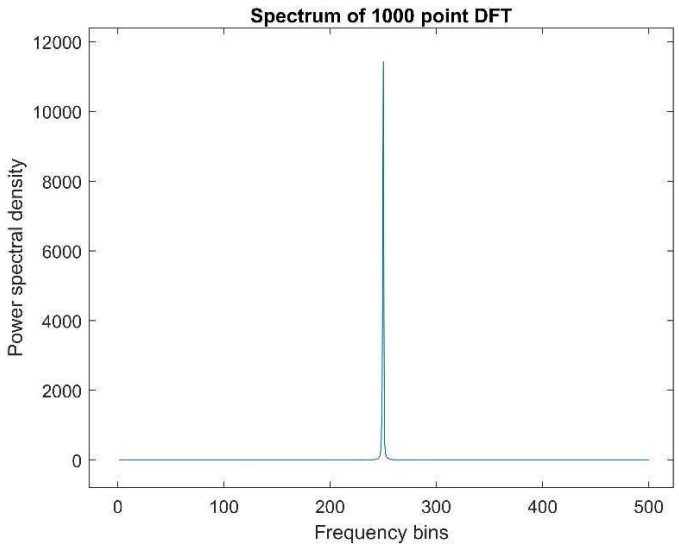


In dB (Normalized),

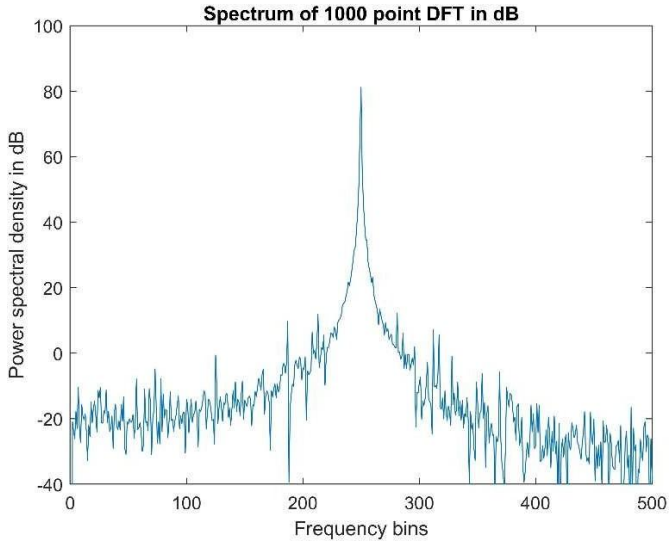


2. A tone close to Nyquist frequency,

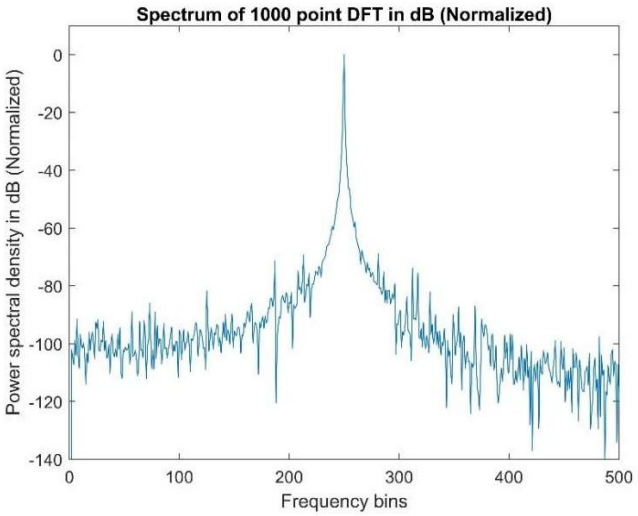
Not on the bin,



In dB,



In dB (Normalized),



SQNR

1. Data points are extracted from strobing.
2. These points are taken exactly equal to the required number of points of DFT. Here I considered a N=1000 point DFT.
3. The DFT data points are squared and divided by N. Thus spectrum is evaluated.
4. Signal power:
   i. Frequency not on bin
      Then the power is distributed over a range of nearby bin. Thus 3or 5 point sum around the nearby bin are considered for signal power. Finally this value is divided by N.
   ii. Frequency on bin
      Then the signal power is the power exactly on the bin. The spectral value divided by N gives the signal power.
5. Quantization power:
   Quantization power = Total power – Signal power
6. SQNR = $10\log\left(\frac{P_{signal}}{P_{guantization}}\right)$

For input frequency = 1.954 MHz, (doesn't fall on bin)

P at bin 98 = 2.112096e+03
P at bin 99 = 1.140535e+04
P at bin 100 = 6.01433e+02

P_signal = 1.4118885e+04
P_quantization = 1.4200041e+03

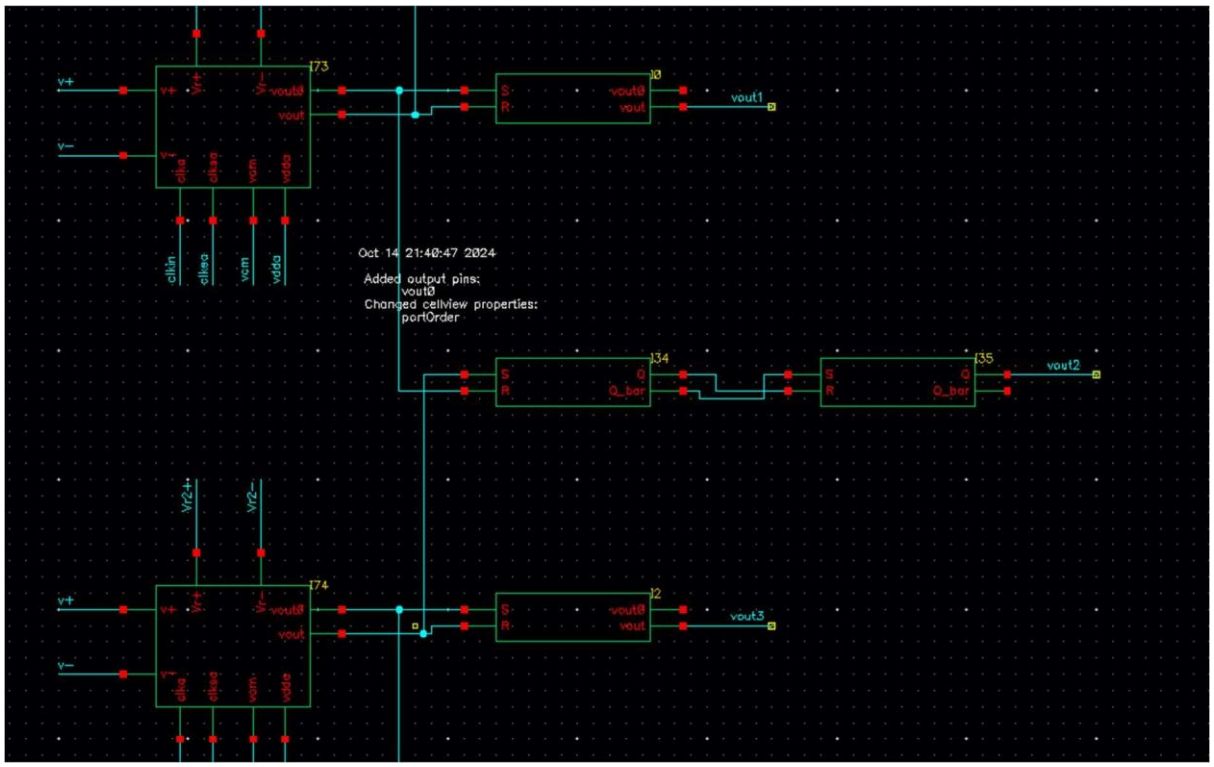
SQNR = 23 dB

For input frequency = 1 MHz (falls on bin)

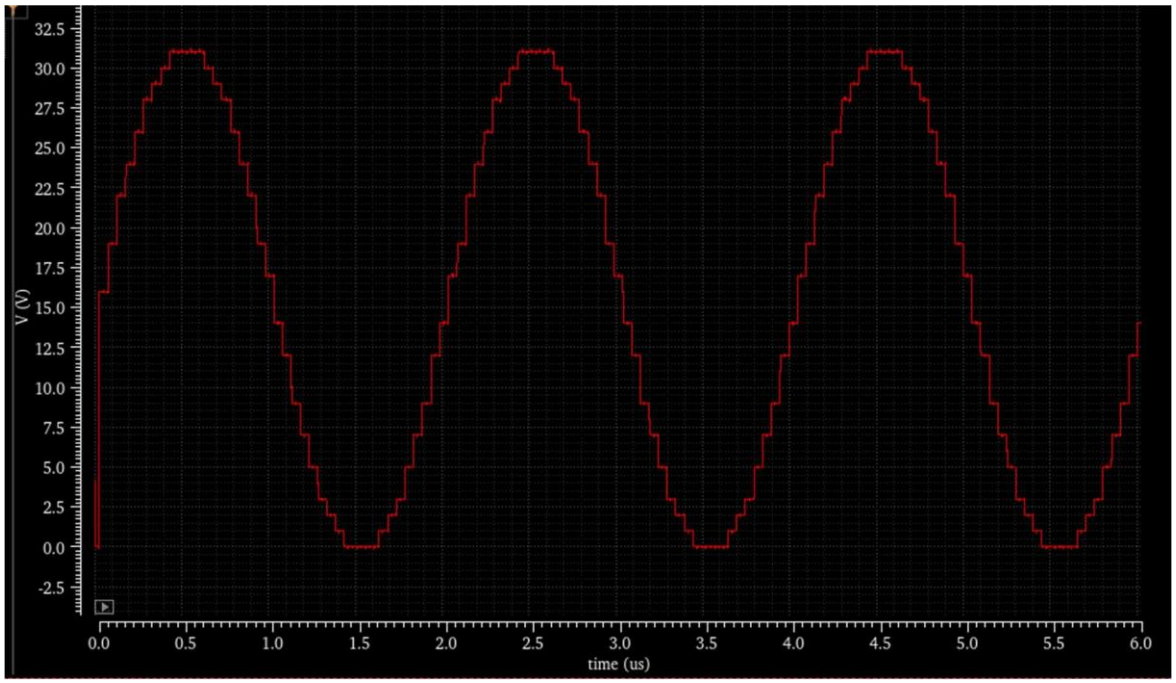
P at bin 98 = 1.549582e+04
P_signal = 1.549582e+04
P_quantization = 43.0576

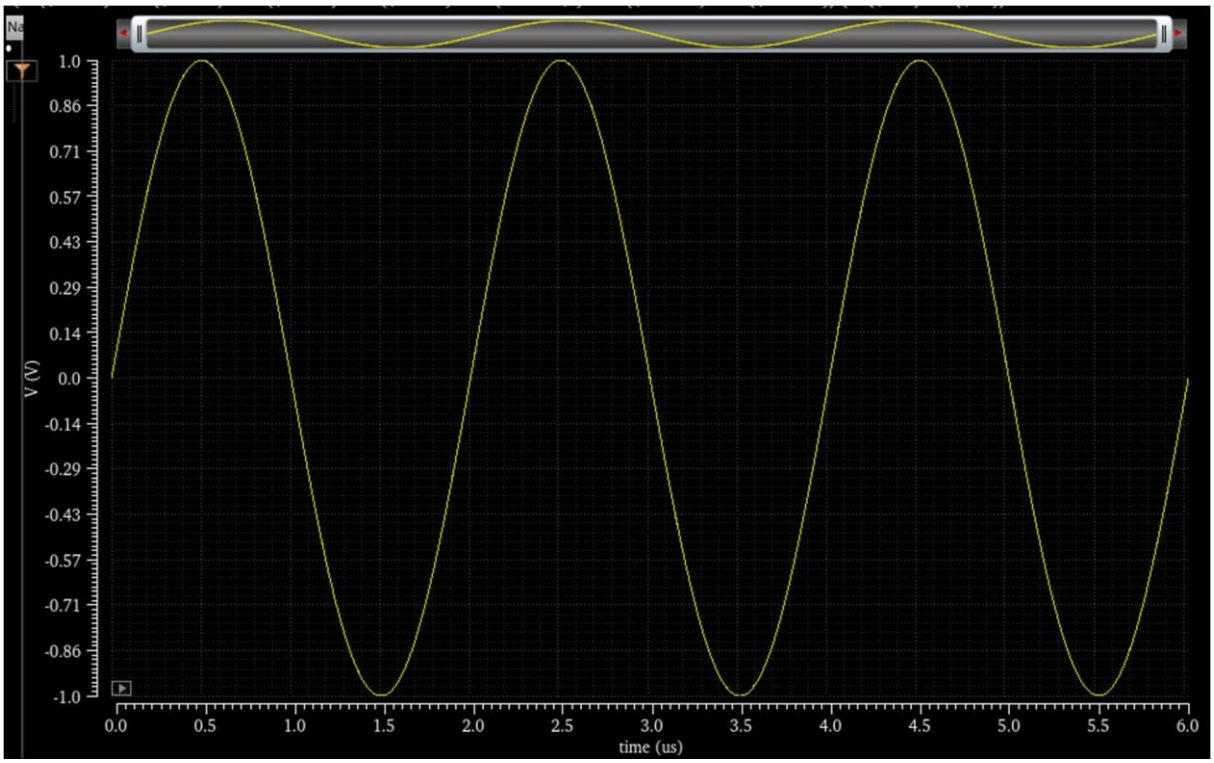
SQNR = 58.86 dB

Time Interpolation



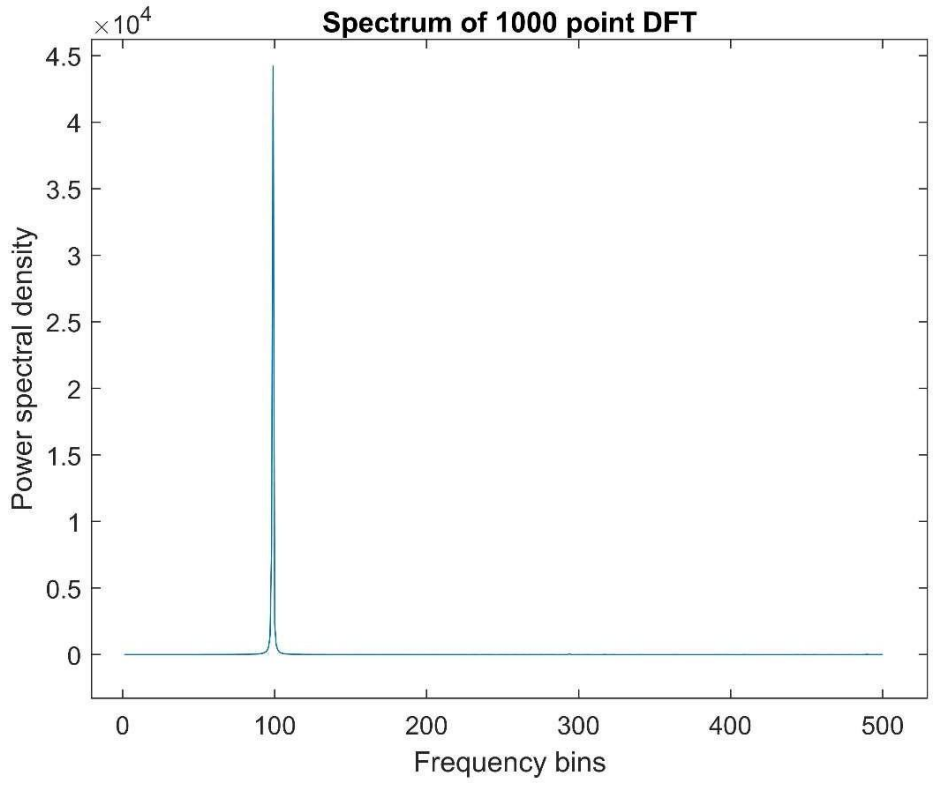
Between every 2 comparators an SR latch is added to give rise to a new bit.



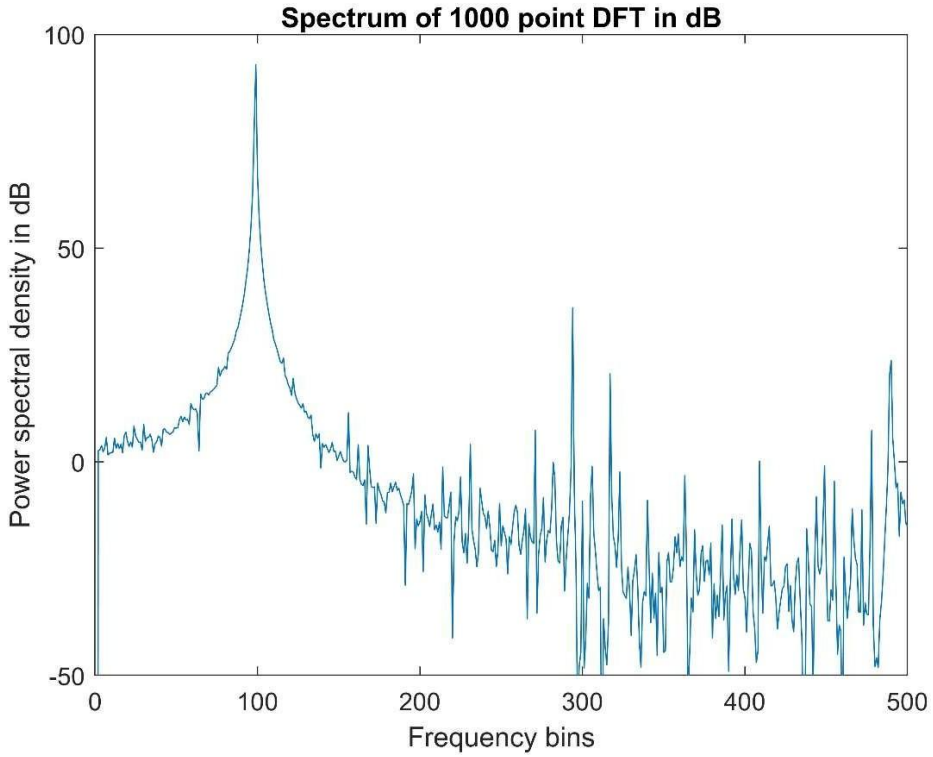

1.0
0.86
0.71
0.57
0.43
0.29
0.14
0.0
-0.14
-0.29
-0.43
-0.57
-0.71
-0.86
-1.0
V (V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
time (us)

Spectrum of 31-bit ADC

Input frequency = (97.7/1000) fs



In dB,



SQNR :

For input frequency = 1.954 MHz, (doesn’t fall on bin)

P at bin 97 to 101 = 5.994e+04 (Considering 5 point sum around signal)

P_signal = 5.994e+04
P_quantization = 3.4147e+03

SQNR = 28.65 dB