HOMEWORK OF THE SEMESTER IN HLS
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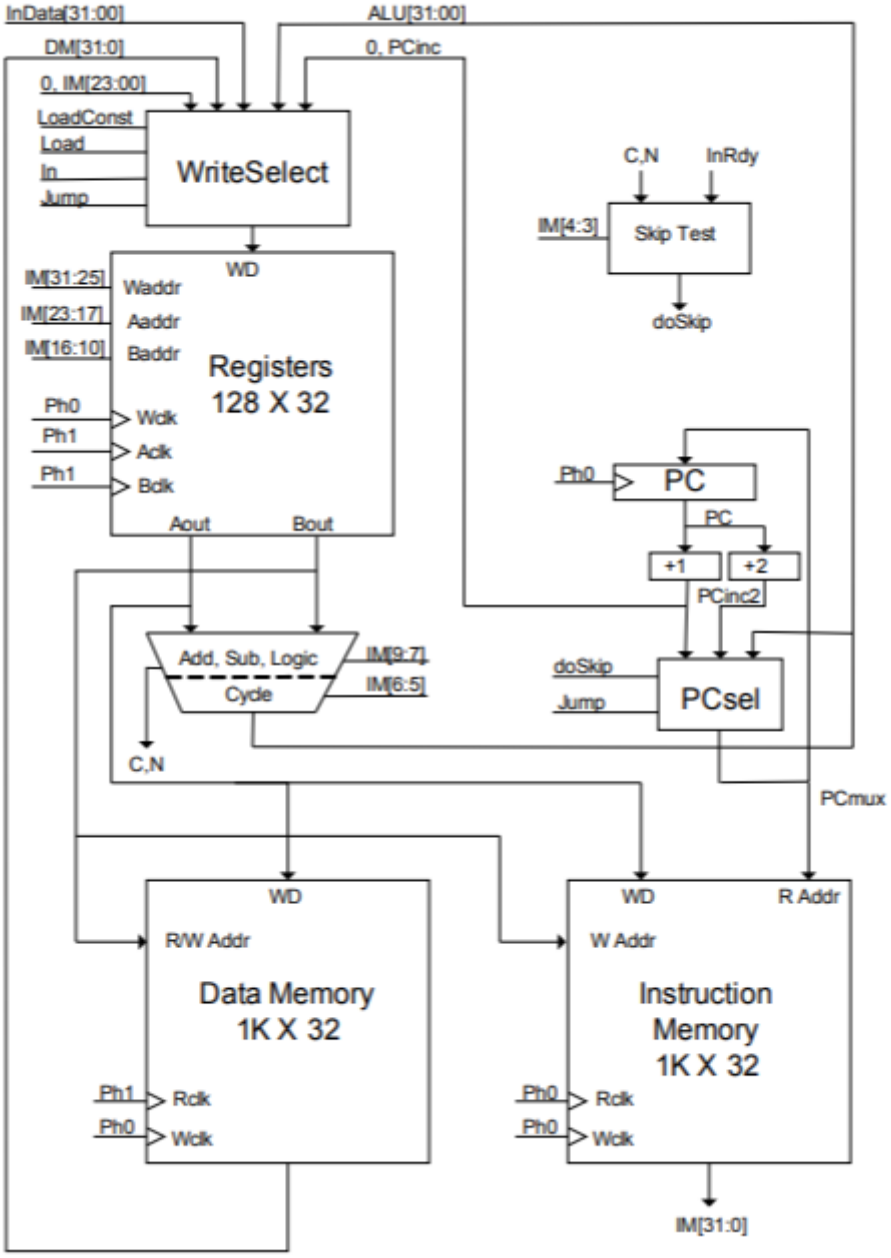
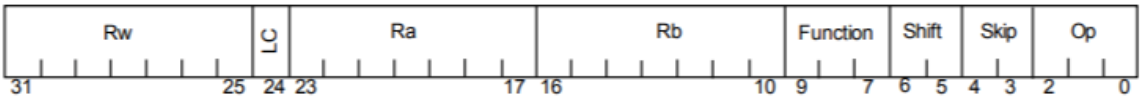
A TINY COMPUTER

The layout of the computer:



The format of instructions is:



The encodings:

OP ENCODINGS	ACTIONS	SKIP IF AVAILABLE	CODE ENCODINGS
000	RW<-Function(Ra,Rb)	Yes	Normal
001	DM[Rb]<-Ra, Rw<-Function(Ra,Rb)	Yes	StoreDM
010	IM[Rb]<-Ra, Rw<-Function(Ra,Rb)	Yes	StoreIM
011	Output_channel<-Ra, Rw<-Function(Ra,Rb)	Yes	Output
100	Rw <- DM[Rb], ALU <- F(Ra, Rb)	Yes	LoadDM
101	Rw<-Input_channel, ALU <- F(Ra, Rb)	Yes	Input
110	Rw <- PC + 1, PC <- Function(Ra, Rb)	No	Jump
111	Reserved	Yes	RsrvdOp

As it is presented from the array above, we are unable to have skip if our opcode is Jump.

SKIP ENCODINGS	ACTIONS	CODE ENCODINGS
00	PC<-PC+1	Never
01	If ALU<0:PC<-PC+2, else: PC<-PC+1	IfNegative
10	If ALU=0:PC<-PC+2, else: PC<-PC+1	IfZero
11	If ALU>0:PC<-PC+2, else: PC<-PC+1	IfPositive

SHIFT ENCODINGS	ACTIONS
00	No shift
01	Right Circular Shift by 1
10	Right Circular Shift by 8
11	Right Circular Shift by 16

FUNCTION ENCODINGS	ACTIONS	CODE ENCODINGS
000	A+B	AplusB
001	A-B	AminusB
010	B+1	Bplusone
011	B-1	Bminusone
100	A and B	AND
101	A or B	OR
110	A xor B	XOR
111	Reserved	RsrvdFun

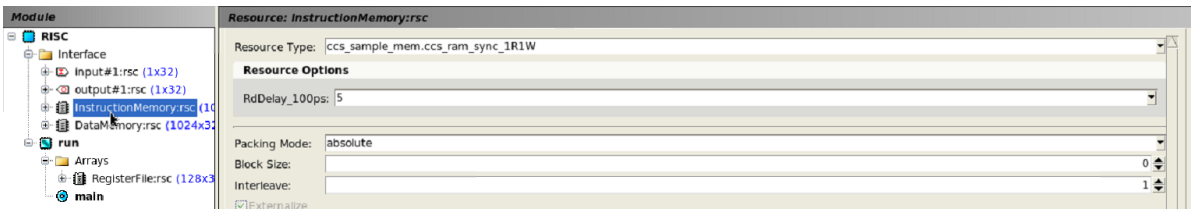
LOAD CONSTANT ENCODINGS	ACTIONS
0	Nothing
1	Rw<-Instruction[23:0]

CATAPULT

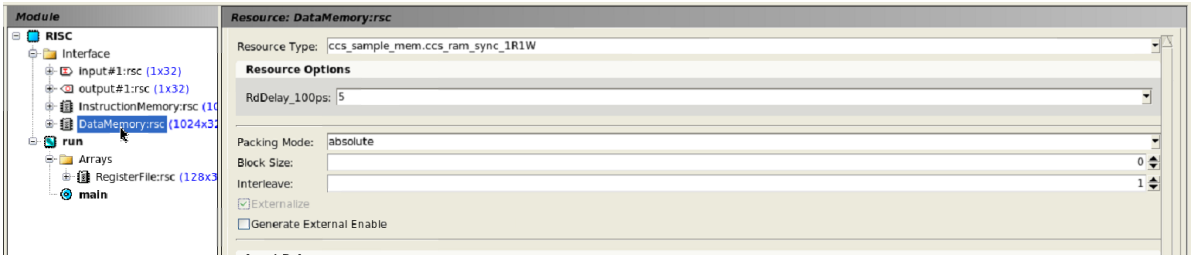
SETTINGS

In the architecture, we chose the following specifications for our memories:

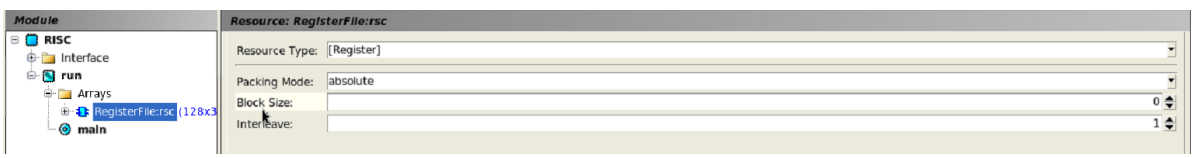
InstructionMemory:



DataMemory:

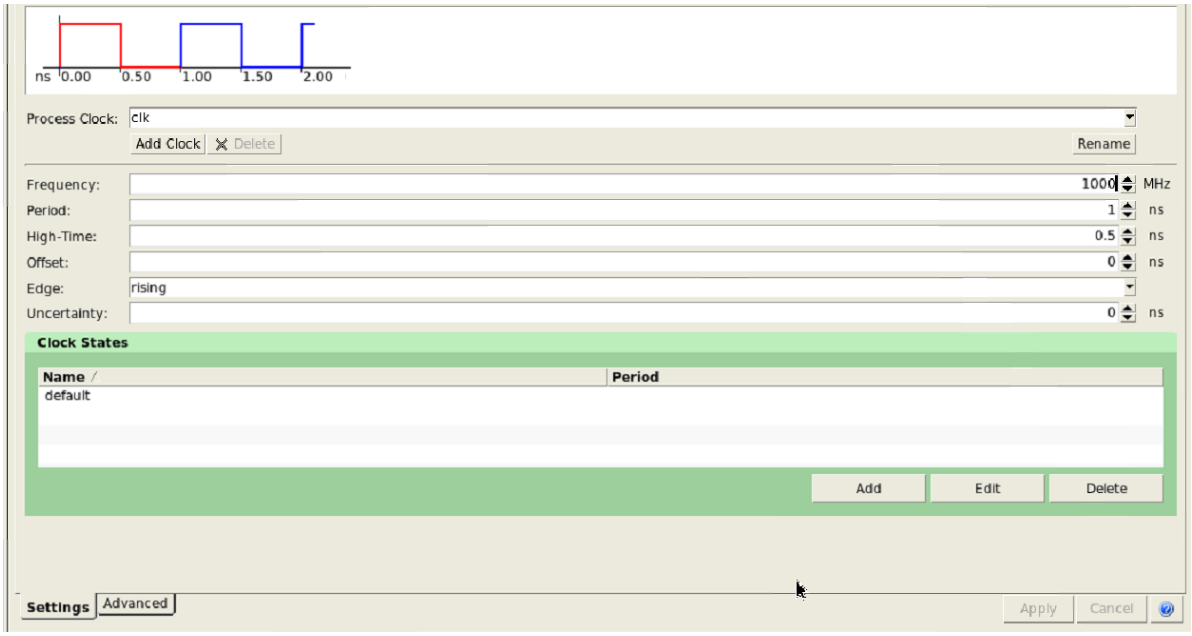


RegisterFile:



Clock:1000 MHz

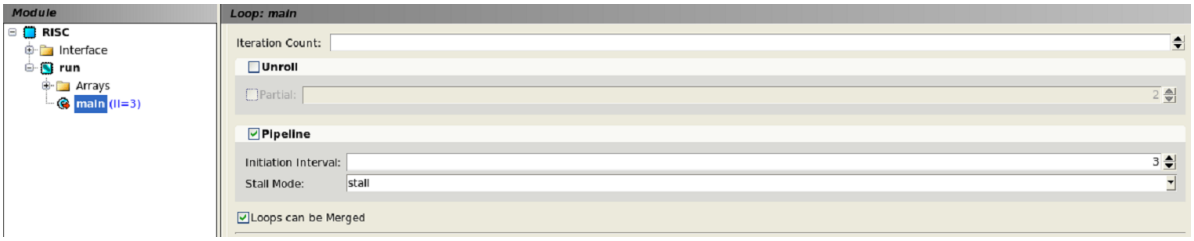
For the mapping we chose a clock of 1 GHz:



WITH WRITE TO INSTRUCTION MEMORY

Initiation Interval

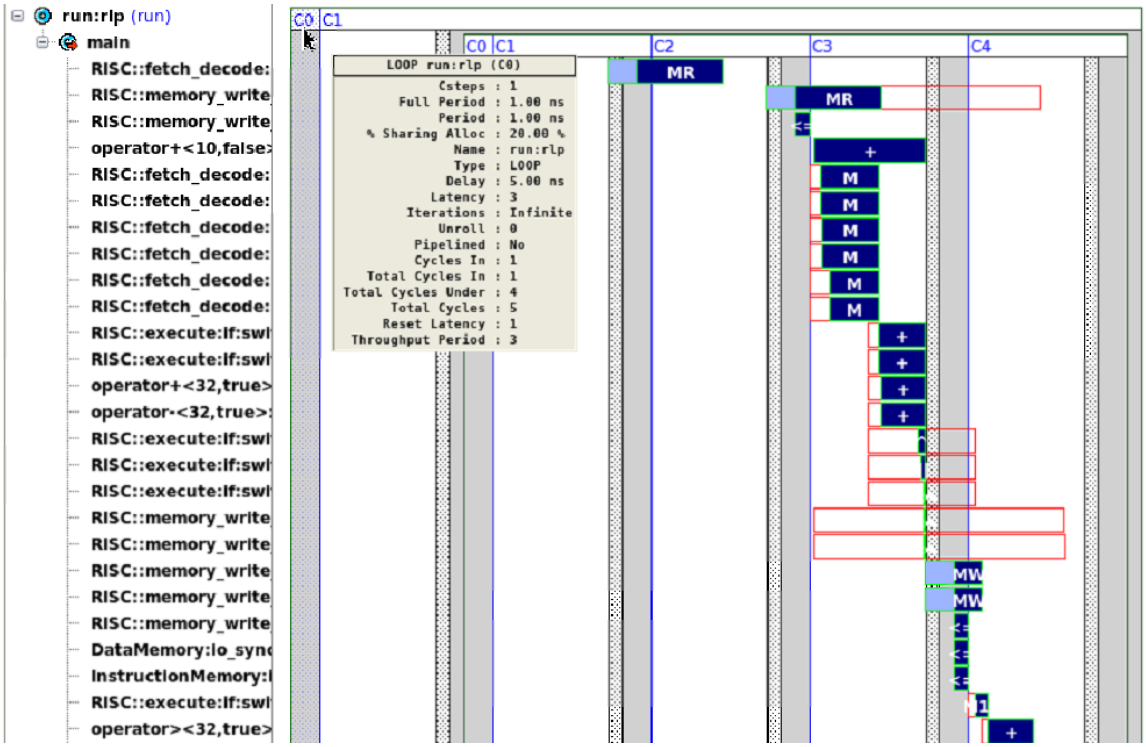
In the architecture, we chose, for our function, pipeline with initiation interval 3:



We were unable to achieve smaller initiation interval with this clock. The error with smaller initiation interval is:

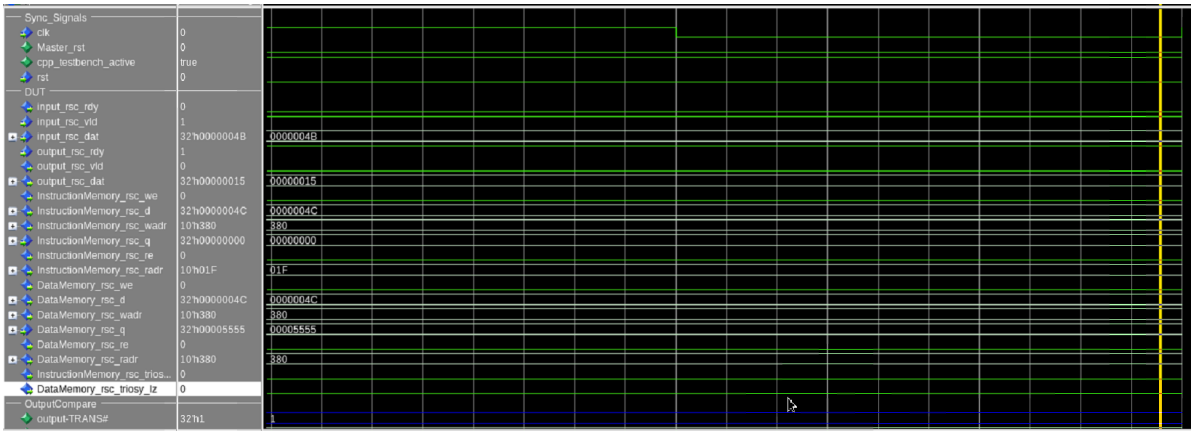
```
Feedback path is too long to schedule design with current pipeline and clock constraints.
```

Schedule



QUESTASIM

The waveforms have the form that is presented below:



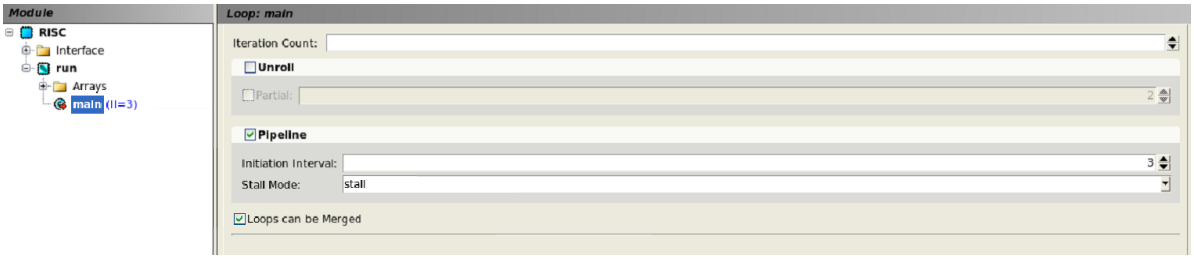
After our simulation, the transcript of Questasim prints the following messages:

```
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of input
#    captured 1 values of output
#    captured 27 values of InstructionMemory_IN
#    captured 27 values of InstructionMemory
#    captured 27 values of DataMemory_IN
#    captured 27 values of DataMemory
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'output'
#    capture count        = 1
#    comparison count     = 1
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'InstructionMemory'
#    capture count        = 27
#    comparison count     = 27
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'DataMemory'
#    capture count        = 27
#    comparison count     = 27
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 85500 ps
# ** Note: (vsim-6574) SystemC simulation stopped by user.
# Info: scverify_top/user_tb: Simulation completed
# ** Warning: (vsim-6614) sc_stop has already been called.
# 1
#
```

WITHOUT WRITE TO INSTRUCTION MEMORY

Initiation Interval

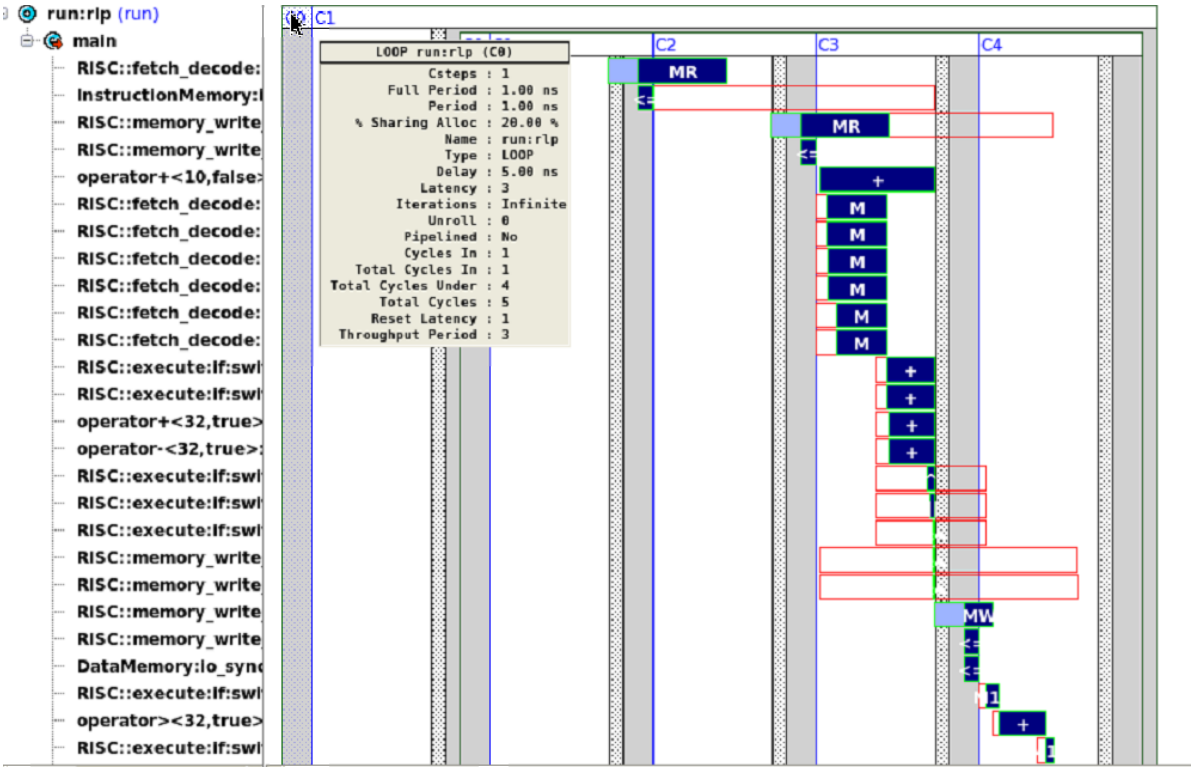
In the architecture, we chose, for our function, pipeline with initiation interval 3:



We were unable to achieve smaller initiation interval with this clock. The error with smaller initiation interval is:

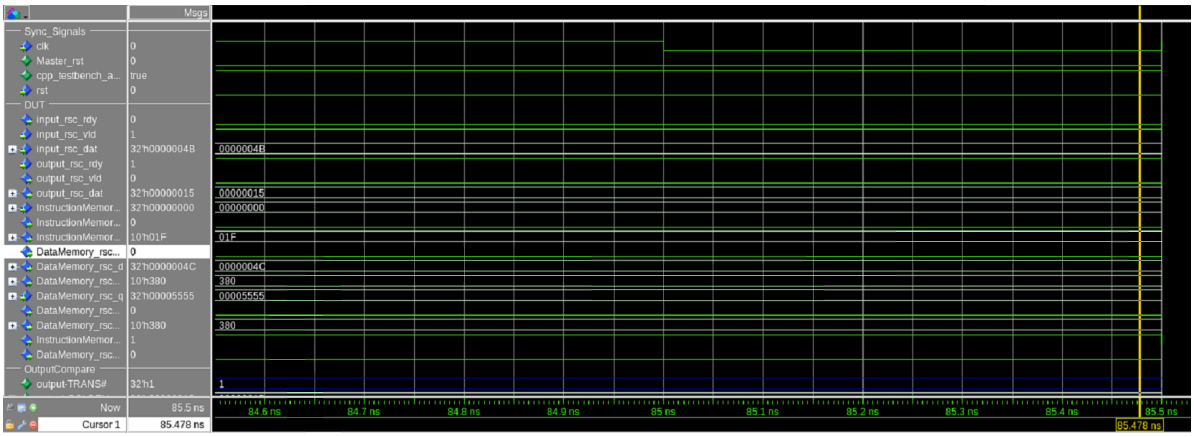
```
Feedback path is too long to schedule design with current pipeline and clock constraints.
```

Schedule



QUESTASIM

The waveforms have the form that is presented below:

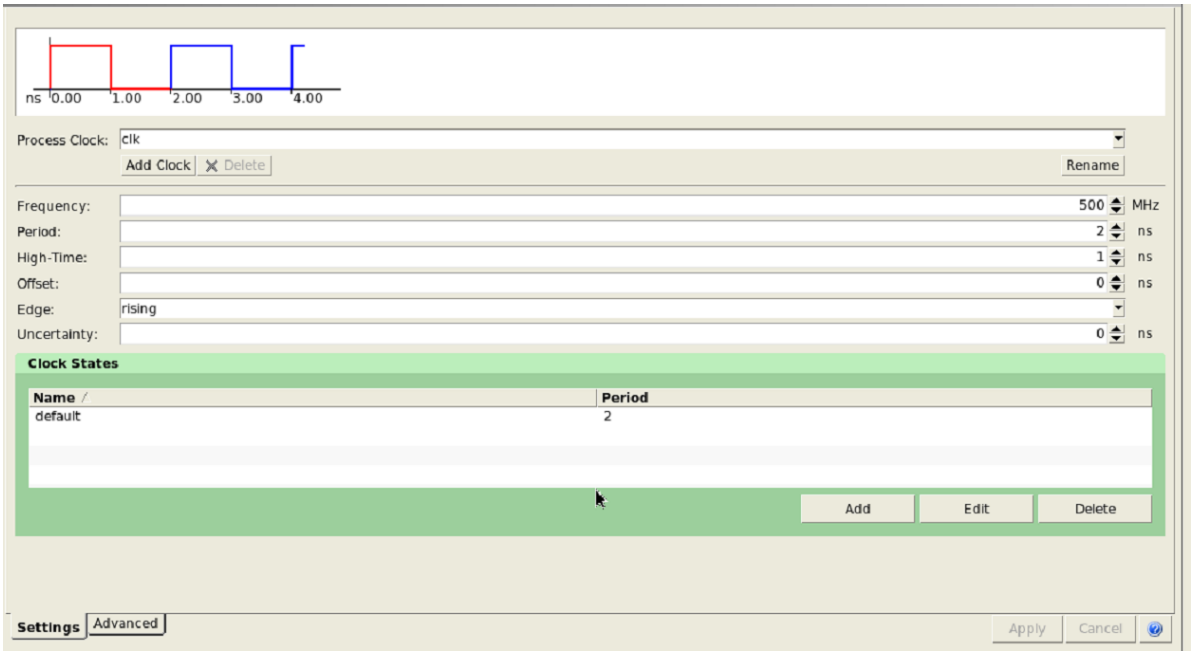


After our simulation, the transcript of Questasim prints the following messages:

```
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of input
#    captured 1 values of output
#    captured 27 values of InstructionMemory
#    captured 27 values of DataMemory_IN
#    captured 27 values of DataMemory
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'output'
#    capture count        = 1
#    comparison count     = 1
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'DataMemory'
#    capture count        = 27
#    comparison count     = 27
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 85500 ps
# ** Note: (vsim-6574) SystemC simulation stopped by user.
# Info: scverify_top/user_tb: Simulation completed
# ** Warning: (vsim-6614) sc_stop has already been called.
# 1
#
```

Clock:500 MHz

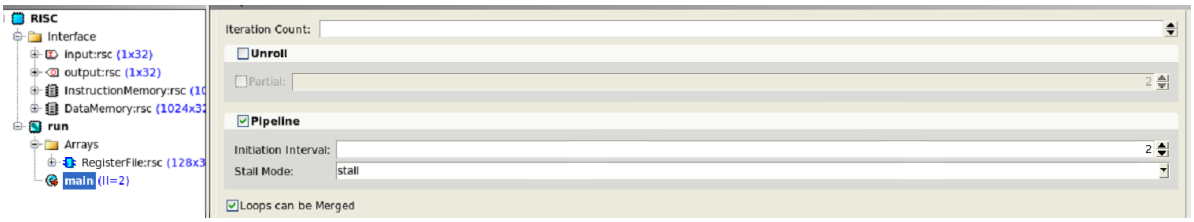
For the mapping we chose a clock of 0.5 GHz:



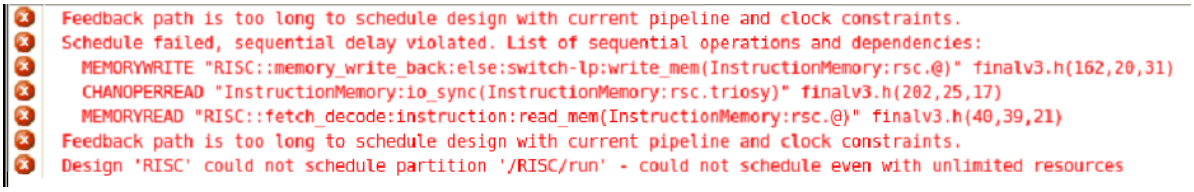
WITH WRITE TO INSTRUCTION MEMORY

Initiation Interval

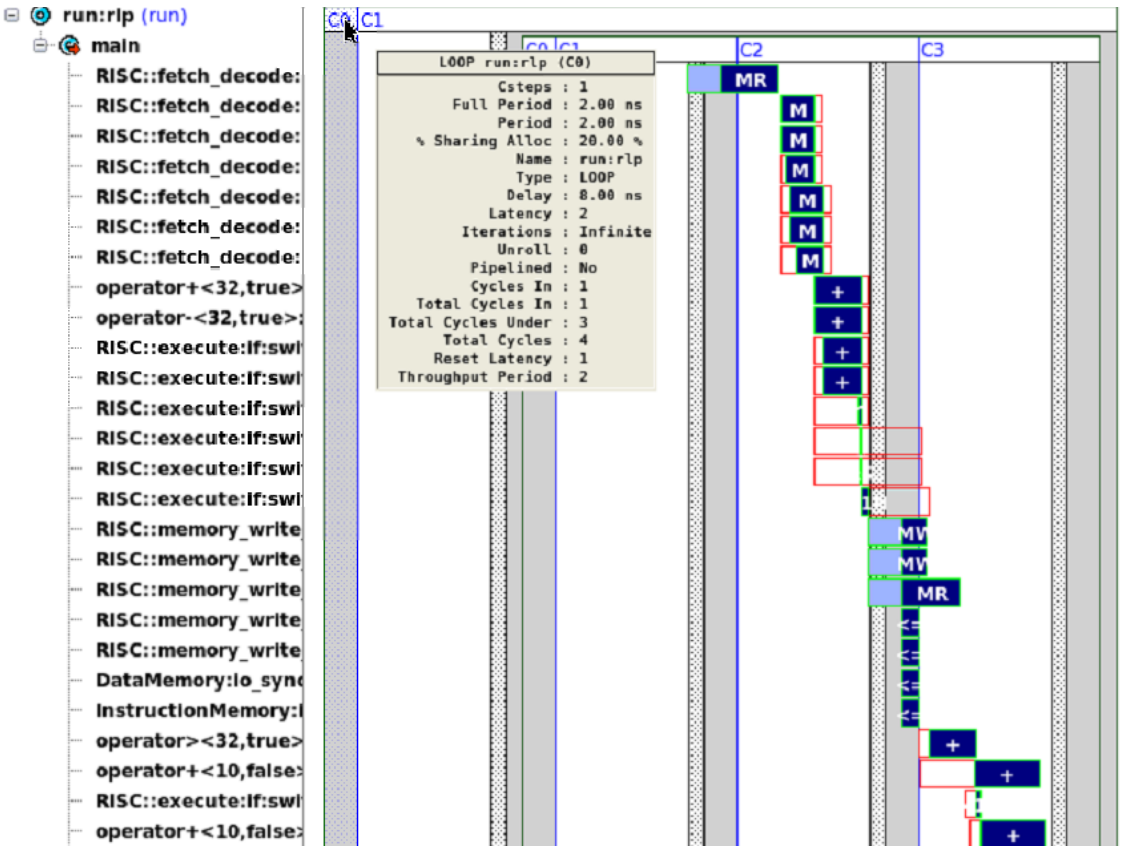
In the architecture, we chose, for our function, pipeline with initiation interval 2:



We were unable to achieve smaller initiation interval with this clock. The error with smaller initiation interval is:

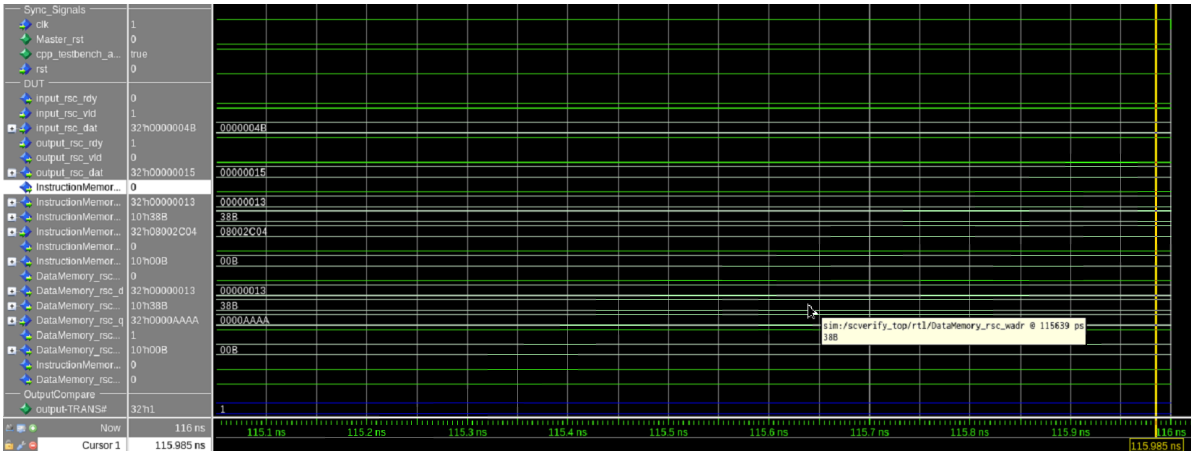


Schedule



QUESTASIM

The waveforms have the form that is presented below:



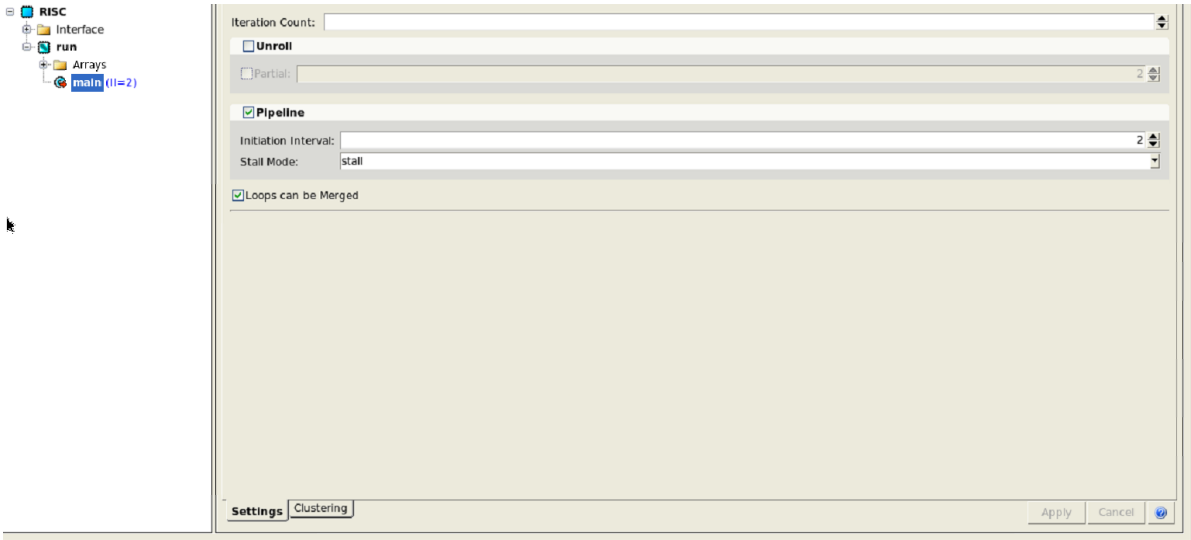
After our simulation, the transcript of Questasim prints the following messages:

```
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of input
#    captured 1 values of output
#    captured 27 values of InstructionMemory_IN
#    captured 27 values of InstructionMemory
#    captured 27 values of DataMemory_IN
#    captured 27 values of DataMemory
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'output'
#    capture count       = 1
#    comparison count    = 1
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
# 'InstructionMemory'
#    capture count       = 27
#    comparison count    = 27
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
# 'DataMemory'
#    capture count       = 27
#    comparison count    = 27
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 116 ns
# ** Note: (vsim-6574) SystemC simulation stopped by user.
# 1
#
```

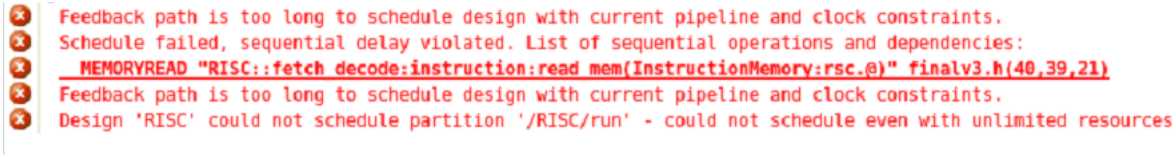
WITHOUT WRITE TO INSTRUCTION MEMORY

Initiation Interval

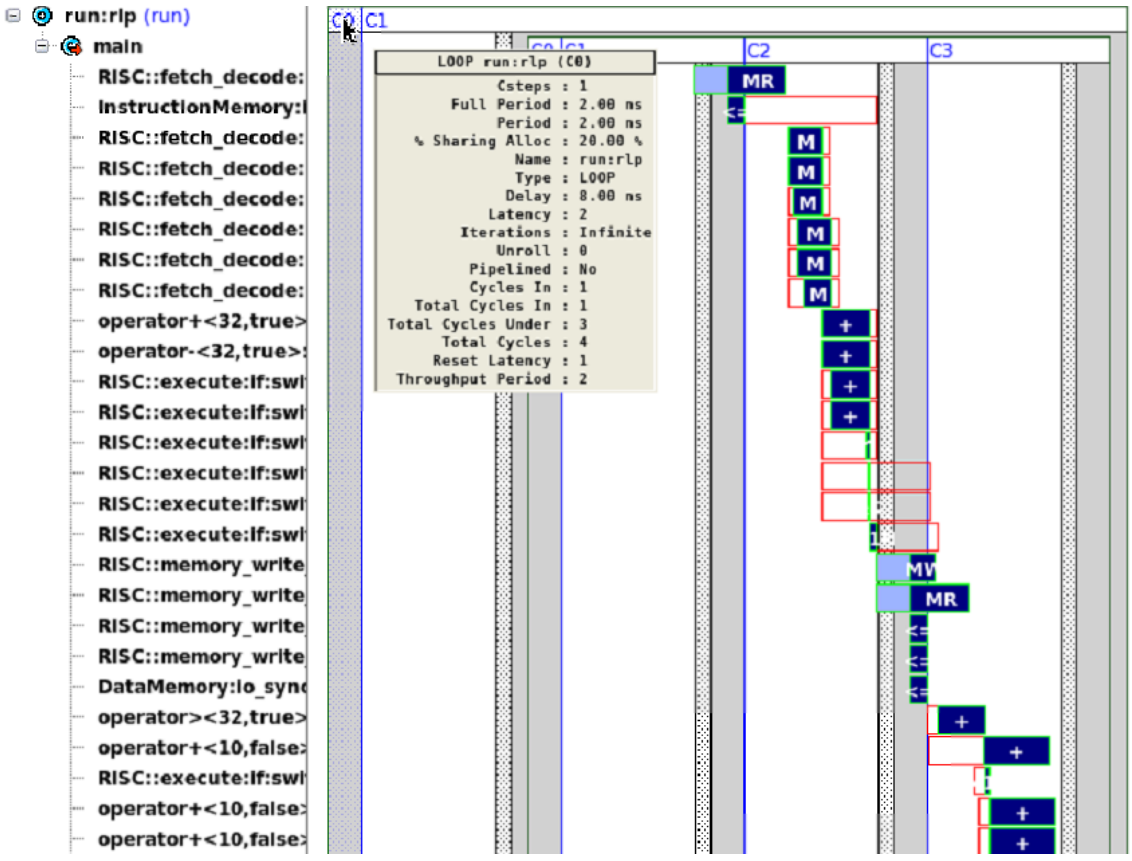
In the architecture, we chose, for our function, pipeline with initiation interval 2:



We were unable to achieve smaller initiation interval with this clock. The error with smaller initiation interval is:

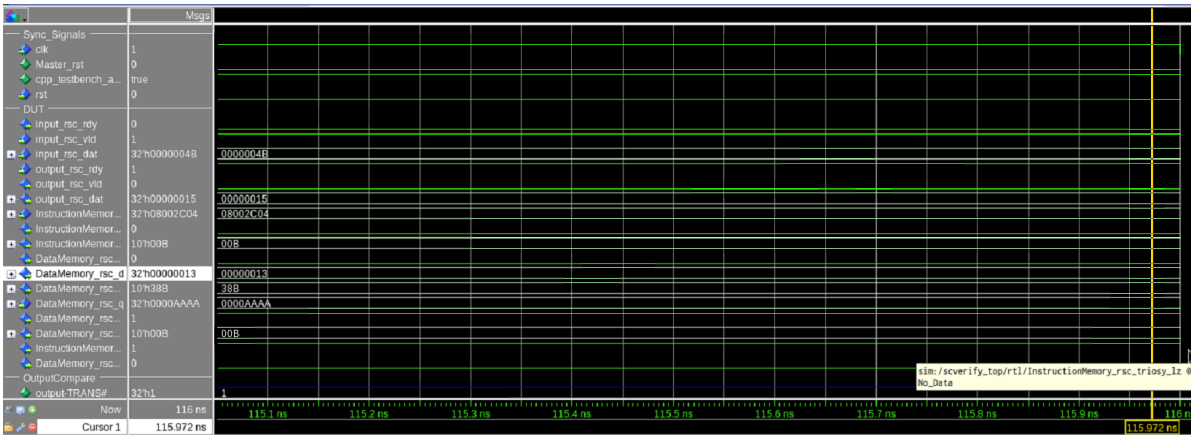


Schedule



QUESTASIM

The waveforms have the form that is presented below:

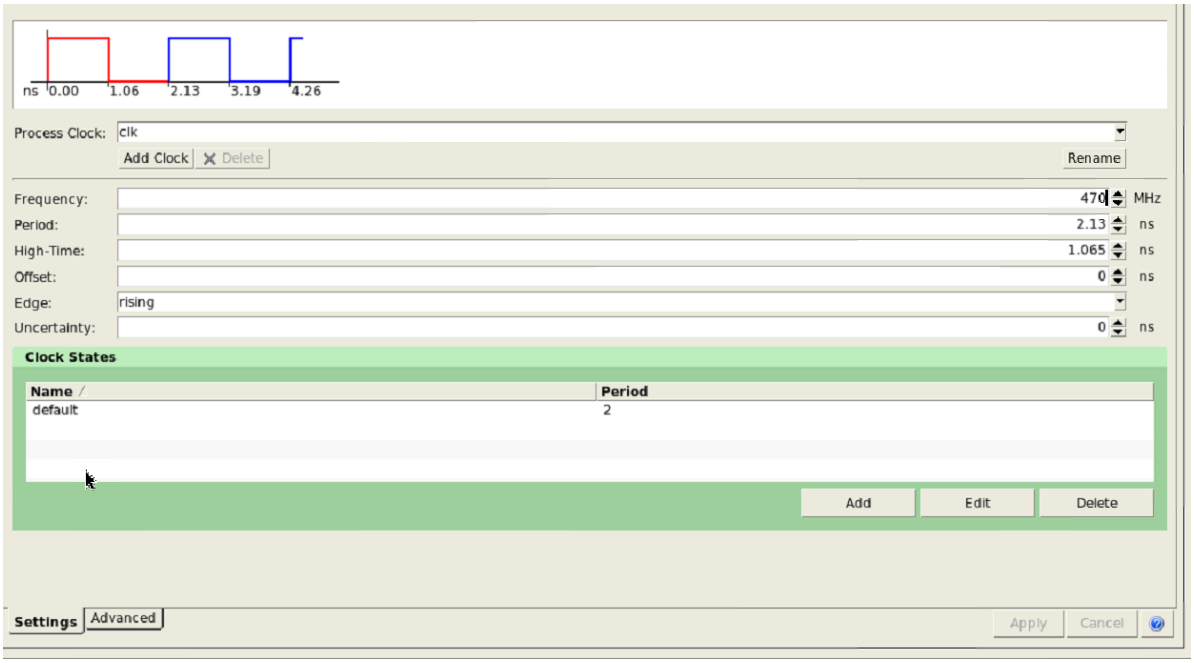


After our simulation, the transcript of Questasim prints the following messages:

```
#
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of input
#    captured 1 values of output
#    captured 27 values of InstructionMemory
#    captured 27 values of DataMemory_IN
#    captured 27 values of DataMemory
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'output'
#    capture count       = 1
#    comparison count    = 1
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
# 'DataMemory'
#    capture count       = 27
#    comparison count    = 27
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 116 ns
# ** Note: (vsim-6574) SystemC simulation stopped by user.
# 1
#
```

Clock:470 MHz

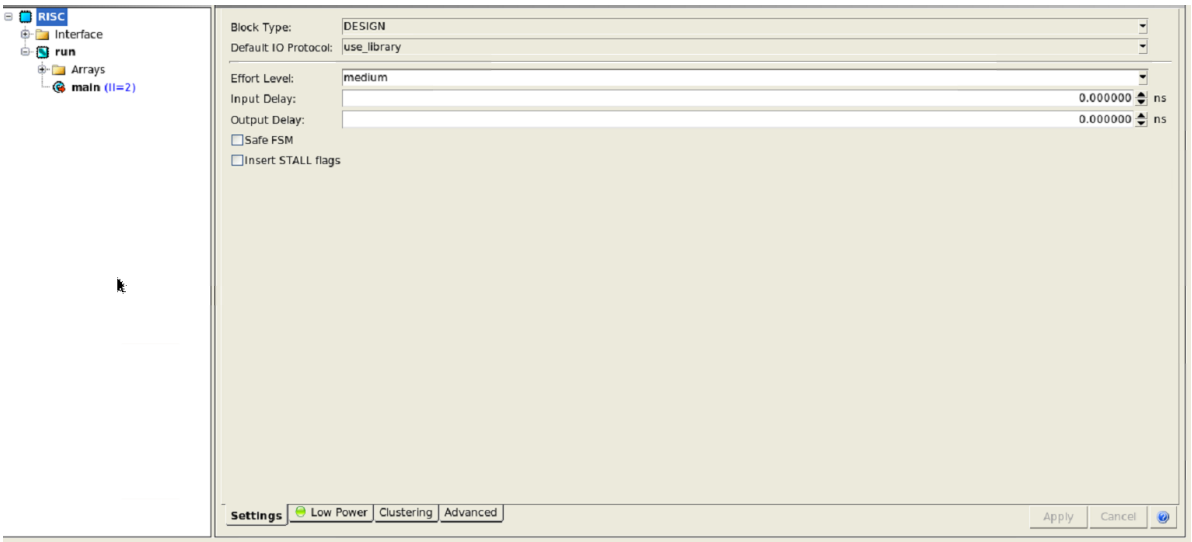
For the mapping we chose a clock of 0.47 GHz:



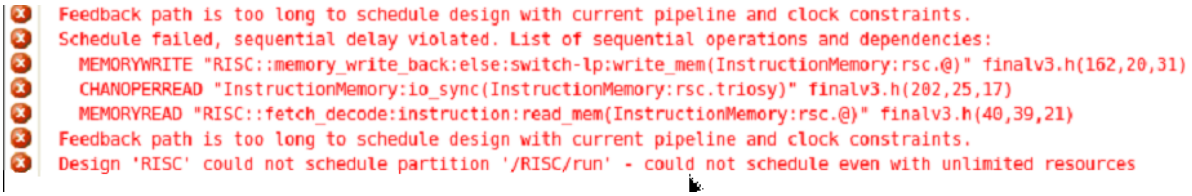
WITH WRITE TO INSTRUCTION MEMORY

Initiation Interval

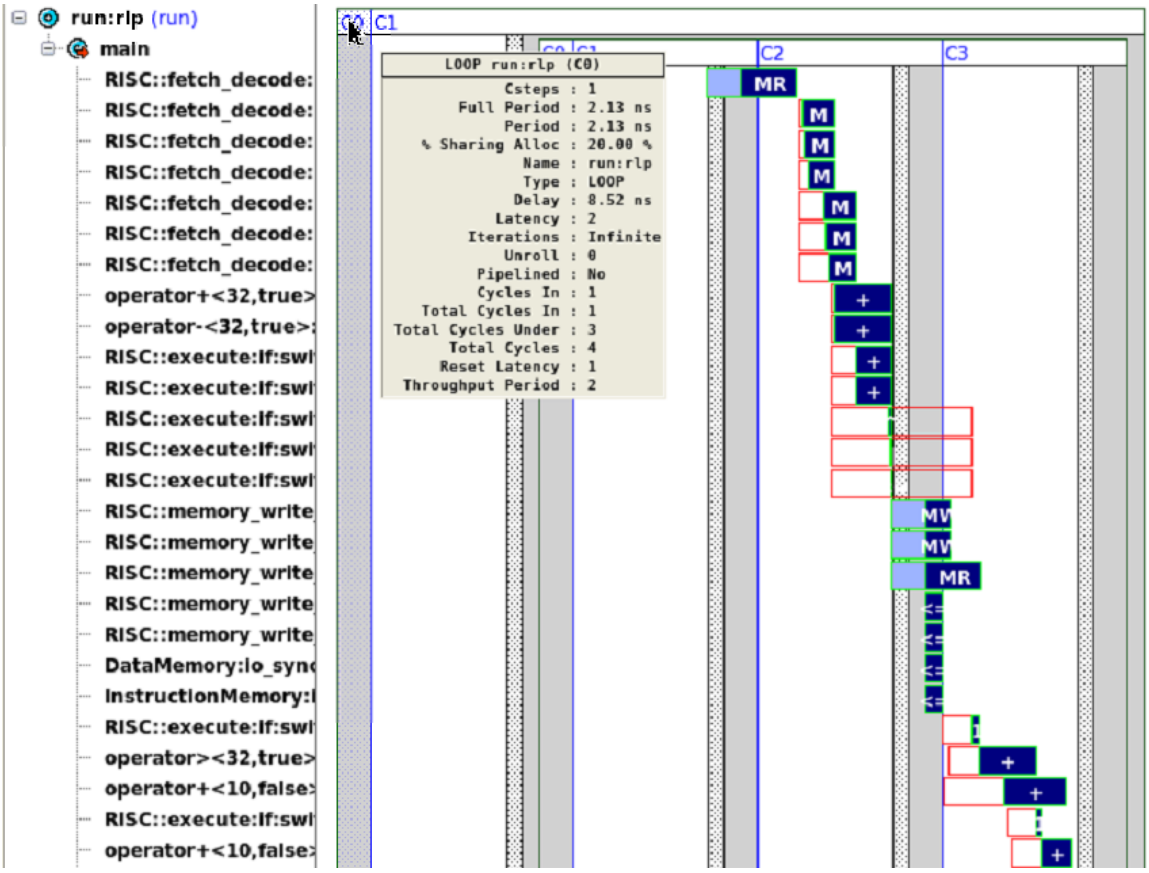
In the architecture, we chose, for our function, pipeline with initiation interval 2:



We were unable to achieve smaller initiation interval with this clock. The error with smaller initiation interval is:



Schedule

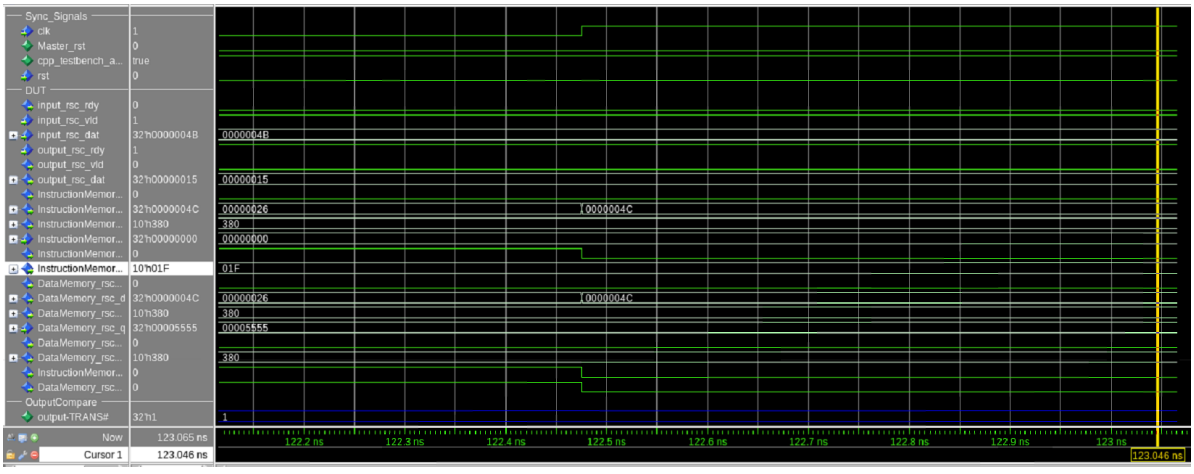


QUESTASIM

The waveforms have the form that is presented below:

```
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of input
#    captured 1 values of output
#    captured 27 values of InstructionMemory_IN
#    captured 27 values of InstructionMemory
#    captured 27 values of DataMemory_IN
#    captured 27 values of DataMemory
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'output'
#    capture count        = 1
#    comparison count     = 1
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'InstructionMemory'
#    capture count        = 27
#    comparison count     = 27
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'DataMemory'
#    capture count        = 27
#    comparison count     = 27
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 123065 ps
# ** Note: (vsim-6574) SystemC simulation stopped by user.
# 1
#
```

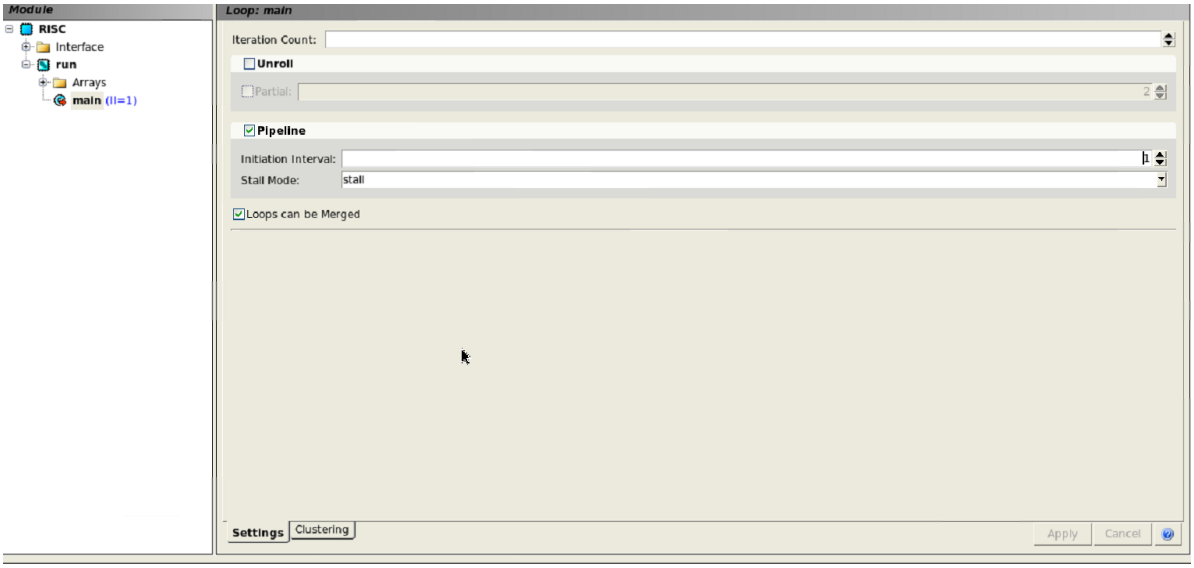
After our simulation, the transcript of Questasim prints the following messages:



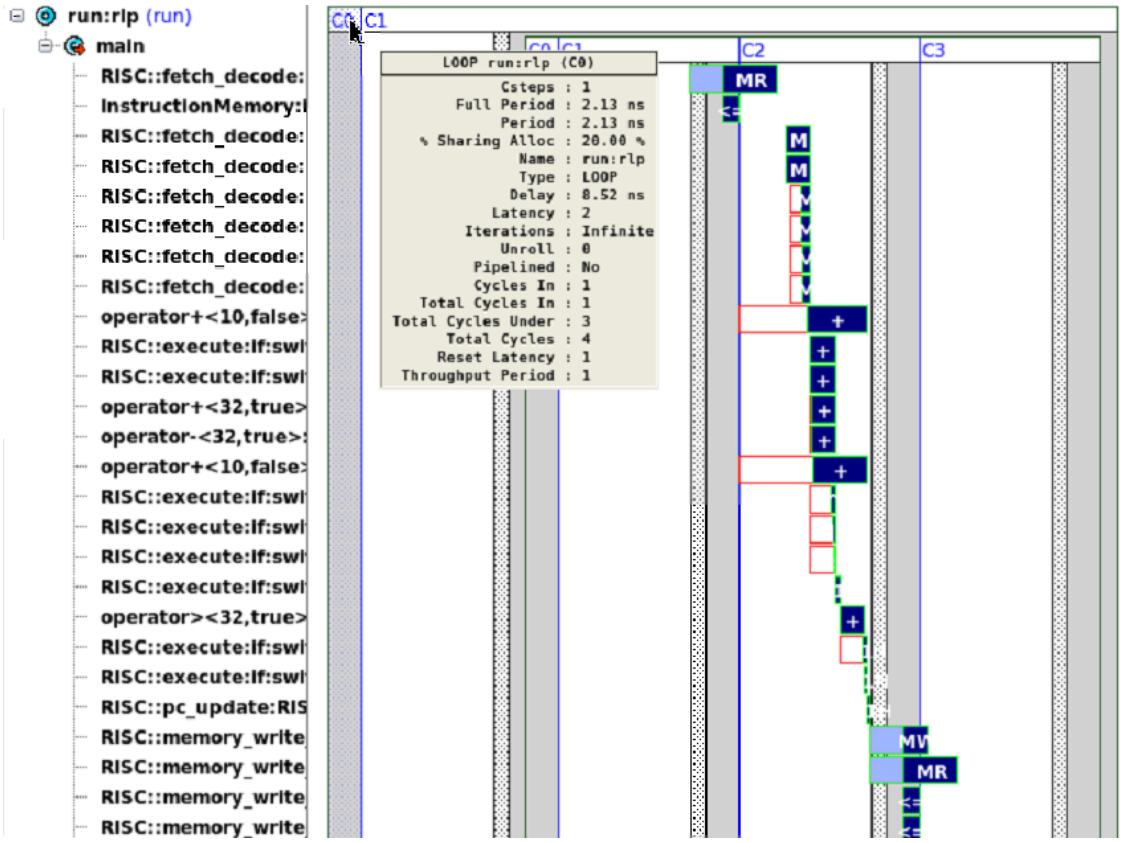
WITHOUT WRITE TO INSTRUCTION MEMORY

Initiation Interval

In the architecture, we chose, for our function, pipeline with initiation interval 1:

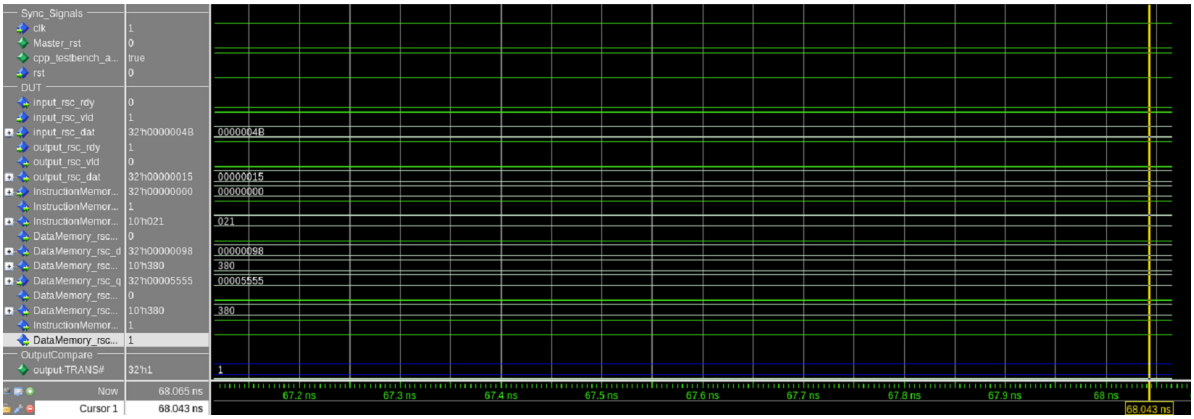


Schedule



QUESTASIM

The waveforms have the form that is presented below:



After our simulation, the transcript of Questasim prints the following messages:

```
#
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of input
#    captured 1 values of output
#    captured 27 values of InstructionMemory
#    captured 27 values of DataMemory_IN
#    captured 27 values of DataMemory
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'output'
#    capture count       = 1
#    comparison count    = 1
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
# 'DataMemory'
#    capture count       = 27
#    comparison count    = 27
#    ignore count        = 0
#    error count         = 0
#    stuck in dut fifo   = 0
#    stuck in golden fifo = 0
#
# Info: scverify_top/user_tb: Simulation PASSED @ 68065 ps
# ** Note: (vsim-6574) SystemC simulation stopped by user.
# 1
#
```

REFERENCES

1. https://www.cl.cam.ac.uk/teaching/1112/ECAD+Arch/files/Thacker-A_Tiny_Computer-3.pdf, A Tiny Computer.