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Nordin

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- [54] COMPUTER IMPLEMENTED MACHINE
LEARNING METHOD AND SYSTEM
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- [22] Filed: Jul. 12, 1996
- [51] Int. Cl.⁶ G06F 15/18
- [52] U.S. Cl. 395/13
- [58] Field of Search 395/13

[56] References Cited

U.S. PATENT DOCUMENTS			
4,697,242	9/1987	Holland et al.	395/13
4,821,333	4/1989	Gillies	382/308
4,881,178	11/1989	Holland et al.	395/51
4,935,877	6/1990	Koza	395/13
4,961,152	10/1990	Davis	395/13
5,048,095	9/1991	Bhanu et al.	382/173
5,136,686	8/1992	Koza	395/13
5,140,530	8/1992	Guha et al.	395/13
5,148,513	9/1992	Koza et al.	395/13
5,182,793	1/1993	Alexander et al.	395/13
5,222,192	6/1993	Shaefer	395/13
5,224,176	6/1993	Crain	382/34
5,245,696	9/1993	Stork et al.	395/13
5,249,259	9/1993	Harvey	395/13
5,255,345	10/1993	Schaefer	395/13
5,274,744	12/1993	Yu et al.	395/24
5,301,256	4/1994	Nakamura	395/10
5,343,554	8/1994	Koza et al.	395/13
5,390,282	2/1995	Koza et al.	395/13
5,390,283	2/1995	Eshelman et al.	395/13
5,394,509	2/1995	Winston	395/13
5,400,436	3/1995	Nara et al.	395/13
5,410,634	4/1995	Li	395/10
5,428,709	6/1995	Banzhaf	395/13
5,434,796	7/1995	Weininger	364/496
5,440,723	8/1995	Arnold et al.	395/181
5,455,938	10/1995	Ahmed et al.	364/488
5,471,593	11/1995	Branigin	395/375

FOREIGN PATENT DOCUMENTS			
0696000	2/1996	European Pat. Off. .	

OTHER PUBLICATIONS

John R. Koza, "Genetic Programming—On the Programming of Computers by Means of Natural Selection", 1992, pp. 1–786, Massachusetts Institute of Technology, USA.

Earl Cox "The Fuzzy Systems Handbook: A Practitioner's Guide To Building, Using, And Maintaining Fuzzy Systems" Chapter 3, 1994, pp. 21–121, by Academic Press, Inc. London.

Valluru Rao, "C++ Neural Networks and Fuzzy Logic", 1995, Chapter 7, pp. 123–177, MIS:Press, USA.

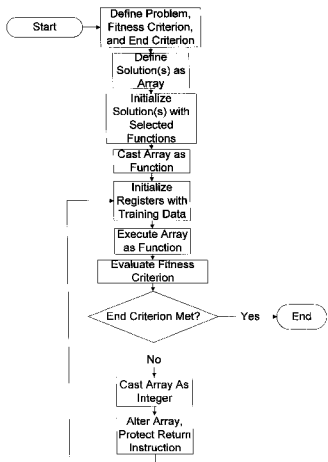
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[57] ABSTRACT

One or more machine code entities such as functions are created which represent solutions to a problem and are directly executable by a computer. The programs are created and altered by a program in a higher level language such as "C" which is not directly executable, but requires translation into executable machine code through compilation, interpretation, translation, etc. The entities are initially created as an integer array that can be altered by the program as data, and are executed by the program by recasting a pointer to the array as a function type. The entities are evaluated by executing them with training data as inputs, and calculating fitnesses based on a predetermined criterion. The entities are then altered based on their fitnesses using a machine learning algorithm by recasting the pointer to the array as a data (e.g. integer) type. This process is iteratively repeated until an end criterion is reached. The entities evolve in such a manner as to improve their fitness, and one entity is ultimately produced which represents an optimal solution to the problem. Each entity includes a plurality of directly executable machine code instructions, a header, a footer, and a return instruction. The alteration process is controlled such that only valid instructions are produced. The headers, footers and return instructions are protected from alteration. The system can be implemented on an integrated circuit chip, with the entities stored in high speed memory in a central processing unit.

111 Claims, 30 Drawing Sheets



OTHER PUBLICATIONS

- Valluru Rao, "C++ Neural Networks and Fuzzy Logic", 1995, Chapter 9, pp. 217–242, MIS:Press, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, Chapter 2, pp. 22–42, Massachusetts Institute of Technology, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, Chapter 14, pp. 311–331, Massachusetts Institute of Technology, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, Chapter 1, pp. 3–19, Massachusetts Institute of Technology, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, Chapter 5, pp. 99–117, Massachusetts Institute of Technology, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, Chapter 13, pp. 285–310, Massachusetts Institute of Technology, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, II, pp. 43–45, Massachusetts Institute of Technology, USA.
- Kenneth B. Kinnear, Jr. "Advances in Genetic Programming", 1994, Chapter 9, pp. 200–219, Massachusetts Institute of Technology, USA.
- Patrik D'Haeseleer "Context Preserving Crossover in Genetic Programming", Jun. 27–29, 1994, pp. 256–261, vol. 1, IEEE Press, USA, In Proceedings of the 1994 IEEE World Congress on Computational Intelligence.
- W. B. Langdon "Directed Crossover within Genetic Programming", Feb. 9, 1996, Dept. of Computer Science, University College London.
- Peter Nordin, Frank Francone and Wolfgang Banzhaf "Explicitly Defined Introns and Destructive Crossover in Genetic Programming", Jul. 30, 1995, MIT Press, Cambridge, MA, Advances in Genetic Programming II.
- Peter Nordin, Wolfgang Banzhaf "Evolving Turing-Complete Programs for a Register Machine with Self-modifying Code", 1995, Proc. of Int. Conference on Genetic Algorithms, USA.
- Peter Nordin, Wolfgang Banzhaf "Complexity Compression and Evolution", 1995, Proc. of Int. Conference on Genetic Algorithms, USA.
- Peter Nordin, Wolfgang Banzhaf "Genetic Programming Controlling a Miniature Robot", Nov. 10–12, 1995, pp. 61–67, AAAI Fall Symposium Series, Symposium on Genetic Programming, MIT, Cambridge, MA.
- Peter Nordin, Wolfgang Banzhaf "Real Time Evolution of Behavior and a World Model for a Miniature Robot using Genetic Programming", Nov. 1995, pp. 1–32, Dept. of CS, University of Dortmund, Germany.
- Arthur S. Bickel, Riva Wenig Bickel "Tree Structured Rules in Genetic Algorithms", Jul. 28–31, 1987 pp. 77–81, Lawrence Erlbaum Associates: Hillsdale, New Jersey, In John J. Grefenstette, editor, Genetic Algorithms and their Applications: Proceedings of the Second International Conference on Genetic Algorithms and Their Applications, MIT, USA.
- Cory Fujiki, John Dickinson "Using the Genetic Algorithm to Generate Lisp Source Code to Solve the Prisoner's Dilemma", Jul. 1987, USA, Grefenstette: Proceedings of Second International Conference on Genetic Algorithms.
- Kenneth De Jong "On Using Genetic Algorithms to Search Program Spaces", 1987, Grefenstette: Proceedings of Second International Conference on Genetic Algorithms.
- Nichael Lynn Cramer "A Representation for the Adaptive Generation of Simple Sequential Programs", 1985, pp. 183–187, Grefenstette: Proceedings of First International Conference on Genetic Algorithms.
- R.M. Friedberg "A Learning Machine", IBM Journal, Jan. 1958, pp. 2–13, Part I.
- R.M. Friedberg "A Learning Machine", IBM Journal, Jul. 1959, pp. 282–287, Part II.
- Walter Alden Tackett "Recombination, Selection, and the Genetic Construction of Computer Programs", 1994, Chapter 5, pp. 84–96, A Dissertation Presented to the Faculty of the Graduate School University of Southern California.
- C.E. Rasmussen, R.M. Neal, G.E. Hinton, D. van Camp, M. Revow, Z. Ghahramani, R. Kustra and R. Tibshirani "The DELVE Manual" 1995–1996, pp. 1–102, Version 1.0a, The University of Toronto, Canada.
- Prof. Dr. Ing. I. Rechenberg, "evoC 2.0 user manual" Jun. 12, 1994, Technical University of Berlin, Germany.
- Douglas Zongker, Dr. Bill Punch, Bill Rand "Lil-GP 1.10 User's Manual", 1995, Michigan State University, USA.
- Overview of GALib, Genetic Algorithm Library, 1995, MIT.
- Andrew Hunter "SUGAL User Manual", Jul. 1995, pp. 1–55, V2.1.
- Helmut Horner "AC++ Class Library for Genetic Programming: The Vienna University of Economics Genetic Programming Kernel", May 29, 1996, pp. 1–67.
- David Levine "User's Guide to the PGAPack Parallel Genetic Algorithm Library", Jan. 31, 1996, pp. 1–47, Mathematics and CS Division, Argonne National Laboratory, USA.
- Ronald L. Crapeau "Genetic Evolution of Machine Language Software", Jul. 9, 1995, pp. 121–134.
- Andrew Schulman, David Maxey, Matt Pietrek, "Undocumented Windows", 1992, pp. 189–398, Addison-Wesley Publishing Company.
- Synthesis: An Efficient Implementation of Fundamental Operating System Services*, (1992) Henry Massalin, Doctorate Thesis of Philosophy, Columbia University.
- Bottom-up Tree Acceptors*, (Nov. 1988, Revised Aug. 1989) C. Hemerick, et al., Dept. of Mathematics and Computing Science, Eindhoven University of Technology.
- Compiler Generation for Interactive Graphics using Intermediate Code*, (Feb. 1996), Scott Draves, Dept. of Computer Science, Carnegie Mellon University.
- A Declarative Approach to Run-Time Code Generation*, (Feb. 1996), Mark Leone, et al., Dept. of Computer Science, Carnegie Mellon University.
- Code Generation Based on Formal BURS Theory and Heuristic Search*, (Nov. 1995), A. Nymeyer, et al., Dept. of Computer Science, University of Twente.
- Optimizing ML with Run-Time Code Generation* (May 1996), Mark Leone, et al., Dept. of Computer Science, Carnegie Mellon University.
- Deferred Compilation: The Automation of Run-Time Code Generation* (Dec. 1993) Mark Leone, et al., Dept. of Computer Science, Carnegie Mellon University.
- Lightweight Run-Time Code Generation*, (Jun. 1994), Mark Leone, et al., Dept. of Computer Science, Carnegie Mellon University.
- Fast Data Breakpoints* (May 3, 1990, Revised Apr. 14, 1993), David Keppel, Dept. of Computer Science and Engineering, University of Washington.
- Evaluating Runtime-Compiled Value-Specific Optimizations*, (Nov. 2, 1993), David Keppel, et al., Dept. of Computer Science and Engineering, University of Washington.

- A Portable Interface for On-The-Fly Instruction Space Modification*, (Apr. 1991), David Keppel, Dept. of Computer Science and Engineering, University of Washington.
- A Case for Runtime Code Generation* (Nov. 4, 1991), David Keppel, et al., Dept. of Computer Science and Engineering, University of Washington.
- Data Specialization* (Feb. 5, 1996), Todd B. Knoblock et al., Advanced Technology Division, Microsoft Corp.
- Fast, Effective Dynamic Compilation* (In PLDI '96), Joel Auslander, et al., Dept. of Computer Science and Engineering, University of Washington, May 1996.
- Specializing Shaders*, (May 12, 1995), Brian Guenter et al., Advanced Technology Division, Microsoft Corp.
- Detection and Optimization of Suspension-Free Logic Programs*, (1994), Saumya Debray et al., Dept. of Computer Science, University of Arizona, Tucson.
- Transit Note #103 Computational Quasistatics* (Feb. 1994, Last update Oct. 25, 1994), Andre DeHon, Ian Eslick.
- Rewriting Executable Files to Measure Program Behavior*, (Mar. 1992), James R. Larus et al.
- The Mahler Experience: Using an Intermediate Language as the Machine Description*, (1987), David W. Wall et al., Western Research Laboratory, Digital Equipment Corporation.
- EEL: Machine-Independent Executable Editing* (Jun. 1995), James R. Larus et al., Dept. of Computer Sciences, University of Wisconsin—Madison.
- Instruction Scheduling and Executable Editing*, (Feb. 2, 1996), Eric Schnarr et al., Dept. of Computer Sciences, University of Wisconsin—Madison.
- Global Register Allocation at Link Time* (1986), David W. Wall, Western Research Laboratory, Digital Equipment Corporation.
- Long Address Traces From RISC Machines: Generation and Analysis* (Sep. 1989), Anita Borg et al., Western Research Laboratory, Digital Equipment Corporation.
- OPT: A Quick Program Profiling and Tracing System*, (May 14, 1996), James R. Laurus, Dept. of Computer Sciences, University of Wisconsin—Madison.
- Experience With a Software-Defined Machine Architecture*, (Aug. 1991), David W. Wall, Western Research Laboratory, Digital Equipment Corporation.
- Systems for Late Code Modification*, (May 1992), David W. Wall, Western Research Laboratory, Digital Equipment Corporation.
- Link-Time Optimization of Address Calculation on a 64-bit Architecture*, (Feb. 1994), Amitabh Srivastava et al., Western Research Laboratory, Digital Equipment Corporation.
- ATOM: A System for Building Customized Program Analysis Tools*, (Mar. 1994), Amitabh Srivastava et al., Western Research Laboratory, Digital Equipment Corporation.
- Shade: A Fast Instruction-Set Simulator for Execution Profiling* (1994), Bob Cmelik, Sun Microsystems, Inc. and David Keppel, Dept. of Computer Science and Engineering, University of Washington.
- EEL: An Executable Editing Library* (Jun. 1996), James R. Larus, Dept. of Computer Science and Engineering, University of Washington.
- GNU Superoptimizer*, (1995) Torbjorn Granlund, HP-UX Porting and Archive Center.
- Superoptimizer—A Look at the Smallest Program*, (1987), Henry Massalin, Dept. of Computer Science, Columbia University.
- Elements of Machine Learning*, Chapter 5—The Construction of Decision Lists, Pat Langley, Stanford University.
- QuaC: Binary Optimization for Fast Runtime Code Generation in C*, Curtis Yarvin, Adam Sah.
- A VCODE Tutorial*, (Apr. 28, 1996), Dawson R. Engler, Laboratory for Computer Science, Massachusetts Institute of Technology.
- VCODE: A Retargetable, Extensible, Very Fast Dynamic Code Generation System* (1995), Dawson R. Engler, Laboratory for Computer Science, Massachusetts Institute of Technology.
- Ray, T.S., "Is It Alive Or Is it GA?", School of Life & Health Sciences, University of Delaware, Jul., 1991, XP 002047764, pp. 527–534.
- Chris Gatercole & Peter Ross, "Dynamic Training Subset Selection for Supervised Learning in Genetic Programming", Feb. 25, 1994, pp. 1–10, Department of Artificial Intelligence University of Edinburgh, Edinburgh EH1 1HN U.K.

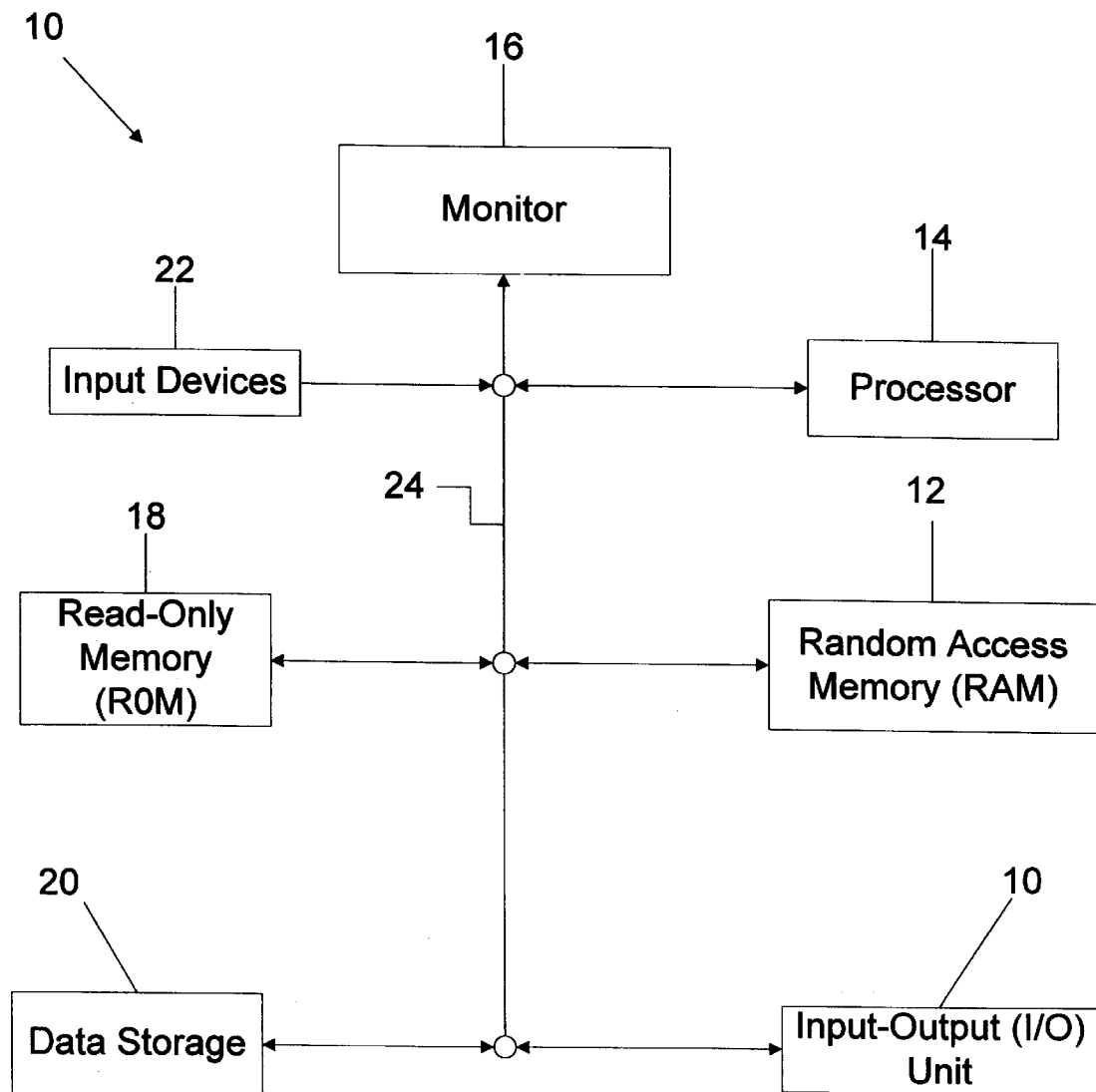


Fig. 1

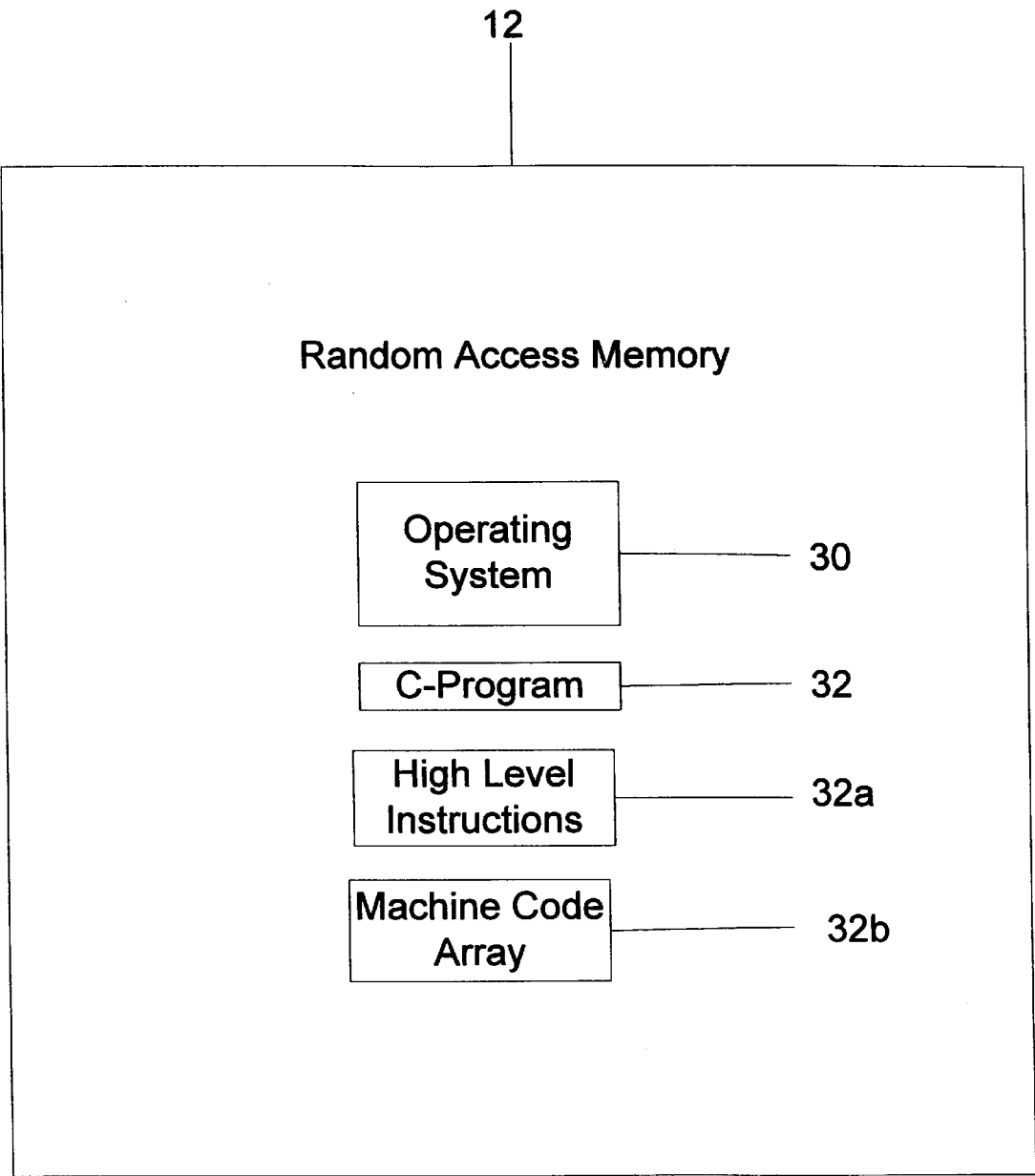


Fig. 2

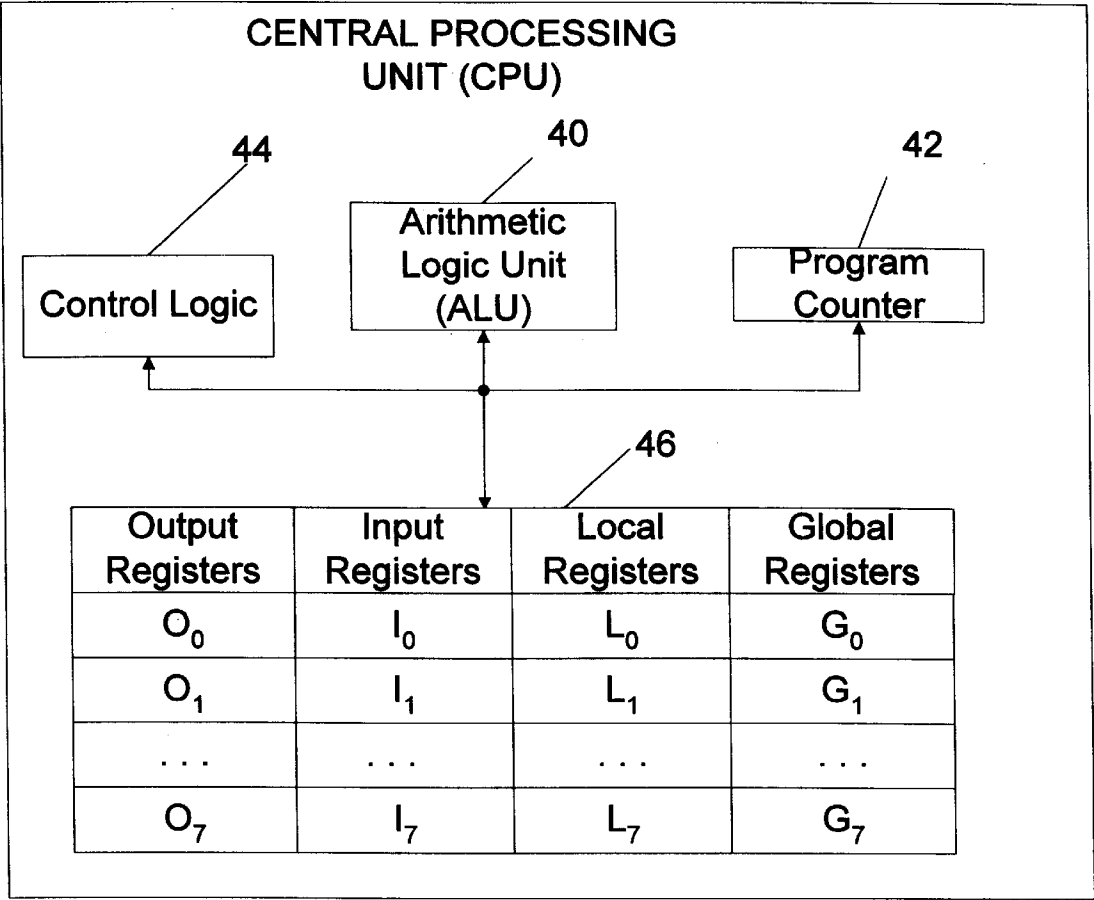


Fig. 3

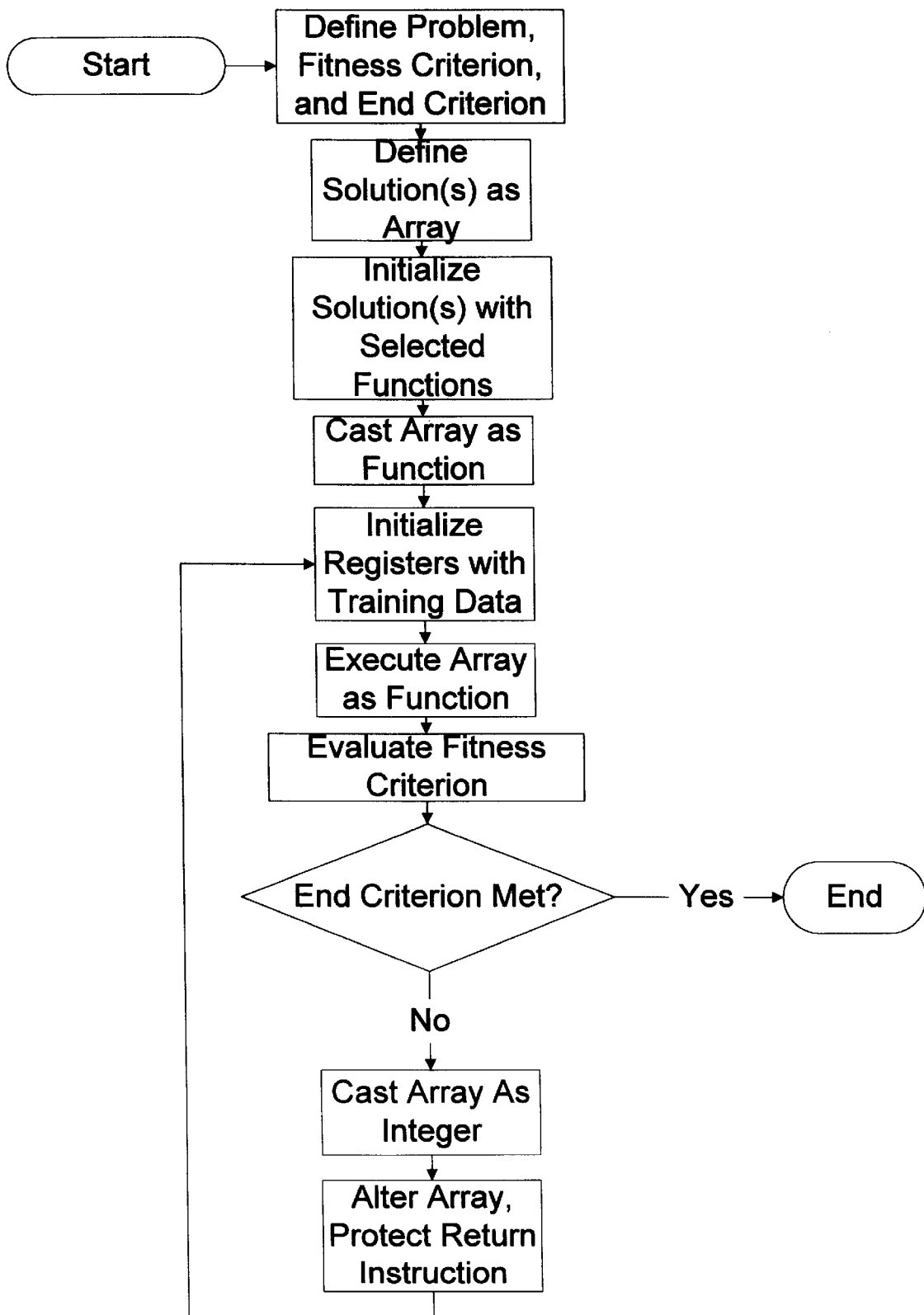


Fig. 4

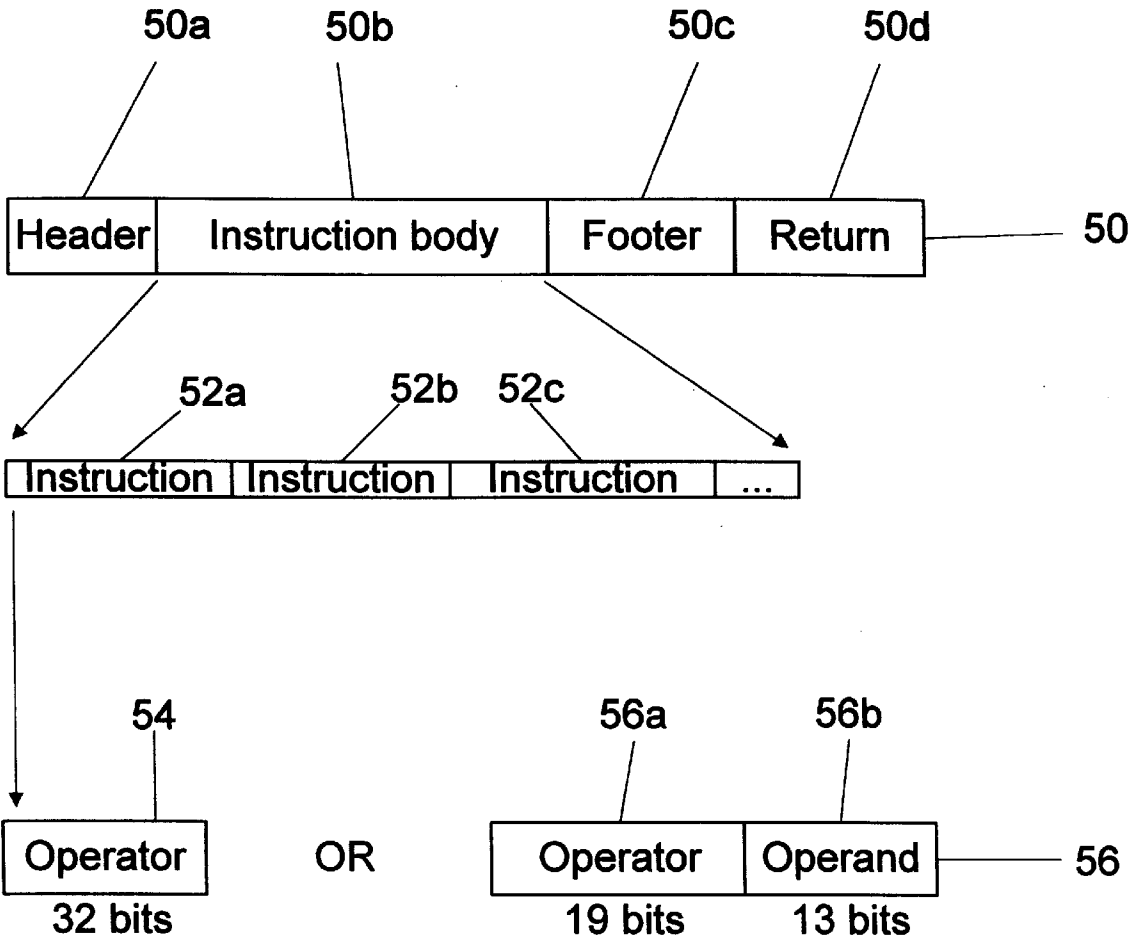


Fig. 5

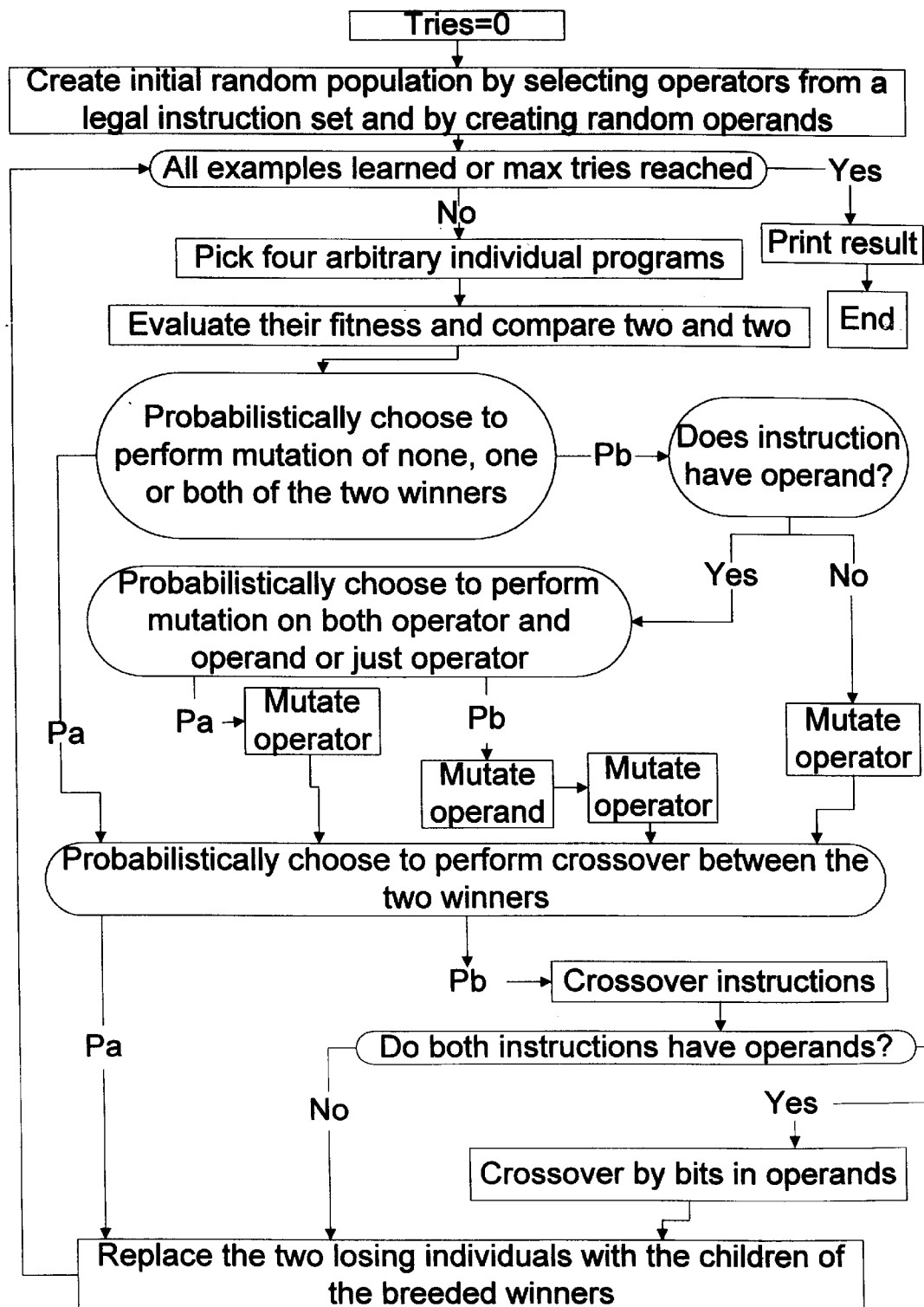


Fig. 6

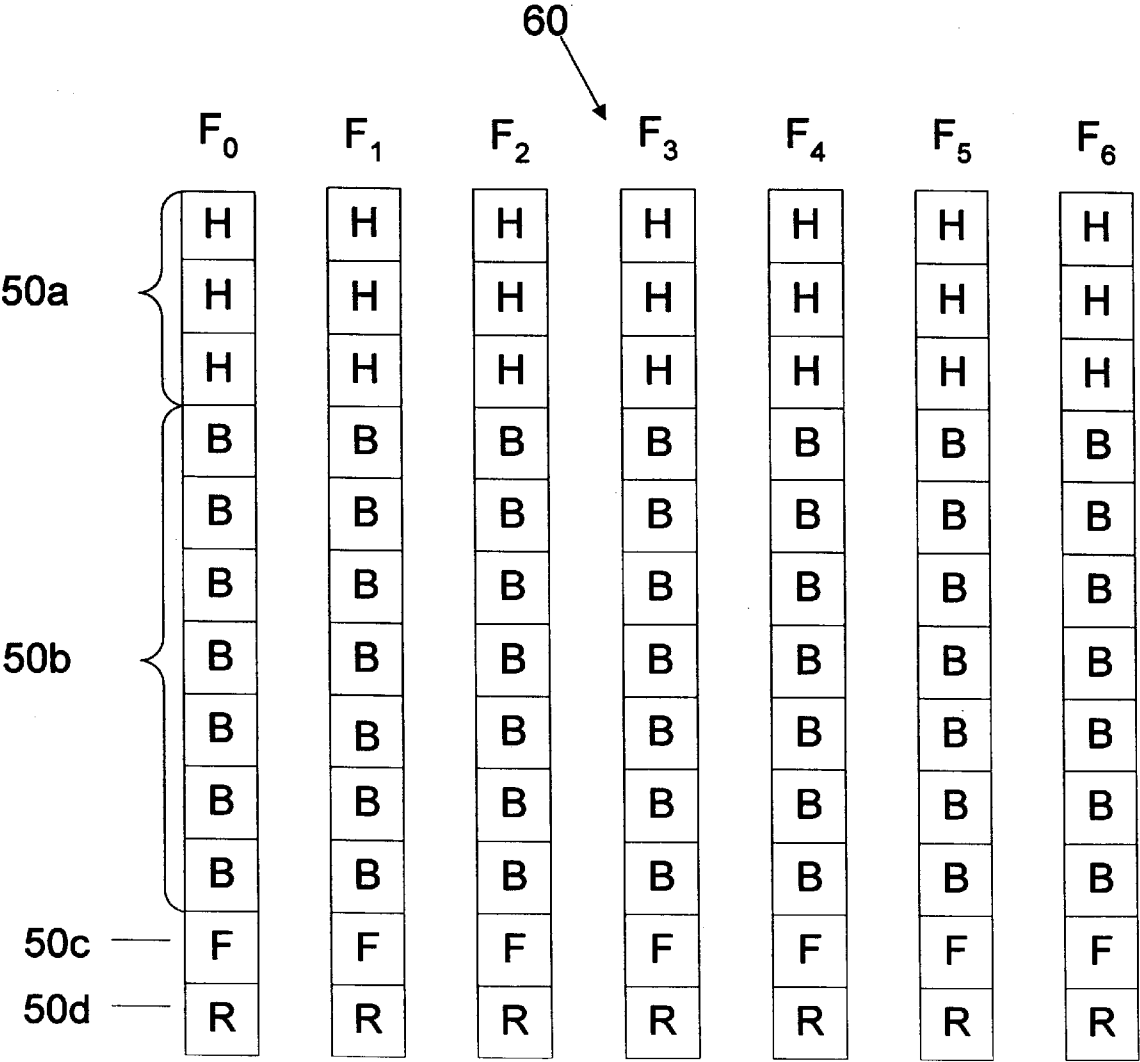


Fig. 7

62 — H H H H B F R

Fig. 8

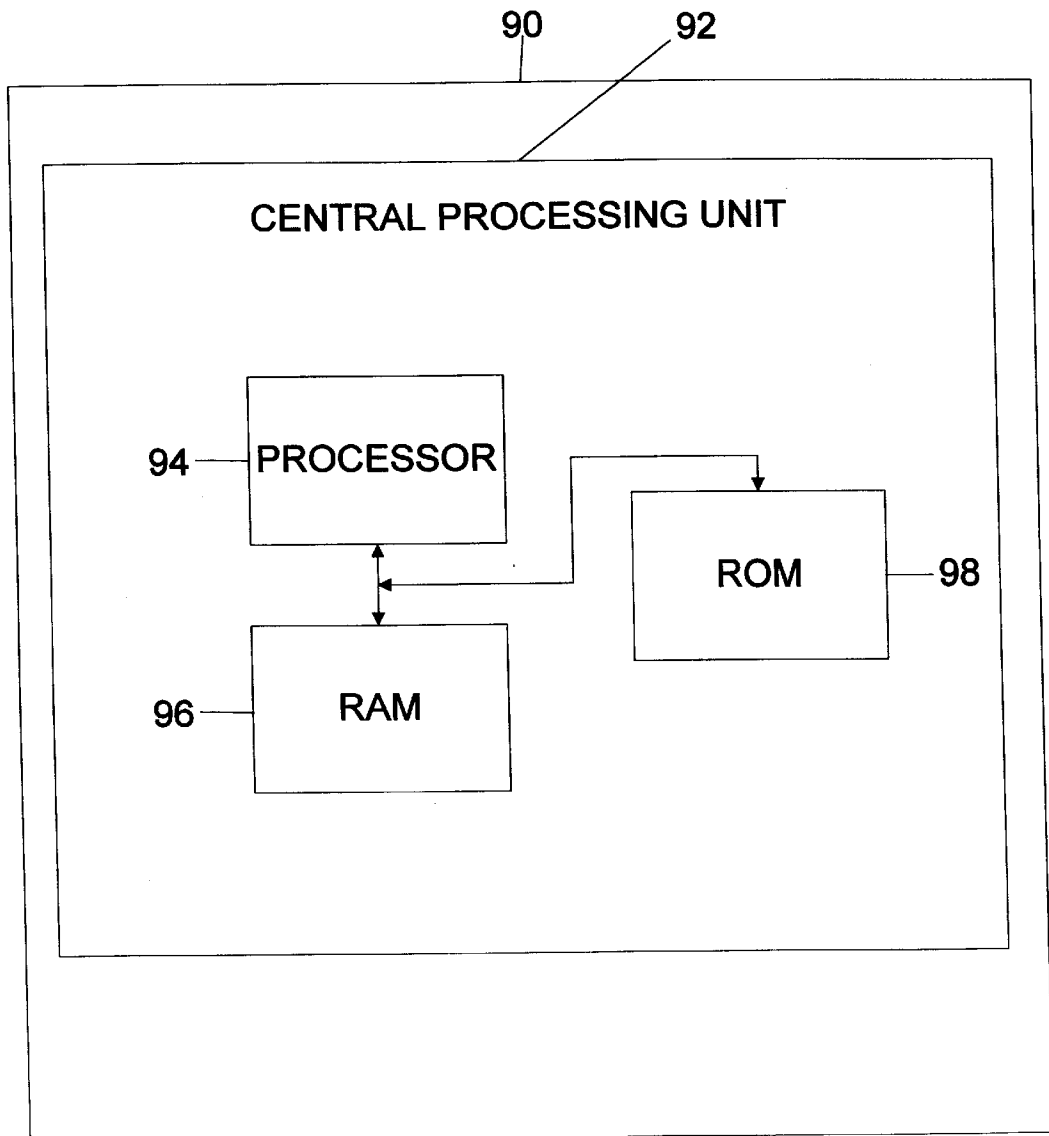


Figure 9

Parents

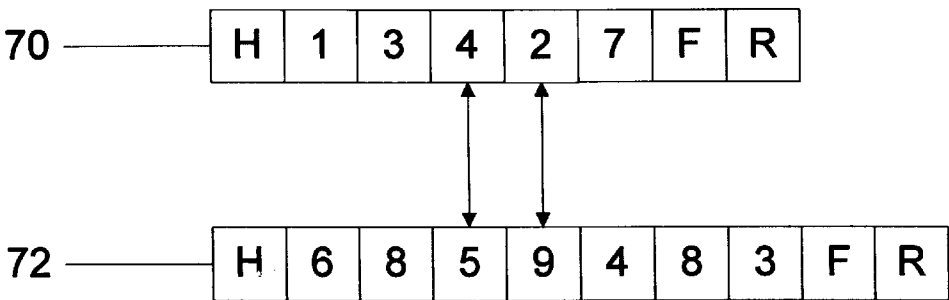


Fig. 10a

Children

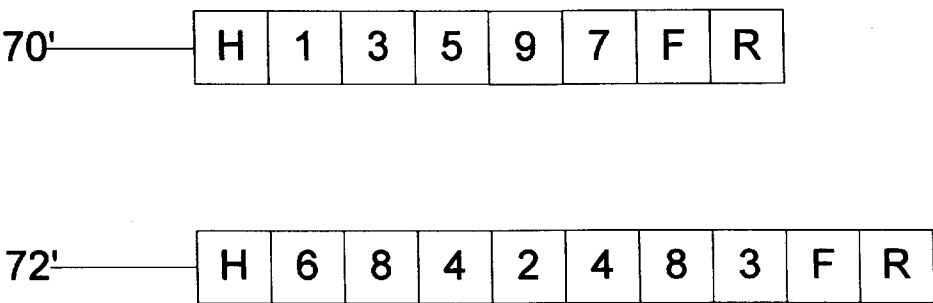


Fig. 10b

Parents

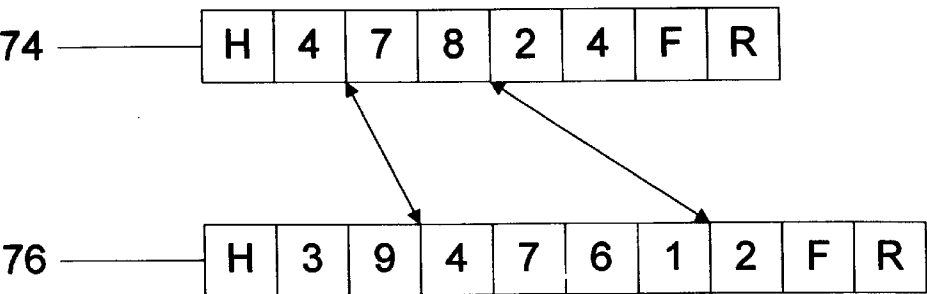


Fig. 11a

Children

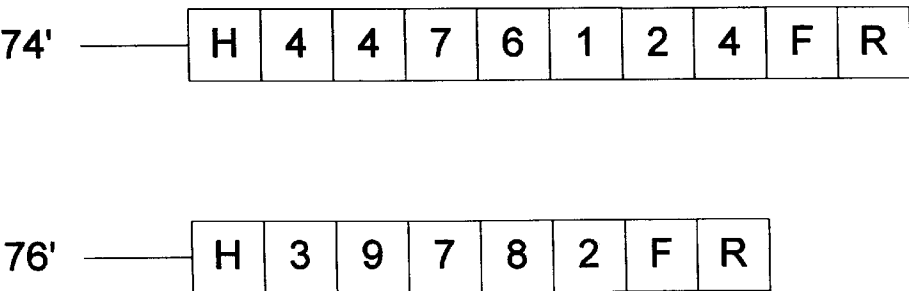


Fig. 11b

PARENTS

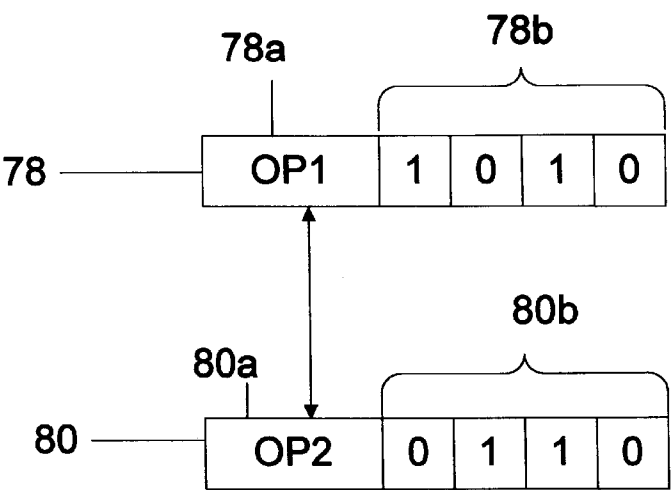


Fig. 12a

CHILDREN

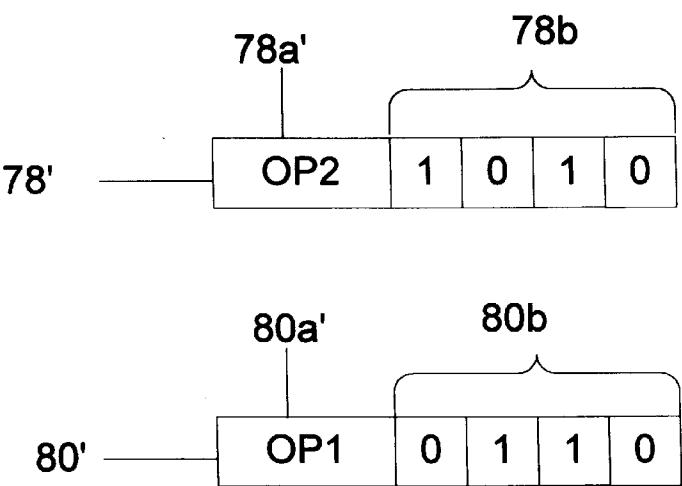


Fig. 12b

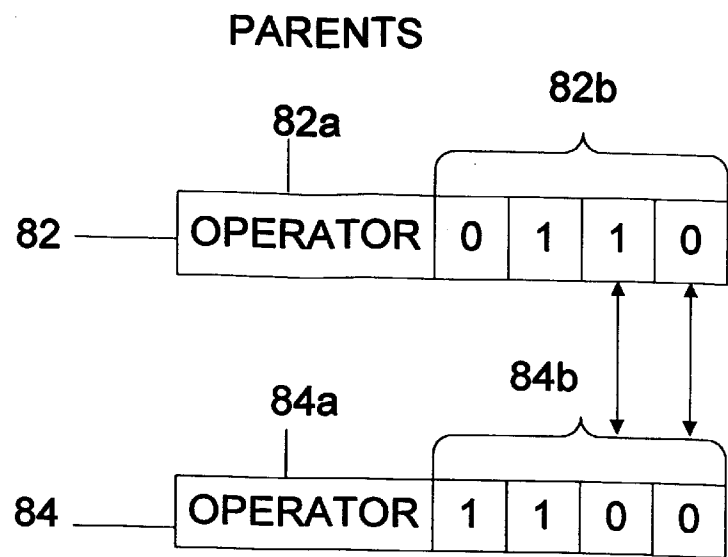


Fig. 13a

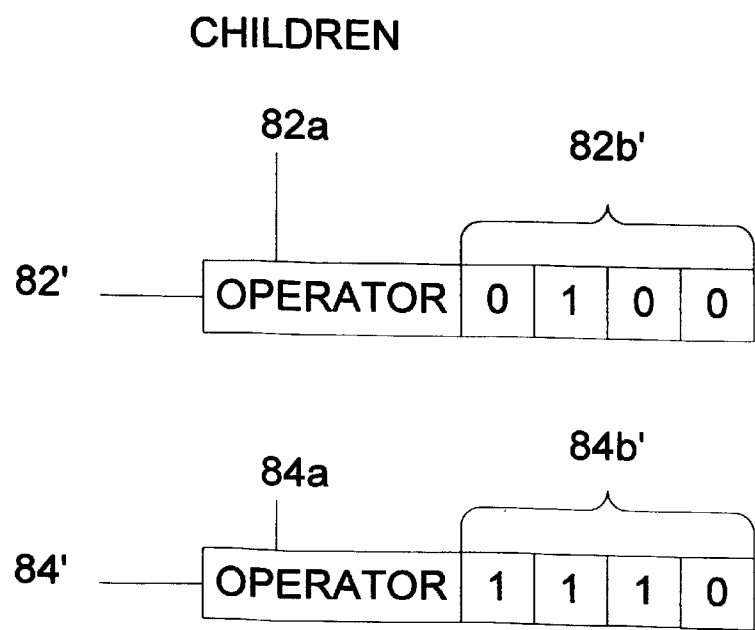


Fig. 13b

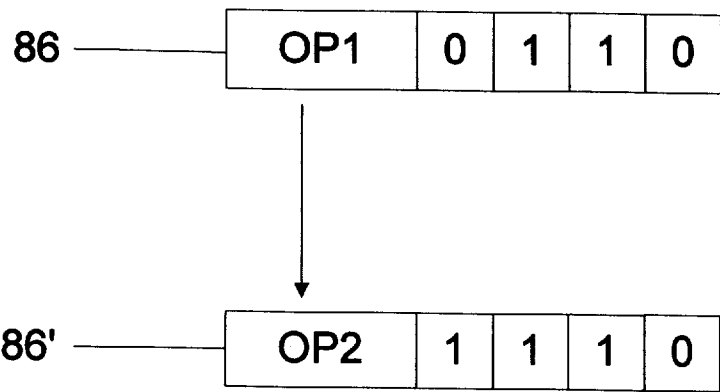


Fig. 14

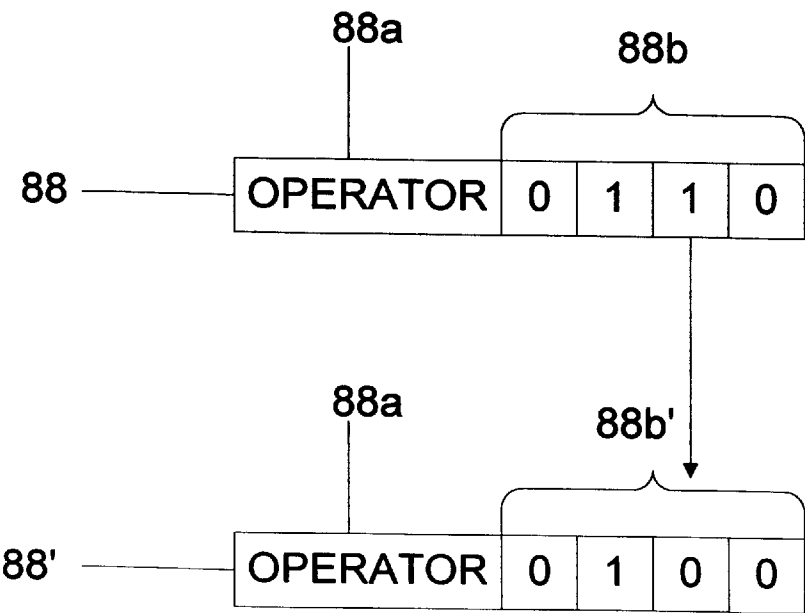
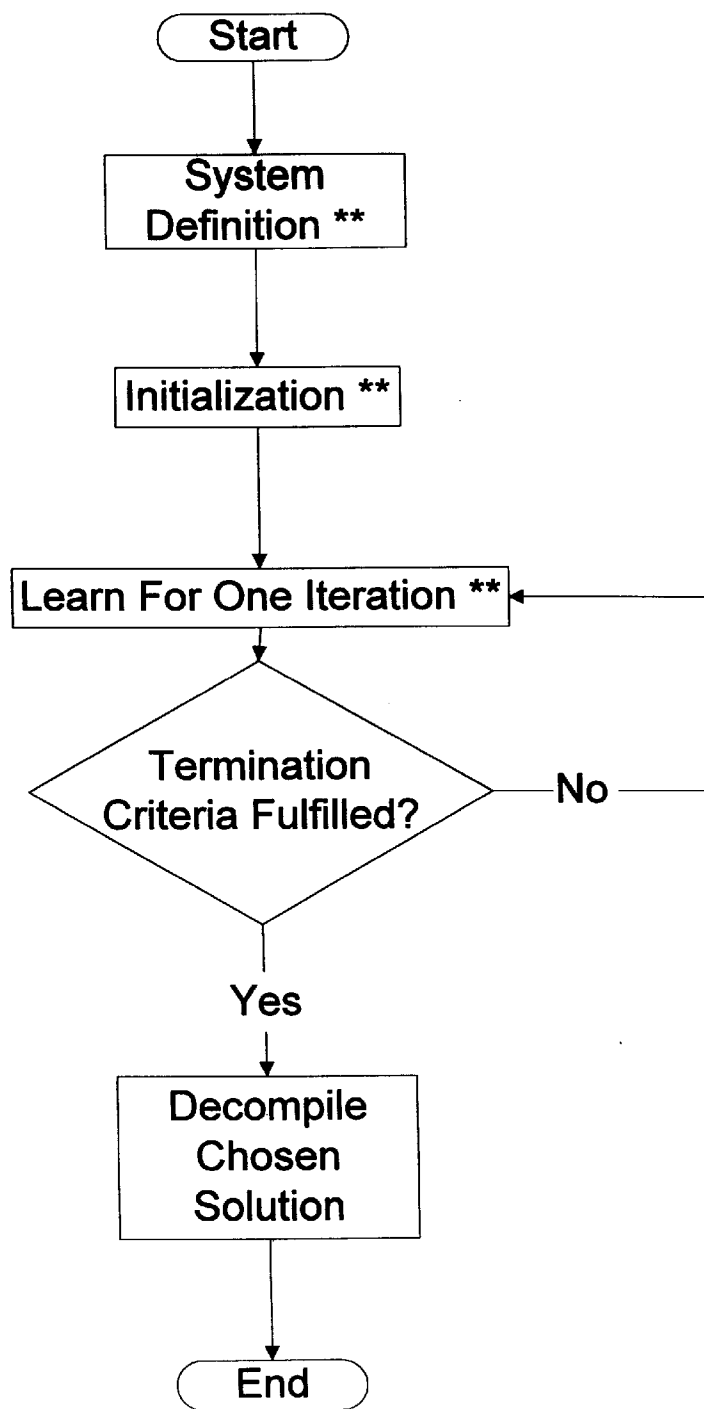
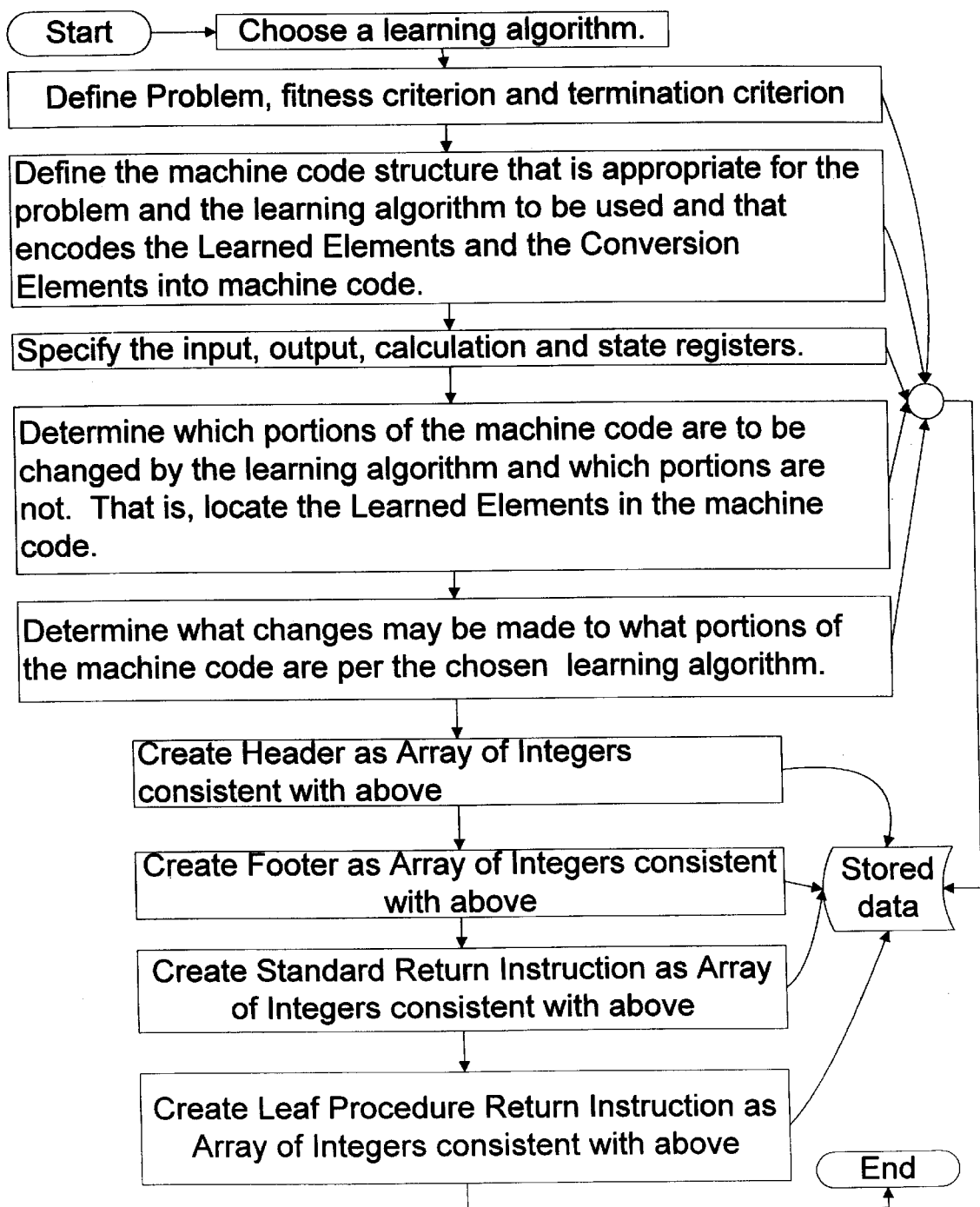


Fig. 15

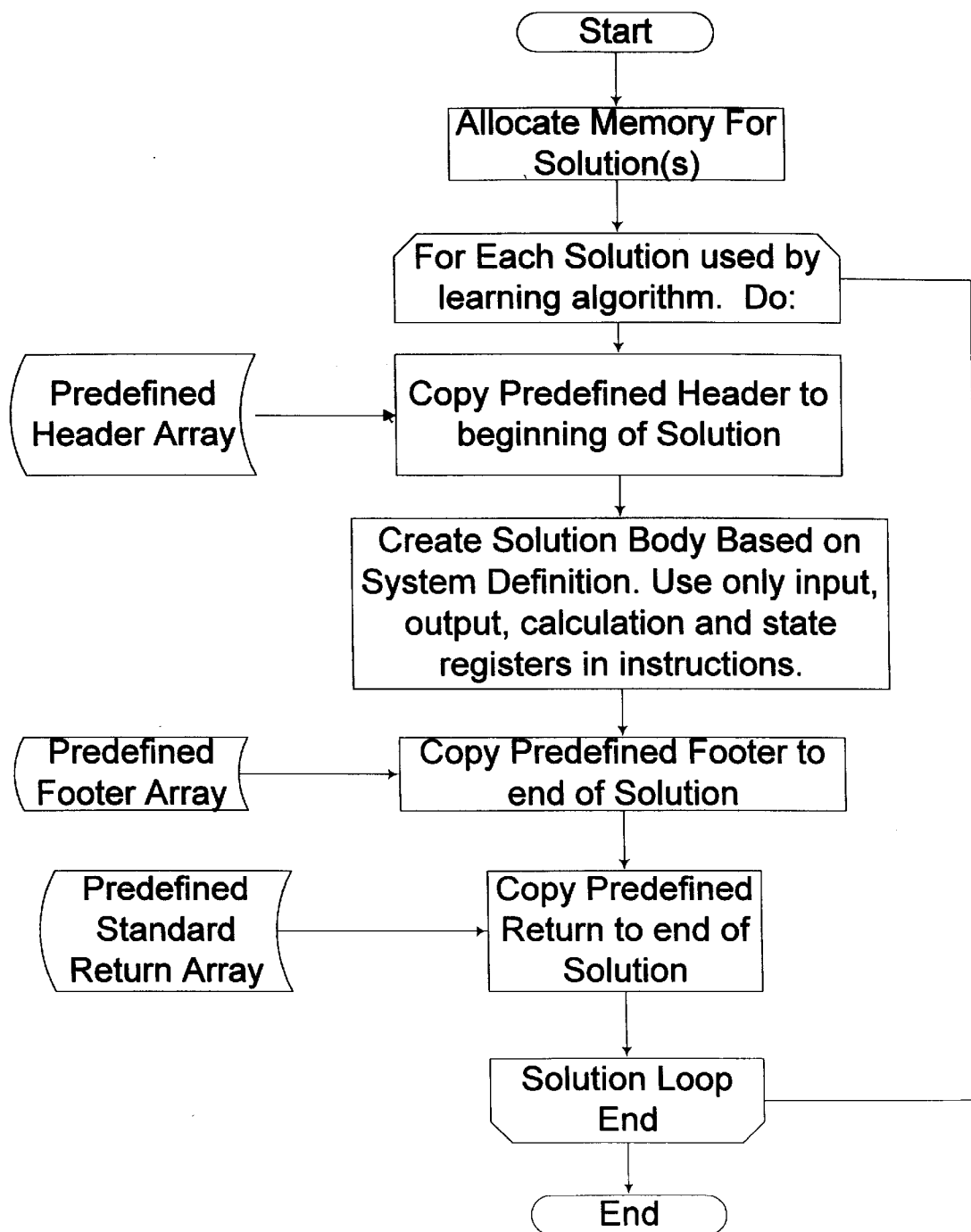


General Operation of the System

Fig. 16a

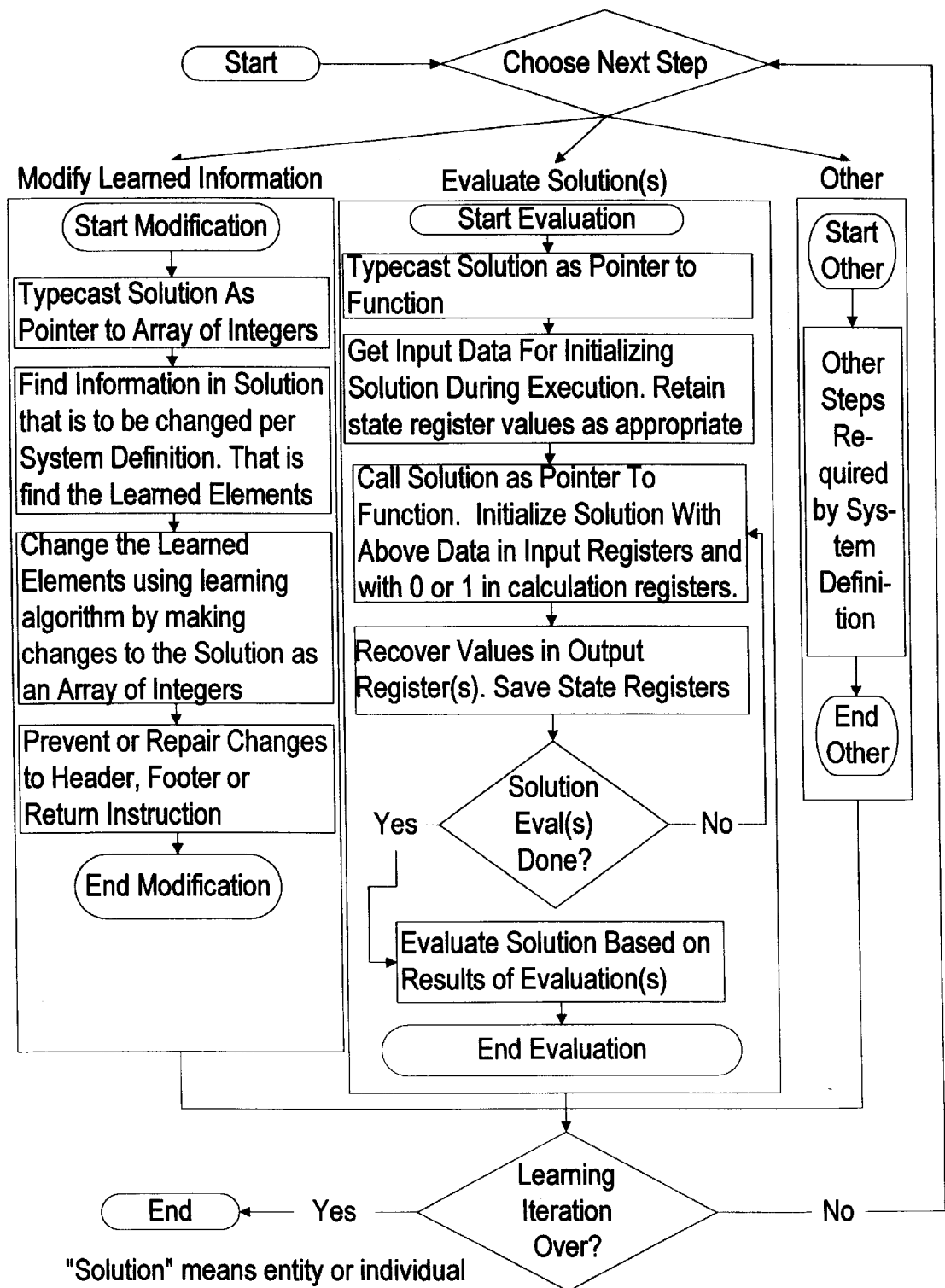


Details of System Definition
Fig. 16b



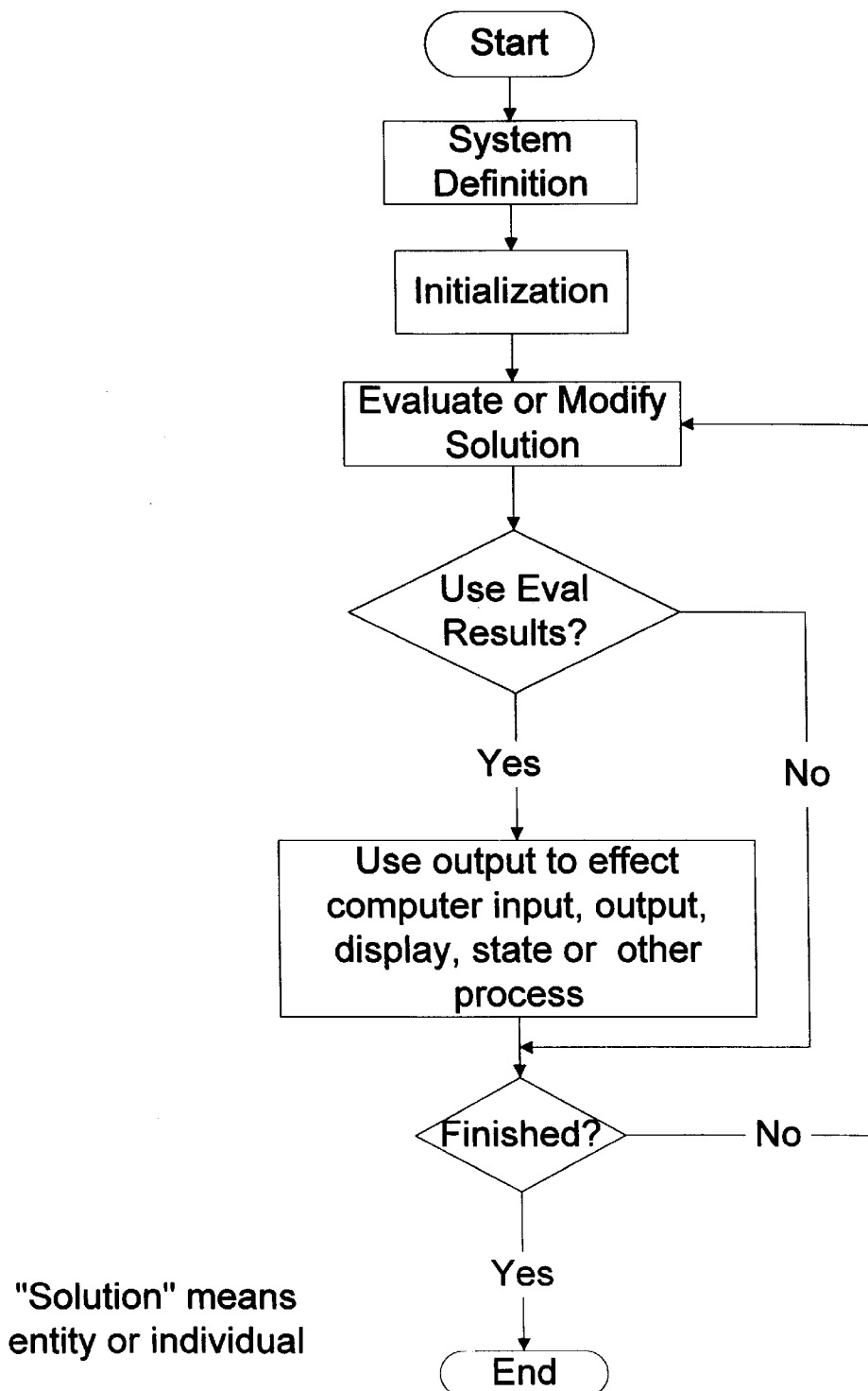
Initialization
Fig. 16c

"Solution" means entity or individual



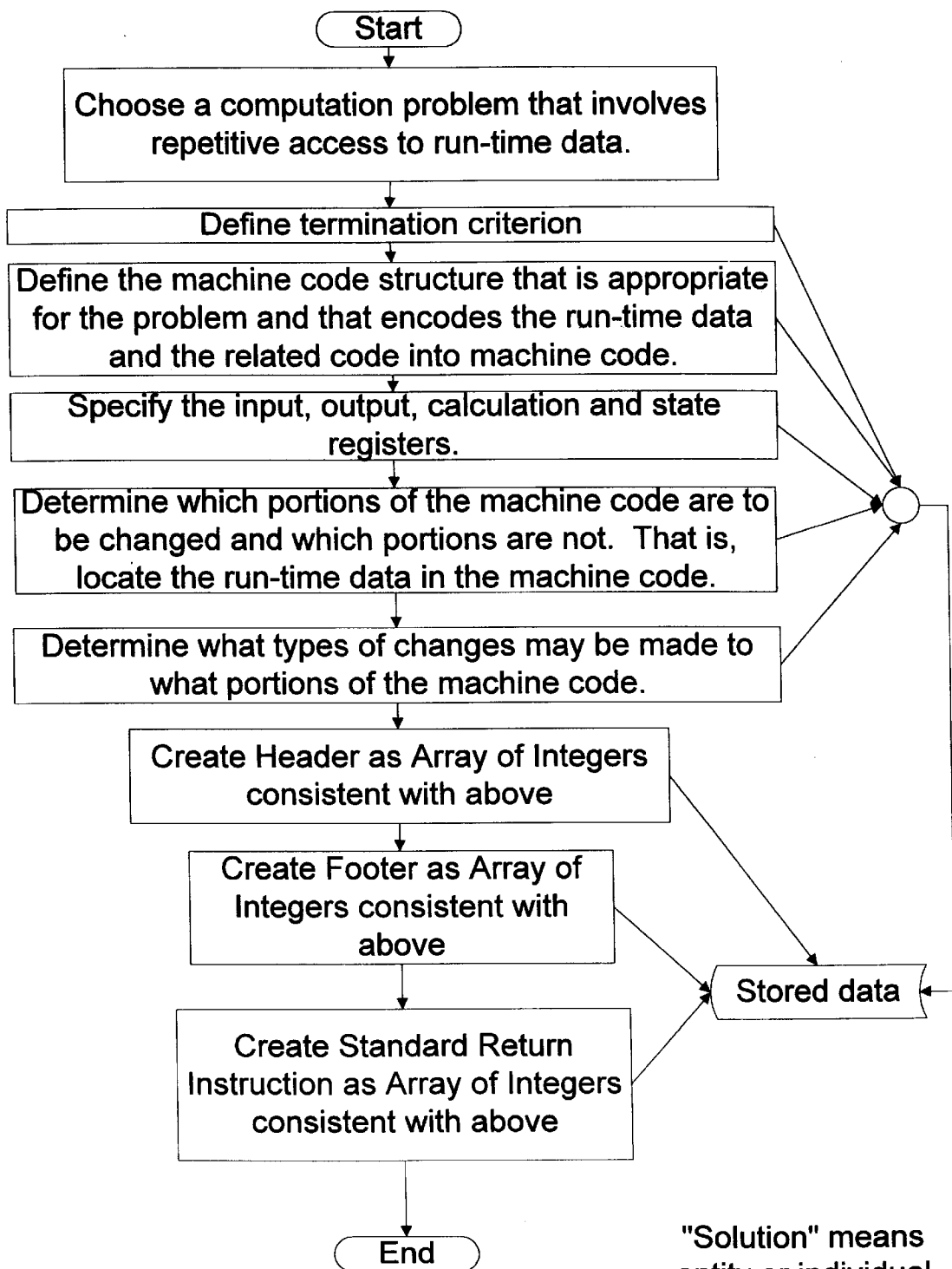
"Solution" means entity or individual

Learn for One Iteration
Fig. 16d

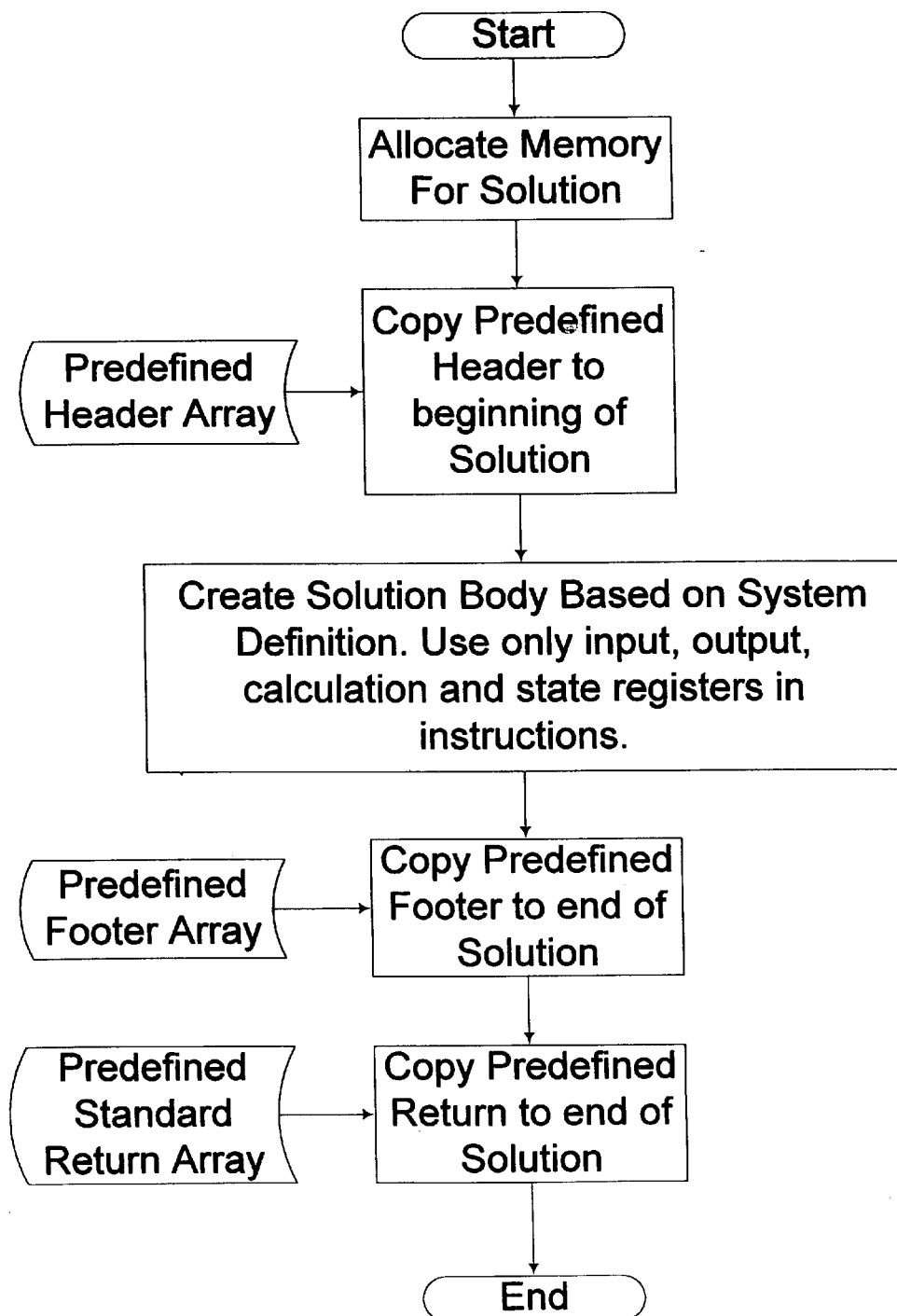


General Operation of the Invention As Repetitive Computation System

Fig. 17a

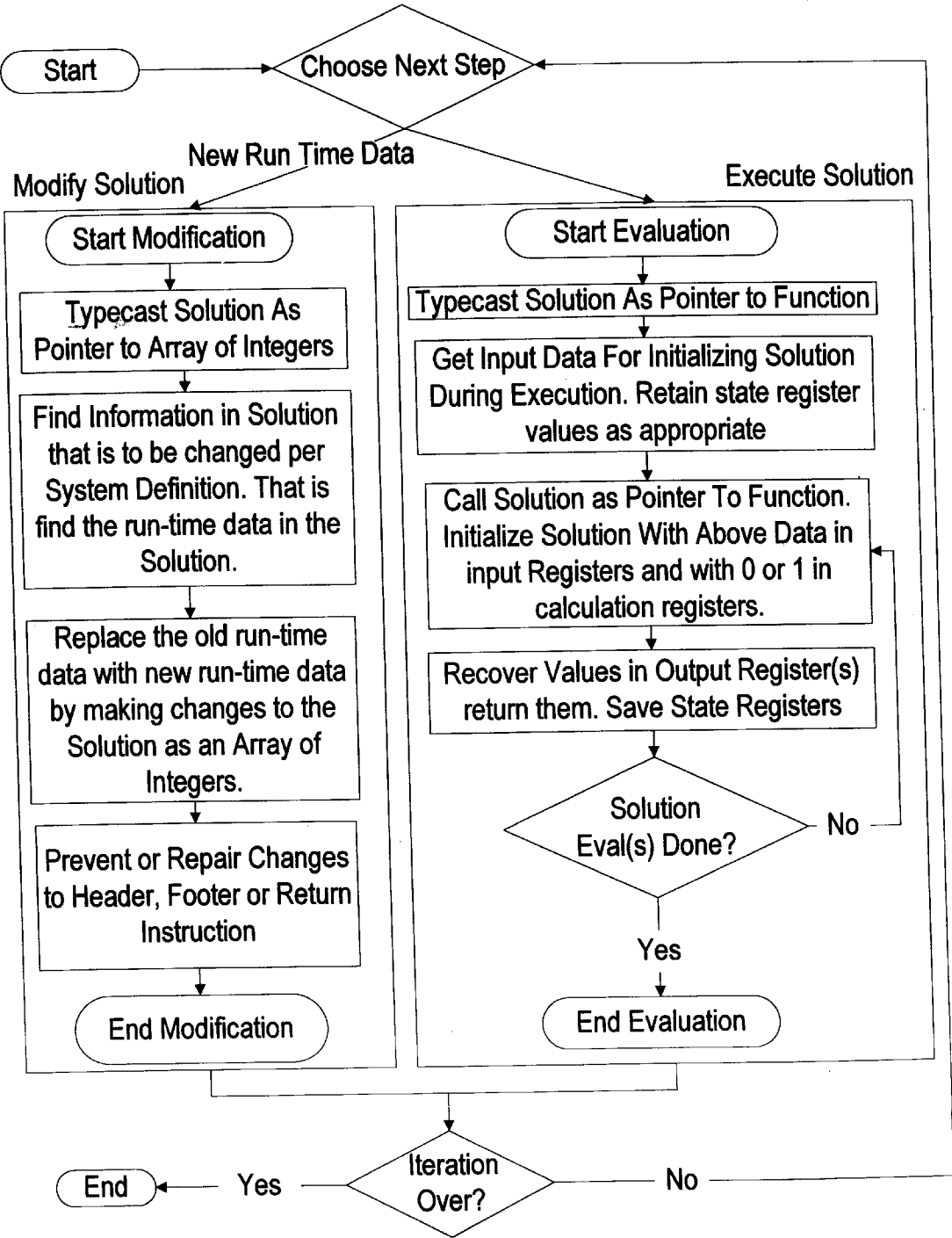


System Definition
Fig. 17b



Initialization
Fig. 17c

"Solution" means entity or individual



"Solution" means
entity or individual

Evaluate or Modify Function
Fig. 17d

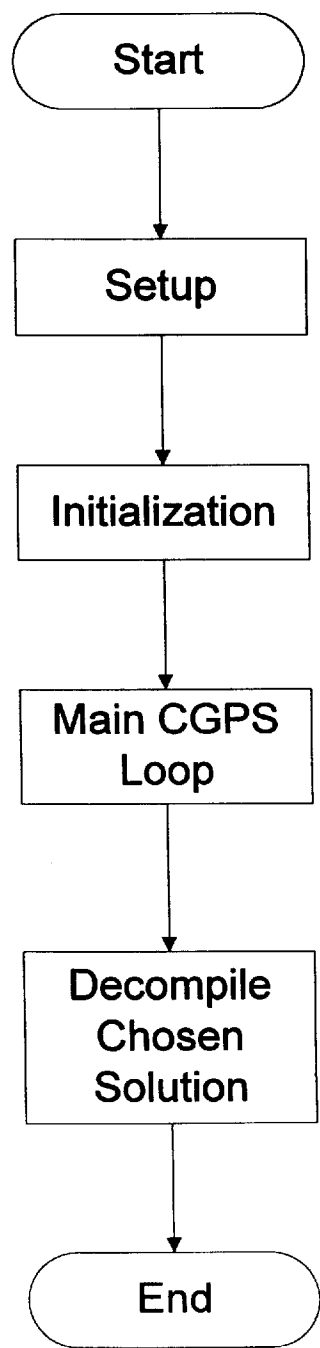
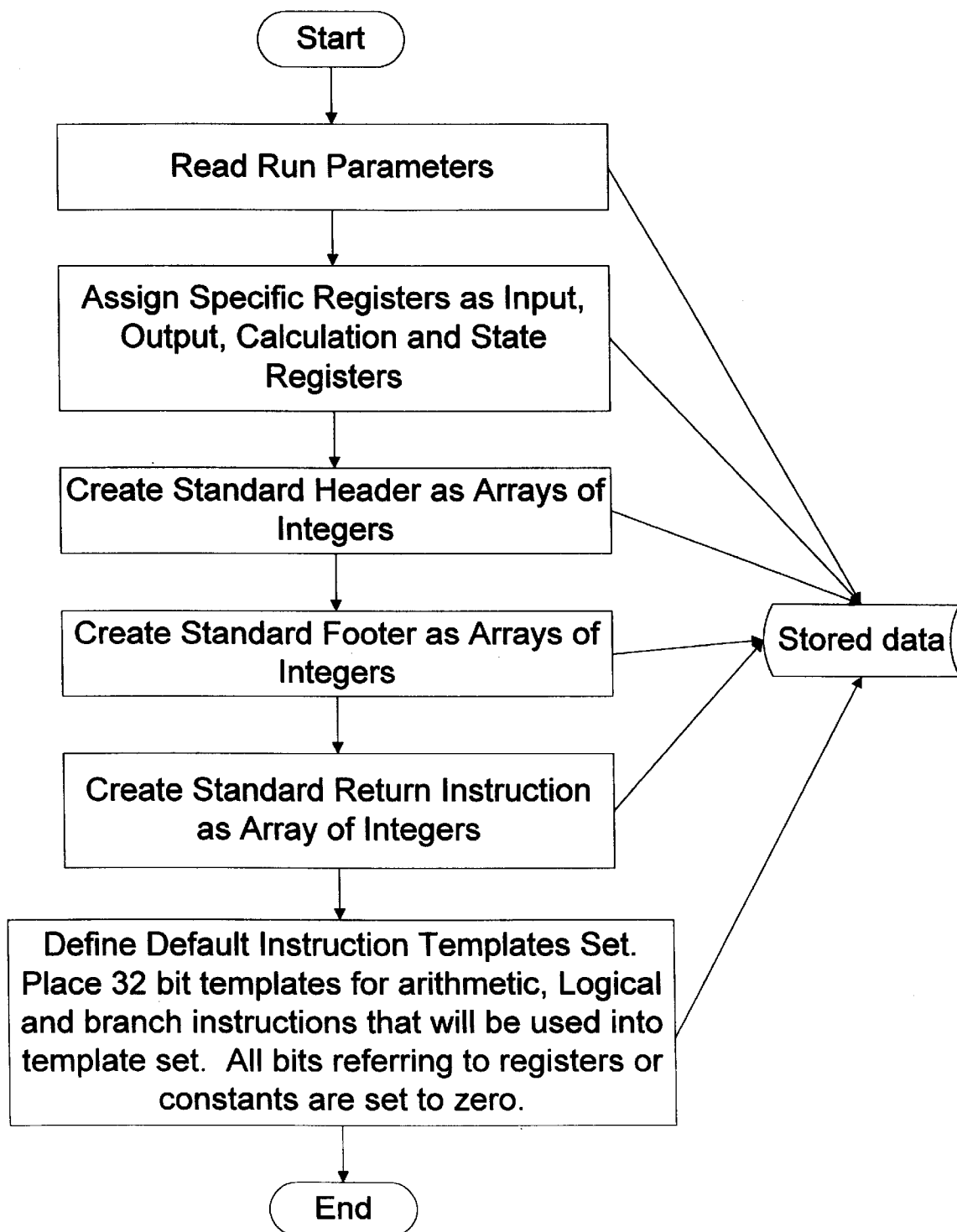
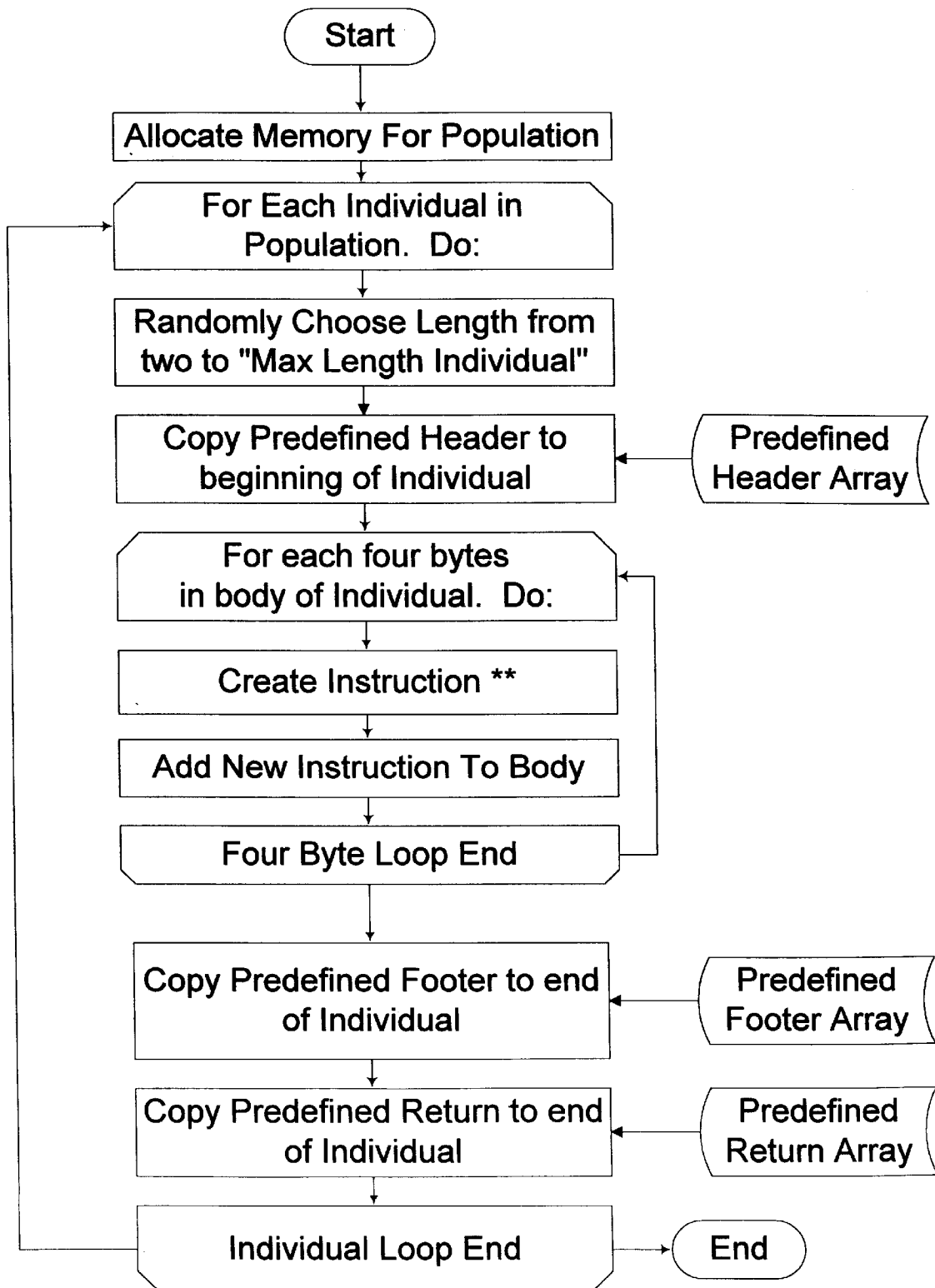


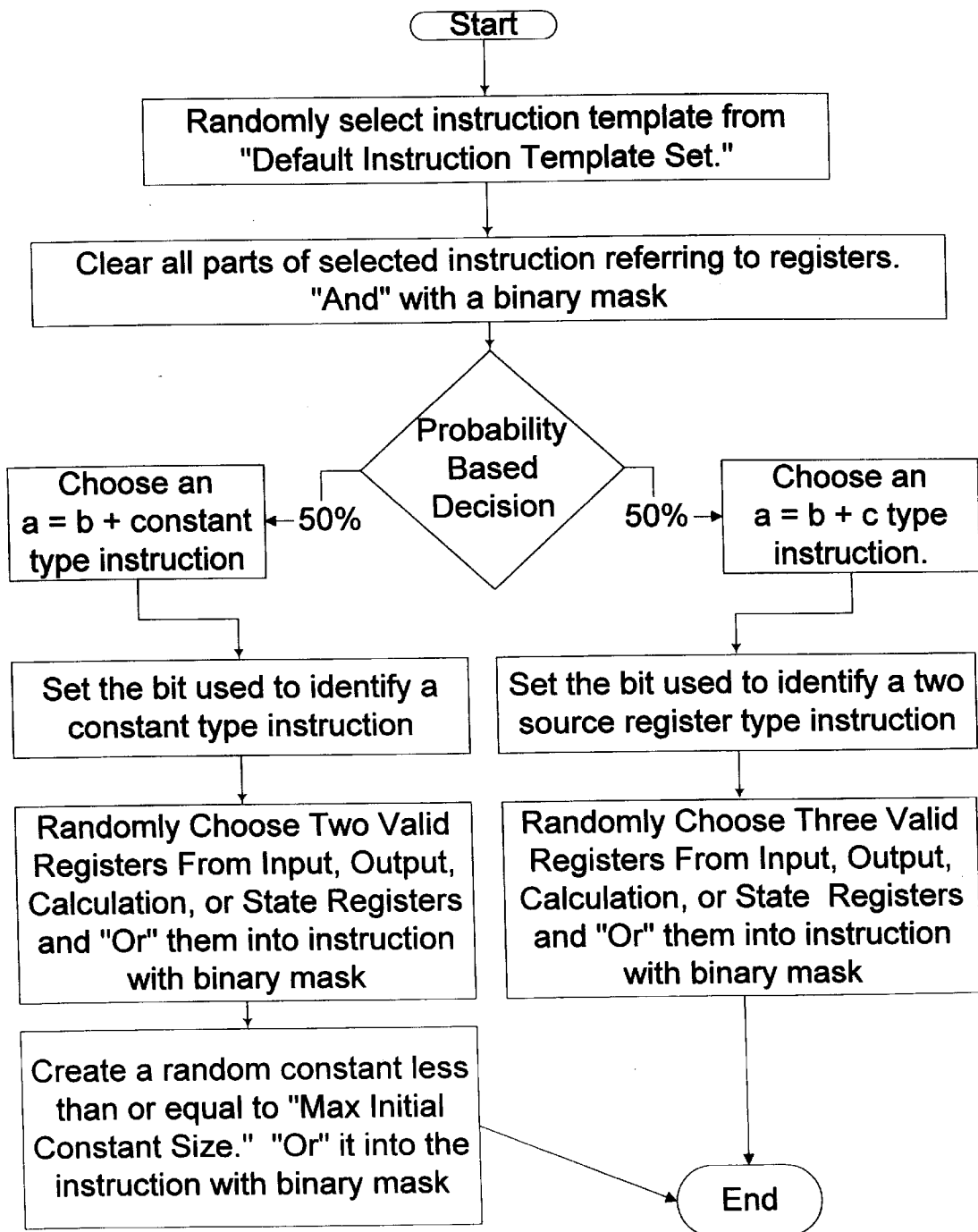
Fig. 18a



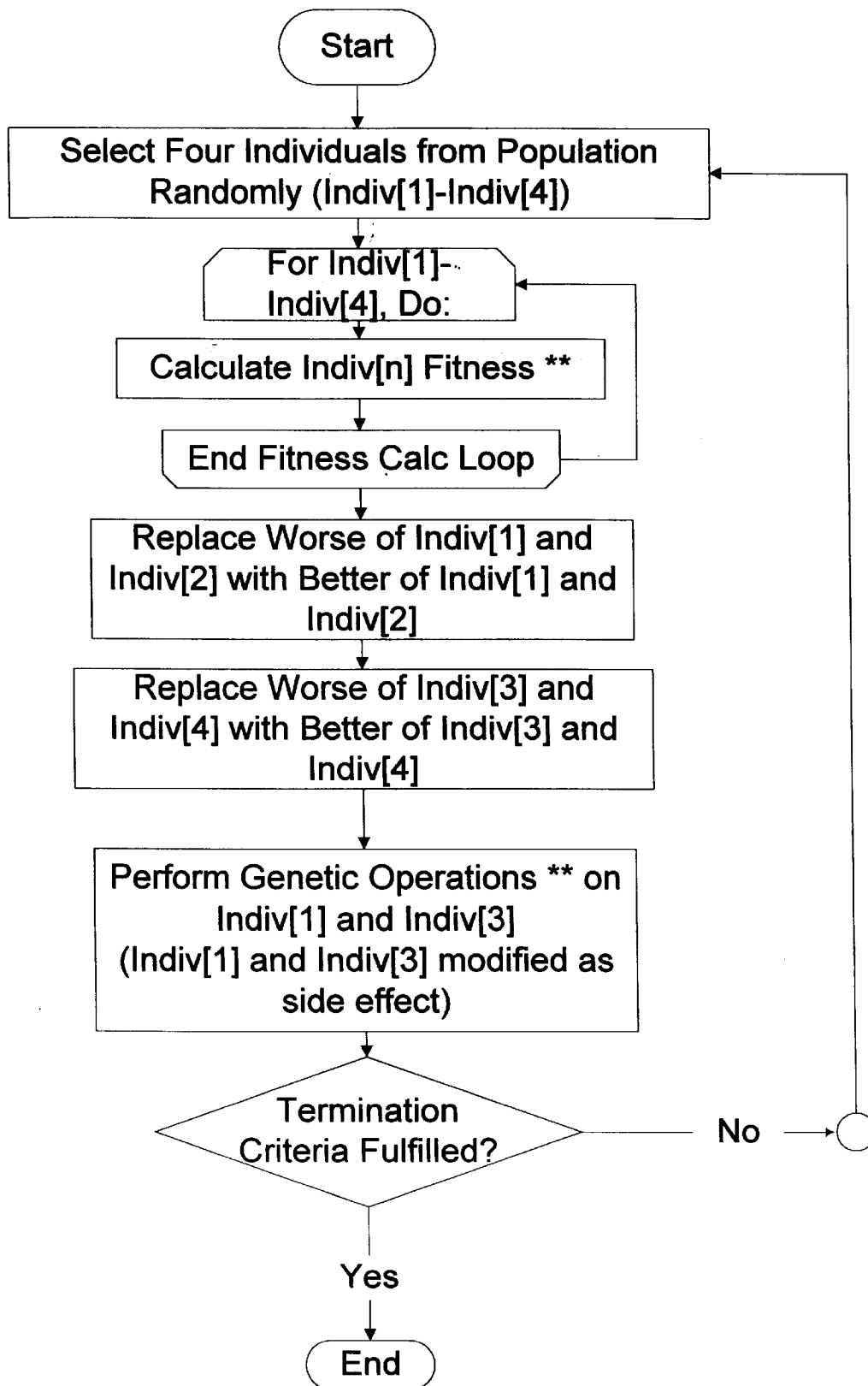
Setup
Fig. 18b



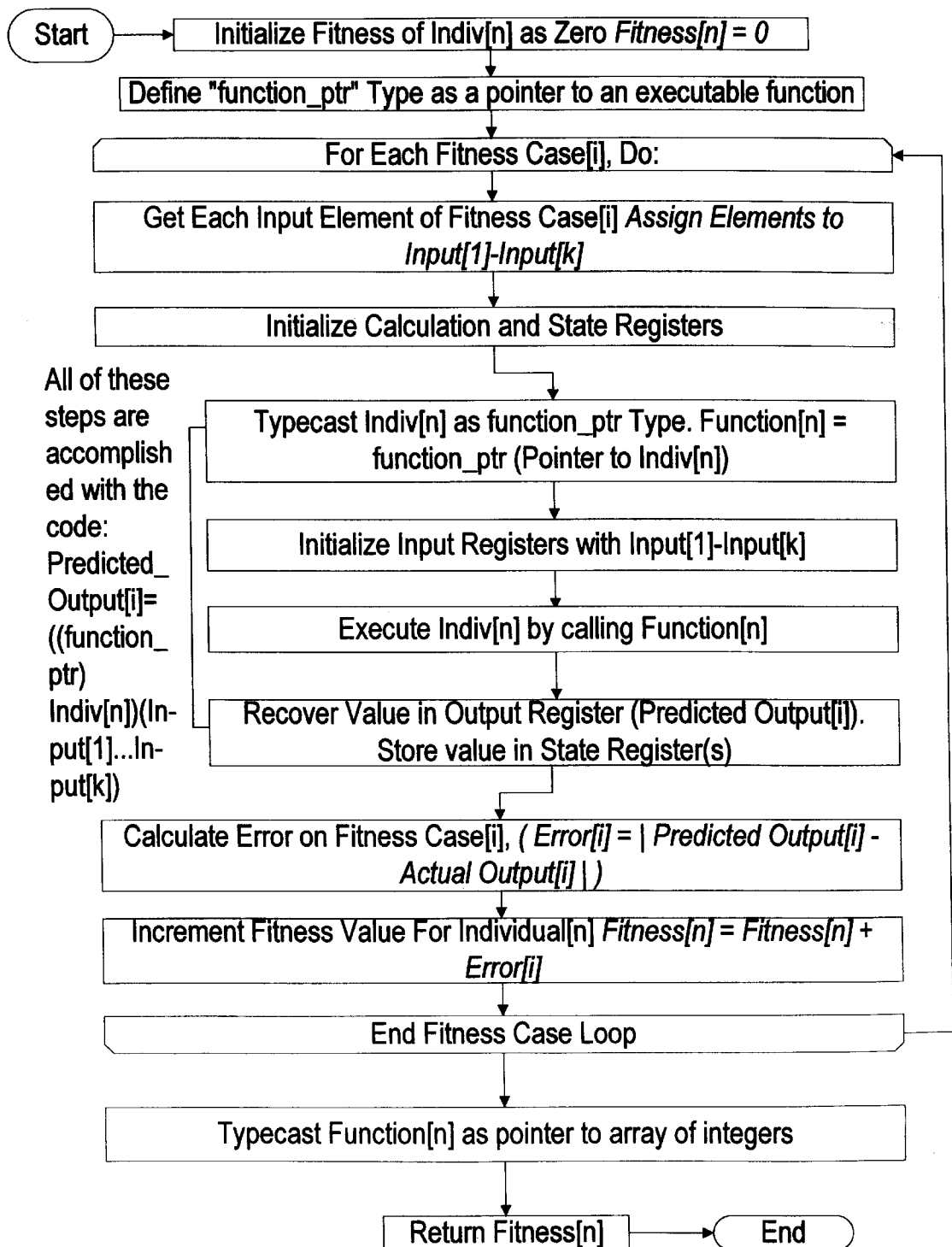
Initialization
Fig. 18c



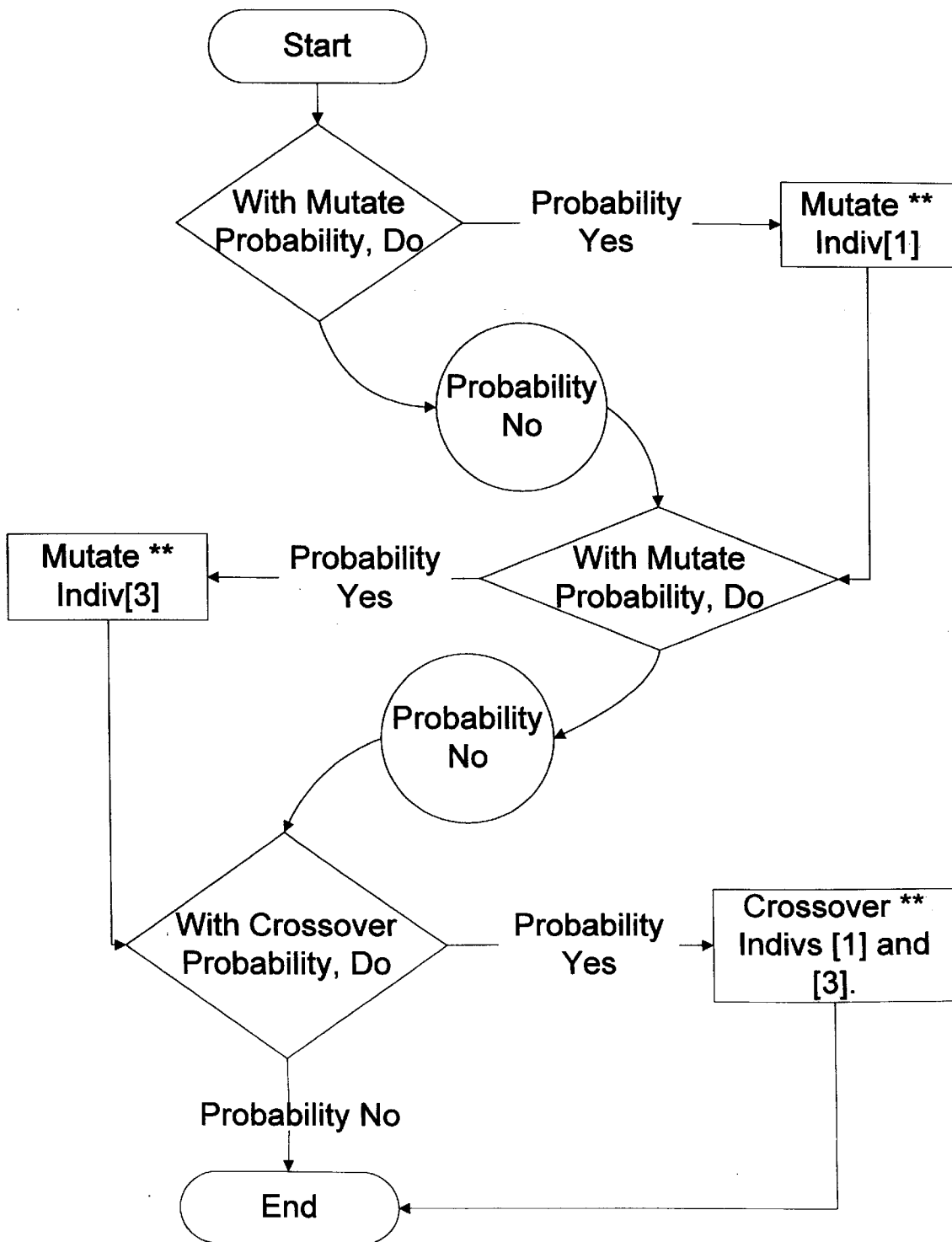
Create Instruction
Fig. 18d



Main CGPS Loop
Fig. 18e



Calculate Indiv[n] Fitness
Fig. 18f



Perform Genetic Operations
Fig. 18g

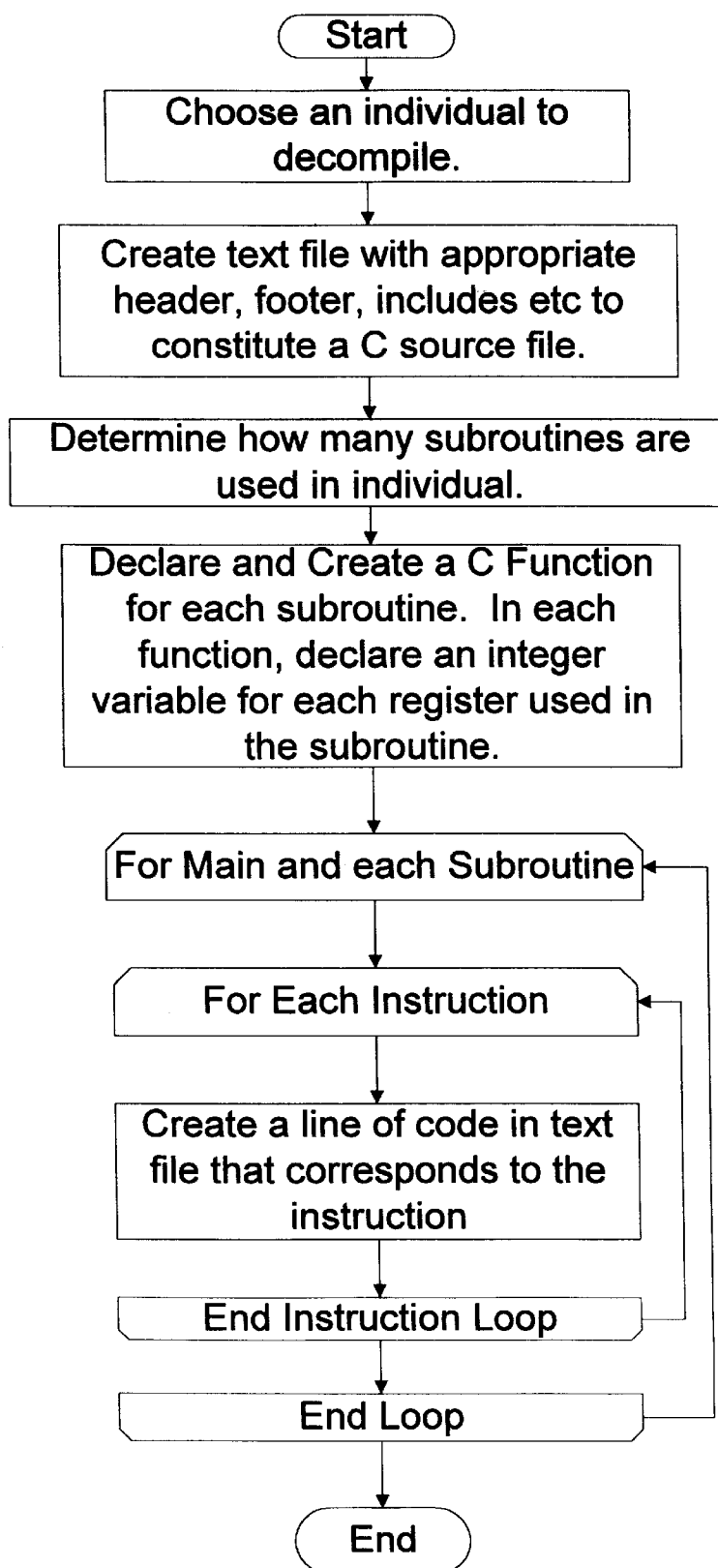


Fig. 18h

COMPUTER IMPLEMENTED MACHINE LEARNING METHOD AND SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to the art of computerized computation systems for performing repeated computations on data that is not known until a computer user is running the system ("run-time", and "run-time data") and more specifically to a system of creating, initializing, storing, altering and executing both the run-time data and the computer code necessary to execute the repeated computations (the "related code") in native machine code operating on a register machine. The present invention relates also to the art of computerized learning systems (which are usually characterized by the need to perform repeated computations on run-time data) and more specifically to a register machine learning method in which the information and/or the computer program(s) that constitute solutions to a problem are created, initialized, stored, altered and executed in native machine code by using a higher level programming language to produce an optimized solution through the direct application of learning algorithms to the information stored in the native machine code.

2. Description of the Related Art

Machine learning systems have been proposed in the art for the solution of problems such as classification, prediction of time-series data, symbolic regression, optimal control, etc. Examples of various machine learning systems are neural networks, fuzzy networks, genetic algorithms (including genetic programming and classifier systems), Evolutionary Strategies, Evolutionary Programming, ADAPTE program induction, cellular automata, Box Jenkins optimization, ARMA optimization and many others. Rather than applying a direct computational approach, these systems create one or more proposed solutions in the form of data and computer "program" entities, and iteratively alter the data and/or entities for the purpose of finding an optimal solution to a problem. One such approach is described in, for example, U.S. Pat. No. 4,935,877, entitled "NON-LINEAR GENETIC ALGORITHMS FOR SOLVING PROBLEMS", issued Jun. 19, 1990 to John Koza.

The set of practically solvable problems is highly related to the efficiency of the algorithm and implementation. It is therefore important to minimize the overhead involved in executing any machine learning system such as genetic programming.

Machine learning systems create learned solutions to problems. These solutions have two elements: (1) Elements that hold the information that is learned during the execution of the machine learning system (the "Learned Elements"); and (2) Elements that are necessary to convert the Learned Elements into meaningful action or output by the computer (the "Conversion Elements"). Existing machine learning approaches other than the present invention can be classified into two categories in terms of how they store and execute both the Learned Elements and the Conversion Elements. Those two categories are compiler based systems and interpreted systems.

An interpreted system is written in a high level language such as LISP and both the Learned and Conversion Elements are held in data-like structures such as LISP lists, which are converted ("interpreted") into native machine code at run-time by an interpreter. The interpreter, itself, also contains Conversion Elements for such interpreted systems. So for example, U.S. Pat. No. 4,935,877 uses, as its Learning

Elements various high level LISP expressions, customized for the problem at hand, to represent, symbolically, a "computer program." That is, a high level "program" structure symbolized by the LISP List, is itself the subject of learning in that system. In this system, the Learned Elements are represented as a hierarchical tree structure. This solution gives good flexibility and the ability to customize the language depending on the constraints of the problem at hand.

The principal disadvantage of this interpreting approach to machine learning is that the Learned Elements and many of the Conversion Elements are stored in high level, symbolic data-like structures. Computers can operate only by executing native machine code. Thus, interpreting machine learning systems learn by modifying high level symbolic representations (the Learned Elements) that are, ultimately, converted into machine code by the interpreter at run-time. The need to convert (interpret) the Learned Elements and some of the Conversion Elements into native machine code at run-time before any useful action or output may be had from a computer is very time consuming and involves a large amount of overhead in machine resources such as CPU time, RAM memory, and disk space. In effect, all of the Learned Elements and the Conversion Elements in the LISP List are treated as run-time data that must be accessed and converted to machine code before any useful action or output may be had. Simply put, interpreted systems are slow and use a lot of a computer system's resources.

Other machine learning systems are written in high level compiled computer languages such as C, C++, Pascal and so forth. This is the "compiler based" approach to machine learning. Large amounts of the Conversion Elements in such systems are compiled before run-time into native machine code in such a compiler based approach. Because those compiled Conversion Elements are already in native machine code at run-time, there is no need to interpret these Conversion Elements at run-time. Using a compiler based approach instead of an interpreted approach usually results in a substantial speed-up of the execution of the machine learning system, often increasing the speed of learning by a factor of ten times. Examples of such compiler based systems are GPC by Walter Tackett (genetic programming), Lil-GP (genetic programming), and EvoC (evolutionary strategies).

The compiler based approach to machine learning, while faster than the interpreted approach, must still access run-time data that is stored in data structures held in RAM memory or in some other form of memory such as hard disk. The reason that run-time data structures must be accessed in compiler based machine learning systems (or any machine learning system other than the present invention) is that the process of learning involves initializing and then altering the Learned Elements at run-time.

For example, the weights in a neural network are Learned Elements for neural network applications. Compiler based neural network systems hold those weights in data structures such as arrays or linked lists. Similarly, compiler based genetic programming systems store symbolic representations of program structures (the Learned Elements in genetic programming) in RAM data structures such as arrays, linked lists or parse trees. In all compiler based machine learning systems, the already compiled Conversion Elements must repeatedly access the Learned Elements (weights or symbolic representations of program structures) from the data structures in RAM memory in order to execute and evaluate the Learned Elements and to modify the Learned Elements according to the learning algorithm that is being used to

modify the Learned Elements during learning. Such repeated access is necessary before any meaningful output or action may be had from a computer based on the Learned Elements. Such repeated accesses to RAM data structures is time consuming and uses extensive amounts of RAM to hold the Learned Elements.

More generally, computing systems that perform repeated calculations on run-time data may also be categorized as compiler based systems or interpreted systems. They store access, alter and execute run-time data in a manner similar to the storage, access, alteration and execution of the Learned Elements in the systems described above and are subject to the same limitations of slow execution and system overhead as the systems described above. By the phrase, "repeated calculations (or computations) on (or of) run-time data," this application means the execution of one or more instructions that must access one or more elements of run-time data (from data storage such as RAM or hard disk) more than once on the same values of the run-time data.

SUMMARY OF THE INVENTION

The present invention utilizes the lowest level binary machine code as the "entities" or individuals or solutions. Every individual is a piece of machine code that is called and manipulated by the genetic operators.

There is no intermediate language or interpreting part of the program. The machine code program segments are invoked with a standard C function call. Legal and valid C-functions are put together, at run time, directly in memory by the genetic algorithm. The present system can therefore be considered as a "compiling" machine learning implementation.

The present system generates binary code directly from an example set, and there are no interpreting steps. The invention uses the real machine instead of a virtual machine, and any loss in flexibility will be well compensated for by increased efficiency.

More specifically, one or more machine code entities such as functions are created which represent (1) solutions to a problem or (2) code that will perform repeated calculations on "run-time data" that is encapsulated into the machine code. These entities are directly executable by a computer. The programs are created and altered by a program in a higher level language such as "C" which is not directly executable, but requires translation into executable machine code through compilation, interpretation, translation, etc.

The entities are initially created as an integer array that can be altered by the program as data, and are executed by the program by recasting a pointer to the array as a function type. The entities are evaluated by executing them with training data (as defined elsewhere) as inputs, and calculating "fitnesses" based on a predetermined criterion or by recovering the output as the result of one of the repeated calculations on run-time data.

After one or more "executions," the entities are then altered by recasting the pointer to the array as a data (e.g. integer) type. Or the original data pointer to the array may have been typecast earlier to a function pointer in a way that did not permanently change the type of the pointer. In that case, the original data pointer is used in its original form. This process is iteratively repeated until an end criterion is reached.

In the case of machine learning, the entities change in such a manner as to improve their fitness, and one entity is ultimately produced which represents an optimal solution to the problem. In the case of repeated calculations on run-time

data, the entity permits very rapid calculations to be performed generating usable output from the run-time data.

Each entity includes a plurality of directly executable machine code instructions, a header, a footer, and a return instruction. The alteration process is controlled such that only valid instructions are produced. The headers, footers and return instructions are protected from alteration.

The system can be implemented on an integrated circuit chip, with the entities stored in high speed memory in a central processing unit.

The present invention overcomes the drawbacks of the prior art by eliminating all compiling, interpreting or other steps that are required to convert a high level programming language instruction such as a LISP S-expression into machine code prior to execution.

Experiments have demonstrated that the present approach can speed up the execution of a machine learning or a repeated calculation system by 1,000 times or more as compared to systems which provide potential solutions in the form of high level "program" expressions in the interpreted approach. The speedup is in excess of 60 times over the compiler based approach. This makes possible the practical solutions to problems which could not heretofore be solved due to excessive computation time. For example, a solution to a difficult problem can be produced by the present system in hours, whereas a comparable solution might take years using conventional techniques.

These and other features and advantages of the present invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which like reference numerals refer to like parts.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a machine learning system according to the present invention as implemented on a general purpose computer;

FIG. 2 is a block diagram illustrating a computer program which implements the functionality of the present invention as stored in a random access memory of the computer of FIG. 1;

FIG. 3 is a block diagram illustrating banks of registers in the computer used in the preferred implementation of the invention;

FIG. 4 is a flowchart illustrating a method of machine learning according to the invention;

FIG. 5 is a diagram illustrating types of machine code instructions which are used by the preferred implementation of the invention;

FIG. 6 is a detailed flowchart illustrating a specific embodiment of the preferred implementation of the invention;

FIG. 7 is a diagram illustrating an array of functions that are used by the invention;

FIG. 8 is a diagram illustrating an alternative function that can be used by the invention;

FIG. 9 is a diagram illustrating the present machine learning system as implemented on a specially designed integrated circuit chip;

FIGS. 10a and 10b are diagrams illustrating a genetic uniform crossover operation;

FIGS. 11a and 11b are diagrams illustrating a genetic 2-point "swap" crossover operation;

FIGS. 12a and 12b are diagrams illustrating a genetic operator crossover operation;

FIGS. 13a and 13b are diagrams illustrating a genetic operand crossover operation;

FIG. 14 is a diagram illustrating a genetic operator mutation operation;

FIG. 15 is a diagram illustrating a genetic operand mutation operation;

FIGS. 16a to 16d in combination constitute a flowchart illustrating a generic implementation of the invention to machine learning;

FIGS. 17a to 17d in combination constitute a flowchart illustrating a generic implementation of the invention to repetitive computations based on run time data; and

FIGS. 18a to 18h in combination constitute a flowchart illustrating a machine learning implementation of the system which induces machine code functions where the Learned Elements are machine code instruction structure and machine code instruction contents. This is one implementation of what is referred to loosely as Compiling Genetic Programming Systems.

DETAILED DESCRIPTION OF THE INVENTION

The present method must be implemented using a computer due to the immense number of complex computations that must be made. The computer can be a general purpose computer, with the functionality of the method being implemented by software. Alternatively, as will be described below, part or all of the functionality of the system can be implemented on a specially designed integrated circuit chip.

Introduction

The present invention utilizes the lowest level native machine code with no immediate step of compilation or interpretation to store, access, initialize, create, alter and execute run-time data and related code where repeated computations (embodied in the related code) must be performed using that run-time data. In the context of machine learning, the run-time data (the Learned Elements) and the computations that are to be performed on the run time data (the Conversion Elements) are created, initialized, stored, altered and executed directly in native machine code with no intermediate step of compilation or interpretation. Thus, in the context of machine learning, the present invention stores both Learned Elements and the Conversion Elements in native machine code. All or many of the Learned Elements and all of the Conversion elements are created, initialized, stored, altered and executed directly in the native machine code with no intermediate step of compilation or interpretation.

The present invention is not limited to any particular machine learning paradigm such as, and by way of example only, genetic programming, genetic algorithms, simulated annealing or neural networks. Rather, it is a method of creating, initializing, storing, altering and executing all or part of the Learned Elements and the Conversion Elements in any machine learning paradigm directly in native machine code.

For example, when the present invention is applied to evolving native machine code structure and contents, it creates, initializes, stores, alters and executes the programs structures that are to be evolved (the Learned Elements) directly in native machine code. The approach of the present invention is completely unlike the compiler based and interpreting approaches to evolving "computer programs," which only create, store, alter and (with the aid of a compiler or an interpreter) execute high level symbolic representations of high level "program structures" in a high level

programming language that, ultimately, represent and are converted into actual machine code by an interpreter or that are executed by compiled code making repeated accesses to the run-time Learned Elements (the representations of high level "program structures") in RAM.

As a further example, when the present invention is applied to neural networks, it creates, initializes, stores, alters and executes the weights of the network (the Learned Elements) and the code that executes a network characterized by those weights (the Conversion Elements) directly in native machine code. This is completely unlike the compiler based and interpreting approaches to neural networks, which create, initialize, store, alter and (with the aid of a compiler or an interpreter) execute high level symbolic representations of weights and network structures that, ultimately, represent and are converted by an interpreter into the actual machine code that executes the neural network or that are executed by compiled code making repeated accesses to the run-time Learned Elements in RAM.

The present invention utilizes functions created in the lowest level machine code as the "learning entity" for machine learning or as the "computation entity" for repeated computations based on run-time data. Every such learning entity or computation entity (also referred to as an "entity" or an "individual" or a "solution") in the present invention is a complete, executable native machine code function that can be executed from a higher level language such as C or assembler by a simple standard function call ("Native Functions"). All of the run-time data and related code, the Learned Elements and the Conversion Elements are assembled by the present invention at run time into Native Functions, which constitute the learning entity or the computation entity, and the learning entity or computation entity are then stored, altered and executed directly as Native Functions. When the run-time data or the Learned Elements change, the learning entities or the computation entities must also be changed because the previous run-time data, including the previous Learned Elements, are already included in the Native Function learning entity. The present invention is, in part, a method of making such changes directly in the learning and computation entities. In a sense, the present system acts as an on-the-fly compiler of both run time data and related code (for computation entities), and of Learned Elements, and Conversion Elements (for learning entities). The present system can therefore be loosely considered as a "compiling" machine learning implementation. In the specific case of evolving machine code structures and contents as the Learned Elements, the present methodology can be loosely described as a "Compiling Genetic Programming System (CGPS)".

The present system generates low level machine code directly from an example set, and there are no interpreting or compiling steps. The invention uses the real machine instead of a virtual machine, and any loss in flexibility will be well compensated for by increased efficiency.

More specifically, one or more individuals (or "entities" or "solutions") are created which represent solutions to a problem and are directly executable by a computer as Native Functions. The programs are created, initialized, stored, altered and executed by a program in a higher level language such as "C" which is not directly executable, but requires translation into executable machine code through compilation, interpretation, translation, etc.

The entities are initially created as an integer array that can be created, initialized, stored and altered by the higher level program as data. Although the present implementation of the system uses arrays of integers, the system could be

implemented as arrays of any other data type and such implementations are within the scope and spirit of the present invention.

To understand how the system chooses what integers are included in this array, one must understand what a low level machine instruction looks like. The low level instructions on all existing CPU's are groups of binary bits. On the Sun system for which most of the development of the present system has taken place, all instructions are 32 bits long. In low level machine code, each bit has a particular meaning to the CPU. In the present system, the integers chosen for the integer arrays that constitute the entities are integers that, when viewed in binary format, correspond to valid low level machine code instructions for the CPU used in the computer system to which the present invention is being applied. Although the present system is implemented on Sun and Intel systems, it could be implemented on any CPU and many other chips. Such alternative implementations are within the scope and spirit of the present invention.

In the present implementation of the invention in C, the entities are executed by typecasting a pointer to the array of integers that constitute the entity to be a pointer to a function. The function pointed to by the entity is then executed by calling the function using the function pointer like a regular C function. The important point here is that the entities are viewed, alternatively, as data and as functions at different times in the system. At the time the entities are created, initialized, stored and altered, the entities are viewed by the system as data-an array of integers. At the time the entities are executed, they are viewed as Native Functions. So if the present system was implemented in assembler, the entities would be created as integers (as data) and they would be executed as Native Functions. No type-cast would be required in assembler but such an implementation is within the scope and spirit of the present invention.

When the entities are executed, they use training data (defined below) as inputs. The results of the execution are converted into some measure of how well the problem is solved by the entity, said measure being determined by the machine learning paradigm or algorithm being used. Said measure will be referred to herein as "fitness" regardless of the machine learning paradigm or algorithm being used. Many machine learning algorithms take the measure of fitness and feed it back into the algorithm. For example, evolutionary based learning algorithms use fitness as the basis for selecting entities in the population for genetic operations. On the other hand simulated annealing uses fitness, inter alia, to determine whether to accept or reject an entity as being the basis for further learning. After entities are initialized, most machine learning algorithms, go through repeated iterations of alteration of entities and execution of entities until some termination criterion is reached.

In the particular implementation of the present invention, the entities are initially created and initialized as an integer array that can be altered by the program as data and are executed by the program by recasting a pointer to the array as a pointer to a function type. The entities are evaluated by executing them with training data as inputs, and calculating fitnesses based on a predetermined criterion applied to the output of an entity after execution.

The entities are then altered based on their fitnesses using a machine learning algorithm by recasting the pointer to the array as a data (e.g. integer) type or by using the original data pointer. This process is iteratively repeated until an end criterion is reached.

The entities evolve in such a manner as to improve their fitness, and one entity is ultimately produced which represents the best solution to the problem.

Each entity includes a plurality of directly executable machine code instructions, a header, a footer, and a return instruction. The alteration process is controlled such that only valid instructions are produced. The headers, footers and return instructions are protected from alteration.

The system can be implemented on an integrated circuit chip, with the entities stored in high speed memory or in special on chip registers in a central processing unit and with the creation initialization, storage, alteration and execution operators stored in chip based microcode or on ROM.

The present invention overcomes the drawbacks of the prior art by eliminating all compiling, interpreting or other steps that are required to convert a high level programming language instruction such as a LISP S-expression into machine code prior to execution. It overcomes the need of compiler based systems to access, repeatedly, the Learned Elements as run-time data, which greatly slows down the system. It also represents the problem to the computer in the native language of the computer, as opposed to high level languages that were designed for human, not for machine, understanding. It acts directly on the native units of the computer, the CPU registers, rather than through the medium of interpreters or compilers. It is believed that by using an intermediate process such as interpretation or compilation of high level codes, previous systems may actually interfere with the ability of computers to evolve good solutions to problems.

Experiments have demonstrated that the present approach can speed up the execution of a machine learning system by 1,000 times or more as compared to systems which provide potential solutions in the form of high symbolic level program expressions and by 60 times or more as compared to compiler based systems. This speed advantage makes possible practical solutions to problems which could not heretofore be solved due to excessive computation time. For example, a solution to a difficult problem can be produced by the present system in hours, whereas a comparable solution might take years using conventional techniques.

These and other features and advantages of the present invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which like reference numerals refer to like parts.

Detailed Description

The modern computer has grown in instruction capabilities and machine word size, which means that there are more tasks that can be carried out elegantly by a straightforward machine language subroutines. For example, the precision of the arithmetic is enough for direct usage, and the memory organization is often flat which makes pointer operations less complex, etc.

Conventional application programs often fail to use the computer to its full potential because the algorithms are not implemented in the most efficient way. This fact is even more relevant in the use of algorithms for machine learning, artificial intelligence, artificial life, etc., repeated computations on run-time data which rely on complex manipulations and are often of the meta type where programs manipulate program structures.

The present machine learning system is a unique approach to implementation of algorithms of this kind. The approach is unknown, in spite of the fact that it is possible to use on the oldest and smallest computer. It can present a number of advantages like a speed up of a 1,000 times, low memory consumption, compact representation, etc.

The execution speed enhancement is important both for real-life applications, and for simulations and experiments in

science. A large efficiency improvement of this magnitude can make real life applications feasible, and it could also mean the difference of whether an experiment or simulation will take three days or one year. This can make a given algorithm useful in a whole new domain of problems.

If an algorithm uses a representation in a program that later can be evaluated by some kind of interpretation as a program, even in a limited sense, this approach can be used. It could be the rules in Cellular Automata, the creatures in artificial life, decision trees, rules, simulations of adaptive behavior, or as demonstrated below evolving Turing complete algorithms with an evolutionary algorithm. As described above, the present approach is referred to as a compiling approach because there are no interpreting parts and the individuals are, in effect, directly compiled.

The present method of binary machine code manipulation should not be confused with translating a machine learning algorithm into assembly code, the way a compiler operates. Instead, the present invention is capable of meta manipulating machine code in an efficient way.

The Present Compiling Approach

It is surprising that there are no existing programming languages with specialized features and tools for this programming paradigm.

The present invention provides advantages of the prior art including the following.

- Higher execution speed
- Compact kernel
- Compact representation
- Uncomplicated memory management
- Low complexity algorithms

The efficiency improvement incomes from a manipulations comes from deletion of the interpreting steps. Instead of using a structure defined by the programmer to be run through an interpreter, a match between the data structures of the application and the binary machine code structures is sought. The algorithm then manipulates the binaries and instead of interpreting, the system executes the binary directly. The efficiency benefit comes mostly from deletion of the interpreting steps, but also from the simplicity of manipulating the linear integer array that constitutes the binary machine code.

The lack of an interpreting or compiling step makes the kernel of the algorithm compact, because no definition of the interpretation is needed. The machine code binary format is often compact in itself, which is important when working with applications that use a large set of structures, for example evolutionary algorithms, cellular automata, etc.

The inherent linear structure of a binary code program forces the design of a system that uses uncomplicated memory management. The decreased use of pointer and garbage collection imposes a straightforward handling of memory that is an advantage in for example real-time applications.

Some parts of the machine learning algorithm might be simplified by the restriction of the instructions to integer arithmetic. Handling of a sequence of integers is a task that a processor handles efficiently and compactly, which could simplify the structure of the algorithm.

The approach of binary manipulating machine learning algorithms builds on the idea behind a von Neumann machine, and it is thus applicable on most of today computers from the largest super computers to the small invisible systems in cars, cameras and washing machines.

Von Neumann Machines

A Von Neumann machine is a machine where the program of the computer resides in the same storage as the data used

by that program. This machine is named after the famous Hungarian/ American mathematician Jon von Neumann, and almost all computers are today of the von Neumann type. The fact that the program could be considered as just another kind of data makes it possible to build programs that manipulate programs, and programs that manipulate themselves.

The memory in a machine of this type could be viewed as an indexed array of integers, and a program is thus also an array of integer numbers. Different machines use different maximal sizes of integers. A 32-bit processor is currently the most commonly commercially available type. This means that the memory of this machine could be viewed as an array of integers with a maximum size of $2^{32}-1$, which is equal to 4294967295, and program in such a machine is nothing more than an array of numbers between zero and 4294967295.

A program that manipulates another program's binary instructions is just a program that manipulates an array of integers. The idea of regarding program and data as something different is however deeply rooted in our way of thinking. It is so deeply rooted that most designers of higher language programmed have made it impossible for the programmer to access and manipulate binary programs. It is also surprising that no languages are designed for this kind of task. There are a no higher level languages that directly support this paradigm with the appropriate tools and structures.

The C language is desirable for practicing the present invention because it makes it possible to manipulate the memory where the program is stored.

The Processor

The processor is a "black box" which does the "intelligent" work in a computer. The principles of different available processors are surprisingly similar. The processor consists of several parts as illustrated in FIG. 3, including the control logic 44 which access the memory 12, the ALU 40, and the registers 46.

The control logic 44 uses a register or some arithmetic combination of registers to get an index number or address. The content of the memory array element with this index number is then placed in one of the registers of the processor.

A register is a place inside the processor where an integer can be stored. Normally a register can store an integer with the same size as the so-called word size of the processor. A 32-bit processor have registers that can store integers between 0 and 4294967295.

The most important register is the program counter (PC) which stores the address of the next instruction to be executed by the processor. The processor looks at the contents of the memory array at the position of the program counter and interprets this integer as an instruction that might be an addition of two registers or placing a value from memory into a register.

An addition of a number to the program counter itself causes transfer of control to another part of the memory, in other words a jump to another part of the program. After doing an instruction the program counter is incremented by one and another instruction is read from memory and executed.

The ALU in the processor perform arithmetic and logic instructions between registers. All processors can do addition, subtraction, logical "and", logical "or", etc. More advanced processors do multiplication and division of integers, and some have floating point units with corresponding registers.

Every behavior we can see in modern computers is based on these simple principles. Computers doing graphics,

animations, controlling a washing machine or watching the ignition system in a car all does these memory manipulations and register operations.

The principles above do not anywhere prevent a program from manipulating the contents of memory locations that later will be placed in the program counter and run by the processor as it interprets it as instructions. This is the basis of the binary manipulating machine learning code in accordance with the present invention.

Machine Code and Assembly Code

Machine language is the integers that constitute the program that the processor is executing. These numbers could be expressed with, for example, different radix such as decimal, octal, hexadecimal or binary. By binary machine code we mean the actual numbers stored (in binary format) in the computer.

When programming or discussing machine language, it is often impractical to use numbers for instructions. To remember that the addition instruction for example is represented by the integer 2416058368 in the SUN SPARC architecture is not natural to the human mind.

If we represent it in hexadecimal radix (E219922D), it will be more compact and it is more easy to deal with than its binary equivalent, but it is still not natural to remember. For this reason, assembly language has been developed. Assembly language uses mnemonics to represent machine code instruction. For example, addition is represented by the three letters "ADD".

The grammar for assembly language is very simple, and the translation or mapping from assembly language to machine code is simple and straightforward. Assembly language is not, however, machine language, and cannot be executed by the processor directly without the translation step.

RISC and CISC

The present invention has been implemented using both processors of the CISC type including the Intel 80486, and of the RISC type including the SUN-SPARC architecture. CISC stands for Complex Instruction Set Computer, and RISC stands for Reduced Instruction Set Computer. As indicated by the acronym, the RISC processor has fewer and less complex instructions than the CISC processor. This means that the RISC processor can be implemented differently in hardware and that it therefore will be faster.

There are advantages of both paradigms when using them for binary manipulating machine learning. The CISC has the advantages of many more types of instructions and addressing modes, and a subset can be readily found which makes a particular implementation straightforward.

The RISC processor on the other hand has the advantage that the structure or "grammar" of an instruction is very simple, for example the number of bits is constant. This sometimes makes the manipulation easier. It is easier to check for a valid instruction. A RISC is also often faster than a CISC.

Although the present invention can be practiced using CISC and RISC systems, it is somewhat easier to administer on an RISC based architecture.

Another important factor is the operating system and hardware support of the development environment. A system like UNIX which offers separate processes and hardware implemented memory protection is definitely to recommend during development, because it will save time when bugs appear during the development phase. These systems do not have to be restarted after a serious bug like an illegal instruction. It should, however, be noted that once the system is debugged it will run as safely on any platform as any other conventional program.

Structure of Machine Code Function

A procedure and a function can be regarded as very similar concepts in machine code or even in C. A procedure is a function that does not return a value. When implementing a machine learning system with a binary manipulating technique, functions are the basic structures. For example, the individuals in compiling genetic algorithms are implemented as machine code functions. A function call has to perform three different subtasks:

Program control transfer and saving the start address

Saving processor registers

Transfer parameters

The most important instruction for functions and procedures is the call instruction. It is present in all kinds of processors, and works as a jump instruction that saves the memory location or address of where it was jumping from. This will allow a return instruction to return back to this memory location when execution of the function is complete.

Most call instructions save the return address in a special memory segment called the stack, but some save it internally in a register in the processor. The SUN SPARC architecture saves the return address in a register, if there is enough room for it.

A call instruction is not sufficient to make a complete function call. The contents of the registers must be saved somewhere before the actual instructions of the function are executed.

This assures that the called function will not interfere with the processing in the calling function, and gives the called function the liberty to manipulate these registers itself. The most common place to store the contents of the calling functions registers, is the stack. Some architectures like the SPARC architecture stores it inside the processor by the special save instruction.

When the execution of the function is done, the registers of the calling function have to be restored to allow this function to continue processing in the context it was working in before the function call.

The last task a processor has to accomplish in order to perform a complete function call is to transfer the parameters to the function. It has to transfer the input parameters when the call is performed, and transfer back the return values after the execution of the function is complete. Again, this is most commonly done by storing these values in the stack, but it can also be done by using special registers inside the processor.

These four important steps: calling the function, saving and restoring registers, transfer of parameters and return of outputs can be done in different ways. It can even be done in different ways on the same processor. Normally it is the job of the compiler to produce machine code instructions that perform these three steps in a suitable way.

In order to make it possible to link object code from different compilers and to increase portability, a number of standards, recommendations and conventions have emerged. There is for example the calling convention whereby it is up to the calling function to save the registers or whereby it is up to the called function to save the registers. In the SPARC architecture, it is the called function that saves the callers registers. In a similar manner there are conventions for how parameters should be transferred.

When working with machine learning at the binary level, it is sometimes allowable to be more free, and for example not always save all registers if it is known that the called function will not use them. This not only provides a more efficient implementation, but also presents the opportunity to

use special features of the architecture that are hard to express in a high level language.

As described above, the structure of a function on the machine code level can be considered as an array of integers divided having four parts:

Header
Body
Footer
Return

The header of a function does one or more of the three steps mentioned above. In the SPARC architecture, the header of the function saves the registers of the calling function and sometimes also transfers parameters. Which of the three steps the header does is different from processor to processor and from compiler to compiler.

Although most function structures need some kind of header to perform a function call, some special kinds of functions do not need a header, such as the leaf procedure in the SPARC architecture.

The header is fairly constant and normally does not have to be manipulated by the machine learning part of the program. It can be defined at an early stage, for example in an initialization phase of the system.

The body of the function does the actual work that the function is supposed to carry out. When the body of the function is entered, all of its parameters are accessible to it, and the registers from the calling function are saved. The body can then use any of the arithmetic instructions or call another function to compute the desired function.

The footer contains the "cleanup" instructions as described elsewhere.

A return instruction must always follow the footer. This instruction finds out where the call to this function was made from, and then jumps back to this location. The address to jump back to is either stored on the stack or in special registers in the processor.

SPARC Architecture

A system that directly manipulates machine code is not easily made portable, so it is recommended to choose one platform as a base for experimentation. The preferred system includes the SPARC architecture and SUN workstations. The reason for this is that is one of the most widely used architectures in the research community, with a stable UNIX operating system. It is also a relatively fast RISC architecture.

SPARC is an open architecture with several different implementations and manufacturers. The SPARC International, Inc. is a non-profit consortium for evolution and standardization of this architecture. A well known user of SPARC is SUN Microsystems Inc., which uses the architecture in all of its modern workstations.

SPARC Registers

As described above with reference to FIG. 3, the most important of the different kinds of registers as applicable to the present invention are the "windowed registers". It is between the windowed registers that almost all arithmetic and logic operators take place. There are a dozen other registers that are more important to the system software than to a client application. The program counter is also an important register.

The windowed registers are divided into four classes:

Output registers O_0 to O_7

Input registers I_0 to I_7

Local registers L_0 to L_7

There are also eight global registers G_0 to G_7 .

There are eight registers in each of these classes. When a save instruction is executed, it copies the contents of the

output registers into a new set or bank of corresponding input registers. Register O_0 is copied into I_0 , O_1 is copied into I_1 , etc. The input register used is a new input register owned by the called function.

5 The values in the old input registers are kept or saved. It will be noted that the contents are not really copied. In reality these registers are the same, and only a pointer to the current set of register is incremented.

The processor has an internal storage for a few banks or 10 sets of register like this (seven in the SPARC architecture), and if this limit is exceeded, the hardware and system software will save the contents in memory. For the user, this banked register mechanism can be thought of as a small internal stack.

15 It is important to note that a save instruction copies the contents of the calling function's output registers into the called function's input registers, while the restore instruction copies the contents of the returning function's input registers into the calling function's output registers.

20 When a function wants to call another function and pass some variables, it thus places the parameters in its output registers and makes the call. After the function call has been completed, the returning values can be found again in the output registers.

25 The local registers are local to the function working for the moment, and are used for temporary storage. A fresh set of local registers is provided when a new function is called, but there is no special transfer of values into these registers.

The global registers are always the same. They keep their 30 meaning and content across function calls, and can thus be used to store global values. There are no alternative sets of this registers like there are with the input, output, and local registers.

Register Implementation

35 Some of the registers have a reserved usage. In some cases the reserved meaning is due to hardware, but in most cases the origin of these constraints are software conventions, as specified by the SUN Application Binary Interface (ABI).

40 In accordance with the present invention, almost all of the actual algorithm is written in a high level language like C. This prevents interference with the work done by the compiler. If this goal is abandoned, and the complete system were written in assembly language, even higher flexibility could be achieved. However, all portability would be lost, and it is therefore preferred to provide the manipulating program in a high level language such as C.

The global registers are preferably not used by the 50 program, because these registers are likely to be used by the code generated by the compiler. Global storage for function structures can be provided in memory.

Global register zero has a special meaning. It is not a register where values can be stored. An attempt to read global register zero, always returns the value zero, and an attempt to write to global register zero does not change 55 anything. This register is used when a zero constant is needed or when the result of an operation should be discarded.

Global register one is by convention assumed to be 60 destroyed across function calls, so this register can be used by the functions that are manipulated by the machine learning algorithm.

Registers I_6 , I_7 , O_6 , and O_7 are by convention used to store 65 stack and frame pointers as well as the return address in a function call, so these should not be used by the program.

Local registers zero and one have special uses during an interrupt but this will not affect the functions.

15

Thus, the registers which are available for use in the SPARC architecture are global register G_1 , input registers I_0 to I_5 , output registers O_0 to O_5 , and local registers L_0 to L_7 . Detailed Implementation

FIG. 1 illustrates a computer system **10** for implementing a machine learning method according to the present invention. The system **10** includes a Random Access Memory (RAM) **12** in which the software program for implementing the functionality of the invention is stored, and a processor **14** for executing the program code. The system **10** further includes a visual display unit or monitor **16** for providing a visual display of relevant information, a read-only memory (ROM) **18** for storing firmware, and an input-output (I/O) unit **10** for connection to a printer, modem, etc.

The system **10** further includes a mass data storage **20** which can be any combination of suitable elements such as a fixed (hard) magnetic disk drive, a removable (floppy) disk drive, an optical (CD-ROM) drive, etc. Especially large programs which implement the invention may be stored in the storage **20**, and blocks of the programs loaded into the RAM **12** for execution as required.

User access to the system **10** is provided using an input device **22** such as alphanumeric keyboard **114** and/or a pointing device such as a mouse (not shown). The elements of the system **10** are interconnected by a bus system **24**.

The system **10** is preferably based on the SUN SPARC architecture due to its register structure. The invention is also preferably implemented using the "C" programming language due to its freedom in the use of data types and the ability to cast between different types, especially pointers to arrays and pointers to functions and a standard SUN operating system compiler, although the invention is not limited to any particular configuration.

The invention has been practiced using the above configuration in the SPARC environment which generally a stable architecture for low level manipulation and program patching. The particular platform used was the SUN SPARCSTATION 1+.

The RAM **12** is illustrated in FIG. 2 as storing an operating system **30** such as UNIX or one of its variants, and a program **32** written in the "C" language which provides the functionality of the invention. The program **32** includes high level machine language instructions **32a**, and one or more machine code arrays **32b**.

The high level instructions **32a** are not directly executable by the processor **14**, but must be converted into directly executable machine code by a compiler. The array **32b**, however, is provided in native (lowest level) machine code including binary instructions that are directly recognized and executed by the processor **14**.

The performance of the present invention is greatly enhanced by implementation thereof using a processor having banks of registers. This architecture is provided by the SPARC system as illustrated in FIG. 3.

The components of the SPARC processor **14** which are most relevant to understanding the present invention include an Arithmetic Logic Unit (ALU) **40** for performing actual numeric and logical computations, a program counter **42** for storing an address of a next instruction to be executed, and a control logic **44** which controls and coordinates the operations of the processor **14** including memory access operations.

The processor **14** further includes banks of registers which are collectively designated as **46**. The processor **14** also includes a number of additional registers which are not necessary for understanding the principles of the present invention, and will not be described. Although the invention

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is presently implemented using integer arithmetic, it may be applied to Floating Point arithmetic easily and such an application is within the scope and spirit of the invention.

More specifically, the registers **46** include eight register banks (only one is shown in the drawing), each of which has 8 output registers O_0 to O_7 , 8 input registers I_0 to I_7 , 8 local registers L_0 to L_7 . There are, also, 8 global registers G_0 to G_7 accessible from any bank. The implementation of the invention using this architecture will be described below.

FIG. 4 is a flowchart illustrating the general machine learning method of the present invention which is implemented by the high level instructions **32a** in the C programming language. The first step is to define a problem to be solved, a fitness criterion for evaluating the quality of individual solutions, and an end criterion. The end criterion can be a predetermined number of iterations for performing the process (e.g. 1,000), achievement of a predetermined fitness level by one or more solutions, a change in total or individual fitness which is smaller than a predetermined value, or any other suitable criterion.

Next, the input, output, calculation, and state registers must be identified.

An input register is a register that is initialized before each calculation with data. In the present implementation of the invention, the input registers may be any one of the registers referred to as I_0 through I_5 in the Sun architecture. See FIG. 3, number 46. In the present implementation of the invention, it is, therefore possible to have up to six input registers. However, it would be easy to extend the system to have many more input registers and such an extension is within the scope and spirit of the present invention. In any event, the designer must pick how many of the eight input registers to use.

There are many ways to initialize these registers but the preferred implementation is to include the input variables as parameters when the individual is called as a Native Function. For example, if `native_function_array` is an array of integers that constitute valid machine code instructions that amount to a Native Function and that amount to an entity in this invention, then the following type definition and function call execute the `native_function_array` individual and pass two input variables to it.

```
Typedef unsigned int(* function_ptr) ();
{the type definition}
a=((function_ptr) native_function_array)(2,3);
{calls the function and passes two inputs (2 and 3), which are placed in 10 and 11.}
```

The items in curly brackets are descriptive and not part of the code. In the present implementation of this invention, the two input variables are put into **10** and **11**. Accordingly, if the designer decides to have two input registers, they must be **10** and **11** in the present implementation. Other methods of initializing registers such as putting instructions in the header of the entity (see FIG. 5, number **50**) that retrieve data from RAM provide more flexibility as to what registers are input registers and more input registers and they are within the scope and spirit of the present invention.

This process of picking and initializing input registers is referred to in FIGS. **16b**, **c**, and **d**; **17b**, **c**, and **d** and **18b**, **d**, and **f**.

An output register is read after the individual has finished executing on a given set of inputs. In other words, an output register is the output of the individual on a given set of inputs. The designer must designate one or more registers to be the output register(s) and the number depends on the problem to be solved. In the present implementation, the value in **10** at the end of the execution of the individual is

automatically set as the single output register and as the output of the individual. The above code automatically puts the value in **10** into the variable "a." It is possible to designate multiple output registers and to preserve the values therein when an individual has been executed. One such method would be to include instructions in the footer of the individual (see FIG. 5, number **50**) that move the value(s) in the designated output registers in the individual that has just executed to storage registers or to locations in RAM memory. Such implementations are within the scope and spirit of the present invention.

This process of picking and recovering the values in output registers is referred to in FIGS. **16b**, **c**, and **d**; **17b**, **c**, and **d** and **18b**, **d**, and **f**.

A calculation register is a register that is neither an input nor an output register but that is initialized to a given value every time the individual is executed. Zero or one is the preferred initialization value. A calculation register may be initialized in the headers of the individuals. (See FIG. 5, number **50**). In any event the designer must decide how many, if any, calculation registers he or she wishes to use and then designate specific registers to be calculation registers. So, for example, if there were two input registers, **10** and **11** and if **10** were the output register, then **12** through **15**, and **L0** through **L7**, among others would be available slots for a calculation register. So if the designer desires one calculation register, he could pick **12** as the calculation register.

This process of picking and initializing calculation registers is referred to in FIGS. **16b**, **c**, and **d**; **17b**, **c**, and **d** and **18b**, **d**, and **f**.

A state register is a register that is neither an input nor an output register but that is not initialized every time the individual is executed. That is, values from some previous execution of the individual are retained in a state register. The precise retention policy is a matter of decision for the designer. At the beginning of the execution of the individual, the state register has to be initialized to the value it held at the end of a previous execution of the individual. If that value was saved in a storage register or in RAM, then the header of the individual (See FIG. 5, number **50**) must have an instruction moving the value from the storage register or RAM to the state register or the previous state could be passed to the individual as a parameter when the individual is called as a Native Function. In this case, the footer of the individual may have an instruction saving the value of the state register at the end of execution to the storage register or to RAM. There are many available ways to implement state registers and to save and initialize their values and all of them are within the scope and spirit of this invention. In any event the designer must decide how many, if any, state registers he or she wishes to use and then designate specific registers to be state registers. So, for example, if there were two input registers, **10** and **11**, and one calculation register, **12**, and if **10** were the output register, then **13** through **15**, and **L0** through **L7**, among others would be available for a state register. So if the designer desires one state register, he or she could pick **13** as the state register.

This process of picking and initializing state registers is referred to in FIGS. **16b**, **c**, and **d**; **17b**, **c**, and **d** and **18b**, **d**, and **f**.

Once all registers have been designated, the designer has established the "Register Set." In the example above, the Register Set would be as follows

input	I0, I1
output	I0
calculation	I2
state	I3

Once the Register Set has been picked, it is essential that all individuals be initialized with instructions that contain only references to valid members of the register set. See FIGS. **16c**, **17c**, and **18d**. It is also essential that all changes to the individuals, including those made with genetic operators, modify the individual in such a way as to make sure that all register references in the modified instructions are to valid members of the Register Set.

Next, a solution or population of solutions is defined as an array of machine code entities. These entities are preferably "C" language functions which each include at least one directly executable (machine language) instruction. An instruction is directly executable by being constituted by the lowest level (native) binary numbers that are directly recognized by the control logic **44** and ALU **40** as valid instructions. These instructions do not require any compilation, interpretation, etc. to be executable.

The invention will be described further using the exemplary case in which the entities are "C" language functions. However, it will be understood that the invention is not so limited, and that the entities can be constituted by any data structures including machine code instructions that can alternatively be manipulated as data and executed by a higher level program.

After the function or array of functions has been defined, they are initialized by inserting valid machine code instructions in the appropriate locations therein. As illustrated in FIG. 5, a function **50** includes a header **50a**, an instruction body **50b**, a footer **50c**, and a return instruction **50d**.

The header **50a** deals with administration which is required when entering a function. This normally involves manipulation of the registers **46**, including passing arguments for the function to and from the various registers **46**, saving the values in the registers that exist when the function is called and saving the address of the calling instruction so that, when the function is finished, program execution can begin from where it left off. The header can also be used to perform many other useful functions at the option of the designer including initializing registers and recovering the values of saved state registers. There can also be processing to ensure consistency of processor registers.

The header **50a** is often constant and can be added at the beginning of the initialization of the individual machine code functions in the population. Mutation, crossover and any other operator that alters the entity must be prevented from changing this header field when they are applied to an individual function or the field must be repaired after the application of the operator.

The footer **50c** is similar to the header **50a**, but does the operations in the opposite order and "cleans up" after the function call by, among other things, restoring the registers to their state before the function call, recovering the output of the function, saving state registers, and many other useful functions at the option of the designer. The footer field must also be protected from change by the genetic or other alteration operators or the field must be repaired after the application of the operator.

The return instruction **Sod** forces the system to leave the function and return program control to the calling procedure via the program counter **42**. If variable length programs are desired, the return instruction can be allowed to move within

a range defined by a minimum and maximum program size. The return instruction must also be protected from change by the genetic or other alteration operators or the field must be repaired after the application of the operator.

The function body 50b includes at least one directly executable machine code instruction, for example instructions 52a, 52b and 52c. In the SPARC architecture, instructions have a fixed length of 32 bits. Instructions can be of two types: a first type which is designated as 54 and consists of a single 32 bit operator; and a second type which is designated as 56 and includes a 19 bit operator and a 13 bit operand. The operand represents data in the form of a numerical variable.

During the initialization step, the instruction bodies 50b of the functions 50 are filled with valid machine code instructions in a suitable manner. In the preferred implementation, the instructions are initialized from a Default Instruction Template Set, which contains partially “blank” instructions that contain information on what types of instruction is represented by a particular template. For example, is it an instruction that adds the values in two registers together or an instruction that adds a constant to a register value? What is left blank in the template is the register(s) to which the instruction applies and the constant values to be included in the instruction. The register references and the constant values may be added by methods such as those described in FIG. 18d. In FIG. 18d, instruction templates are randomly chosen and then the blanks are filled out so that the integer array constituting the individual contains only valid machine code instructions, taking care to limit the register references therein members of the Register Set. See FIGS. 17c, 18b and 18d. The instructions can be selected randomly, or using any suitable selection criterion.

In the most basic form of the invention, to limit the search space and to avoid complex control mechanisms and thus achieve maximum performance, the set of machine code instructions is limited in a number of ways. Only two registers and only those machine code instructions of two addressing mode types are used. All of them operate internally in the processor. However, more lengthy and complex implementations of the Register Set are described above and more complex implementations of the instruction set are within the spirit and scope of the invention.

The first addressing mode takes one argument from memory immediately afterwards and performs an operation on this argument and a processor register and leaves the result in a register. The other takes the operand from the second register, performs the operation and leaves the result in the first register.

With these kinds of instructions it is possible to reach the maximum processor throughput. The instructions are also constrained to those which take an integer as argument and return an integer. This however does not limit the problem space to mathematical problems or just to integer arithmetic. No control instructions such as jump instructions are allowed which means that no loops can be formed. These limitations reduce the complexity and thus execution time of the individual programs.

The basic instructions are listed in the following TABLE.

TABLE	
ADD (imm), ADD (reg2)	Add register one to an immediate operand or add register one to register two.
SUB (imm), SUB (reg2)	Subtract register one from an immediate operand or subtract

TABLE-continued

MUL (imm), MUL (reg2)	register one from register two. Multiply register one by an immediate operand or multiply register one by register two.
DIV (imm), DIV (reg2)	Divide register one by an immediate operand or divide register one by register two.
OR (imm), OR (reg2)	Logical OR of register one and an immediate operand or logical OR of register one and register 2.
AND (imm), AND (reg2)	Logical AND of register one and an immediate operand or logical AND of register one and register two.
XOR (imm), XOR (reg2)	Logical EXCLUSIVE OR of register one and an immediate operand or logical EXCLUSIVE OR of register one and register two.
SETHI	Set the high bits of a register, used when an operand bigger than 13 bits hits needs to be loaded into a register.
SRL	Logical shift right of register one to an immediate operand or logical shift right of register one a number of steps defined by register two.
SLL	Logical shift left of register one to an immediate operand or logical shift left of register one and register two.
XNOR	Logical EXCLUSIVE NOR of register one to an immediate operand or logical EXCLUSIVE NOR of register one and register two.

These functions can and are used to implement other common processor functions. Loading of operands into registers is performed by the OR instruction, clearing a register is performed by the AND instruction, and the negation instruction can be performed by the XNOR instruction etc.

An exemplary array 60 of functions F₀ to F₆ is illustrated in FIG. 7. Each function includes a header 50a including instructions which are collectively designated as H, a body 50b including instructions B, a footer 50c including one or more instructions F, and a return instruction 50d which is indicated as R. Although the figure shows a length of three instructions for the header and one for the footer, those particular numbers are for illustrative purposes only.

The functions of the array 60 are illustrated as having a fixed length. However, the invention is not so limited, and the functions can have variable lengths.

FIG. 8 illustrates an alternative embodiment of the invention in which only a single solution in the form of a function 62 is provided. The function 62 is configured as a continuous array that contains valid machine code instructions, and is typically larger than the functions of the array 60. Such a single array would be a typical way to implement a system not involving machine learning but involving repeated computations on run time data. Certain machine learning approaches would use such a single structure also.

After the array is initialized, it is recast as a function type array, and the registers 46 are initialized with training data. The training data is normally part of a “training set”, each element of which consists of one or more inputs and a desired output. The training set represents the problem that is to be solved. However, the invention is not so limited, and the training data can alternatively include testing, validation, prediction, or any other data suitable for machine learning or for repetitive calculations on run-time data.

For machine learning applications, the purpose of the learning process is to train the functions using the training

data by causing the functions to evolve until one of them produces outputs in the output register(s) in response to the training inputs in the input register(s) that closely approximate the desired outputs. The inputs are passed to the functions by initializing the registers with the training data as described elsewhere.

The functions of the array (or single function as illustrated in FIG. 8) are then executed with the training data as inputs. This execution causes the functions to produce output(s) in the output register(s) which are calculated in accordance with the instructions in the functions.

The output register or registers are then read, stored and compared with actual or desired outputs from the training data to calculate fitnesses of the functions. A function has a high fitness if its output closely approximates the desired output, and vice-versa. If the end criterion is met, the program ends.

If the end criterion is not met, the array is recast or used as a data array (e.g. integer), and the instruction bodies are altered. During this process, selected individual instructions are altered, replaced, added or deleted such that the altered function includes at least one valid machine code instruction. In other words, regardless of the manner in which a particular function is altered, the program ensures that the altered function will not include any invalid instructions.

The function(s) can be altered using any machine learning algorithm. One preferred methodology is genetic evolution of machine code structures and content, including crossover and mutation operators as will be described in detail below. However, the invention is not limited to any particular learning paradigm, nor is it limited to machine learning applications. The invention can be used, for example, to alter run-time data encoded in the machine code for the purpose of performing repetitive calculations on the run-time data.

As described above, it is important that the header, footer and return instruction will not be altered. This can be accomplished by protecting these elements from alteration using masking or other programming techniques. Alternatively, these elements can be allowed to be altered, and their initial states subsequently restored by repair or replacement. As another alternative, the instructions can be separated from the function, altered, and then returned to the function. There are other ways to protect the header, footer and return instructions from being altered, all of which are within the scope and spirit of this invention.

After performing the alteration, the program loops back to the step of recasting the array as a function and executing the function. The program iteratively repeats these steps until the end criterion is met.

The output of the system, when used for machine learning, is the function that has the highest fitness and thereby produces outputs that are closest to the desired outputs in response to the training inputs. The functions evolve as the result of the alterations, with one individual finally emerging as being improved to the highest fitness. The policy for selecting a "best individual(s)" is a matter of discretion by the designer. This system applies to any such policy.

As described above with reference to FIG. 3, the registers include banks of input registers and output registers. These registers are used to pass data from a calling function to a called function, and are used to initialize the functions with training data as further described above.

More specifically, functions use their input registers to store variables. When a function calls another function, the Sparc Architecture transfers the contents of its input regis-

ters to its output registers. The called function transfers the contents of the calling function's output registers into its own input registers, and operates on the data using its input registers. The opposite operation takes place when control is returned from the called function to the calling function.

Thus, the C program initializes a function with training data by storing the training data in its output registers and then calling the function. This method of initialization is preferred in the SPARC implementation, but the invention is not so limited. Other mechanisms for initializing functions with training data may be preferable with other computer architectures or for more complex application on the SPARC architecture.

An important feature of the present invention is to create and alter machine code functions as data, and execute the functions, from a high level language such as C. The following illustrates how this manipulation can be accomplished using the SPARC architecture.

As a simplified example, define a simple function that computes the sum of two input parameters and returns the result from this addition.

```
sum(a,b)=a+b
```

This function can be translated by a compiler in the SPARC architecture to the following five assembly language instructions.

```
save
add %i0,%i1,%i0
restore
ret
nop
```

These five assembly language instructions are stored sequentially in memory as five 32-bit numbers having the following decimal equivalents.

```
2178940928
2953183257
2179465216
2177359880
16777216
```

The "save" instruction corresponds to the number 2178940928, and is a special machine code instruction in the SPARC architecture that saves the contents of the calling function's registers and transfers the parameters to the called function.

The "add" instruction adds the contents of input register "i0" to the contents of input register "i1", and stores the result in input register "i0". This instruction is coded as the integer 2953183257. Additions between other registers are represented by other integers.

The "restore" instruction restores the registers from the calling function and transfers the result from the addition (present in register i0) for access from the calling function.

The return instruction "ret" jumps back to the memory location from where the function was called.

The "nop" instruction is a no operation instruction that does nothing but "entertain" the processor while jumping back. This instruction could be left out if the order of the "restore" and "ret" instructions was reversed as will be described below.

Implementation of the present invention involves calling a machine code function as exemplified above from the C or other high level language. Adding the numbers 2 and 3 by calling the function sum(2,3) can be represented in assembly language as follows.

```

...
mov 2, %o1
mov 3, %o0
call _sum
nop
...

```

These instructions are represented by these four integers:
 2450530306
 2484084739
 2147483646
 16777216

The first instruction stores the input parameter “2” in the output register %o1. The second instruction stores the input parameter “3” in the output register %o0.

The call instruction jumps to the location of the sum function and stores the address of itself in a register (output register %o7 by convention). This causes the program counter 42 to contain the address or location of the first instruction of the sum function. In other words, it contains the address of a memory location which stores the integer 2178940928 (save), and execution continues from here until the return instruction is encountered. After the return from the function, the output register %o0 will contain the result from the summation which can be used in further calculations.

When a save instruction is executed, it copies the contents of all output registers to an unused set of input registers. In this way the sets of input and output registers are used as a small internal stack for transfer of parameters and saving of register contents. The calling function stores the parameters of the called function in the output registers, the save instruction copies them to the input registers of the called function, and the restore instruction later copies all input registers of the called function into the output registers of the calling function. If the number of parameters is larger than the number of registers, the memory in the stack has to be used, as in most other processors.

In this manner, the input data (training data in the machine learning system and run-time data for computational entities) is passed to the array of functions (solutions) by storing the data in the output registers of the calling function, and then calling the array.

The “nop” does nothing but keep the processor occupied while jumping to the function. In a more effective but less clear version, the “mov 3, %o0” instruction is placed after the “call”, which makes the processor execute this instruction “while” jumping to the function.

The following illustrates how to call the sum function defined above from the C-language.

```

typedef unsigned int(* function_ptr) ()
unsigned int summary[]={2178940928, 2953183257,
  2179465216, 2177359880, 16777216};

```

```

a=((function_ptr) summary)(2,3);

```

These three lines of C-code will compute the sum of 2 and 3 and put the result in a variable “a” by calling a function defined by the integers in the “summary”.

The first line of code defines the function pointer type in C, because this type is not predefined in the C-language.

The second line of code declares an integer array containing integers for the instructions in the sum function as defined above.

The last line of code converts the address of the summary from a pointer to an integer array to a pointer to a function, and then calls this function with the arguments 2 and 3. The result from the function call is placed in variable “a”.

This example illustrates the basic principles of manipulating binary programs. The summary can be altered like any other array as long as its contents are valid functions that can be called (executed) to evaluate the results of the algorithm.

The present method as implemented in the C programming language utilizes four instructions for initializing, altering, and executing machine code functions.

1. A first instruction that points to and designates machine code stored in a memory as data.

2. A second instruction that points to and designates machine code stored in the memory as at least one directly executable function.

3. A third instruction that alters machine code pointed to by the first instruction.

4. A fourth instruction that executes machine code pointed to by the second instruction.

Examples of the four instructions are presented below.

```

1.  unsigned int * theintegerpointer;
    {declaration of integer pointer variable}
    theintegerpointer = (unsigned int *)
    malloc (Max_Individual_Size * Instruction_Size)
    {The instruction creating a pointer to an integer
array}
2.  Alternative 1
    -----
    typedef unsigned int (*function_ptr) ();
    {definition of the function_ptr type as a pointer to
a function}
    function_ptr thefunctionpointer
    {declares thefunctionpointer as a variable of type
function_ptr}
    thefunctionpointer=(function_ptr) theintegerpointer;
    {Instruction that typecasts theintegerpointer as a
pointer to a function}
    Alternative 2
    -----
    typedef unsigned int (*function_ptr) ();
    {definition of the function_ptr type as a pointer to
a function}
    Predicted_Output = ((function_ptr)
theintegerpointer) (Input Data Here);
    {the code "((function_ptr) theintegerpointer)" is an
expression within an instruction that performs a typecast.}
3.  theintegerpointer[2] = theintegerpointer[2] | 1234;
    {XOR's the value in the second instruction with the
integer 1234}
    or
    theintegerpointer[3] = 16777216;
    {places an nop instruction in the third instruction
slot, overwriting the previous instruction}
4.  var_a = thefunctionpointer (Input Data Here);
    or
    Predicted_Output= ((function_ptr)
theintegerpointer) (Input Data Here);

```

In the CGPS embodiment of the invention which utilizes genetic crossover and mutation operations, the types of operations that can be performed depend on the type of instruction; more specifically if the instruction includes only an operator, or if it includes an operator and an operand. Examples of genetic crossover and mutation operations are illustrated in FIGS. 10 to 15.

FIGS. 10a and 10b illustrates a uniform crossover operation in which like numbers of adjacent complete instructions are exchanged or swapped between two functions. FIG. 10a illustrates two functions 70 and 72. Uniform crossover is performed by exchanging, for example, two instructions indicated as “4”, and “2” in the function 70 for two instructions indicated as “5” and “9” in the function 72.

The results are illustrated in FIG. 10b. An altered function 70' includes all of its original instructions except for the “4” and the “2” which are replaced by the “5” and the “9” from

the function 72. The function 72 includes all of its original instructions except for the "5" and the "9" which are replaced by the "4" and the "2" from the function 70.

FIGS. 11a and 11b illustrate "2-point crossover", in which blocks of different numbers of complete instructions are exchanged between two functions. In this case, two points are selected in each function, and all of the instructions between the two points in one function are exchanged for all of the instructions between the two points in the other function.

In the example of FIG. 11a, instructions indicated as "7" and "8" in a function 74 are exchanged for instructions "4", "7", "6", and "1" in a function 76 to produce functions 74' and 76' as illustrated in FIG. 11b.

FIGS. 12a and 12b illustrate how components of functions can be crossed over. In FIG. 12a, two instructions 78 and 80 have operators 78a and 80a and operands 78b and 80b respectively. In this case, the operator 78a of the function 78 which is indicated as "OP1" is exchanged for the operator 80a of the function which is indicated as OP2. The result of the crossover is illustrated in FIG. 12b.

FIGS. 13a and 13b illustrate an example of how uniform crossover can be performed between all or parts of operands. In FIG. 13a, a function 82 has an operator 82a and an operand 82b, whereas a function 84 has an operator 84a and an operand 84b. The rightmost two bits of the operand 82b are exchanged for the rightmost two bits of the operand 84b to produce functions 82' and 84' with operands 82' and 84' as illustrated in FIG. 13b.

FIG. 14 illustrates how the operator of a function 86 can be mutated. In this case, the function 86 initially has an operator which is indicated as OP1, and is altered or replaced so that a mutated function 86' has an operator OP2. It is necessary that both operators OP1 and OP2 be valid machine code instructions in the set of instructions used by the system.

FIG. 15 illustrates how all or part of an operand can be mutated. A function 88 has an operator 88a and an operand 88b. In this example, the second least significant bit of the operand 88 is changed from "1" to "0" or "flipped" to produce an altered function 88' having an altered operand 88b'.

As set forth above, the present invention can be applied to any applicable problem by using any suitable machine learning algorithm. The principles described in detail above can be applied to implement a particular application and computing environment.

In addition to implementing the present machine learning system on a general purpose computer as described above, it is possible to implement part or all of the system as a specially designed integrated circuit chip 90 such as an Application Specific Integrated Circuit (ASIC) which is symbolically illustrated in FIG. 9.

The chip 90 comprises a Central Processing Unit (CPU) 92 including a processor 94 and a RAM 96. The processor 94 includes normal CPU microcode plus microcode implementing storage, initialization, creation, and alteration operators. The RAM 96 is preferably a high speed cache memory which the processor 94 can access at a much higher speed than the processor 94 can access off-chip memory.

The RAM 96 can include a number of registers, or can have a conventional address based architecture. Preferably, the population of functions (solutions) is stored in the RAM 96 for rapid manipulation and execution by the processor 94. Other alternatives include additionally storing the high level program in the RAM 96. As yet another alternative, the chip 90 can include a ROM 98 for storing, for example, a kernel of the high level program.

The on chip memory, alternatively could be registers dedicated to storing individuals or high speed, on chip RAM that is not a cache. In addition, the CPU could alternatively execute machine learning operators such as crossover and mutation or any other operators that initialize, create, evaluate or alter individuals in microcode or in high speed ROM.

A preferred implementation of the invention evolves machine code structures and machine code contents, as a way of learning the solution to a problem. A detailed flowchart of this system is presented in FIG. 6 as an example for reference purposes.

The program utilizes a small tournament in combination with genetic crossover and mutation operations, and includes the following basic steps.

1. Randomly pick four individuals from the population.
2. Evaluate them in pairs, two at a time according to their fitness.
3. Let the two winners breed.
4. Replace the losers with the children of the two winners.
5. Repeat step 1-4 until the success predicate is true or the maximum number of tries is reached.

The flowchart is believed to be self-explanatory except for probabilistically choosing one operation or another. These choices are analogous to flipping a coin, and can be implemented using, for example, a random number generator which generates random numbers between 0 and 1. If the number is 0.5 or less, a first probabilistic branch Pa is taken. If the number is higher than 0.5, a second probabilistic branch Pb is taken. Choices having more than two options can be implemented by dividing the range between 0 and 1 into a number of subranges equal to the number of choices.

FIGS. 16a to 16d are further provided for reference, and in combination constitute a detailed flowchart of the generic machine learning system of the present invention. The entries in the flowchart are believed to be self-explanatory, and will not be described in detail.

FIG. 16a outlines the general operation of the system. FIG. 16b sets forth the details of the block entitled "SYSTEM DEFINITION" in FIG. 16a. FIG. 16c sets forth the details of the block entitled "INITIALIZATION" in FIG. 16a, whereas FIG. 16d sets forth the details of the block entitled "LEARN FOR ONE ITERATION" in FIG. 16a.

FIGS. 17a through 17d are further provided for reference, and in combination constitute a detailed flowchart of the application of the invention to any computation problem that involves repeated access to run-time data. The entries in the flowchart use the terminology of this application and are believed to be self explanatory in the context of this application, and will not be described in detail.

FIGS. 18a through 18g are further provided for reference, and in combination constitute a detailed flowchart of the application of the invention as a system that induces the solution to problems by learning the structure and content of machine code entities. The entries in the flowchart use the terminology of this application and are believed to be self explanatory in the context of this application, and will not be described in detail. The mutation and crossover operators referred to in said FIG. 18g are the operators described elsewhere in this application.

FIG. 16a outlines the general operation of the system when it is applied to a generic machine learning problem.

FIG. 16b sets forth the details of the block entitled "SYSTEM DEFINITION" in FIG. 16a. The steps in this figure show, inter alia, what steps to take to analyze any machine learning problem to permit the designer to encode entities that contain both the Learned Elements and the

Conversion Elements into a machine code entity that can be created, initialized, stored, modified and executed by the means described in this application. Numeric or other values may be encoded in the machine code as constants.

FIG. 16c sets forth the details of the block entitled "INITIALIZATION" in FIG. 16a. This Figure sets forth, inter alia, a set of steps that will result in the creation of one or more learning entity or entities that will be the learning entity or entities in the machine learning system that is being implemented using the present invention. Such entity or entities will be created, stored, initialized, modified and executed by the methods set forth herein but when and how such steps take place will be set according to the requirements of the particular machine learning algorithm being implemented, as shown in FIG. 16d. It is important to note that the entity created according to the procedure outlined in FIG. 16c ordinarily includes not only the Conversion Elements but also contains the first set of Learning Elements for evaluation. Should said first set not be available when the initialization occurs, then the entity should be initialized with dummy values in the places in the instructions where the real Learning Elements will reside. Then, when the first set of real Learning Elements are known, it can be placed into those places using the procedure under "Start Modification" in FIG. 16d.

FIG. 16d sets forth the details of the block entitled "LEARN FOR ONE ITERATION" in FIG. 16a. This figure shows, inter alia, how to modify and how to evaluate an entity when the particular machine learning algorithm being implemented calls for either of those steps. The particular implementation of an application of the invention to a particular machine learning problem will vary substantially from problem to problem and among various machine learning systems. So this Figure is general in terms of when to evaluate the entity (referred to in FIGS. 16a-16d as a "solution") and when to modify the entity. Because of the breadth of various approaches to machine learning, this Figure indicates that steps other than the ones shown specifically are appropriate and that systems including such other steps are within the spirit and scope of the present invention.

FIG. 17a outlines the general operation of the invention when the invention is to be used to perform repeated computations on run-time data. This application of the invention could be handled in other and alternative manners both in the general matters set forth in FIG. 17a and in 17b through 17d and those other and alternative manners are within the scope and spirit of this invention.

FIG. 17b sets forth the details of the block entitled "SYSTEM DEFINITION" in FIG. 17a. This Figure shows, inter alia, how to define a repeated computation on run-time data problem so that it may be implemented using the invention. Numeric or other values may be encoded in the machine code as constants.

FIG. 17c sets forth the details of the block entitled "INITIALIZATION" in FIG. 17a. This Figure sets forth, inter alia, a set of steps that will result in the creation of a computational entity that will perform repeated computations on run-time data based on the system definition performed in FIG. 17b. It is important to note that the computation entity created ordinarily includes not only the related code but also contains the first set of run-time data on which the system will perform repeated calculations. Should said first set not be available when the initialization occurs, then the computational entity should be initialized with dummy values in the places in the instructions where the real run-time data will reside. Then, when the real run-time data

is known, it can be placed into those places using the procedure under "Start Modification" in FIG. 17d.

FIG. 17d sets forth the details of the block entitled "EVALUATE OR MODIFY FUNCTION" in FIG. 17a. The particular implementation of an application of the invention to repeated computations on run-time data will vary substantially from problem to problem. So this Figure is general in terms of when to execute the computational entity (referred to in FIGS. 17a-17d as a "solution") and when to modify the computational entity. The computational entity should be modified each time that the designer wishes to perform a particular computation (related code) on run-time data of the type that is encoded in the computational entity but that has not yet been placed in the computational entity. The computational entity should be executed every time the designer wants to perform a calculation on run-time data that has been encoded into the machine code of the computational entity.

FIG. 18a outlines the general operation of the invention when it is applied to learning machine code structures and machine code contents that will operate a register machine for the purpose of learning a solution to a problem. This application of the invention could be handled in other and alternative manners both in the general matters set forth in FIG. 18a and in 18b through 18h and those other and alternative manners are within the scope and spirit of this invention.

FIG. 18b sets forth the details of the block entitled "SETUP" in FIG. 18a. This Figure describes various steps necessary to setup an application of the invention to a CGPS run on a particular problem. Numeric or other values may be encoded in the machine code as constants.

FIG. 18c sets forth the details of the block entitled "INITIALIZATION" in FIG. 18a. This Figure describes, inter alia, a method for initializing a population of entities for the purpose of conducting a CGPS run.

FIG. 18d sets forth the details of the block entitled "CREATE INSTRUCTION" in FIG. 18c. This Figure describes, inter alia, one method of creating a single machine code instruction to be included in the body of an entity.

FIG. 18e sets forth the details of the block entitled "MAIN CGPS LOOP" in FIG. 18a. This Figure sets forth, inter alia, one approach to implementing the basic CGPS learning algorithm.

FIG. 18f sets forth the details of the block entitled "CALCULATE INDIV[N] FITNESS*" in FIG. 18e. The fitness function described therein is simple. More complex fitness functions may easily be implemented and are within the spirit and scope of this invention.

FIG. 18g sets forth the details of the block entitled "PERFORM GENETIC OPERATIONS . . ." in FIG. 18e. The mutation and crossover operators referred to in FIG. 18g may be all or any of the operators described elsewhere in this application.

FIG. 18h sets forth the details of the block entitled "DECOMPILE CHOSEN SOLUTION" in FIG. 18a. This Figure describes a method of converting an individual into a standard C language function that may then be linked and compiled into any C application. Other and more complex methods may be easily implemented and are within the spirit and scope of this invention.

In summary, the present invention overcomes the drawbacks of the prior art by eliminating all compiling, interpreting or other steps that are required to convert a high level programming language instruction such as a LISP S-expression into machine code prior to execution or that are required to access Learned Elements or run-time data in data structures.

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This makes possible the practical solutions to problems which could not heretofore be solved due to excessive computation time. For example, a solution to a difficult problem can be produced by the present system in hours, whereas a comparable solution might take years using conventional techniques.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

I claim:

1. A computer implemented learning method comprising the steps of:

- (a) providing a computer with an indirectly executable program including:
 - a first instruction that points to and designates machine code stored in a memory as data;
 - a second instruction that points to and designates machine code stored in a memory as directly executable code;
 - a third instruction that alters machine code pointed to by the first instruction; and
 - a fourth instruction that executes machine code pointed to by the second instruction; and
- (b) controlling the computer to execute the program which performs the steps of:
 - (b1) creating and storing a machine code entity including a directly executable instruction which includes run time data in a memory;
 - (b2) executing the second instruction to point to the entity;
 - (b3) executing the fourth instruction using input data to produce a result;
 - (b4) evaluating the result;
 - (b5) executing the first instruction to point to the entity;
 - (b6) executing the third instruction to alter the entity to include a different directly executable instruction; and
 - (b7) repeating steps (b3) to (b6) until an end criterion is reached.

2. A method as in claim 1, in which:

the first instruction points to and designates machine code stored in a memory as data by casting a pointer thereto as a data pointer; and

the second instruction points to and designates machine code stored in a memory as directly executable code by casting a pointer thereto as a function pointer.

3. A method as in claim 1, in which:

the first instruction points to and designates machine code stored in a memory as data by creating a data pointer thereto; and

the second instruction points to and designates machine code stored in a memory as directly executable code by creating a function pointer thereto.

4. A method as in claim 1, in which:

step (b1) comprises creating the entity as comprising a header and a footer; and
step (b6) comprises preventing the header and footer from being altered.

5. A method as in claim 1, in which:

step (b1) comprises creating the entity as comprising a return instruction; and
step (b6) comprises preventing the return instruction from being altered.

6. A method as in claim 1, in which the learning algorithm in step (b4) and the alteration algorithm in step (b6) in combination comprise a genetic algorithm.

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7. A method as in claim 1, in which step (b1) comprises creating the entity as comprising a plurality of directly executable instructions.

8. A method as in claim 7, in which step (b1) comprises randomly selecting the directly executable instructions from a set of directly executable instructions.

9. A method as in claim 7, in which step (b6) comprises genetically altering the directly executable instructions.

10. A method as in claim 7, in which:

one of the directly executable instructions comprises an operator and an operand; and

step (b6) comprises genetically mutating the operand.

11. A method as in claim 7, in which two of the directly executable instructions comprise operators respectively; and

step (b6) comprises genetically crossing the operators.

12. A method as in claim 1, in which: an array of directly executable functions; step (b1) comprises randomly selecting the directly executable instruction from a set of directly executable instructions.

13. A method as in claim 1, in which step (b6) comprises genetically altering the directly executable instruction.

14. A method as in claim 1, in which:

the directly executable instruction comprises an operator and an operand; and

step (b6) comprises genetically mutating the operand.

15. A computer implemented learning method comprising the steps of:

(a) providing a computer with an indirectly executable program; and

(b) controlling the computer to execute the program which performs the steps of:

(b1) creating a directly executable machine code entity including a directly executable program instruction which includes run time data and a directly executable return instruction;

(b2) executing the entity using input data to produce a result;

(b3) evaluating the result;

(b4) altering only the program instruction to include a different directly executable program instruction; and

(b6) repeating steps (b2) to (b4) until an end criterion is reached.

16. A method as in claim 15, in which step (b4) comprises preventing the return instruction from being altered.

17. A method as in claim 15, in which step (b4) comprises allowing the return instruction to be altered, and then restoring the return instruction to its original state.

18. A method as in claim 15, in which step (b4) comprises separating the program instruction from the entity, altering the program instruction to include the different program instruction, and returning the different program instruction to the entity.

19. A method of manipulating and executing computer machine code, comprising the steps of:

(a) providing a computer with an indirectly executable program including:

a first instruction that points to and designates machine code stored in a memory as data;

a second instruction that points to and designates machine code stored in a memory as directly executable code;

a third instruction that alters machine code pointed to by the first instruction; and

a fourth instruction that executes machine code pointed to by the second instruction; and

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- (b) controlling the computer to execute the program which performs the steps of:
- (b1) creating and storing a machine code entity including a directly executable instruction which includes run time data in a memory;
 - (b2) executing the second instruction to point to the entity;
 - (b3) executing the fourth instruction to execute the entity;
 - (b4) executing the first instruction to point to the entity; and
 - (b5) executing the third instruction to alter the entity to include a different directly executable instruction.
20. A method as in claim 19, in which:
- step (b1) comprises creating the entity as including a directly executable program instruction and a directly executable return instruction; and
- step (b5) comprises preventing the return instruction from being altered.
21. A computer learning system comprising:
- a memory for storing an indirectly executable computer program including:
 - a first instruction that points to and designates machine code stored in the memory as data;
 - a second instruction that points to and designates machine code stored in the memory as directly executable machine code;
 - a third instruction that alters machine code pointed to by the first instruction; and
 - a fourth instruction that executes machine code pointed to by the second instruction; and
 - a processor for executing the program;
- the processor, memory and program operating in combination for performing the steps of:
- (a) creating and storing a machine code entity including a directly executable instruction which includes run time data in the memory;
 - (b) executing the second instruction to point to the entity;
 - (c) executing the instruction using input data to produce a result;
 - (d) evaluating the result;
 - (e) executing the first instruction to point to the entity;
 - (f) executing the third instruction to alter the entity using an alteration algorithm to include a different directly executable instruction; and
 - (g) repeating steps (b) to (f) until an end criterion is reached.
22. A system as in claim 21, in which:
- the first instruction points to and designates machine code stored in the memory as data by casting a pointer thereto as a data pointer; and
- the second instruction points to and designates machine code stored in the memory as directly executable code by casting a pointer thereto as a function pointer.
23. A system as in claim 21, in which:
- the first instruction points to and designates machine code stored in the memory as data by creating a data pointer thereto; and
- the second instruction points to and designates machine code stored in the memory as directly executable code by creating a function pointer thereto.
24. A system as in claim 21, in which:
- step (a) comprises creating the entity as comprising a header and a footer; and

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- step (f) comprises preventing the header and footer from being altered.
25. A system as in claim 21, in which:
- step (a) comprises creating the entity as comprising a return instruction; and
 - step (f) comprises preventing the return instruction from being altered.
26. A system as in claim 21, in which the learning algorithm in step (d) and the alteration algorithm in step (f) in combination comprise a genetic algorithm.
27. A system as in claim 21, in which step (a) comprises creating the entity as comprising a plurality of directly executable instructions.
28. A system as in claim 27, in which step (a) comprises randomly selecting the directly executable instructions from a set of directly executable instructions.
29. A system as in claim 27, in which step (f) comprises genetically altering the directly executable instructions.
30. A system as in claim 27, in which:
- one of the directly executable instructions comprises an operator and an operand; and
 - step (f) comprises genetically mutating the operand.
31. A system as in claim 27, in which two of the directly executable instructions comprise operators respectively; and step (f) comprises genetically crossing the operators.
32. A system as in claim 21, in which: step (a) comprises randomly selecting the directly executable instruction from a set of directly executable instructions.
33. A system as in claim 21, in which step (f) comprises genetically altering the directly executable instruction.
34. A system as in claim 21, in which:
- the directly executable instruction comprises an operator and an operand; and
 - step (f) comprises genetically mutating the operand.
35. A system as in claim 21, in which:
- the memory comprises a main memory and a processor memory that is part of the processor; and
 - step (a) comprises storing the entity in the processor memory.
36. A system as in claim 35, comprising an integrated circuit chip, in which the processor and the processor memory are formed on the chip.
37. A system as in claim 36, in which at least a portion of the program is stored processor memory.
38. A system as in claim 37, in which:
- the processor memory comprises a non-volatile memory section; and
 - said at least a portion of the program is stored in the non-volatile memory section.
39. A method of creating and executing machine code for learning using a digital computer which includes a processor and a memory, comprising the steps of:
- (a) selecting a directly executable machine code program instruction which includes run time data;
 - (b) determining a binary number which represents the program instruction to the processor;
 - (c) selecting a location in the memory;
 - (d) creating a directly executable machine code entity which includes the binary number;
 - (e) storing the entity as data in said location;
 - (f) providing an indirectly executable instruction which causes the processor to directly execute machine code stored in said location; and
 - (g) controlling the processor to process the indirectly executable instruction, resulting in the processor directly executing the entity as including the program instruction.

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40. A method as in claim 39, in which step (f) comprises providing the indirectly executable instruction such that said processing thereof in step (g) includes compiling.

41. A method as in claim 39, in which step (f) comprises providing the indirectly executable instruction such that said processing thereof in step (g) includes interpreting.

42. A method as in claim 39, in which step (f) comprises creating the indirectly executable instruction such that said processing thereof in step (g) includes assembling.

43. A method as in claim 39, further comprising the step of:

(h) repeating step (g) at least one time.

44. A method as in claim 39, further comprising the step of:

(h) evaluating a result produced by executing the program instruction in step (g).

45. A method as in claim 39, further comprising the step, performed after step (g), of:

(h) altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor.

46. A method as in claim 45, further comprising the step, performed after step (h), of:

(i) controlling the processor to process the indirectly executable instruction, resulting in the processor directly executing the entity as including the program instruction.

47. A method as in claim 46, further comprising the step of:

(j) evaluating a result produced by executing the program instruction in step (i).

48. A method as in claim 39, further comprising the steps, performed after step (g), of:

(h) copying the entity to produce a copied entity; and
(i) altering the copied entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor.

49. A method as in claim 39, further comprising the steps of:

(h) evaluating a result produced by executing the program instruction in step (g);

(i) altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor;

(j) controlling the processor to process the indirectly executable instruction, resulting in the processor directly executing the entity as including the program instruction; and

(k) evaluating a result produced by executing the program instruction in step (j).

50. A method as in claim 49, further comprising the step of:

(l) comparing the evaluation of step (k) with the evaluation of step (h).

51. A method as in claim 50, further comprising the step of:

(m) selecting a subsequent action in accordance with said comparison of step (l).

52. A method as in claim 39, in which step (d) comprises creating the entity to further include a return instruction.

53. A method as in claim 52, further comprising the steps, performed after step (g), of:

(h) altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor; and

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(i) preventing the return instruction from being altered while performing step (h).

54. A method as in claim 52, further comprising the steps, performed after step (g), of:

(h) altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor, and the return instruction is allowed to be altered; and

(i) restoring the return instruction to original state after alteration in step (h).

55. A method as in claim 39, in which step (d) comprises creating the entity to further include at least one of a header and a footer.

56. A method as in claim 55, further comprising the steps, performed after step (g), of:

(h) altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor; and

(i) preventing said at least one of a header and a footer from being altered while performing step (h).

57. A method as in claim 55, further comprising the steps, performed after step (g), of:

(h) altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor, and said at least one of a header and a footer is allowed to be altered; and

(i) restoring said at least one of a header and a footer to original state after alteration in step (h).

58. A method as in claim 55, further comprising the steps, performed after step (g), of:

(h) separating the binary number from the entity;

(i) altering the binary number to produce a different binary number which represents a different directly executable machine code program instruction to the processor; and
(j) replacing the binary number with the different binary number in the entity.

59. A method as in claim 39, further comprising the step, performed after step (g), of:

(h) altering the entity as data such that the run time data is changed.

60. A method as in claim 59, further comprising the step, performed after step (h), of:

(i) controlling the processor to process the indirectly executable instruction, resulting in the processor directly executing the entity as including the program instruction.

61. A method as in claim 60, in which step (h) further comprises altering the entity as data such that the binary number is changed to represent a different directly executable machine code program instruction to the processor.

62. A method as in claim 60, further comprising the step of:

(j) evaluating a result produced by executing the program instruction in step (i).

63. A method as in claim 39, further comprising the steps, performed after step (g), of:

(h) copying the entity to produce a copied entity; and

(i) altering the copied entity as data such that the run time data is changed.

64. A method as in claim 39, further comprising the steps of:

(h) evaluating a result produced by executing the program instruction in step (g);

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- (i) altering the entity as data such that the run time data is changed;
- (j) controlling the processor to process the indirectly executable instruction, resulting in the processor directly executing the entity as including the program instruction; and
- (k) evaluating a result produced by executing the program instruction in step (j).
- 65. A method as in claim 64, further comprising the step of:
 - (l) comparing the evaluation of step (k) with the evaluation of step (h).
- 66. A method as in claim 65, further comprising the step of:
 - (m) selecting a subsequent action in accordance with said comparison of step (l).
- 67. A method as in claim 39, in which step (a) comprises selecting the program instruction from a set of directly executable program instructions.
- 68. A method as in claim 39, further comprising the step, performed before step (a), of:
 - selecting a subset of program instructions from a set of directly executable program instructions; and
 - step (a) comprises selecting the program instruction from said subset.
- 69. A method as in claim 39, in which:
 - step (d) comprises creating the program instruction to include run time data; and
 - the method further comprises the step of:
 - (h) repeating step (g) for different input values of the run time data.
- 70. A method as in claim 69, further comprising the step of:
 - (i) determining a value of the run time data which produces a predetermined result.
- 71. A method as in claim 69, in which step (h) further comprises repeating step (g) for different program instructions.
- 72. A method as in claim 39, in which the method further comprises the step, performed after step (g), of:
 - (h) creating a representation of the entity in a selected computer programming language.
- 73. A method as in claim 72, in which step (h) comprises decompiling the entity.
- 74. A method as in claim 39, in which
 - the method further comprises the steps of:
 - (h) determining if execution of step (g) produced a predetermined result; and
 - (i) if step (g) produced said predetermined result, creating a representation of the entity including said input value of the run time data in a selected computer programming language.
- 75. A method as in claim 74, further comprising the step of:
 - (j) repeating step (g) for different input values of the run time data;
 - (k) determining a value of the run time data which produced a predetermined result; and
 - (l) creating a representation of the entity including said value of the run time data which produced the predetermined result in a selected computer programming language.
- 76. A method as in claim 39, in which
 - the method further comprises the step of:

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- (h) repeating step (g) on the run time data a plurality of times.
- 77. A method as in claim 76, further comprising the steps of:
 - (i) altering the run time data; and
 - (j) repeating step (g) on the run time data which was altered in step (i) a plurality of times.
- 78. A method as in claim 39, in which step (d) comprises creating the entity to further include additional run time data.
- 79. A method as in claim 39, in which step (d) comprises creating the program instruction to further include related code which operates on the run time data.
- 80. A method as in claim 39, in which
 - step (d) comprises creating the entity such that the program instruction includes a learned element.
- 81. A method as in claim 80, in which step (d) comprises creating the entity to further include an additional learned element.
- 82. A method as in claim 80, in which the method performs more than one calculation on the learned element.
- 83. A method as in claim 39, in which
 - step (d) comprises creating the entity to further include a learned element, and creating the program instruction to include a conversion element which operates on the learned element.
- 84. A method as in claim 83, in which the method performs more than one calculation on the learned element.
- 85. A method as in claim 39, in which:
 - the computer comprises a plurality of registers;
 - the method further comprises the step, performed prior to step (d), of:
 - (h) designating one of the registers as an input register for execution of the entity by the processor; and
 - step (d) comprises creating the entity to further include a section of directly executable code which, upon execution thereof during step (g), causes the processor to store input data in the input register prior to execution of the program instruction.
- 86. A method as in claim 85, further comprising the step, performed prior to step (d), of:
 - (i) storing the input data in the memory;
 - in which the directly executable code in said section causes the processor to transfer the input data from the memory to the input register.
- 87. A method as in claim 85, in which said section comprises a header of the entity.
- 88. A method as in claim 85, further comprising the step of:
 - (i) preventing said section from being altered while performing step (g).
- 89. A method as in claim 39, in which:
 - the computer comprises a plurality of registers;
 - the method further comprises the step, performed prior to step (d), of:
 - (h) designating one of the registers as a calculation register for execution of the entity by the processor; and
 - step (d) comprises creating the entity to further include a section of directly executable code which causes the processor to store a predetermined value in the calculation register prior to execution of the program instruction.
- 90. A method as in claim 39, in which:
 - the computer comprises a plurality of registers;
 - the method further comprises the step, performed prior to step (d), of:

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(h) designating one of the registers as a state register for execution of the entity by the processor; and
 step (d) comprises creating the entity to further include a section of directly executable code which causes the processor to store a state value which was produced by a previous execution of the program instruction in the state register prior to execution of the program instruction.

91. A method as in claim 90, in which:

the state value is stored in the memory prior to executing step (g); and

the directly executable code in said section causes the processor to transfer the state value from the memory to the state register.

92. A method as in claim 39, in which:

the computer comprises a plurality of registers;

the method further comprises the step, performed prior to step (d), of:

(h) designating one of the registers as an output register for execution of the entity by the processor; and
 step (d) comprises creating the entity to further include a section of directly executable code which, upon execution thereof during step (g), causes the processor to store output run time data which is produced by execution of the program instruction in the output register.

93. A method as in claim 92, in which the directly executable code in said section further causes the processor to transfer the output run time data from the output register to the memory.

94. A method as in claim 92, in which said section comprises a footer of the entity.

95. A method as in claim 92, further comprising the step of:

(i) preventing said section footer from being altered while performing step (g).

96. A method as in claim 39, in which:

the computer comprises a plurality of registers;

the method further comprises the step, performed prior to step (d), of:

(h) designating one of the registers as a calculation register for execution of the entity by the processor; and

step (d) comprises creating the entity to further include a first instruction which causes the processor to read a calculation value which was produced by a previous execution of the program instruction from the calculation register; and a second instruction which causes the processor to store a calculation value produced by a current execution of the program instruction in the calculation register.

97. A method as in claim 96, in which the first instruction causes the processor to transfer the calculation value from the calculation register to the memory.

98. A method as in claim 39, in which:

the computer comprises a plurality of registers;

the method further comprises the step, performed prior to step (d), of:

(h) designating one of the registers as a state register for execution of the entity by the processor; and
 step (d) comprises creating the entity to further include a section of directly executable code which causes the processor to store a state value which is produced by execution of the program instruction in the state register.

99. A method as in claim 98, in which in which the directly executable code in said section further causes the processor to transfer the state value from the state register to the memory.

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100. A method as in claim 39, in which:

the computer comprises a plurality of registers; and

the method further comprises the step, performed prior to step (b), of:

(h) designating one of the registers as an input register for execution of the entity by the processor.

101. A method as in claim 100, in which step (f) comprises providing the indirectly executable instruction such that the processor will store input data in the input register prior to execution of the program instruction.

102. A method as in claim 39, in which:

the computer comprises a plurality of registers; and

the method further comprises the step, performed prior to step (b); of:

(h) designating one of the registers as a calculation register for execution of the entity by the processor.

103. A method as in claim 102, in which step (f) comprises providing the indirectly executable instruction such that the processor will store a predetermined value in the calculation register prior to execution of the program instruction.

104. A method as in claim 39, in which:

the computer comprises a plurality of registers; and

the method further comprises the step, performed prior to step (b); of:

(h) designating one of the registers as a state register for execution of the entity by the processor.

105. A method as in claim 104, in which step (f) comprises providing the indirectly executable instruction such that the processor will store a state value which was produced by execution of a previous program instruction in the state register prior to execution of the program instruction.

106. A method as in claim 39, in which:

the computer comprises a plurality of registers; and

the method further comprises the step, performed prior to step (b); of:

(h) designating one of the registers as an output register for execution of the entity by the processor.

107. A method as in claim 106, in which step (f) comprises providing the indirectly executable instruction such that the processor will store output data which is produced by execution of the program instruction in the output register.

108. A method as in claim 107, in which step (f) comprises providing the indirectly executable instruction such that the output data is stored in the output register as a return value of the indirectly executable instruction.

109. A method as in claim 39, in which step (d) comprises the substeps of:

(d1) creating the entity to further include a header and a footer; and

(d2) creating a leaf function which includes the program instruction, is pointed to by the header, and returns to the footer upon execution of the entity.

110. A method as in claim 109, in which step (d2) comprises creating the leaf function to further include a return instruction.

111. A method as in claim 109, further comprising the step of:

(h) altering the leaf function as data without altering the header and the footer such that the binary number is changed to represent a different directly executable machine code program instruction to the processor.