CPE301 – SPRING 2019

Design Assignment 2C

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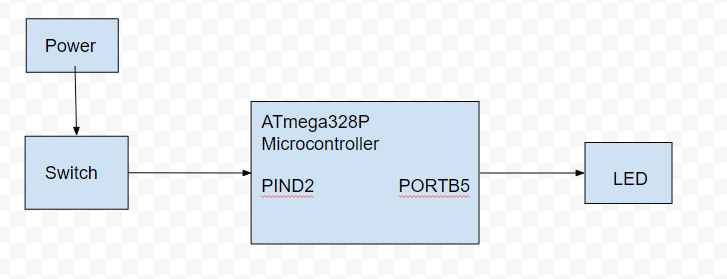
Student Email: kengneta@unlv.nevada.edu

Primary Github address: vasty1995

Directory: https://github.com/Vasty1995/submission\_da

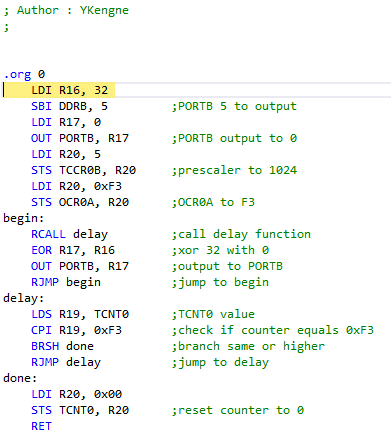
Submit the following for all Labs:

1. Implement Design Assignment 2A using Timer 0 – normal mode. Count OVF occurrence if needed. Do not use interrupts.
2. Implement Design Assignment 2A using TIMER0\_OVF\_vect interrupt mechanism in normal mode.
3. Implement Design Assignment 2A using TIMER0\_COMPA\_vect interrupt mechanism in CTC mode.
4. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

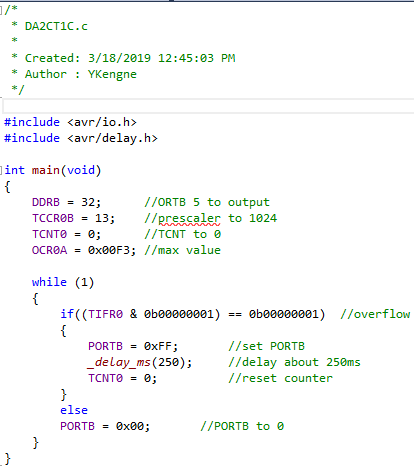


1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1**

Task 1 Assembly Code:



Task 1 C Code:

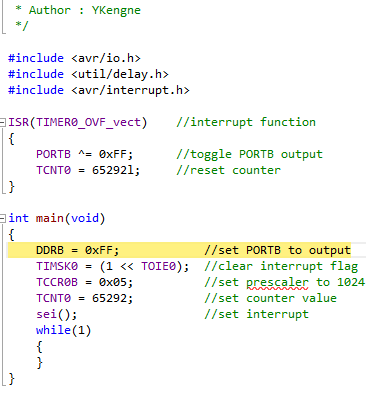


1. **DEVELOPED MODIFIED CODE OF TASK 2 from TASK 1**

Task 2 A Code:

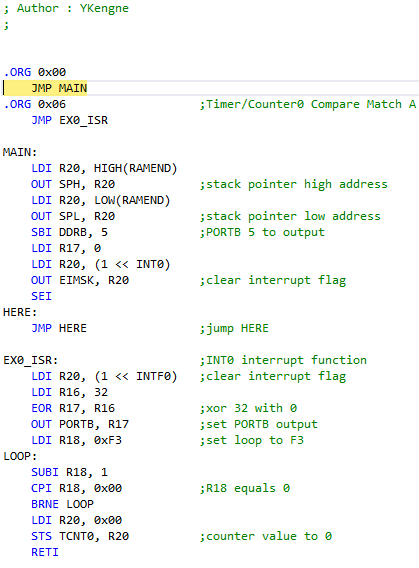


Task 2 C Code:

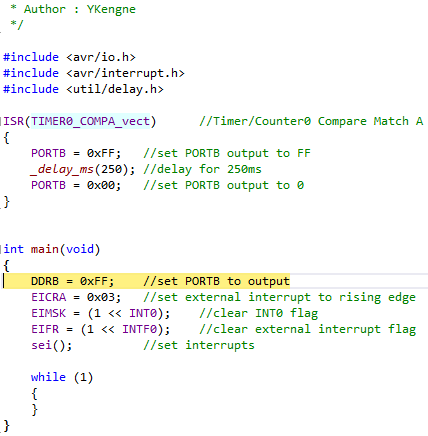


1. **DEVELOPED MODIFIED CODE OF TASK 3 from TASK 2**

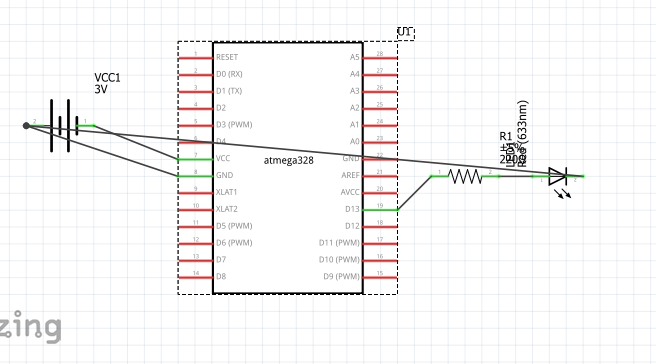
Task 3 A Code:

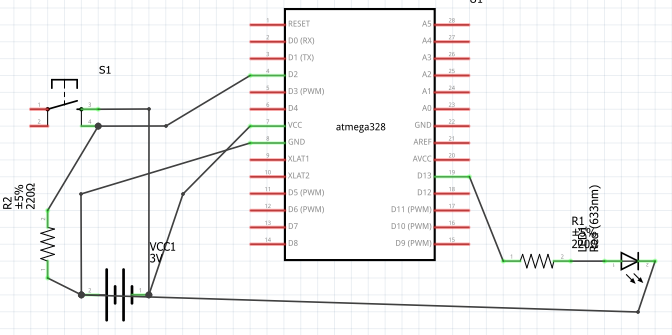


Task 3 C Code:



1. **SCHEMATICS**





1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**

Task 1:

Assembly:

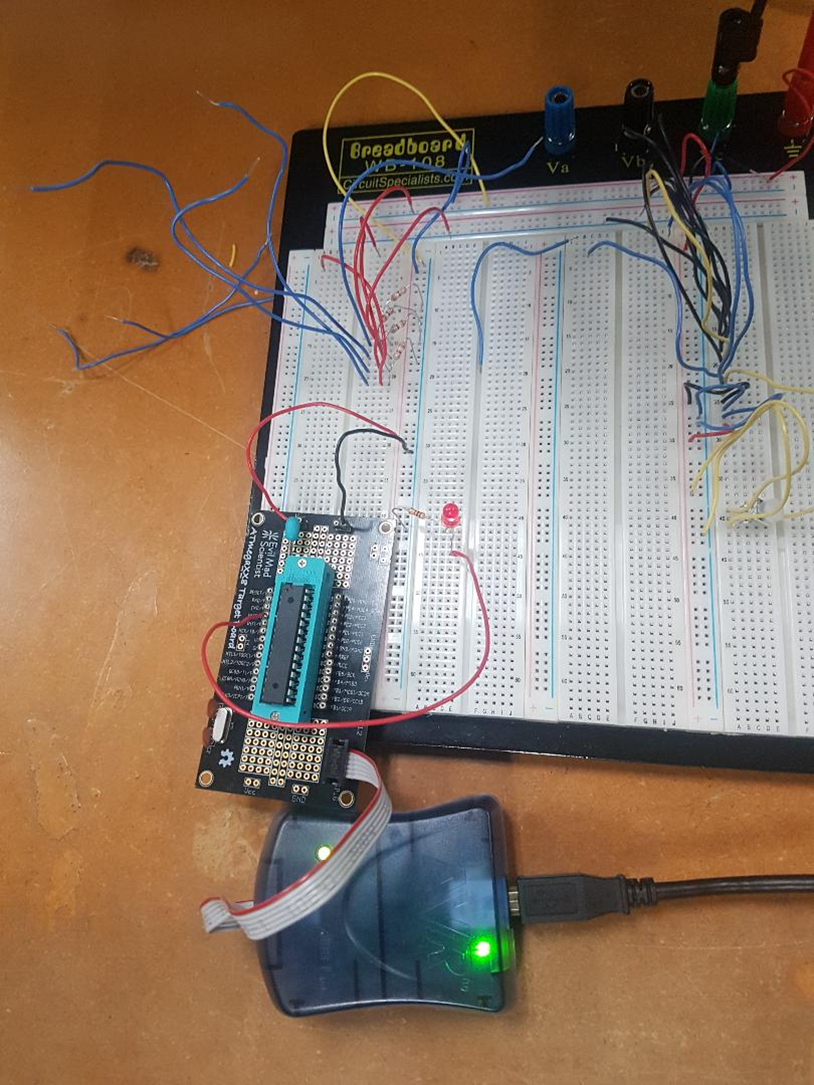


C:



1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**

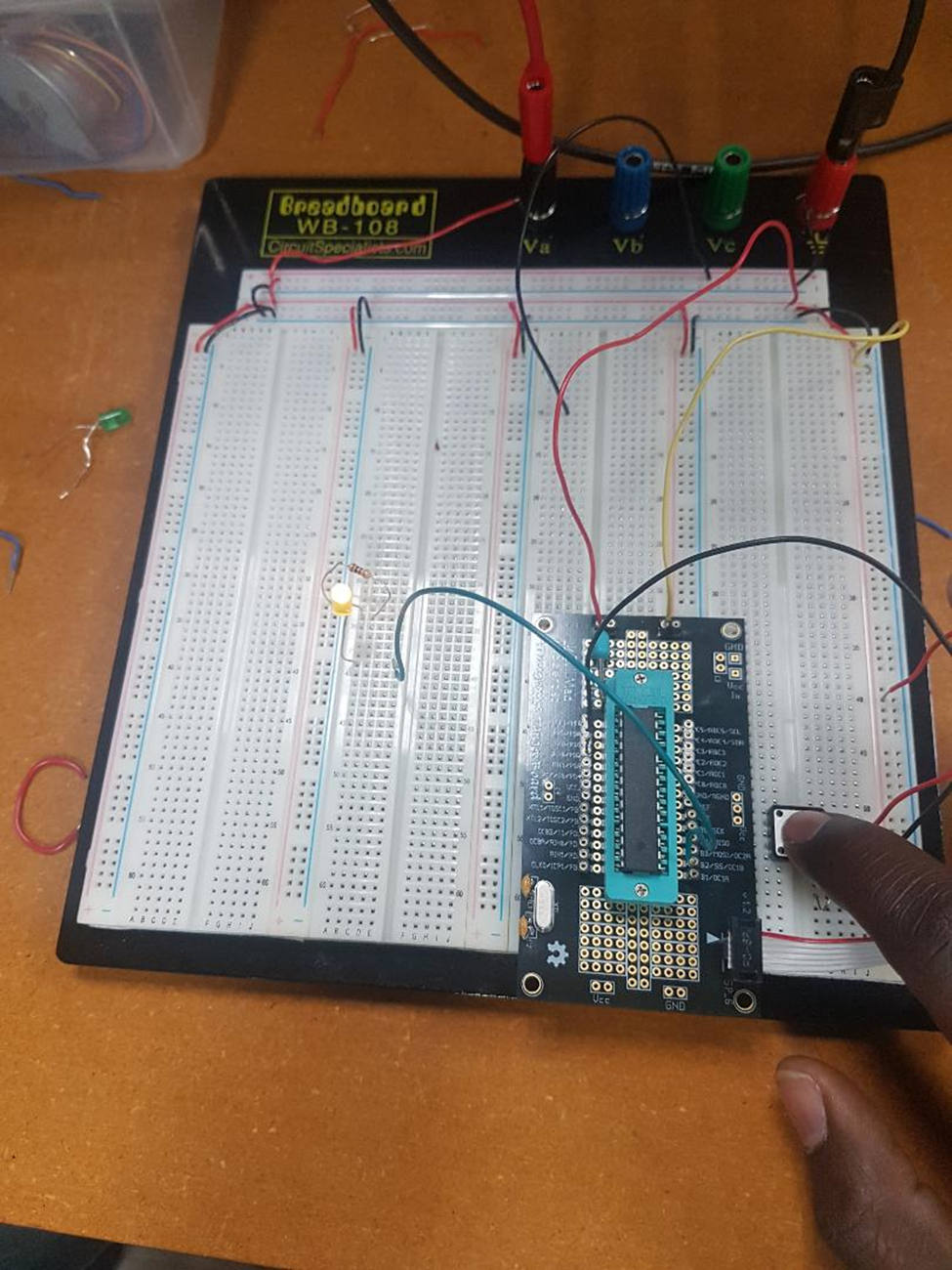
TASK 1:



TASK 2:



TASK 3:



1. **VIDEO LINKS OF EACH DEMO**

<https://youtu.be/GTSQulz4by8>

<https://youtu.be/jT_ADkS-RB0>

<https://youtu.be/Kj-vRlfve_Y>

1. **GITHUB LINK OF THIS DA**

https://github.com/Vasty1995/submission\_da

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Yannick Kengne Tatcha