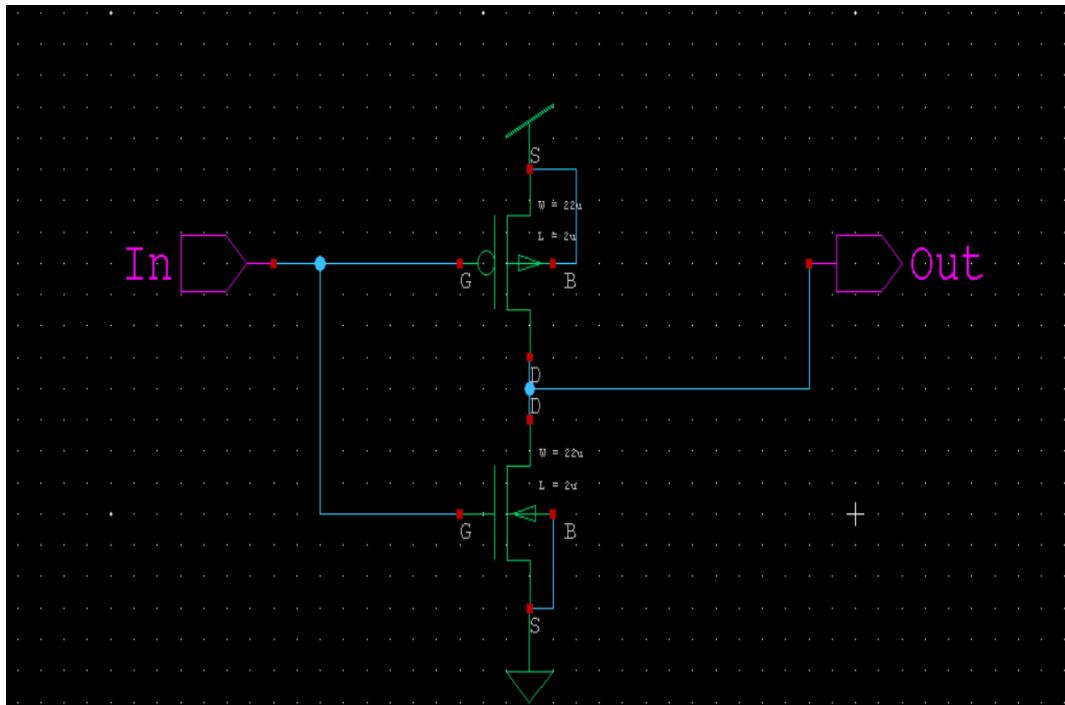


# ALL Tanner Tools Projects

## INVERTER

### S-EDIT



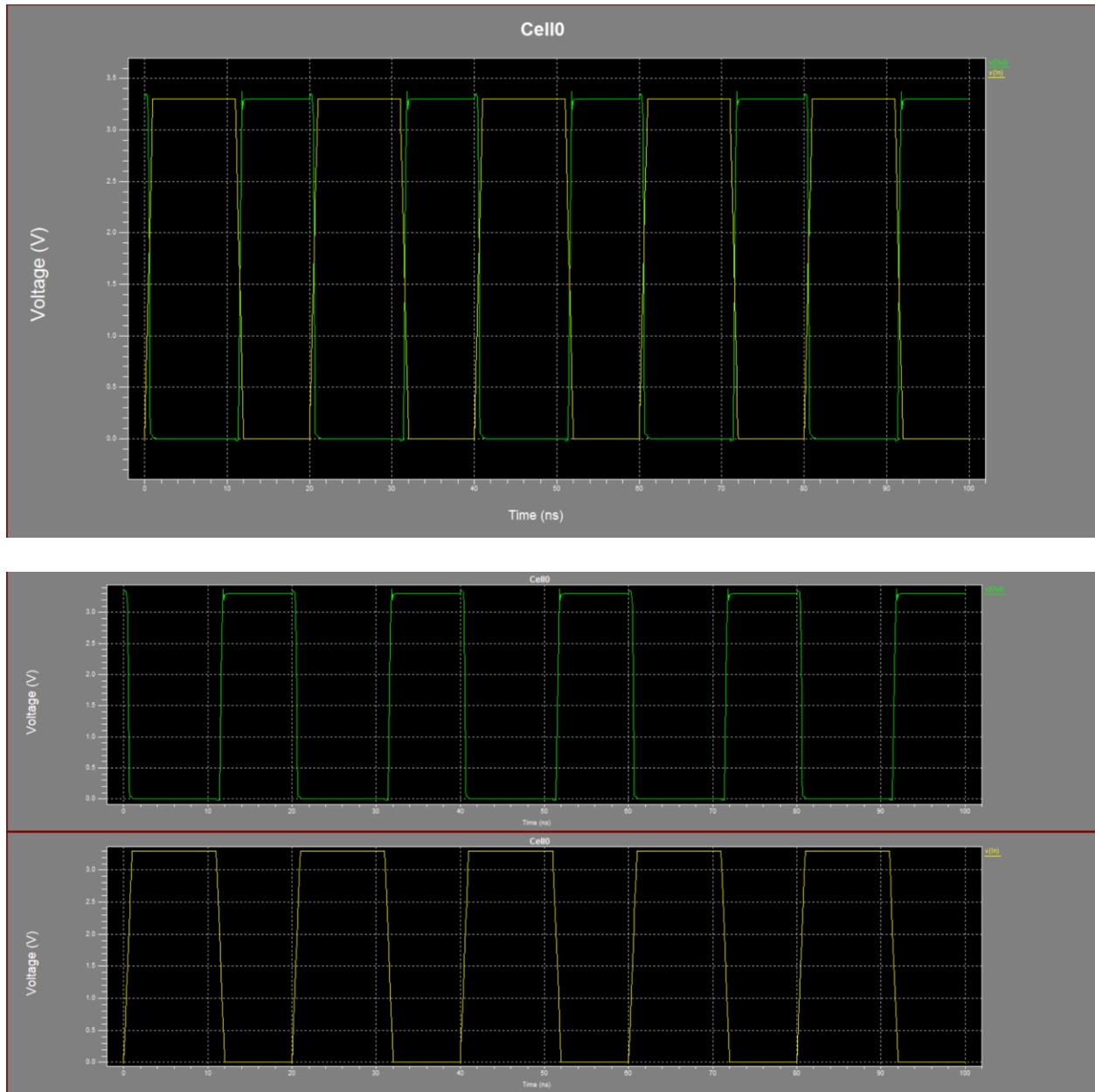
### T – SPICE

```
***** Simulation Settings - General section *****

***** Simulation Settings - Parameters and SPICE Options *****

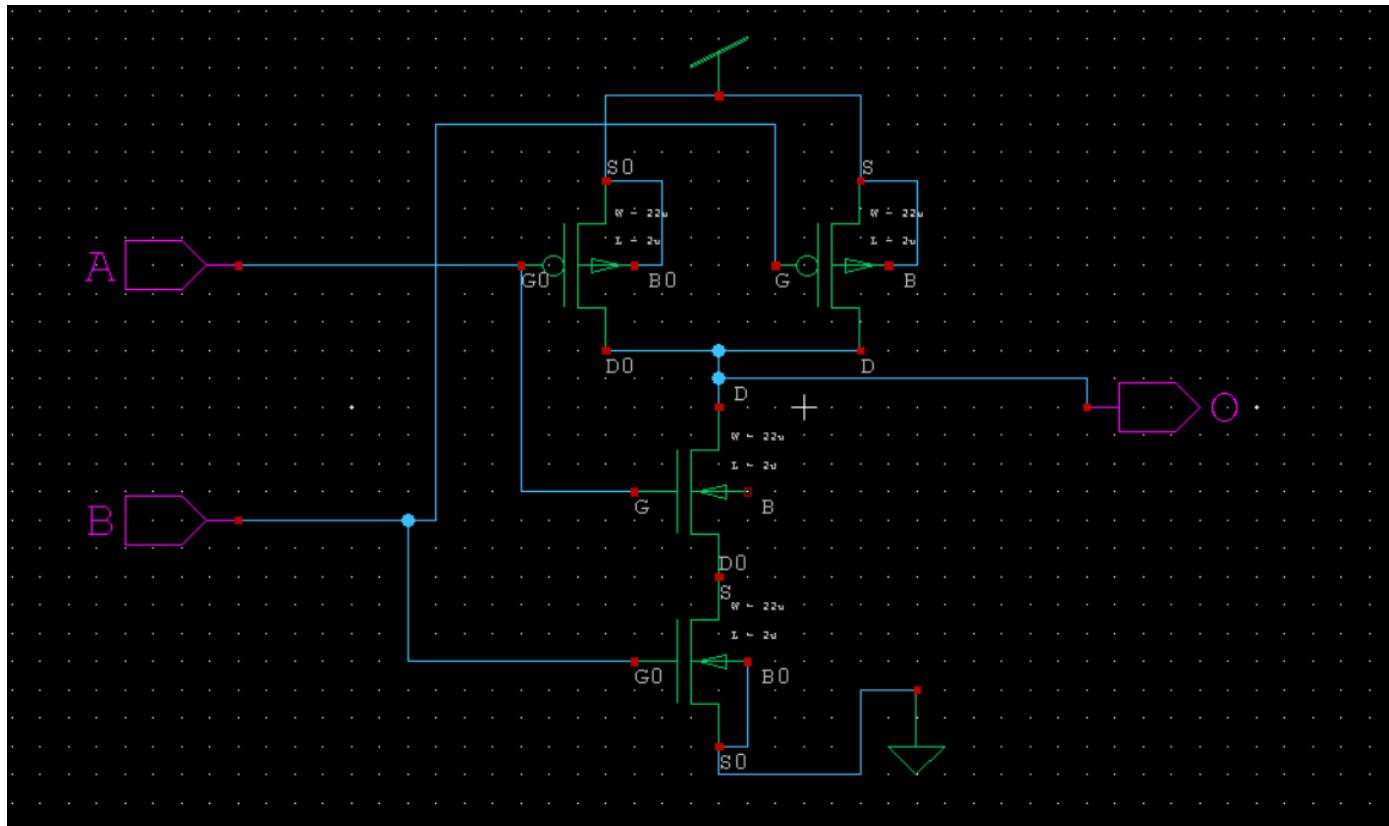
MMOSFET_N_1 Out In Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 Out In Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
**1
Vdd Vdd Gnd 3.3V
**2
Vin In Gnd pulse(0 3.3v 0 1n 1n 10n 20n)
**3
.tran lns 100ns
**4
.print V(In) V(Out)
.end
```

## W-EDIT WAVEFORM



# NAND GATE

## S-EDIT



## T-SPICE

```
***** Simulation Settings - General section *****

***** Simulation Settings - Parameters and SPICE Options *****

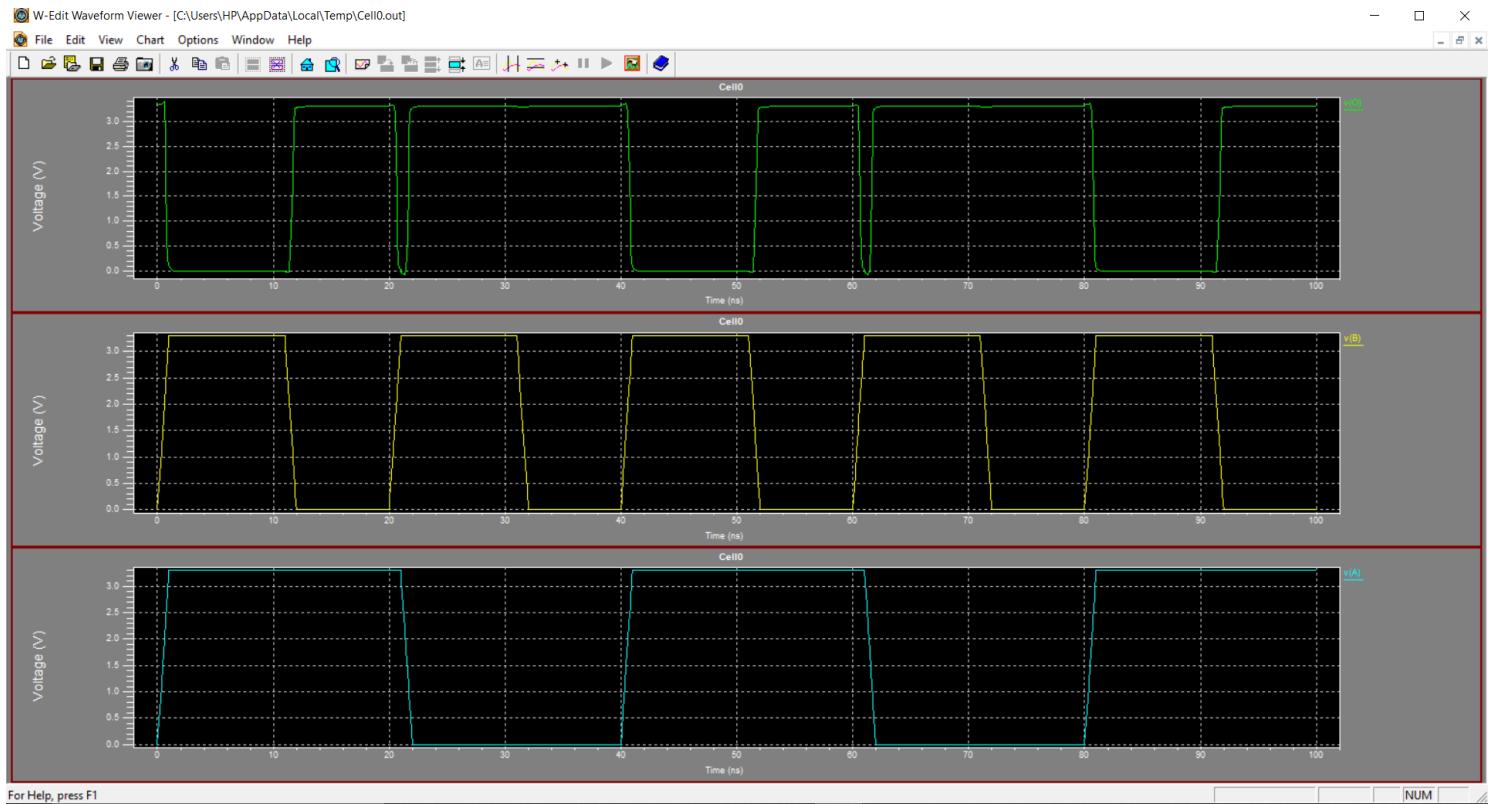
MMOSFET_N_1 Out A N_2 N_1 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 N_2 B Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 Out A Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 Out B Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 3.3V
Vin1 A Gnd pulse(0 3.3v 0 1n 1n 20n 40n)
Vin2 B Gnd pulse(0 3.3v 0 1n 1n 10n 20n)
.Tran lns 100ns
**.power Vdd A 10000ns
.print V(A) V(B) V(C)

***** Simulation Settings - Additional SPICE commands *****

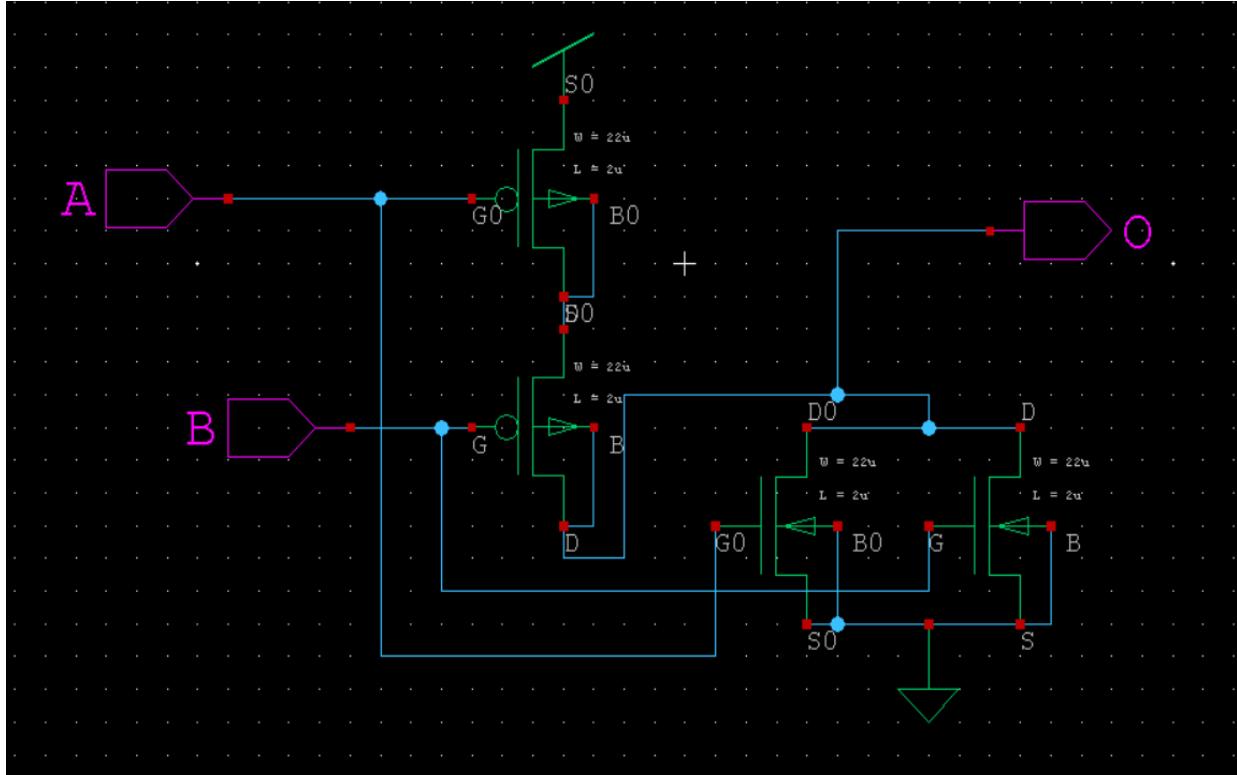
.end
```

# W-EDIT WAVEFORM



# NOR GATE

## S-EDIT



## T-SPICE

```
***** Simulation Settings - General section *****

***** Simulation Settings - Parameters and SPICE Options *****

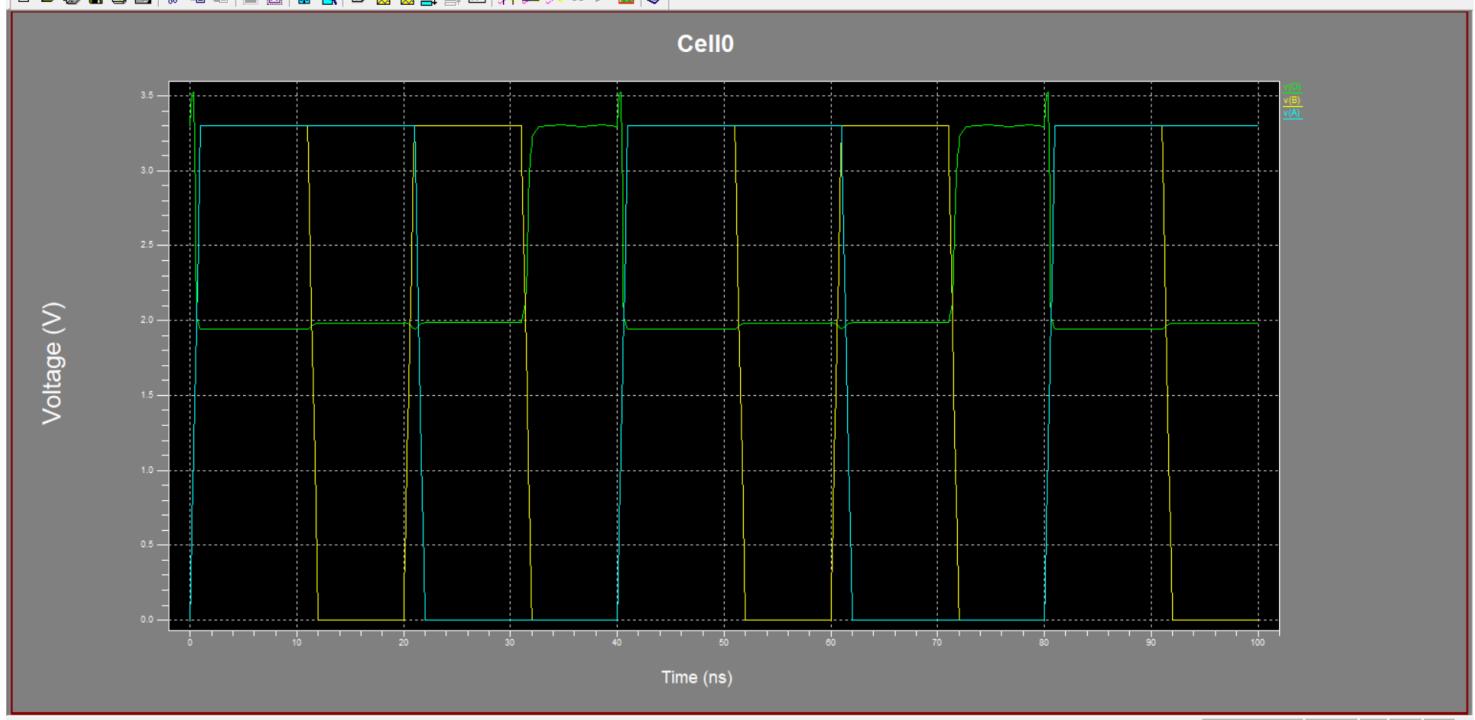
MMOSFET_N_1 C A Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 C B Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 N_1 A Vdd N_1 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 C B N_1 C PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 3.3V
Vin1 A Gnd pulse(0 3.3v 0 1n 1n 20n 40n)
Vin2 B Gnd pulse(0 3.3v 0 1n 1n 10n 20n)
.Tran 1ns 100ns
**.dc Vin 0 3.3v 1.1v
**.power Vdd 1n 10000ns
.print V(A) V(B) V(C)
.end
***** Simulation Settings - Additional SPICE commands *****
```

## W-EDIT WAVEFORM

W-Edit Waveform Viewer - [D:\3 - 1\ECE-390 (Workshop on analog design)\NOR using CMOS\Cell0.out]

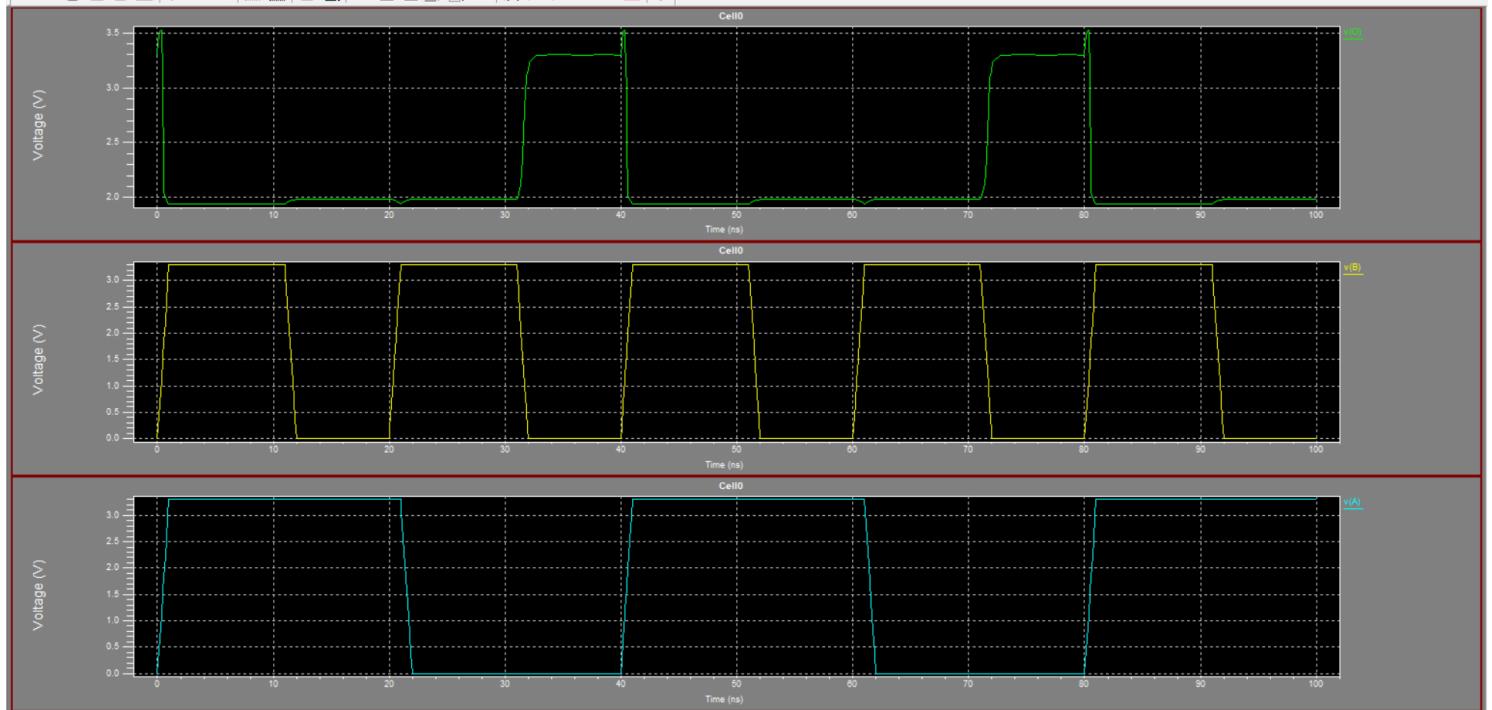
File Edit View Chart Options Window Help



For Help, press F1

W-Edit Waveform Viewer - [D:\3 - 1\ECE-390 (Workshop on analog design)\NOR using CMOS\Cell0.out]

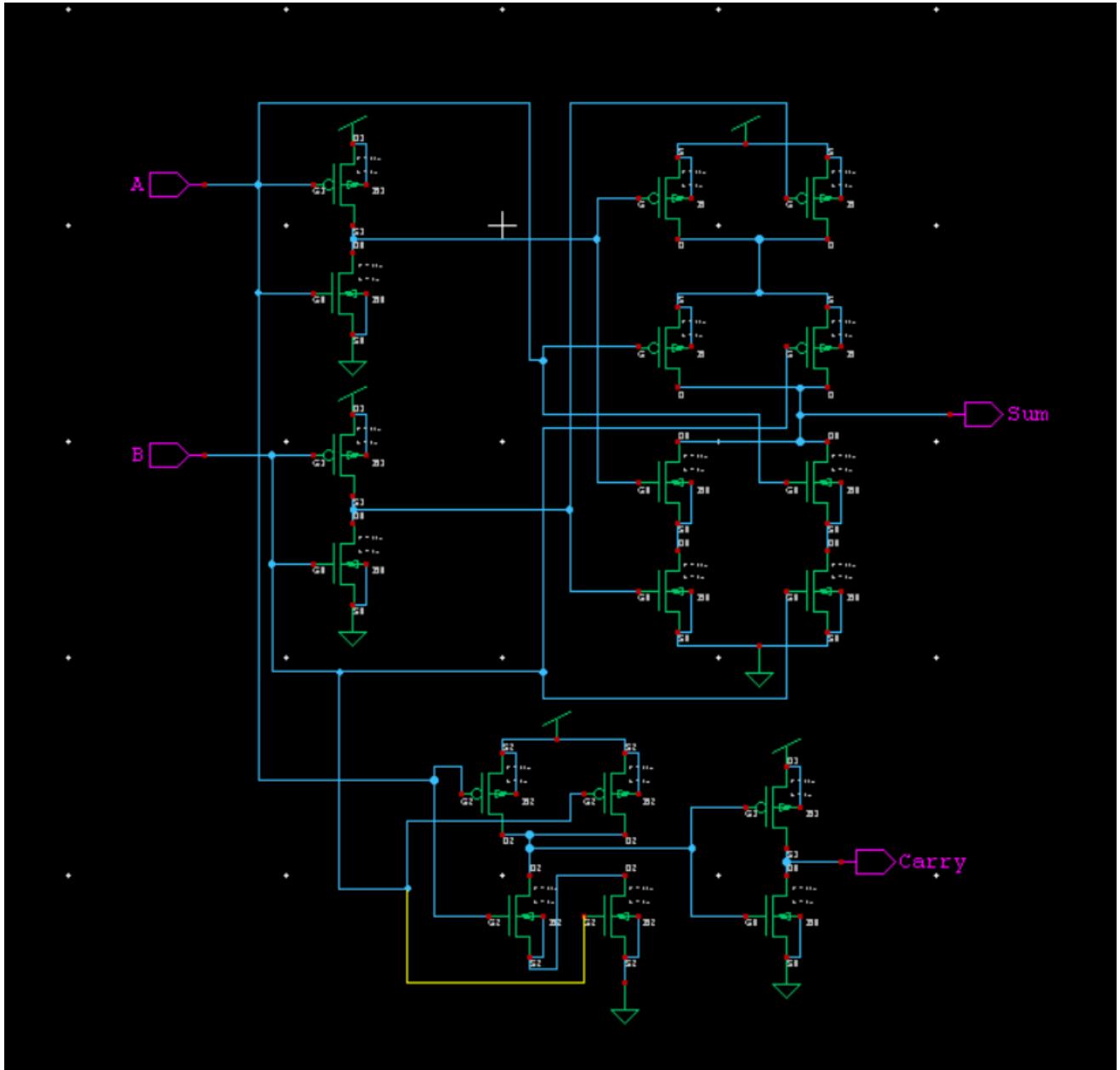
File Edit View Chart Options Window Help



For Help, press F1

## HALF ADDER

S-EDIT



## T-SPICE

\*\*\*\*\* Simulation Settings - Parameters and SPICE Options \*\*\*\*\*

```

MMOSFET_N_1 N_1 A Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 N_1 A Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_5 N_14 N_4 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_6 N_17 B Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 N_4 B Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_3 N_8 N_1 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_4 N_8 N_4 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_5 Sum A N_8 N_8 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_6 Sum B N_8 N_8 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 N_4 B Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_3 Sum N_1 N_14 N_14 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_4 Sum A N_17 N_17 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_7 N_3 A Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_7 N_3 A N_2 N_2 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_8 N_2 B Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_8 N_3 B Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_9 Carry N_3 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_9 Carry N_3 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

```

\*\*\*\*\* Simulation Settings - Analysis section \*\*\*\*\*

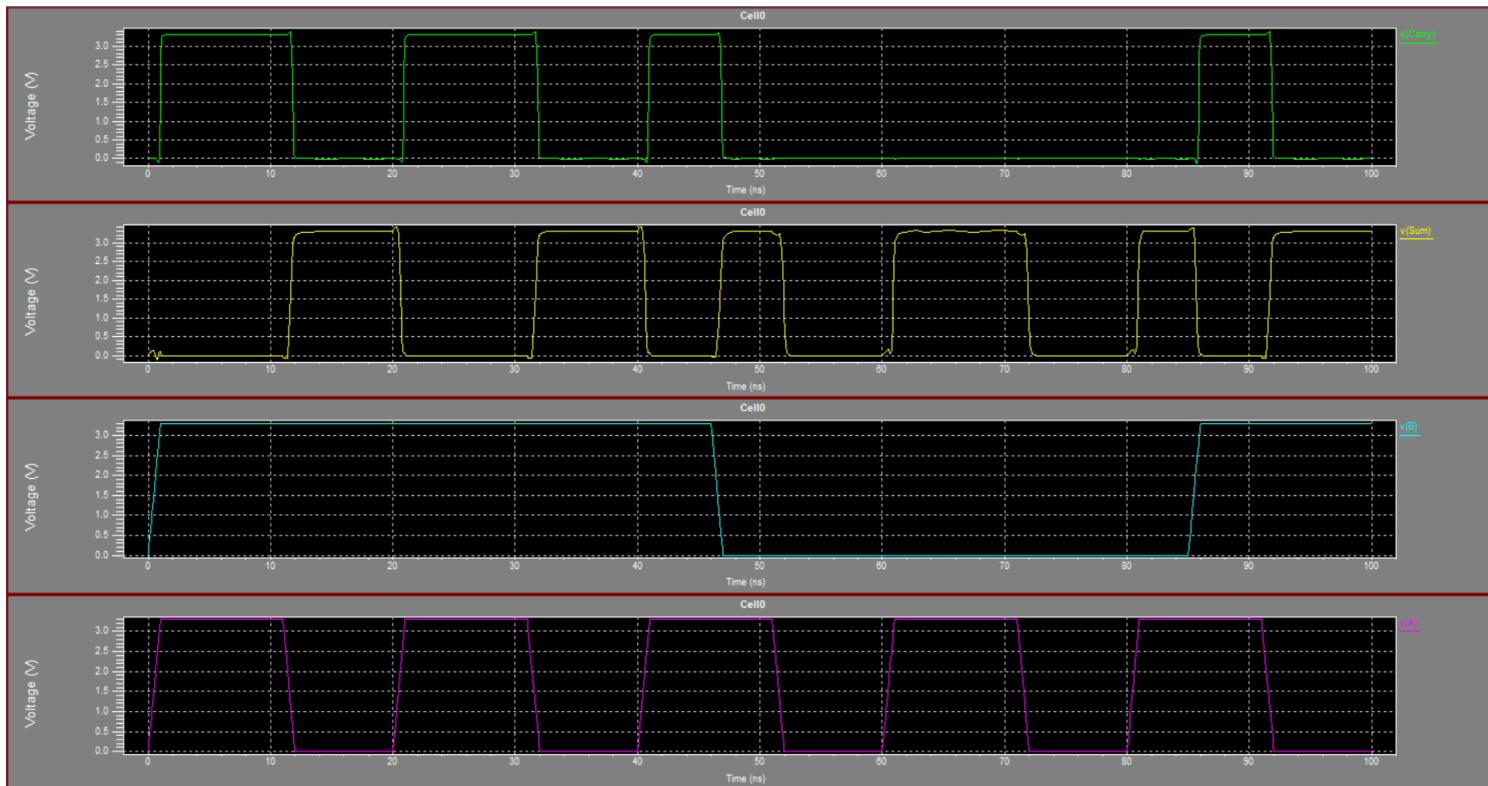
```

.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 3.3V
Vin1 A Gnd pulse(0 3.3v 0 1n 1n 10n 20n)
Vin2 B Gnd pulse(0 3.3v 0 1n 1n 45n 85n)
.Tran 1ns 100ns
**.power Vdd A 10000ns
.print V(A) V(B) V(Sum) V(Carry)
***** Simulation Settings - Additional SPICE commands *****

```

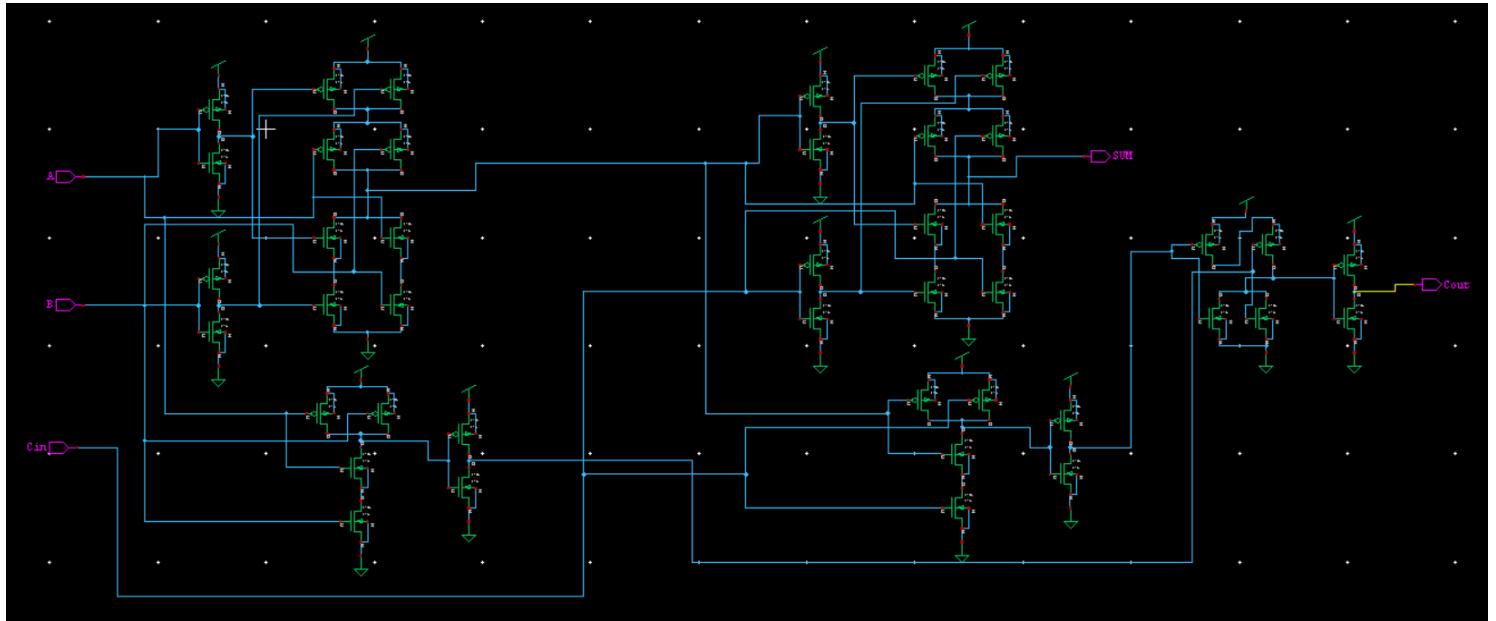
```
.end
```

## W-EDIT WAVEFORM



# FULL ADDER

## S-EDIT

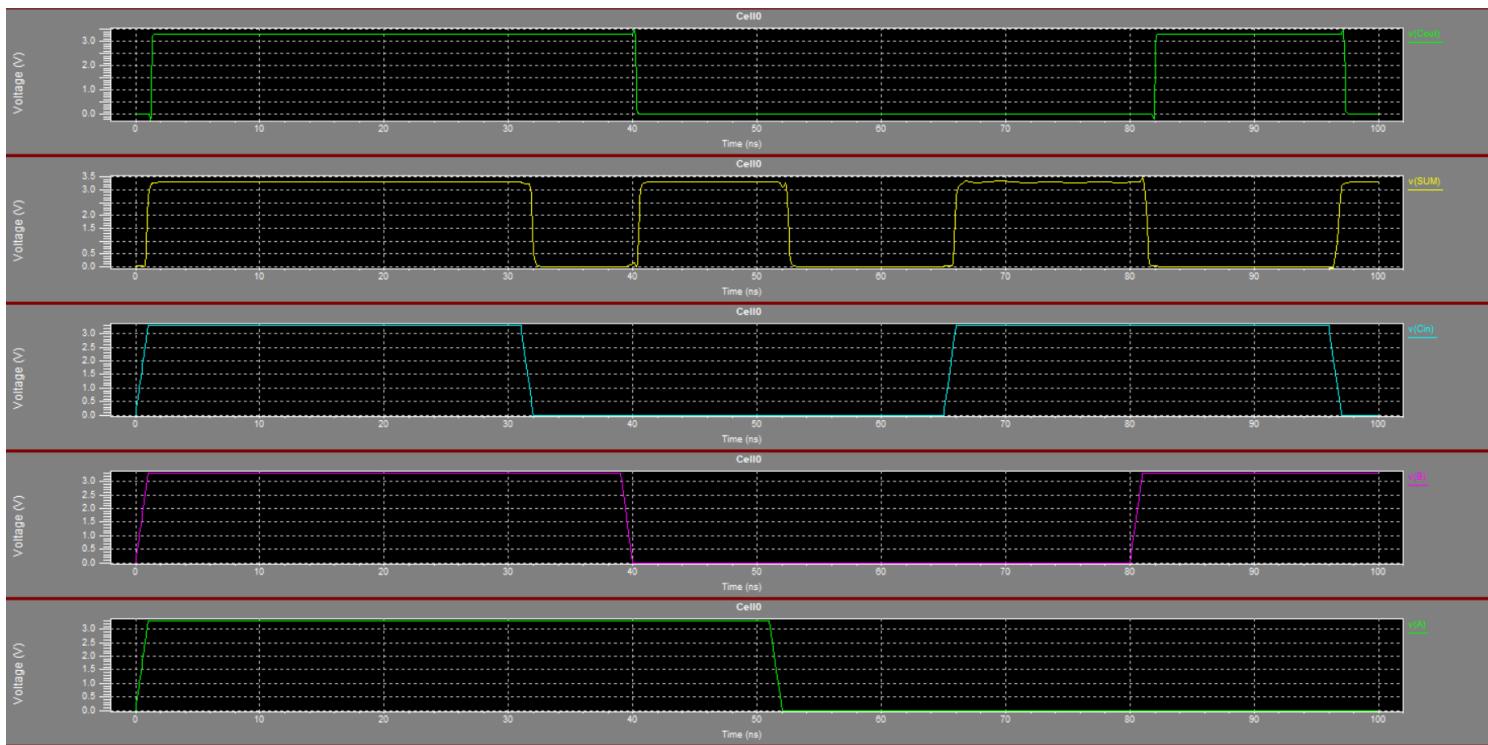


## T-SPICE

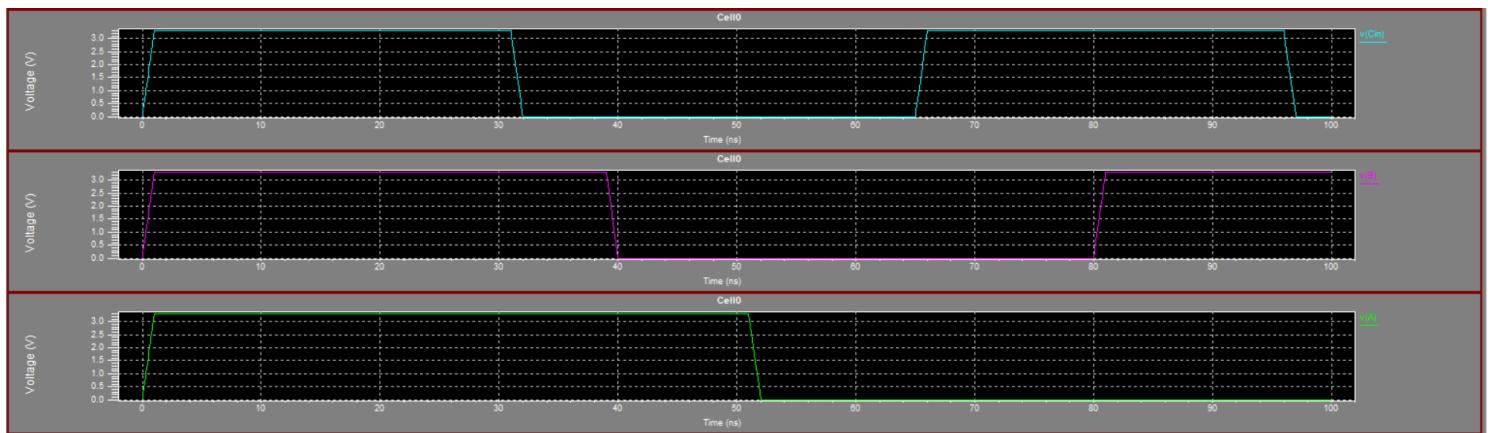
```
MMOSFET_P_21 N_19 N_9 N_20 N_20 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u  
MMOSFET_N_20 N_19 N_16 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u  
MMOSFET_N_21 N_19 N_9 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
```

```
***** Simulation Settings - Analysis section *****  
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)  
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)  
Vdd Vdd Gnd 3.3V  
Vin1 A Gnd pulse(0 3.3v 0 1n 1n 50n 100n)  
Vin2 B Gnd pulse(0 3.3v 0 1n 1n 38n 80n)  
Vin3 Cin Gnd pulse(0 3.3v 0 1n 1n 30n 65n)  
.Tran 1ns 100ns  
**.power Vdd A 10000ns  
.print V(A) V(B) V(Cin) V(SUM) V(Cout)  
***** Simulation Settings - Additional SPICE commands *****  
.end
```

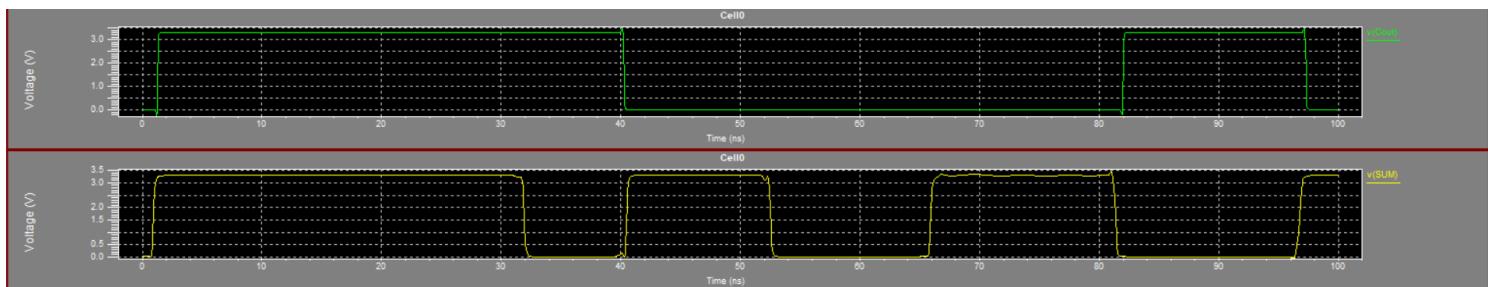
## W-EDIT WAVEFORM



## INPUT WAVEFORM

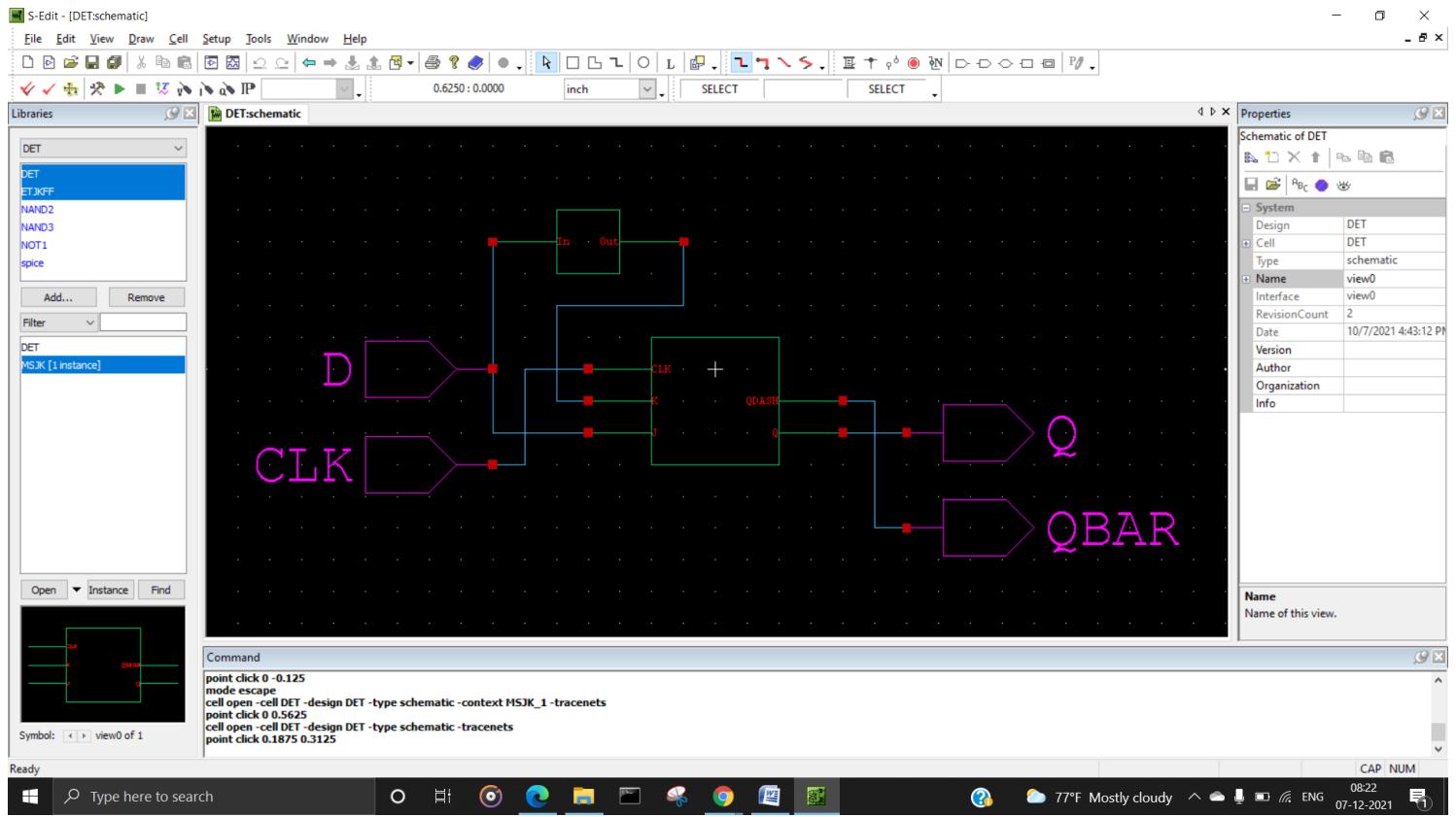


## OUTPUT WAVEFORM

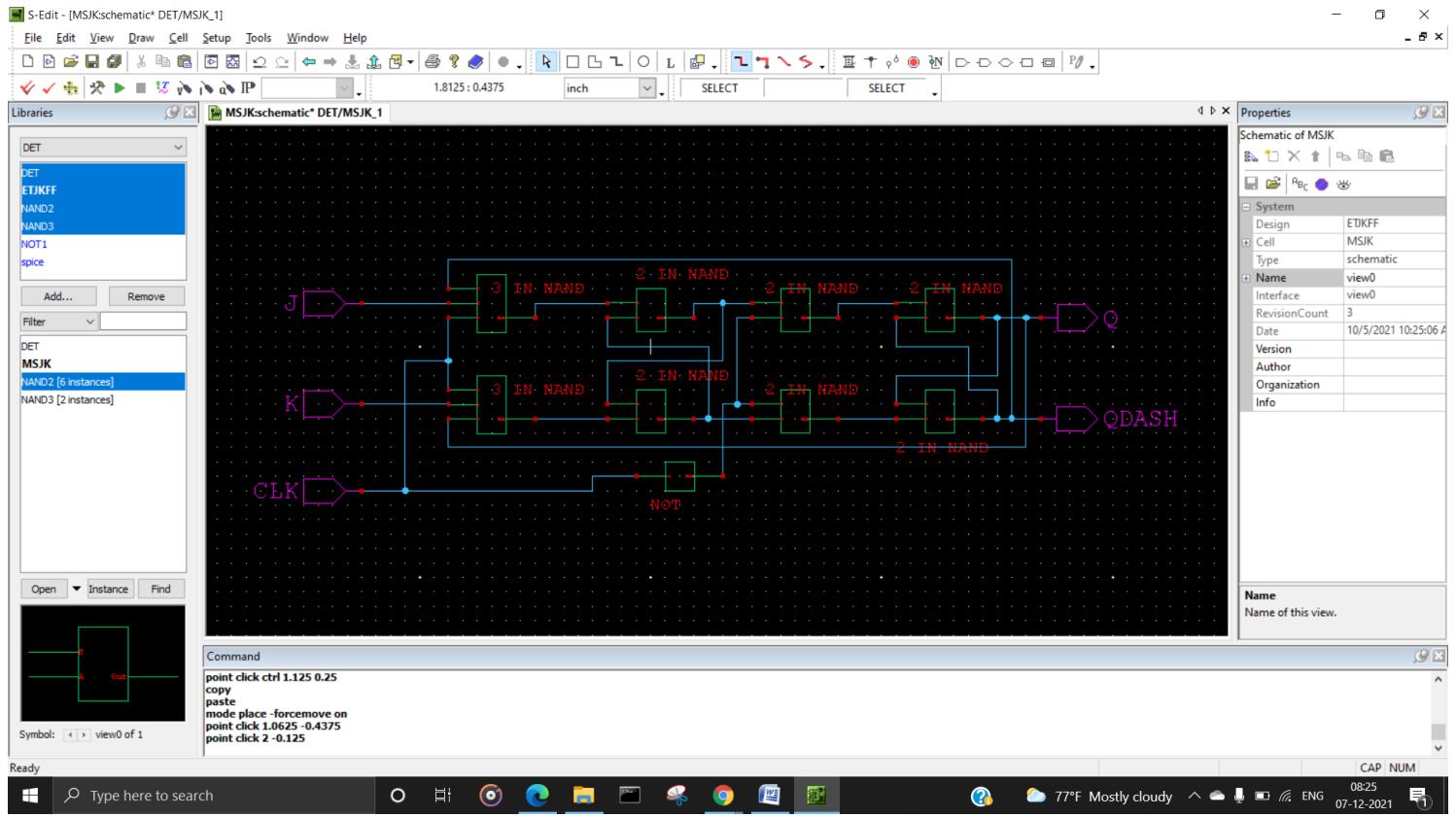


# EDGE TRIGGERED D FLIP FLOP

## S-EDIT



## INTERNAL MASTER SLAVE jk flipflop



## T-SPICE

```

XNAND2_1 N_3 N_1 N_4 Gnd Vdd NAND2
XNAND3_1 CLK J QDASH N_1 Gnd Vdd NAND3
XNAND2_2 N_2 N_4 N_3 Gnd Vdd NAND2
XNAND3_2 Q K CLK N_2 Gnd Vdd NAND3
XNAND2_3 N_5 N_4 N_6 Gnd Vdd NAND2
XNAND2_4 N_3 N_5 N_7 Gnd Vdd NAND2
XNAND2_5 QDASH N_6 Q Gnd Vdd NAND2
XNAND2_6 N_7 Q QDASH Gnd Vdd NAND2
.ends

***** Simulation Settings - Parameters and SPICE Options *****

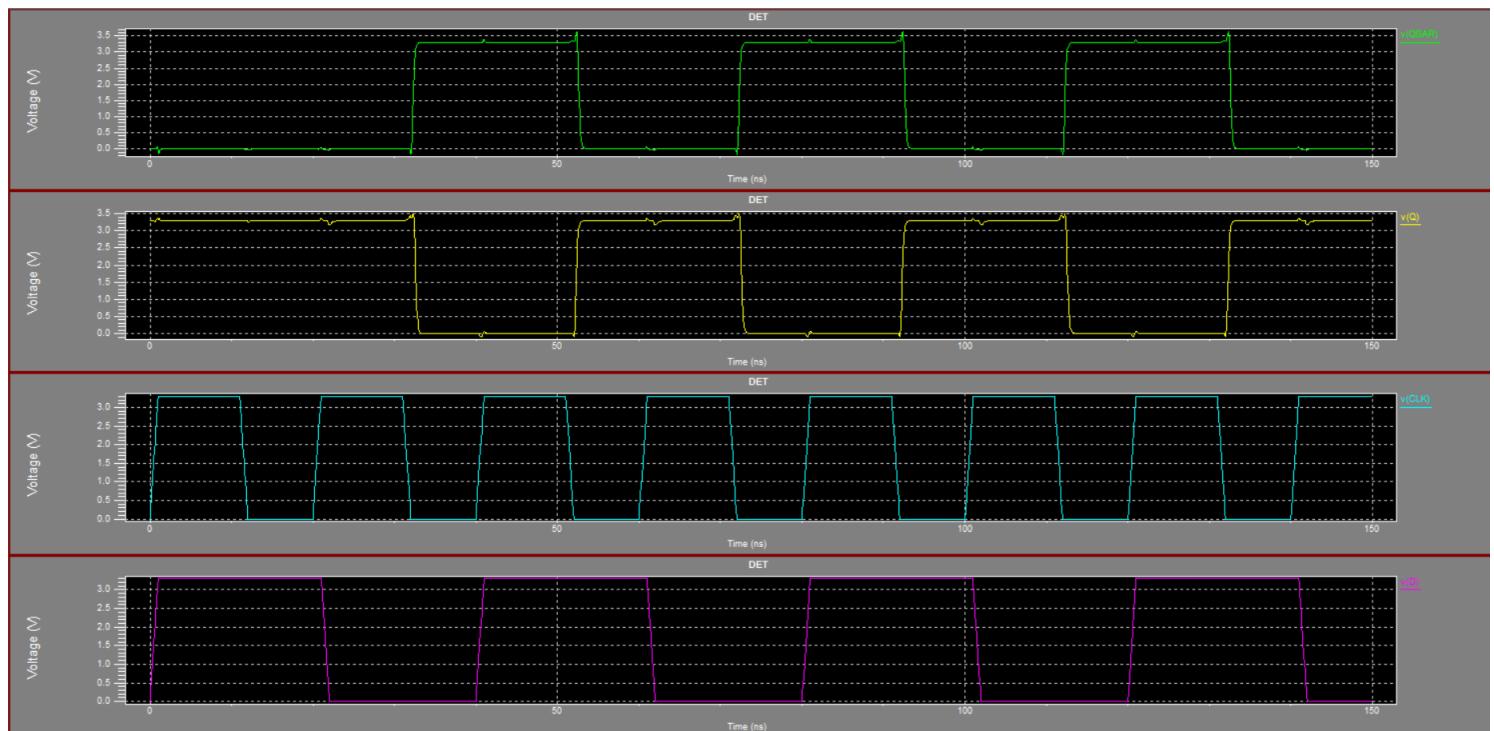
XMSJK_1 CLK D N_1 Q QBAR Gnd Vdd MSJK
XNOT_1 D N_1 Gnd Vdd NOT

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 3.3V
Vin1 D Gnd pulse(0 3.3v 0 1n 1n 20n 40n)
Vin2 CLK Gnd pulse(0 3.3v 0 1n 1n 10n 20n)
.tran 1ns 150ns
.print V(D) V(CLK) V(Q) V(QBAR)
***** Simulation Settings - Additional SPICE commands *****

.end

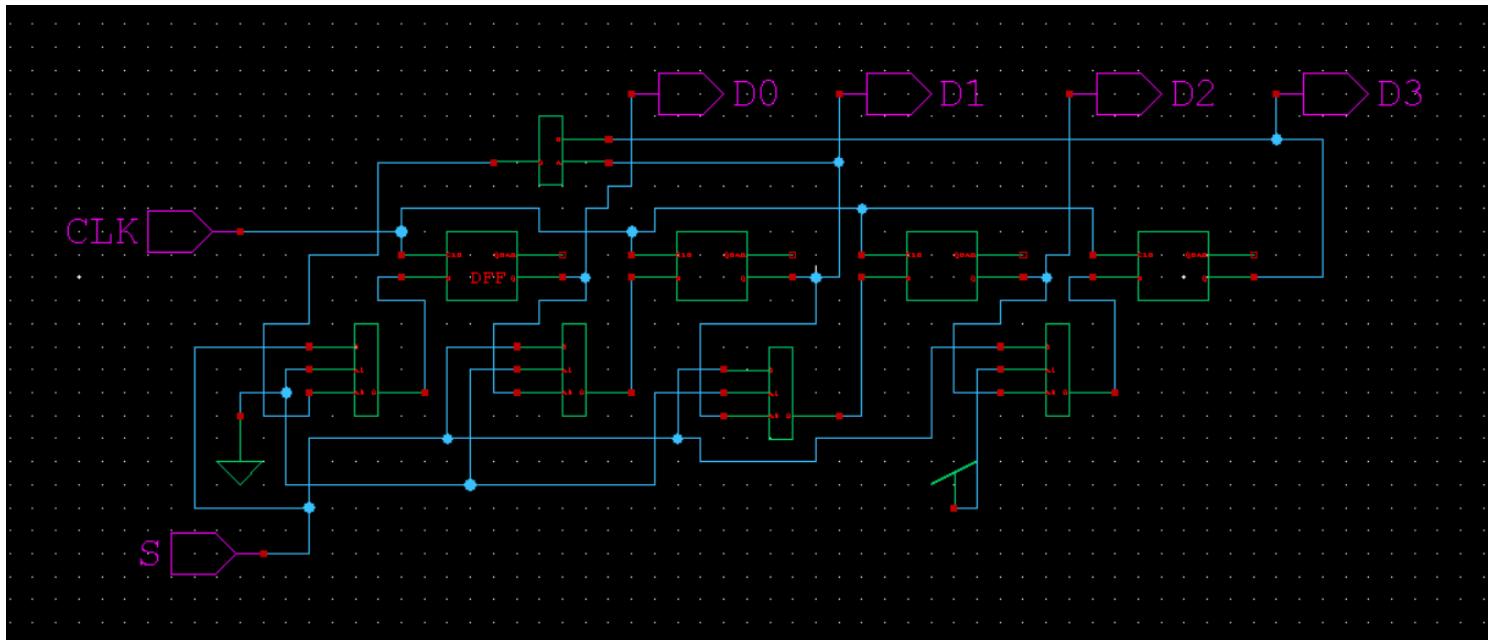
```

## W-EDIT WAVEFORM



## STANDARD LFSR

### S-EDIT



### T-SPICE

```
***** Simulation Settings - Parameters and SPICE Options *****

X2X1_2 D0 Gnd N_3 S Gnd Vdd 2X1
X2X1_3 D1 Gnd N_5 S Gnd Vdd 2X1
X2X1_4 D2 Vdd N_7 S Gnd Vdd 2X1
XDET_1 CLK N_1 D0 N_2 Gnd Vdd DET
XDET_2 CLK N_3 D1 N_4 Gnd Vdd DET
XDET_3 CLK N_5 D2 N_6 Gnd Vdd DET
XDET_4 CLK N_7 D3 N_8 Gnd Vdd DET
XXOR_1 D1 D3 N_9 Gnd Vdd XOR
X2X1_1 N_9 Gnd N_1 S Gnd Vdd 2X1

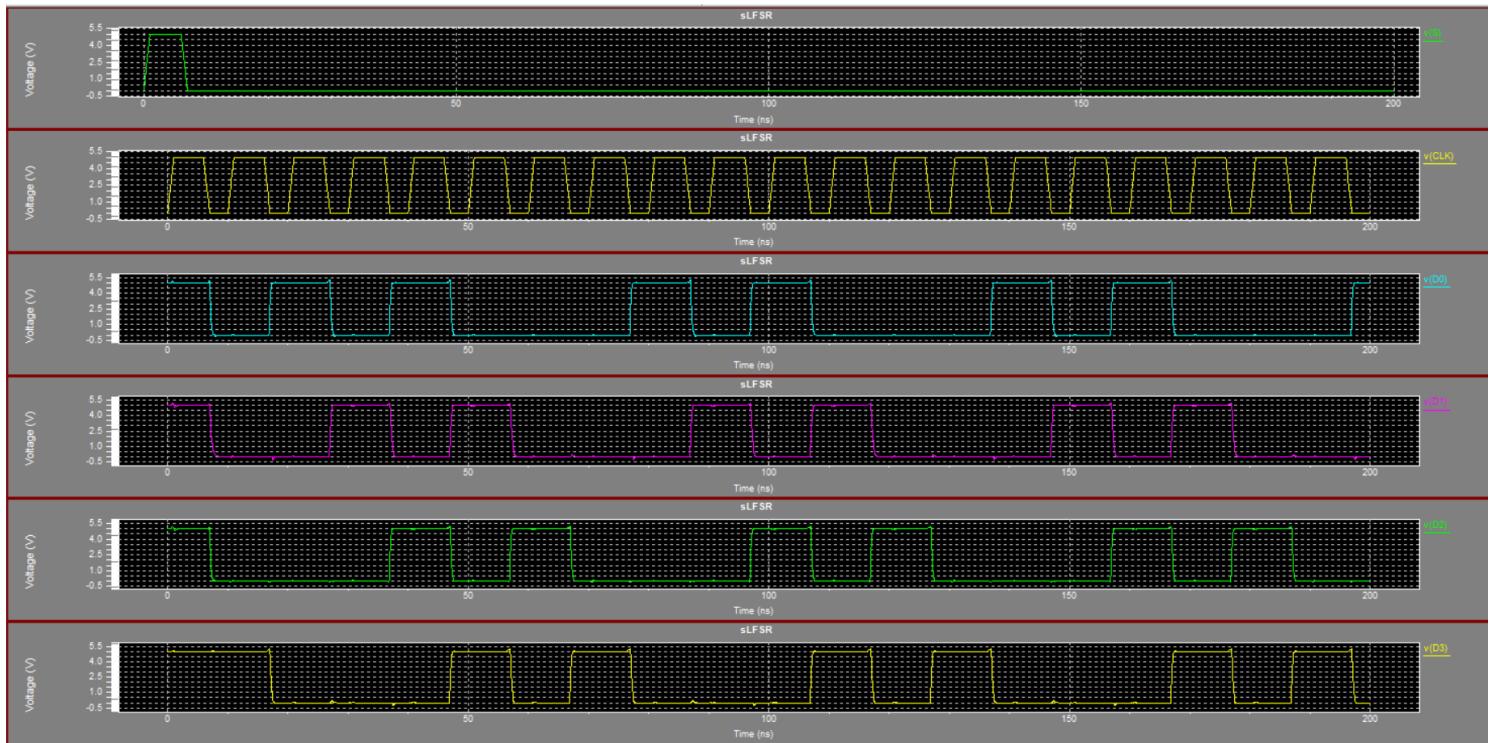
***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V

Vin4 CLK Gnd pulse(0 5v 0 1n 1n 5n 10n)
Vin3 S Gnd pulse(0 5v 0 1n 1n 5n 200n)

.Tran 1ns 200ns
.print V(D3) V(D2) V(D1) V(D0) V(CLK) V(A0) V(A1) V(S)
***** Simulation Settings - Additional SPICE commands *****

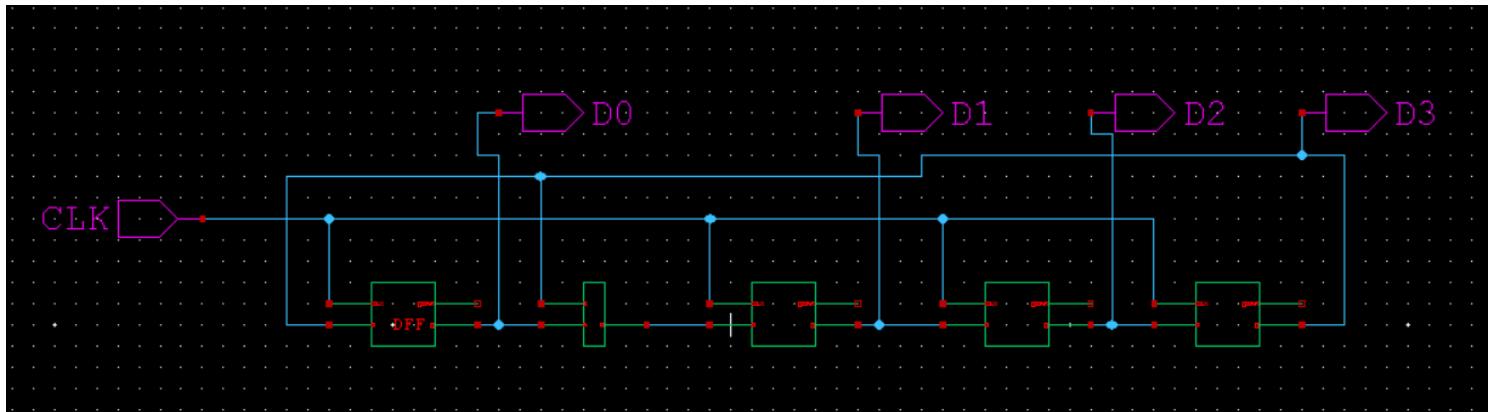
.end
```

## W-EDIT WAVEFORM



# MODULAR LFSR

## S-EDIT



## T-SPICE

```
XMSJK_1 CLK D N_1 Q QBAR Gnd Vdd MSJK
.ends

***** Simulation Settings - Parameters and SPICE Options *****

XDET_1 CLK D3 D0 N_1 Gnd Vdd DET
XDET_2 CLK N_2 D1 N_3 Gnd Vdd DET
XDET_3 CLK D1 D2 N_4 Gnd Vdd DET
XDET_4 CLK D2 D3 N_5 Gnd Vdd DET
XXOR_1 D0 D3 N_2 Gnd Vdd XOR

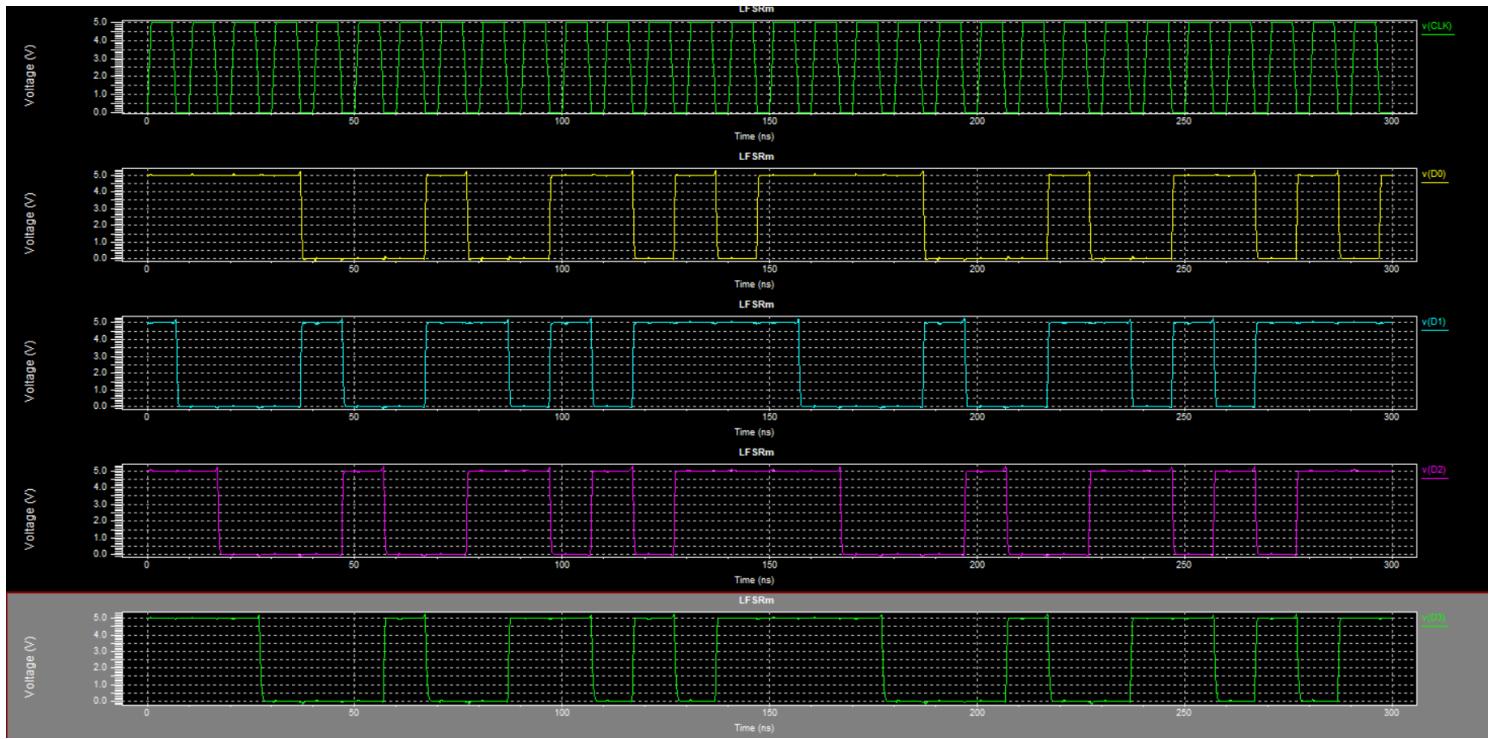
***** Simulation Settings - Analysis section *****
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V

Vin4 CLK Gnd pulse(0 5v 0 1n 1n 5n 10n)

.Tran lns 300ns
.print V(D3) V(D2) V(D1) V(D0) V(CLK)
***** Simulation Settings - Additional SPICE commands *****

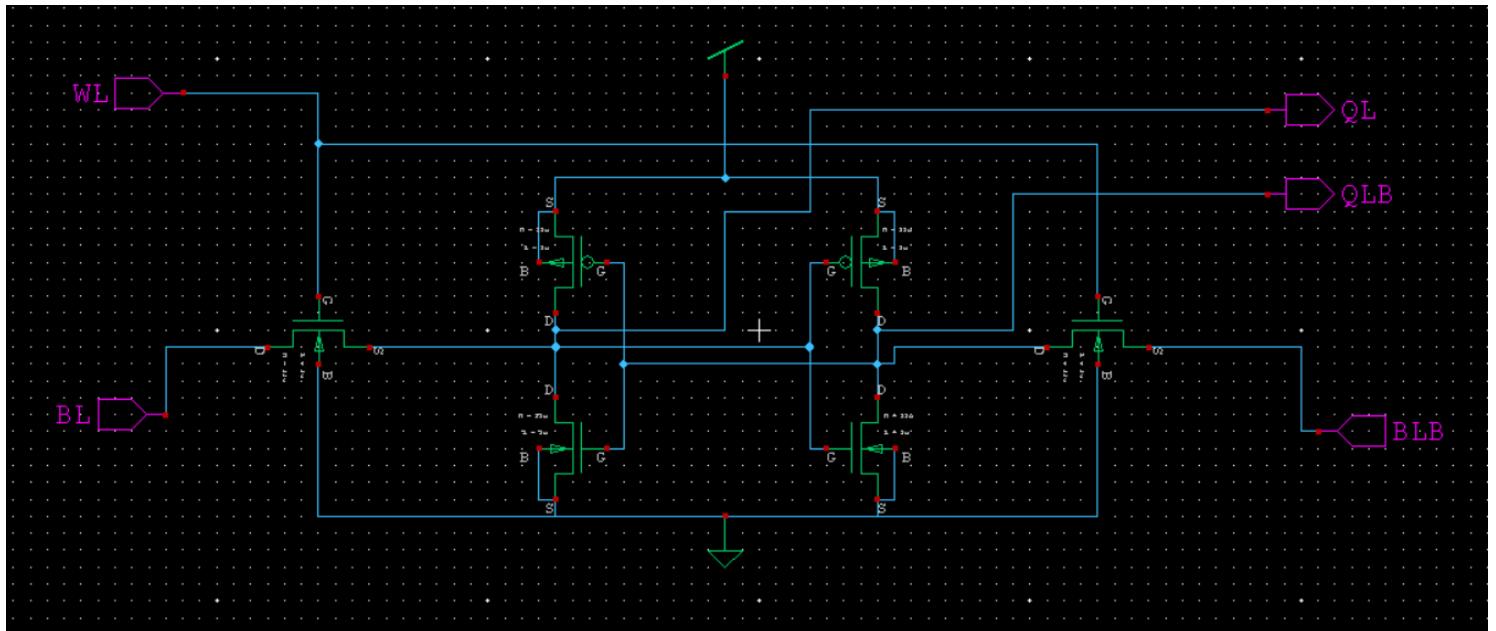
.end
```

## W-EDIT WAVEFORM



# SRAM CELL

## S-EDIT



## T-SPICE

```
***** Simulation Settings - General section *****

***** Simulation Settings - Parameters and SPICE Options *****

MMOSFET_N_1 QL QLB Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 QLB QL Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_3 BL WL QL N_1 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 QL QLB Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_4 QLB WL BLB N_1 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 QLB QL Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V
Vin1 BL Gnd pulse(0 5v 0 ln ln 10n 20n)
Vin2 BLB Gnd pulse(5v 0 0 ln ln 10n 20n)
Vin3 WL Gnd pulse(0 5v 0 ln ln 35n 75n)

.Tran 1ns 200ns
**.power Vdd A 10000ns
.print V(QLB) V(QL)V(BLB) V(BL) V(WL)
***** Simulation Settings - Additional SPICE commands *****

.end
```

## W-EDIT WAVEFORM





Case 1: when WL(Word Line) is 1 , it will read from BL (Bit Line) and writes it in QL output

And reads data from BLB(Bit Line Bar) and writes it in QLB output.

Case 2 : When WL is 0 , then no read and write operations will perform , and the previous existing

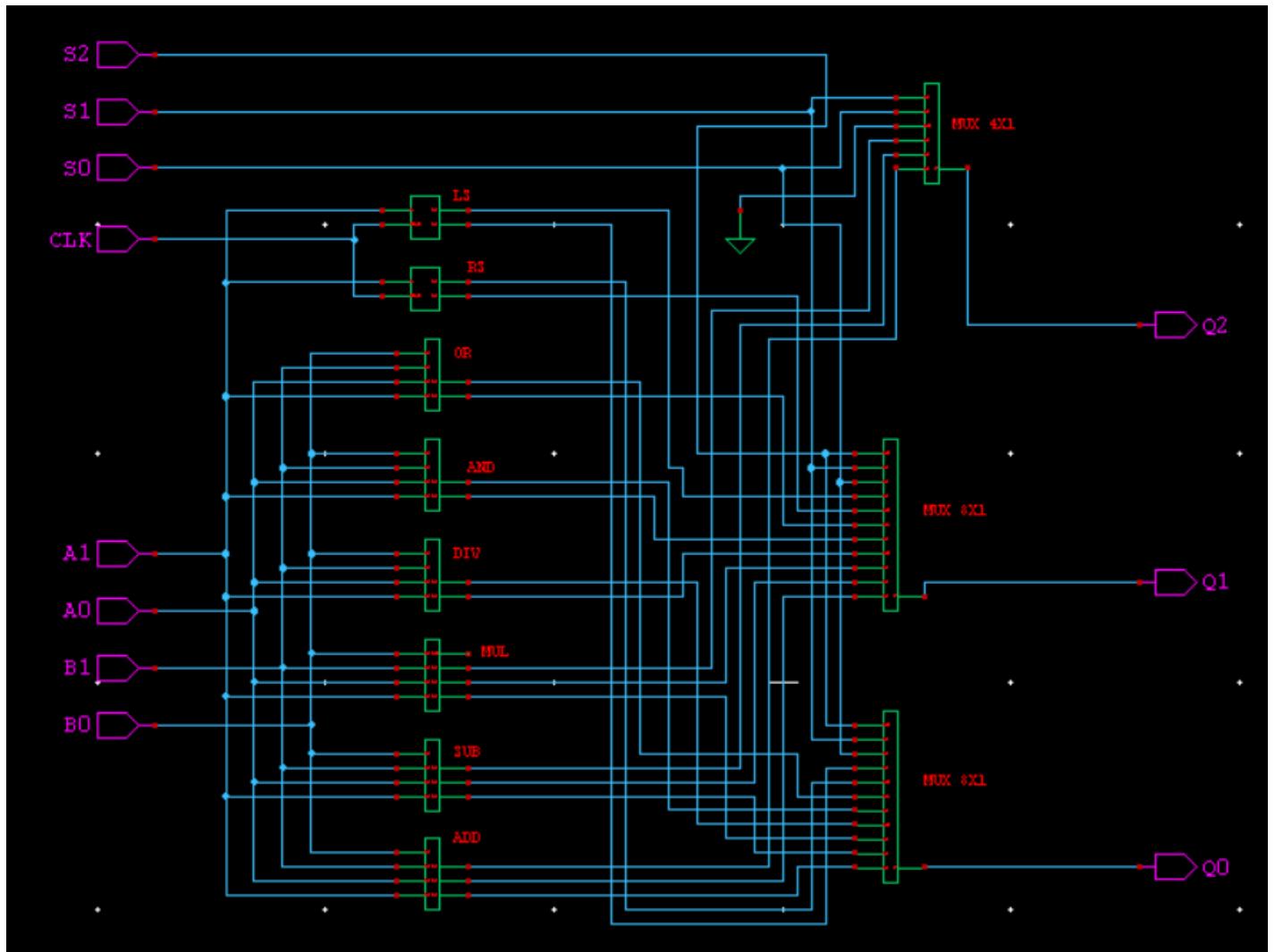
Bit at QL and QLB will be stored inside Until again WL is made HIGH.

Case 3 : Here we arranged the delay of inputs in such a way , so that at QL we will store **0** when WL

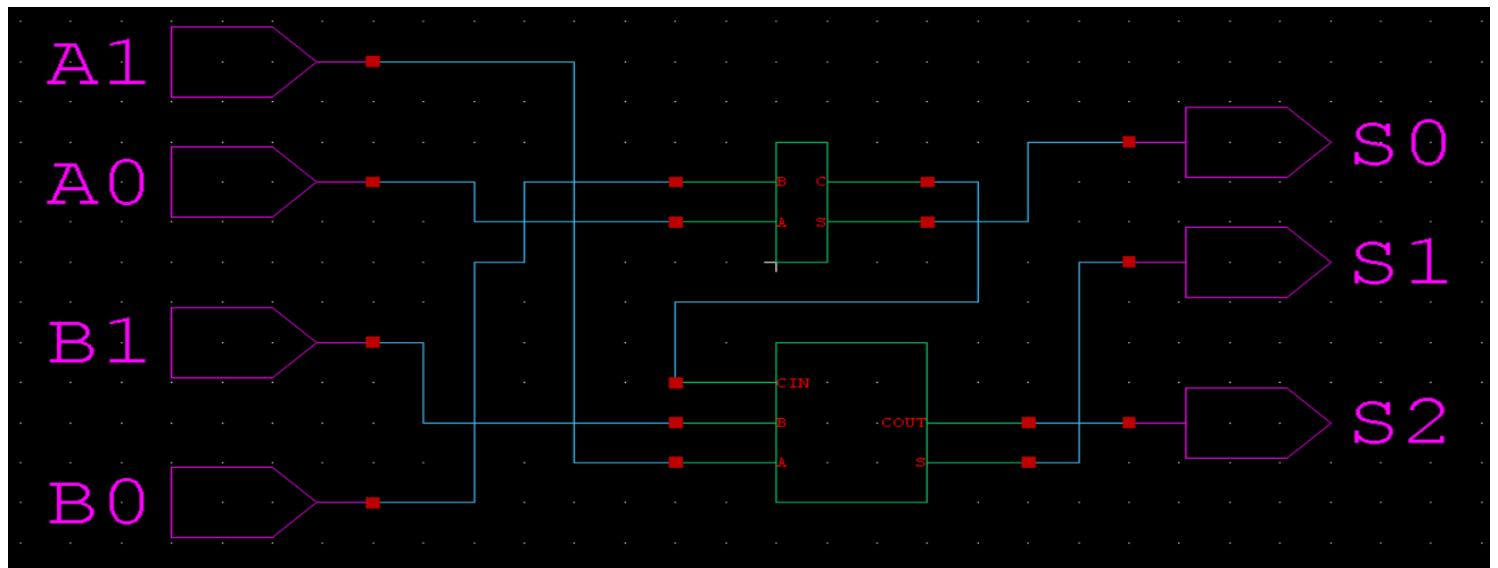
becomes 0 For first time and , it will store **1** when WL becomes 0 for second time .

## 2 BIT ALU

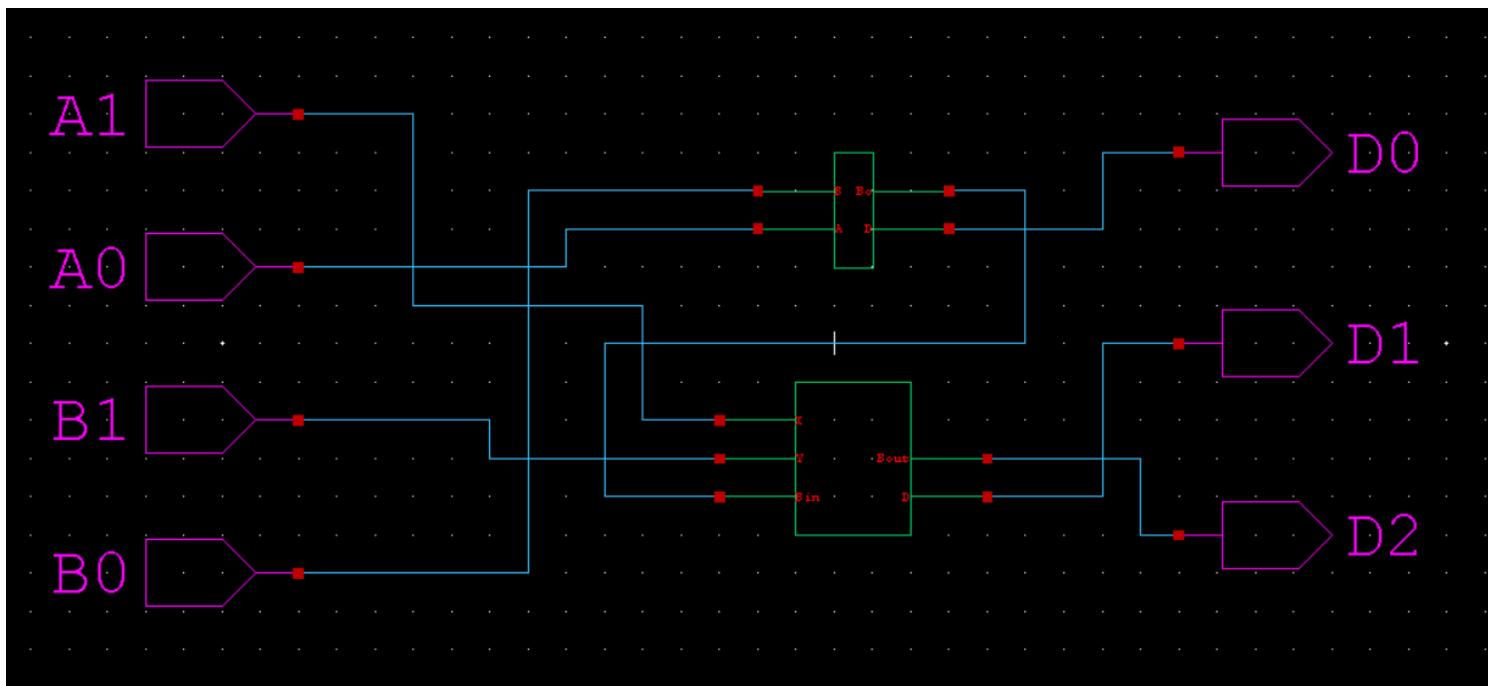
### S-EDIT



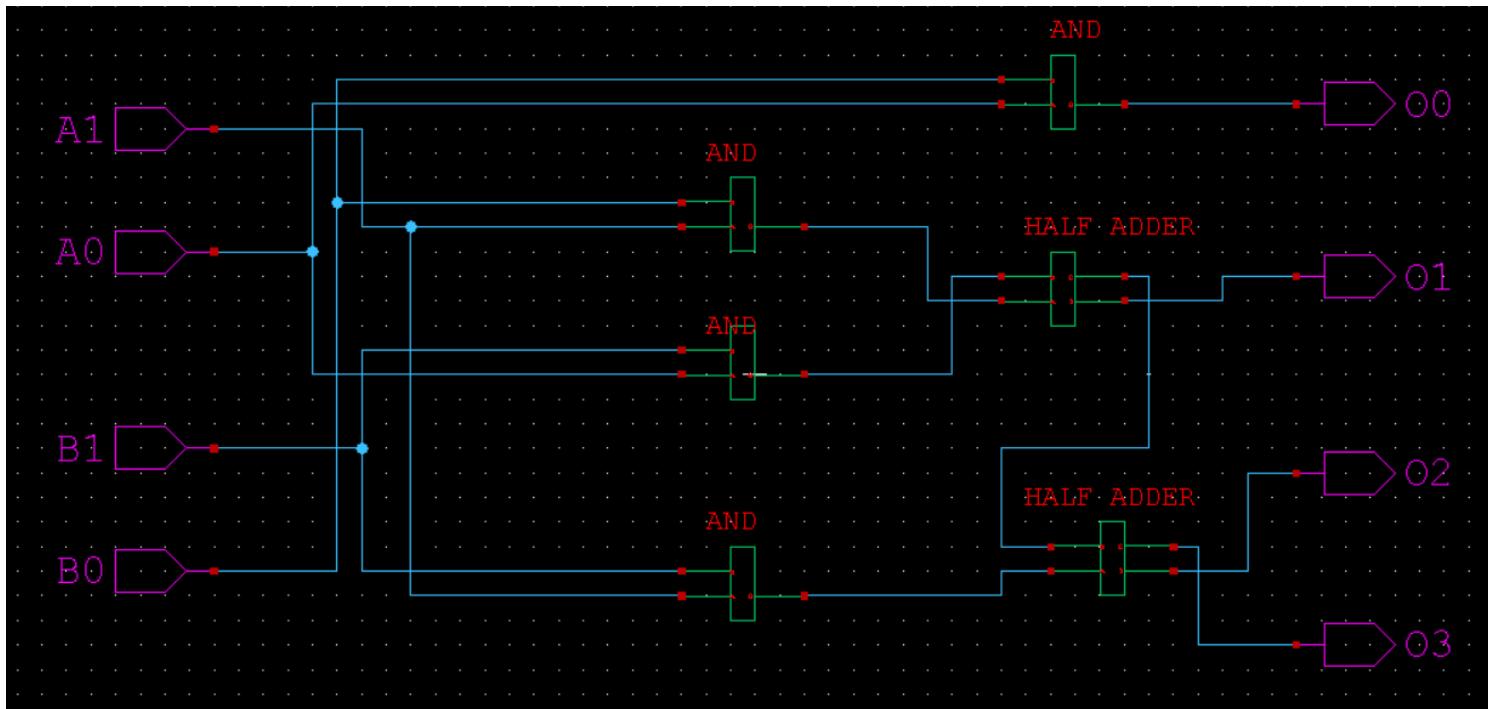
### INTERNAL CIRCUITS ADDER



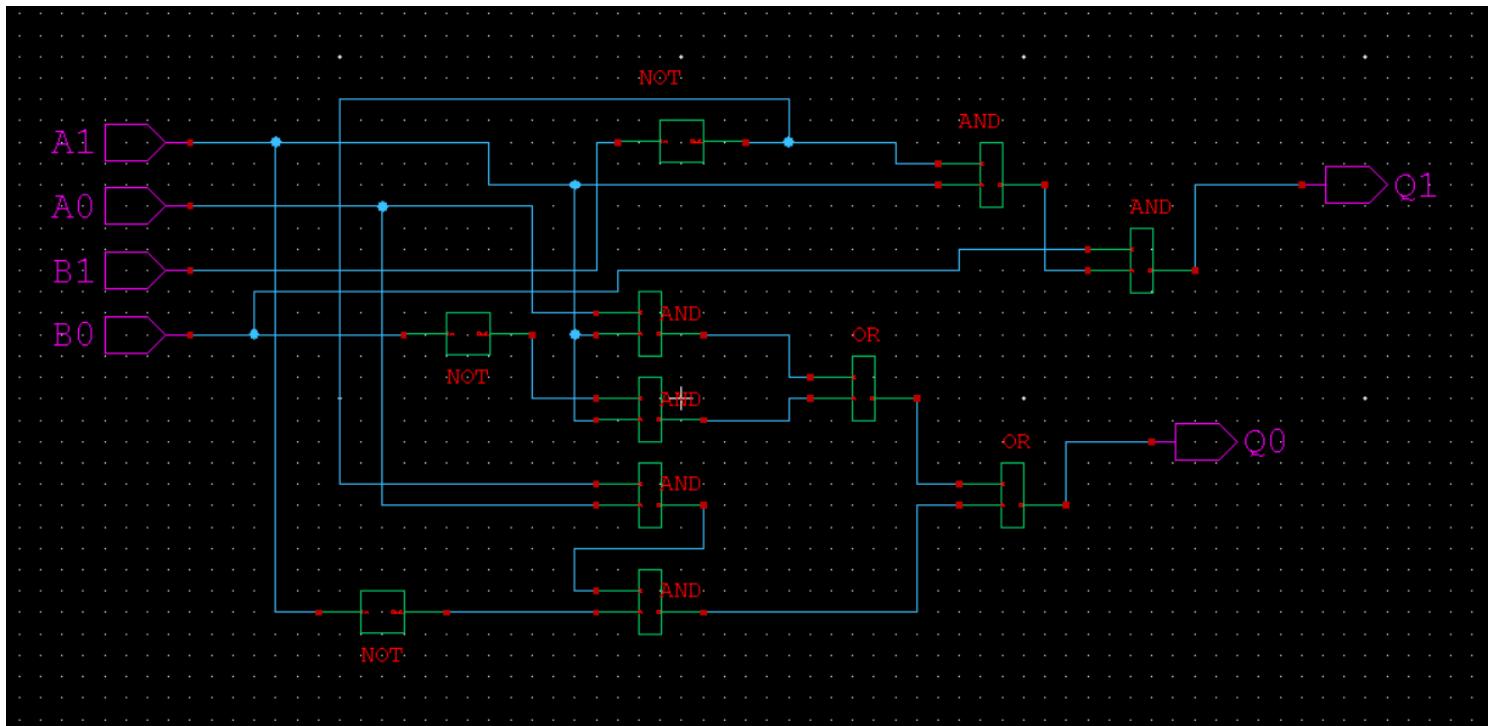
## SUBTRACTOR



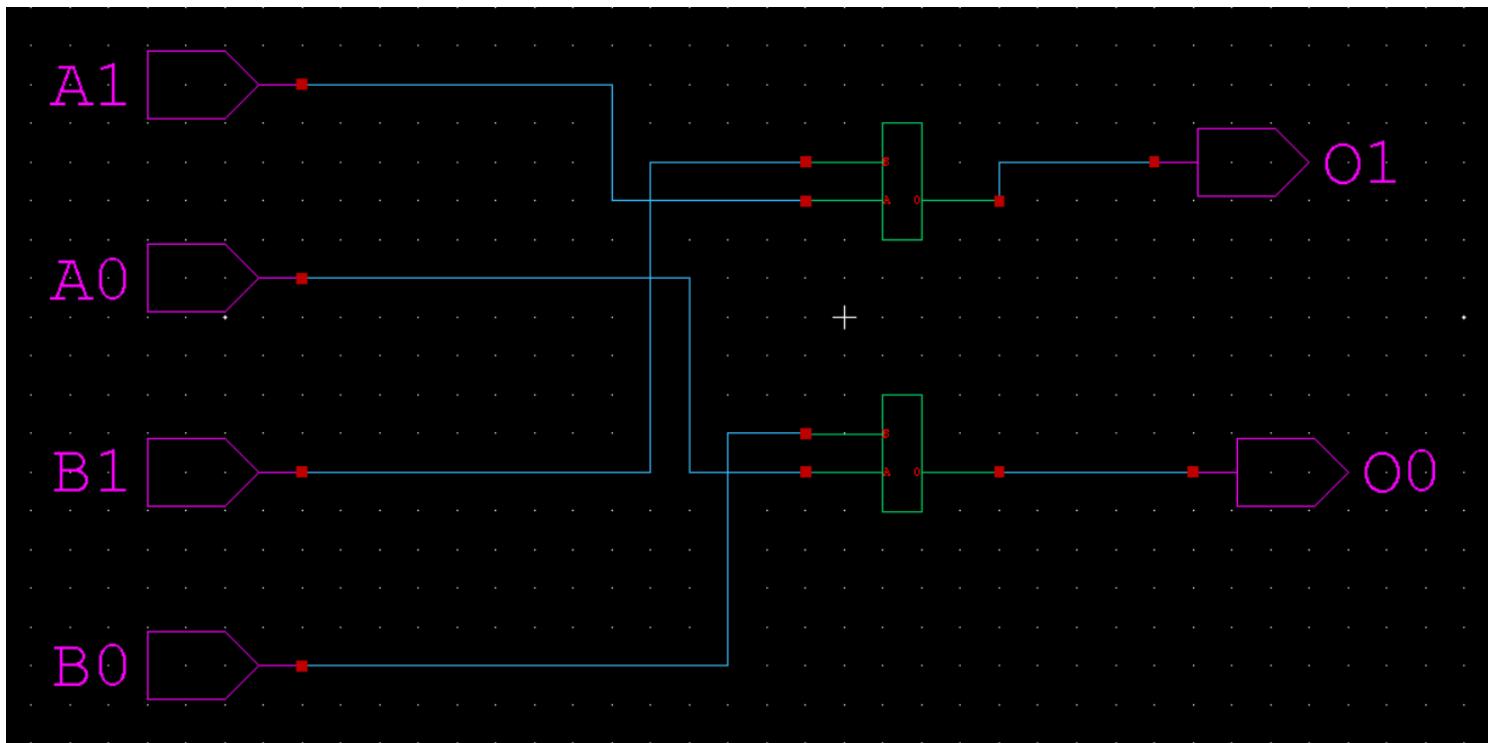
## MULTIPLIER



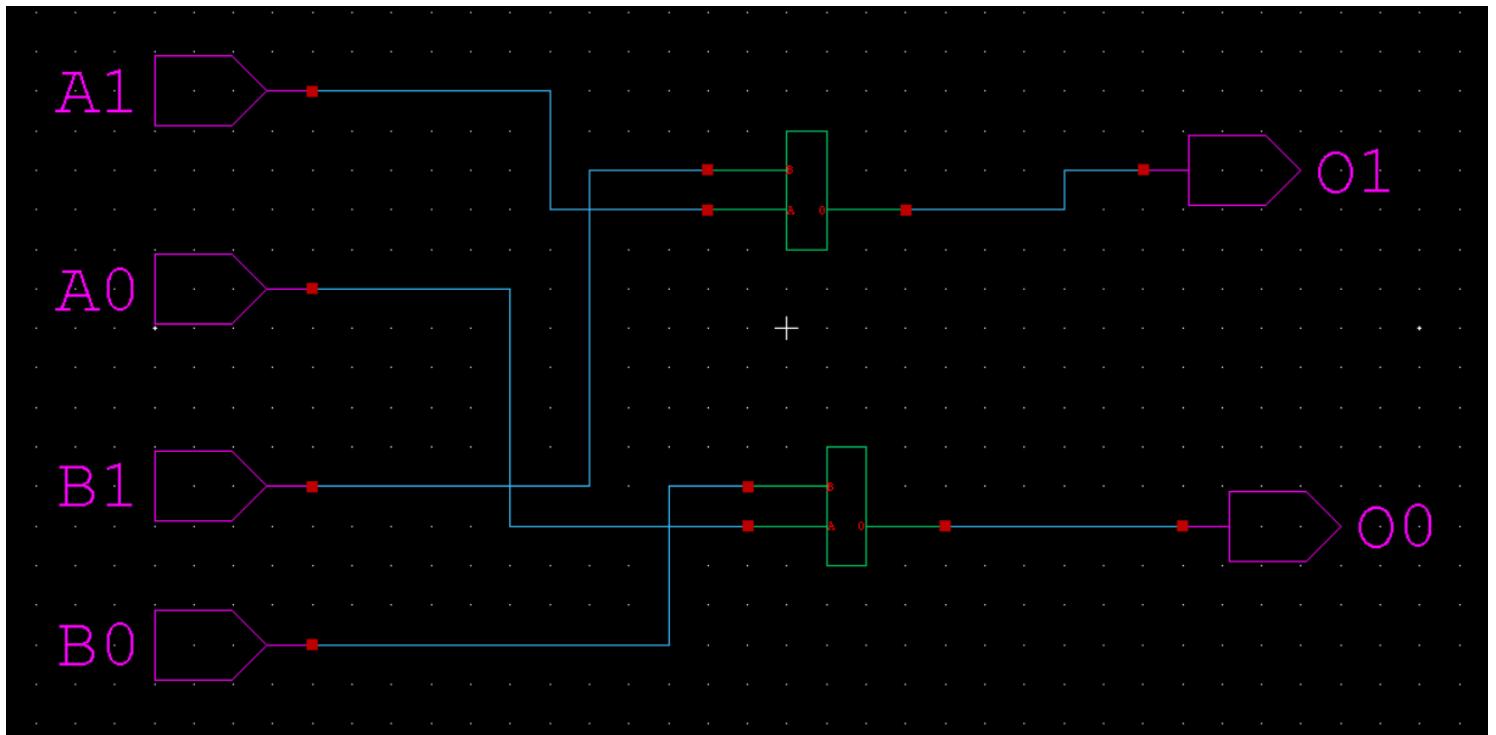
## DIVIDER



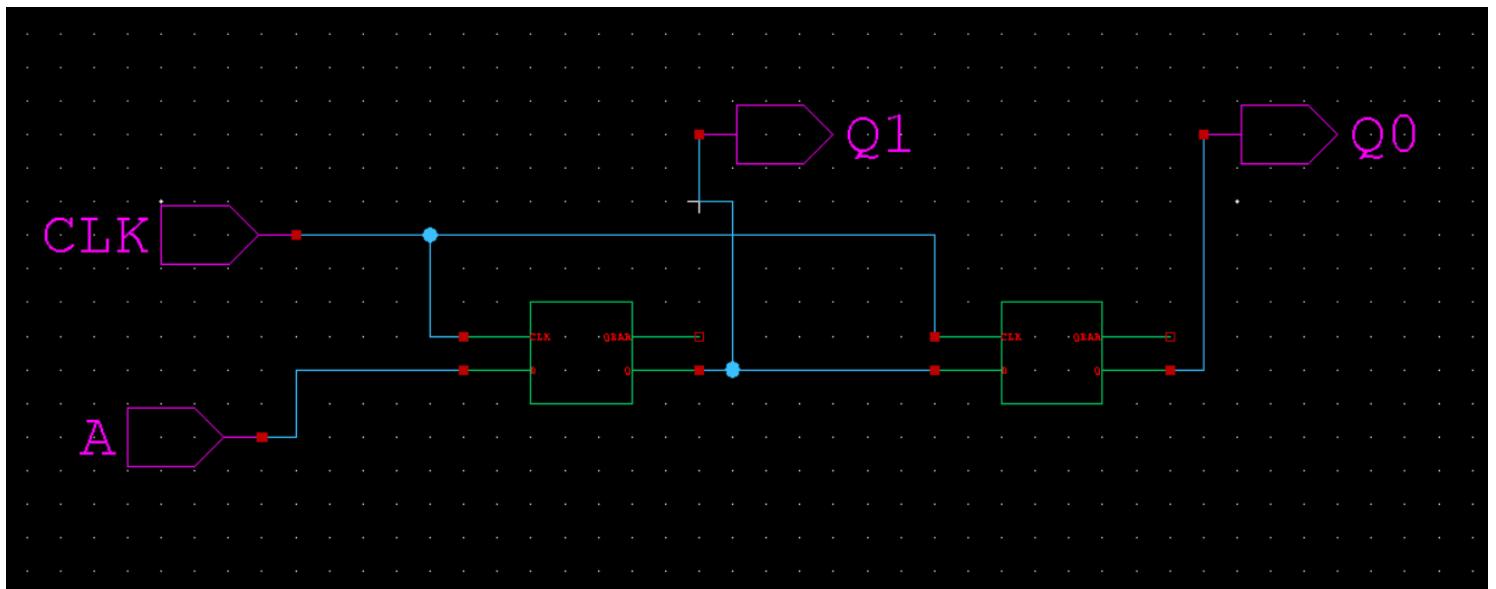
## 2 BIT LOGICAL AND



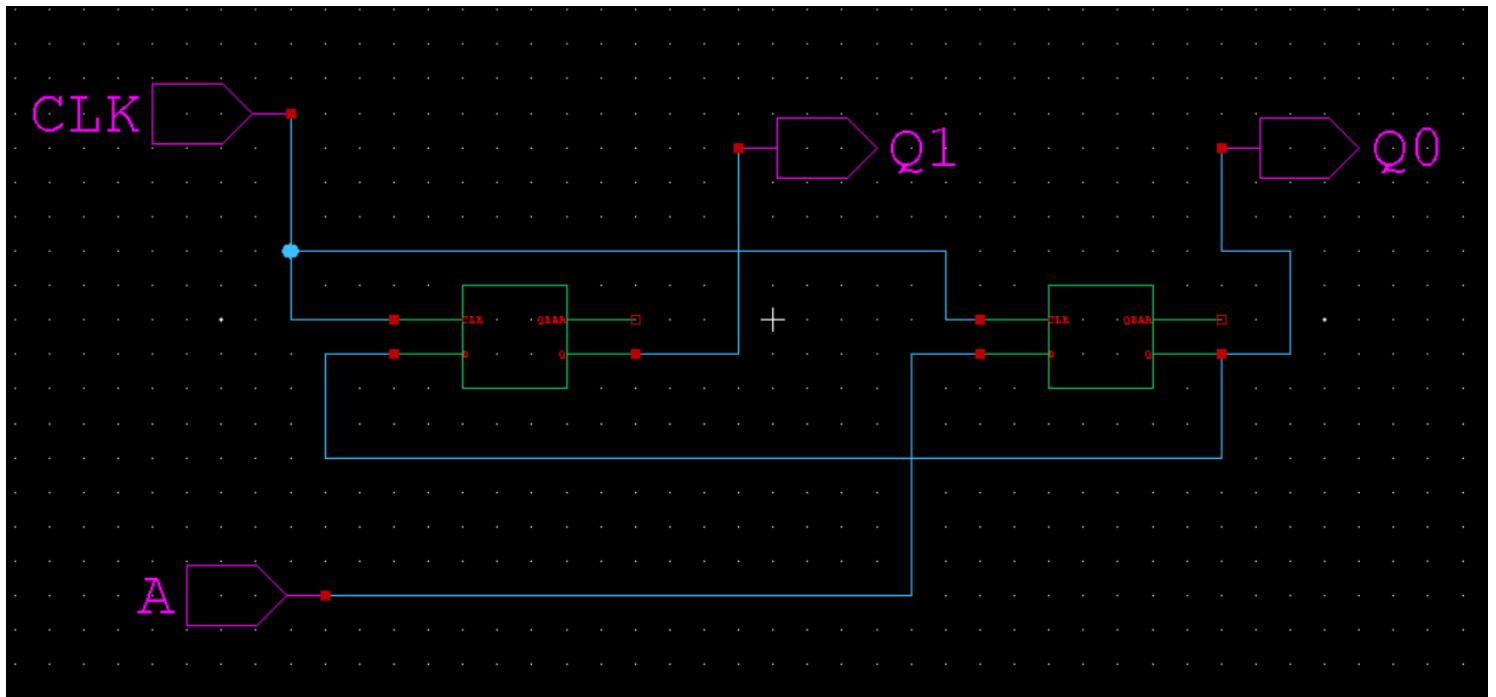
## 2 BIT LOGICAL OR



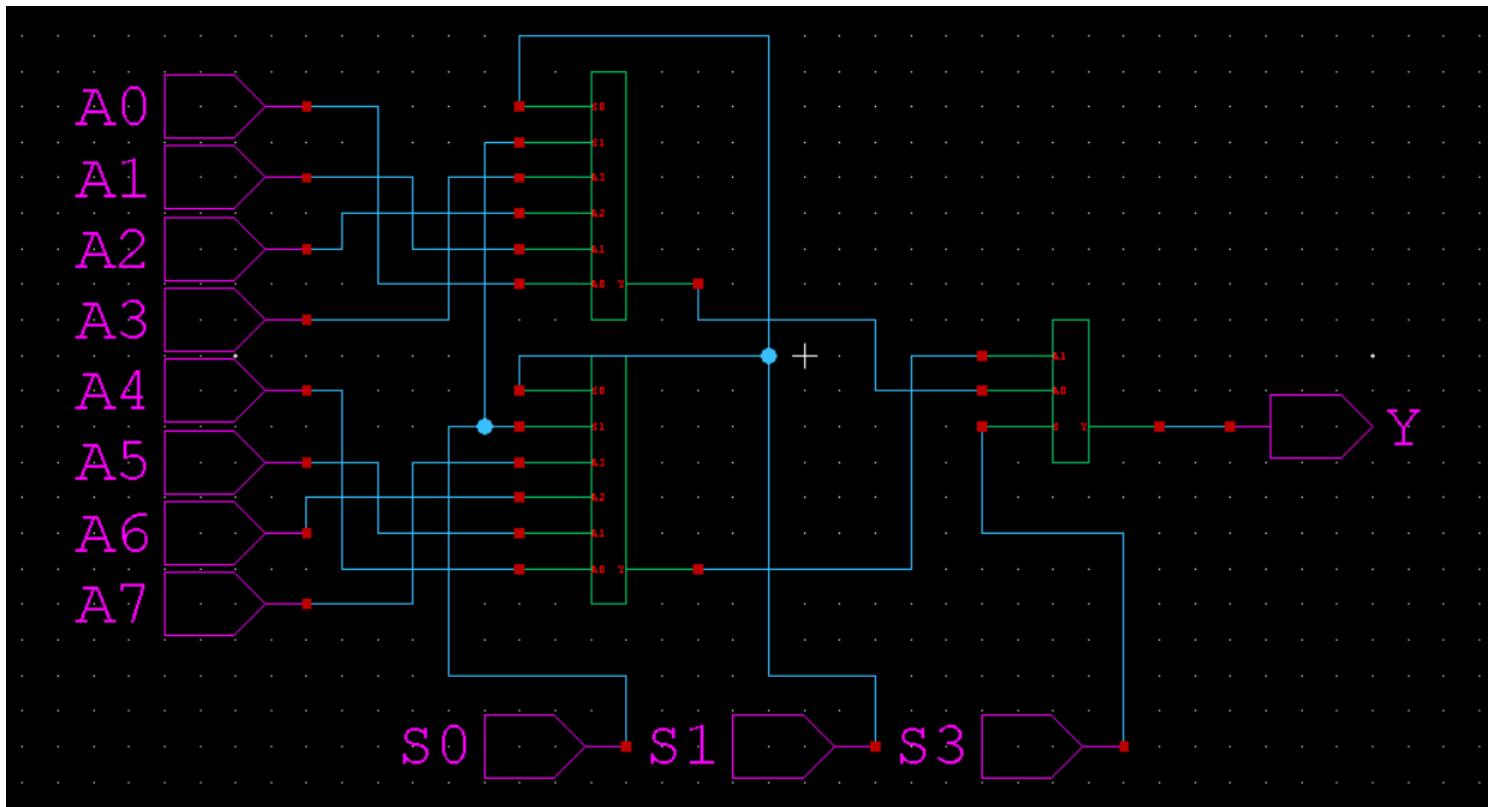
## RIGHT SHIFT



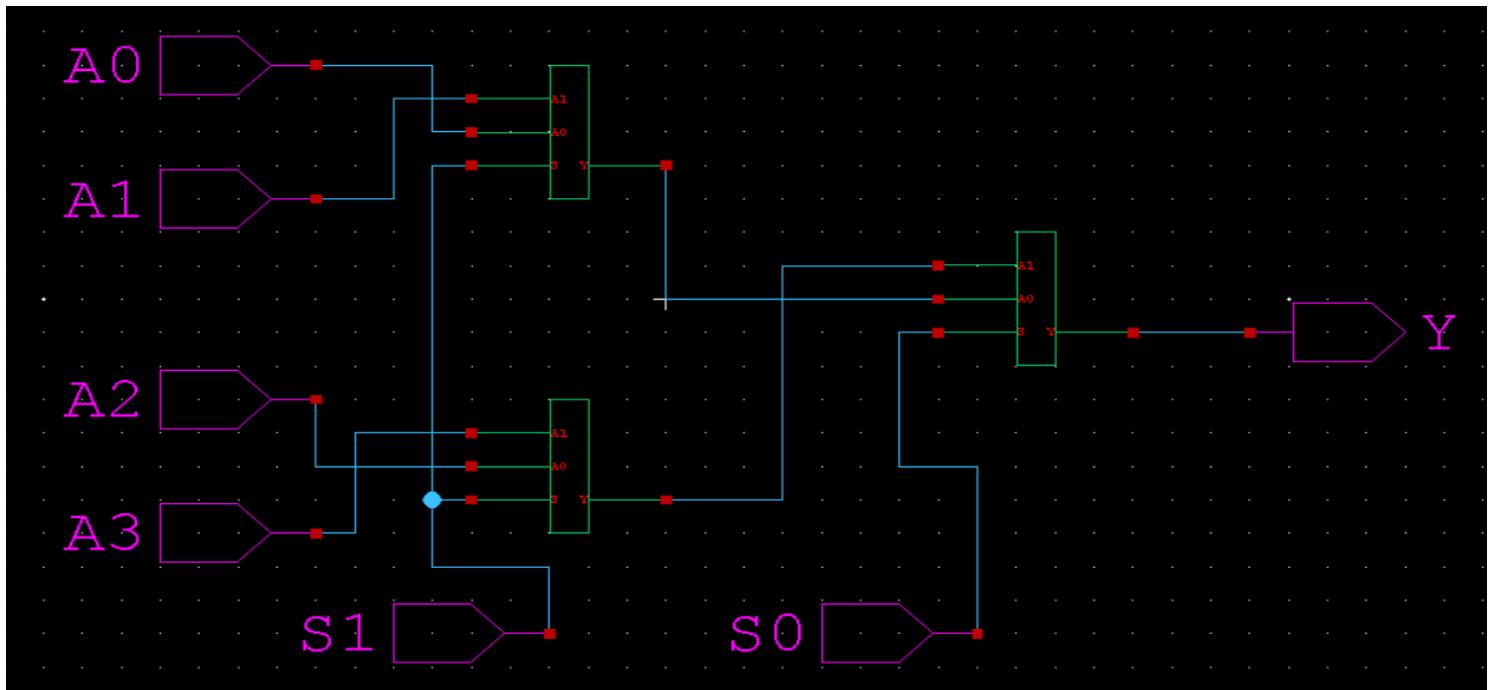
### LEFT SHIFT



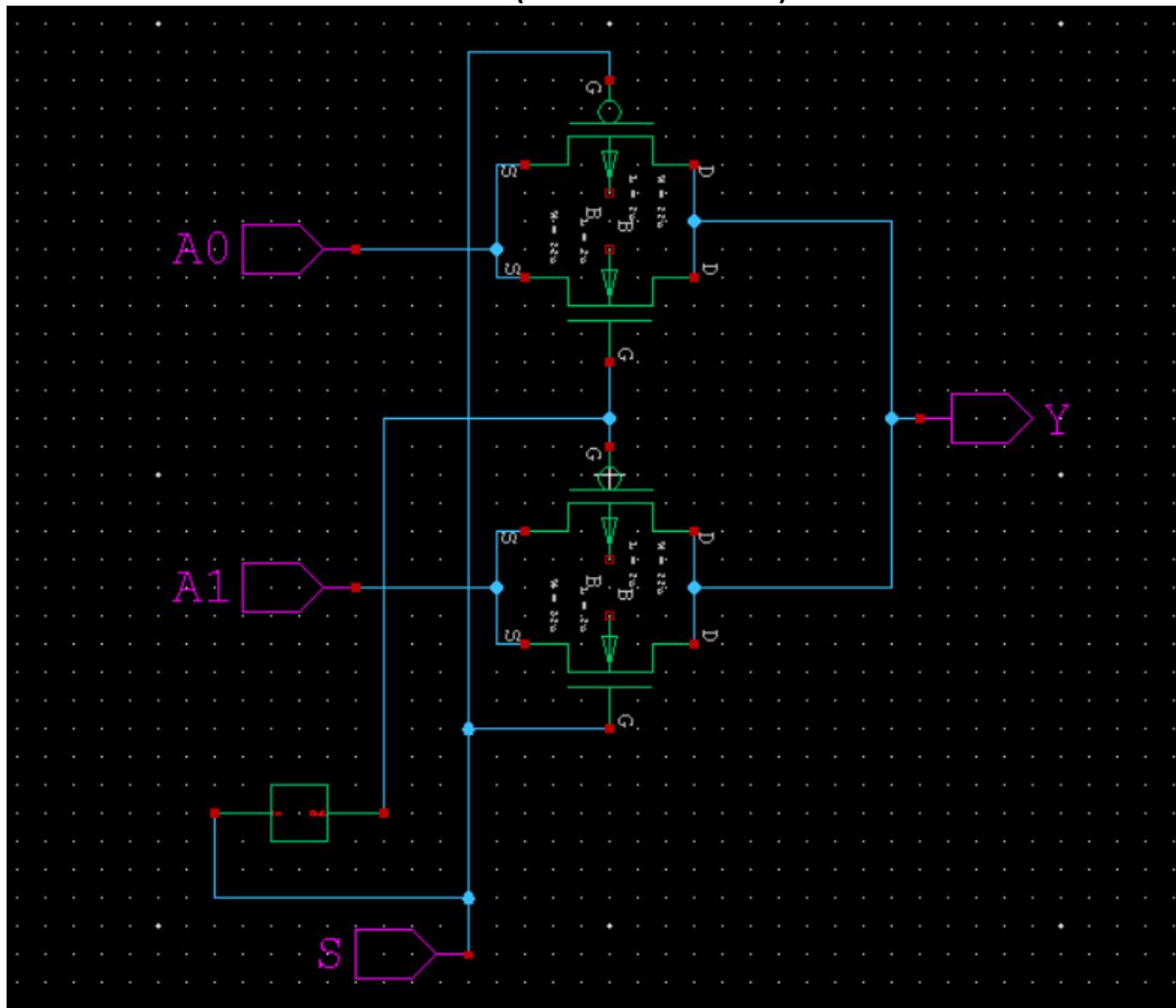
### 8X1 MUX



**4X1 MUX**



**2X1 MUX (TRANSITION MODEL)**



## T-SPICE

```
XB2DIV_1 A0 A1 B0 B1 N_6 N_13 Gnd Vdd B2DIV
X2bitRS_1 A1 CLK N_8 N_18 Gnd Vdd 2bitRS
XB2ADD_1 A0 A1 B0 B1 N_3 N_4 N_5 Gnd Vdd B2ADD
```

### \*\*\*\*\* Simulation Settings - Analysis section \*\*\*\*\*

```
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
```

```
Vdd Vdd Gnd 5V
Vin1 A1 Gnd 5V
Vin2 A0 Gnd 5V
Vin3 B1 Gnd 5V
Vin4 B0 Gnd 0
```

```
Vin8 CLK Gnd pulse(0 5v 0 1n 1n 5n 10n)
```

```
Vin5 S2 Gnd pulse(0 5v 0 1n 1n 50n 100n)
Vin6 S1 Gnd pulse(0 5v 0 1n 1n 25n 60n)
Vin7 S0 Gnd pulse(0 5v 0 1n 1n 12.2n 33n)
```

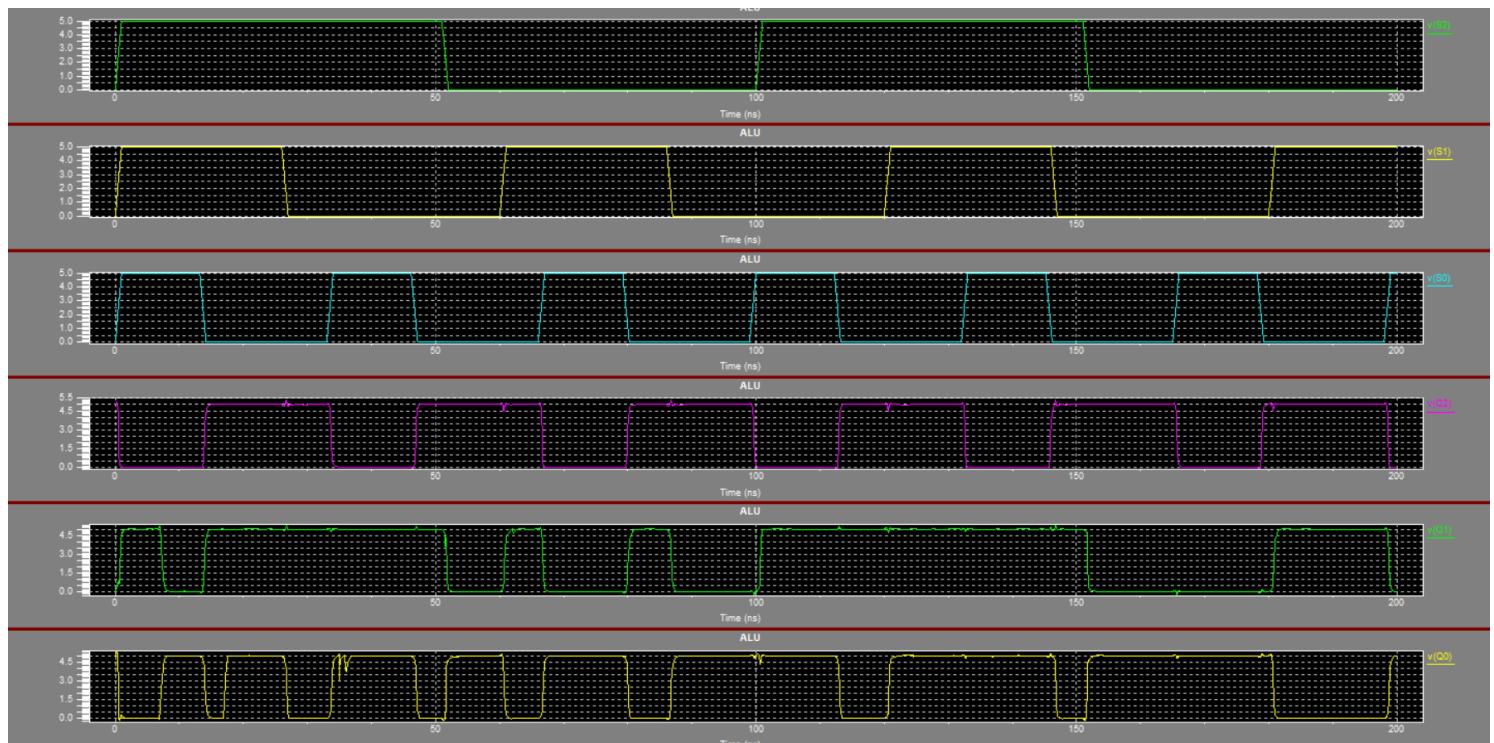
```
.Tran 1ns 200ns
```

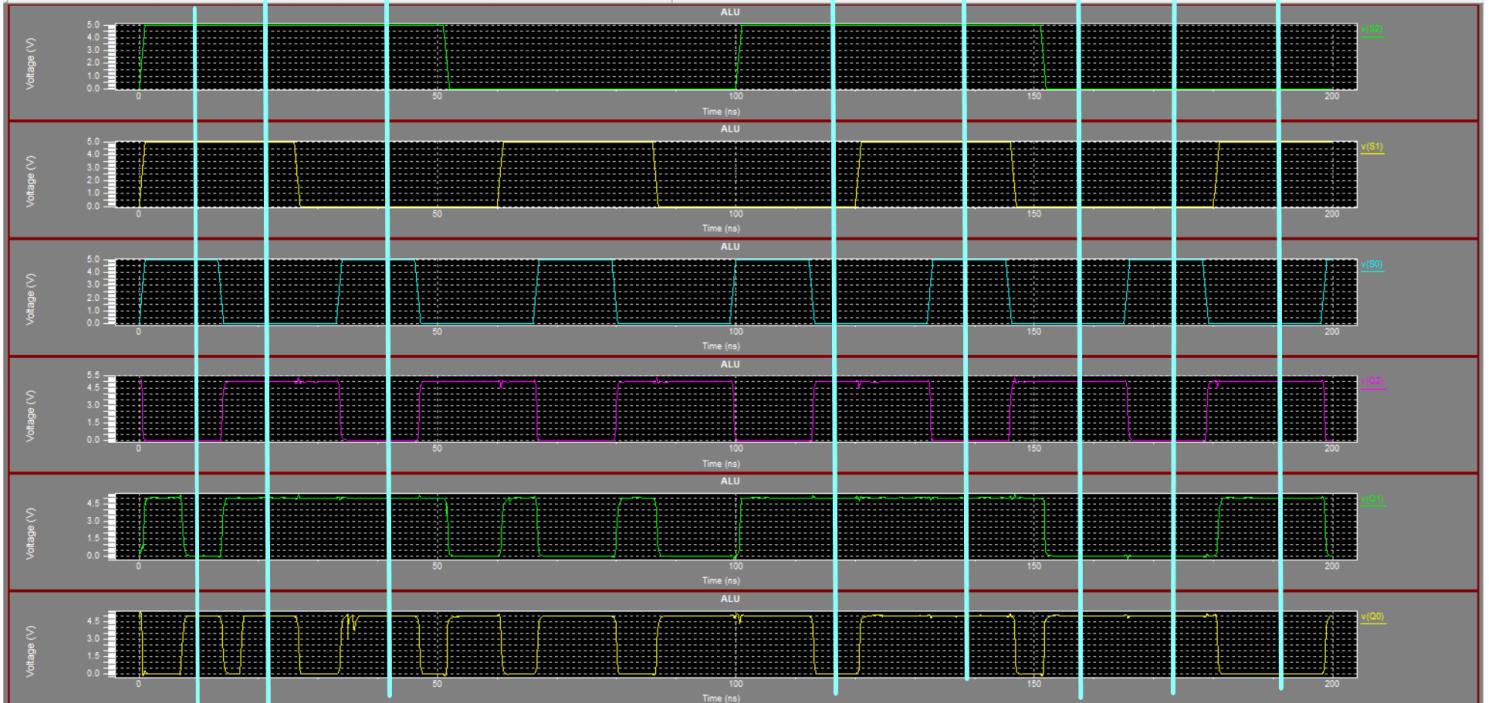
```
.print V(Q0) V(Q1) V(Q2) V(S0) V(S1) V(S2)
```

### \*\*\*\*\* Simulation Settings - Additional SPICE commands \*\*\*\*\*

```
.end
```

## W-EDIT WAVEFORM



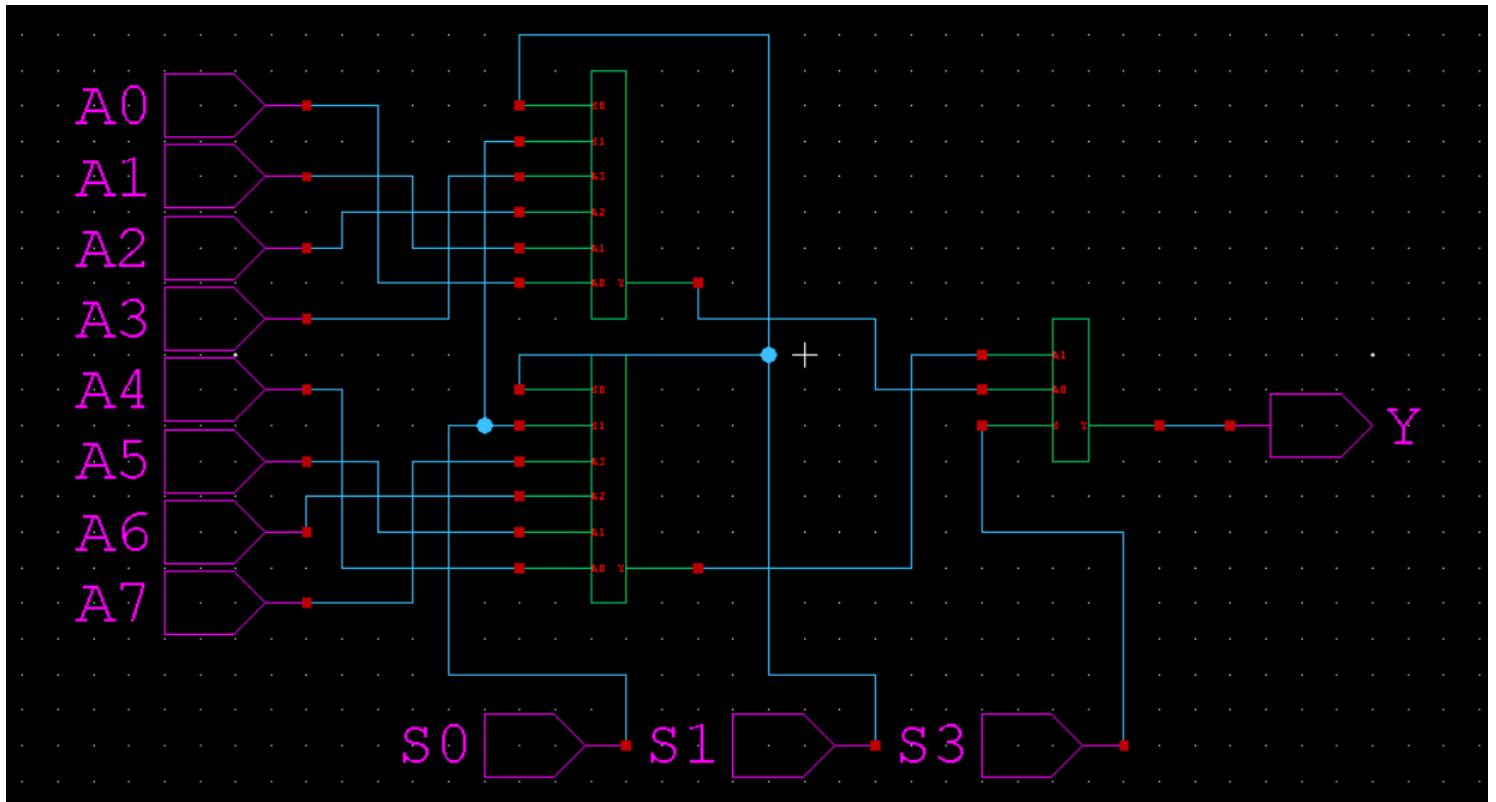


For Help, press F1



# 8 BIT MULTIPLEXER

S-EDIT



T-SPICE

```

X4X1_1 A0 A1 A2 A3 S1 S0 N_1 Gnd Vdd 4X1
X4X1_2 A4 A5 A6 A7 S1 S0 N_2 Gnd Vdd 4X1

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V

Vin1 A0 Gnd pulse(0 5v 0 1n 1n 2n 4n)
Vin2 A1 Gnd pulse(0 5v 0 1n 1n 7n 14n)
Vin3 A2 Gnd pulse(0 5v 0 1n 1n 14n 28n)
Vin4 A3 Gnd pulse(0 5v 0 1n 1n 20n 40n)
Vin5 A4 Gnd pulse(0 5v 0 1n 1n 25n 50n)
Vin6 A5 Gnd pulse(0 5v 0 1n 1n 30n 60n)
Vin7 A6 Gnd pulse(0 5v 0 1n 1n 35n 70n)
Vin8 A7 Gnd pulse(0 5v 0 1n 1n 45n 90n)

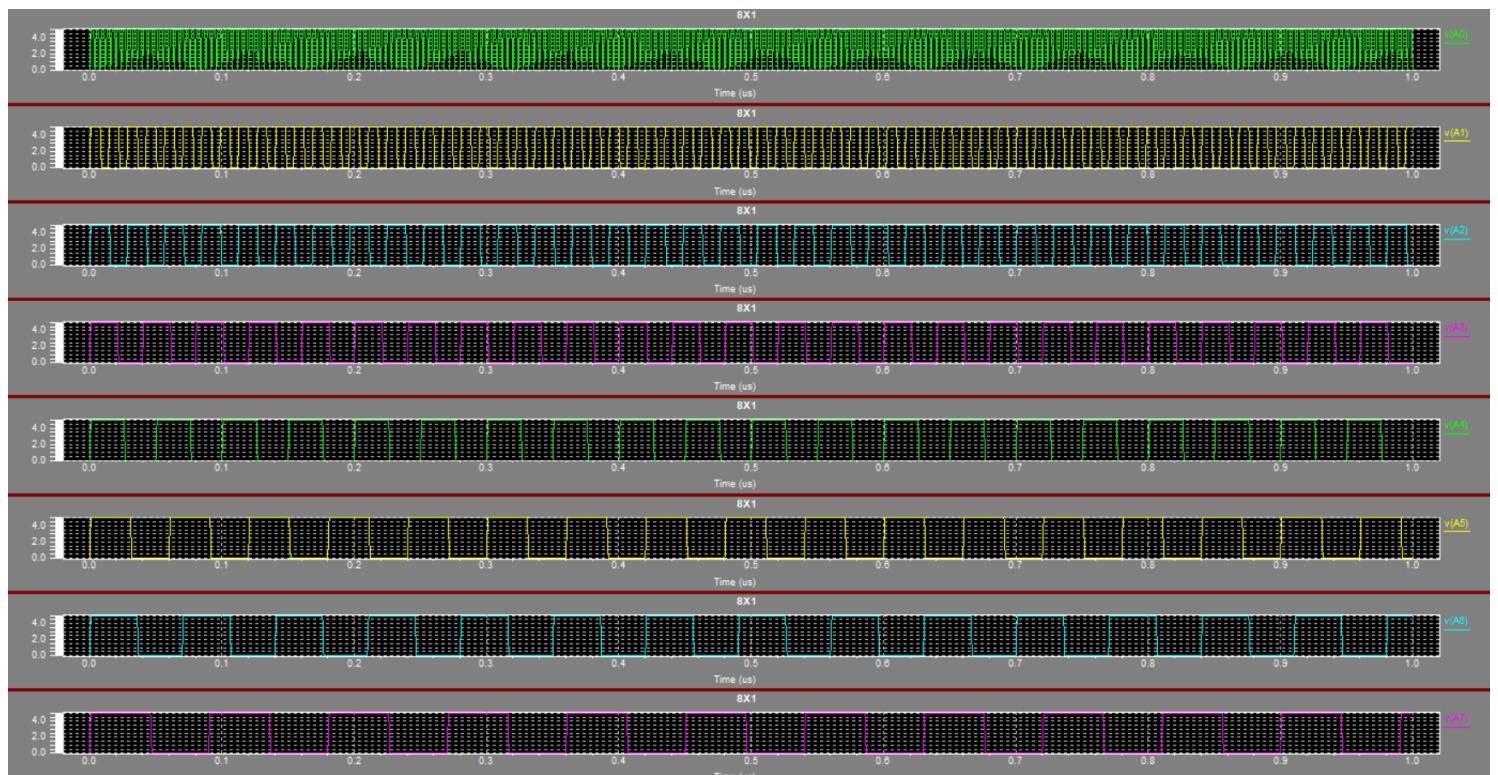
Vin9 S3 Gnd pulse(0 5v 0 1n 1n 100n 250n)
Vin10 S1 Gnd pulse(0 5v 0 1n 1n 200n 500n)
Vin11 S0 Gnd pulse(0 5v 0 1n 1n 500n 1000n)

.Tran 1ns 1000ns
**.power Vdd A 10000ns
.print V(Y) V(S0) V(S1) V(S3)
***** Simulation Settings - Additional SPICE commands *****

.end

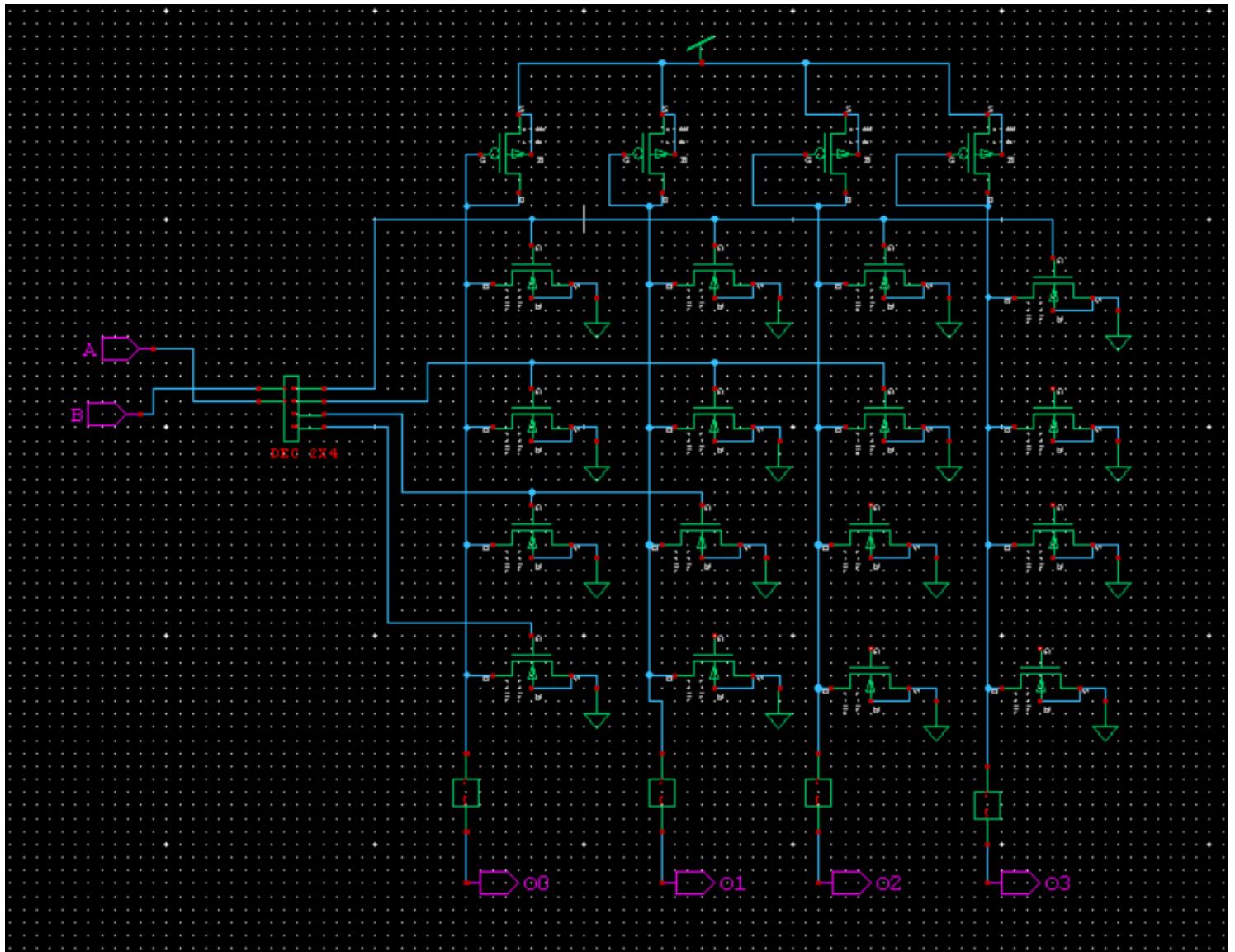
```

## W-EDIT WAVEFORM



# ROM

## S-EDIT



## T-SPICE

```

MMOSFET_N_7 N_9 N_4 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_11 N_9 N_6 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_8 N_10 N_5 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_12 N_10 N_11 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_9 N_7 N_1 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_13 N_7 N_2 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_14 N_8 N_12 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_15 N_9 N_13 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_16 N_10 N_14 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
XNOT_1 N_7 O0 Gnd Vdd NOT
XNOT_2 N_8 O1 Gnd Vdd NOT
XNOT_3 N_9 O2 Gnd Vdd NOT
XNOT_4 N_10 O3 Gnd Vdd NOT

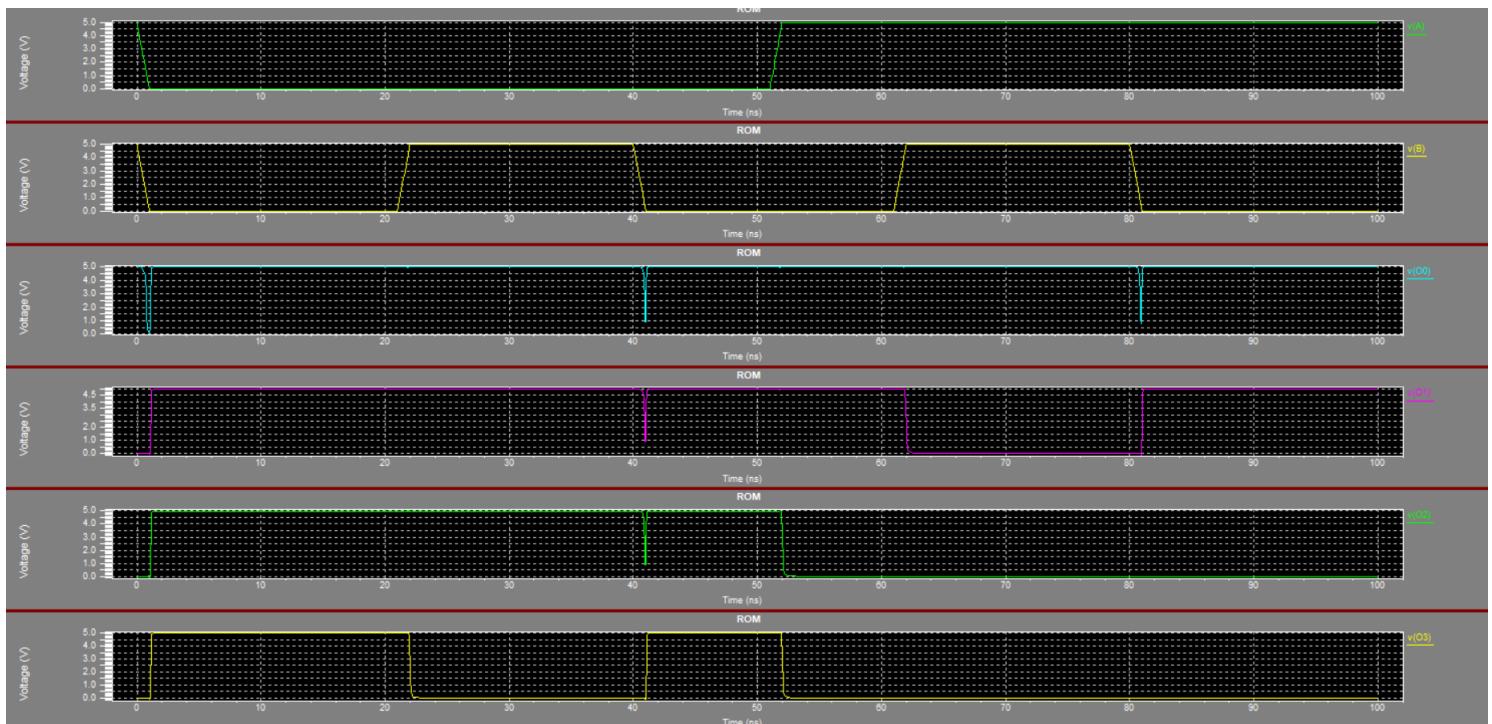
***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V
Vin1 A Gnd pulse(5v 0 0 On On 50n 100n)
Vin2 B Gnd pulse(5v 0 0 On On 20n 40n)

.Tran lns 100ns
**.power Vdd A 10000ns
.print V(O3) V(O2) V(O1) V(O0) V(B) V(A)
***** Simulation Settings - Additional SPICE commands *****

.end

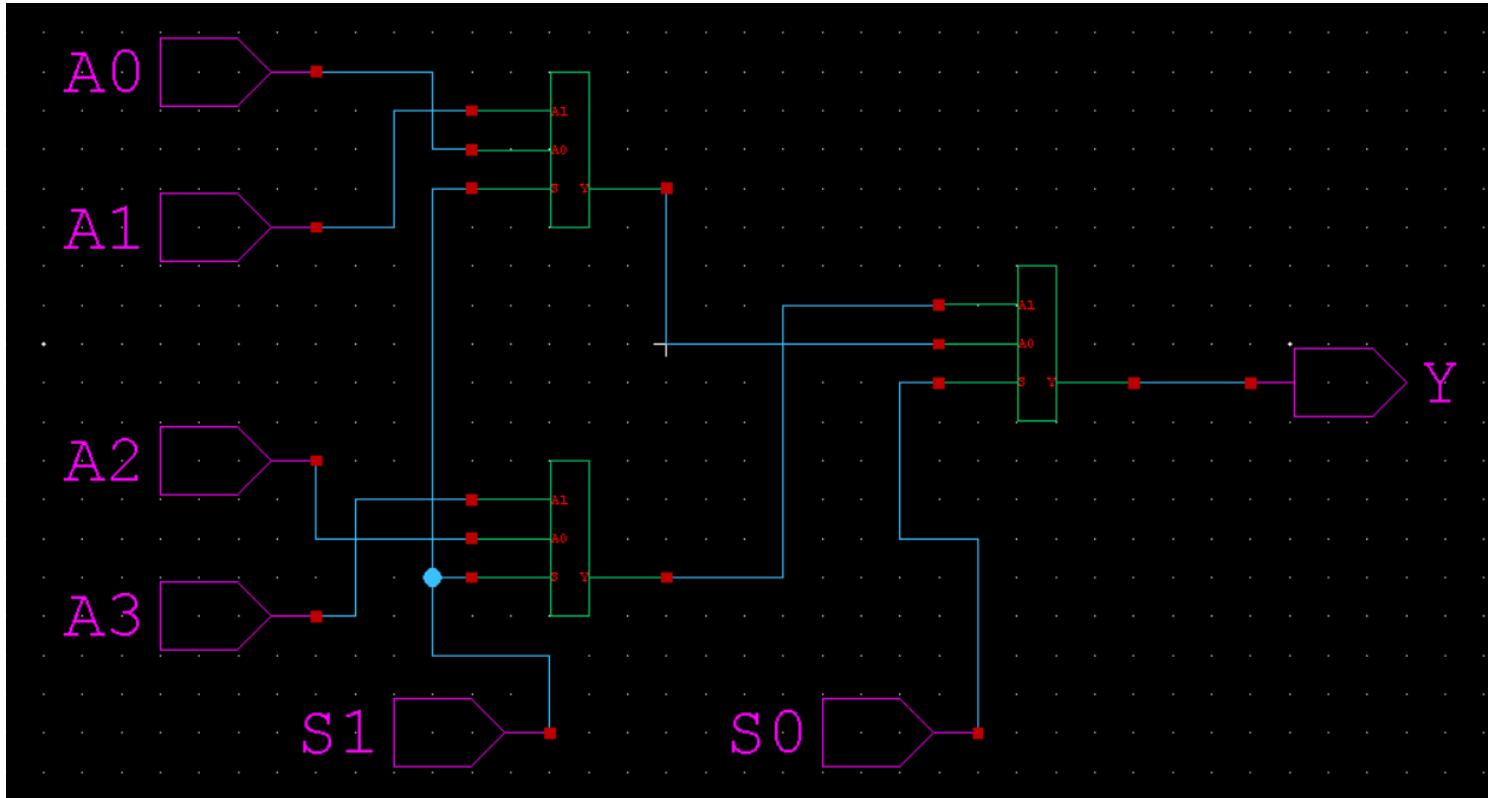
```

## W-EDIT WAVEFORM



# 4X1 MUX

## S-EDIT



## T-SPICE

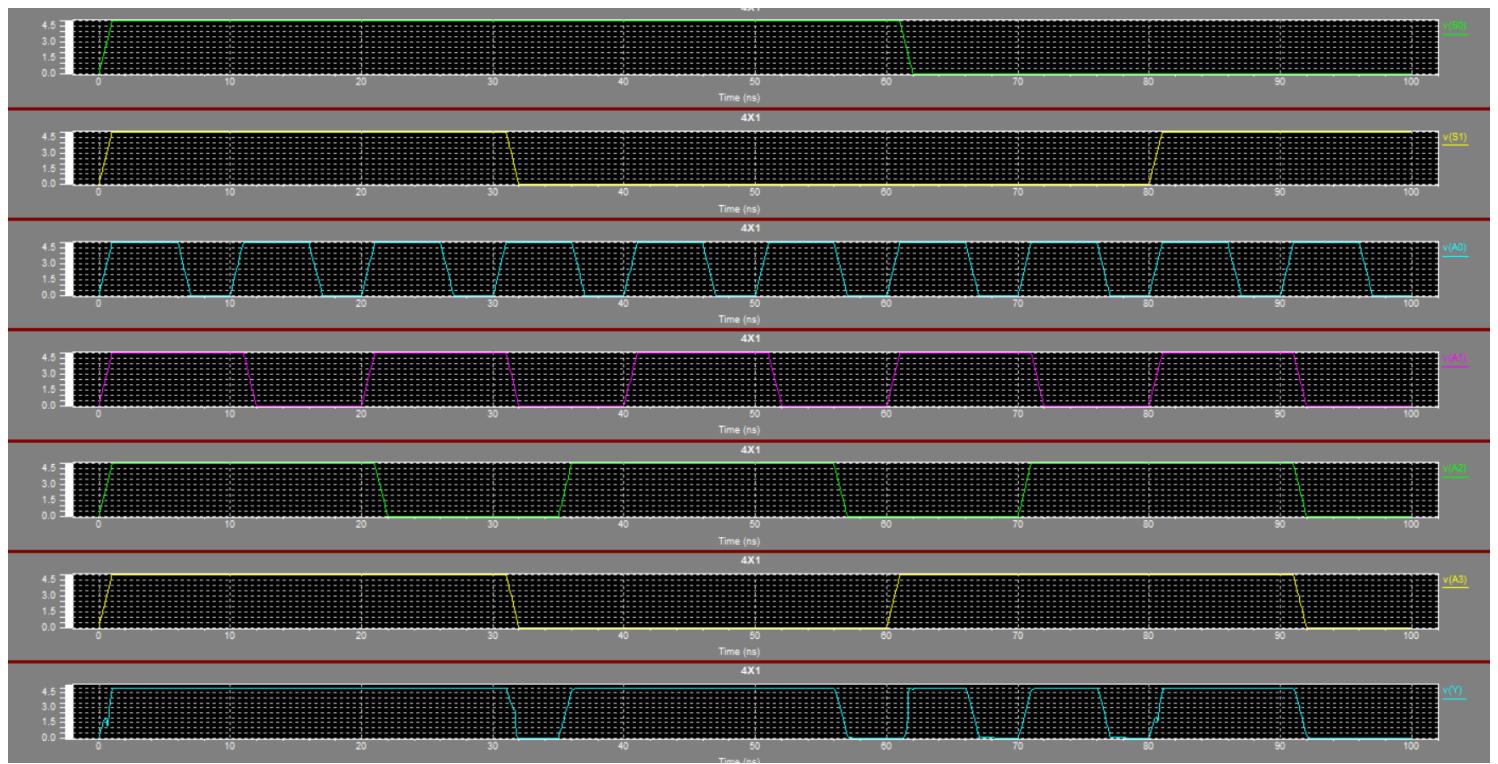
```
***** Simulation Settings - Parameters and SPICE Options *****
X2x1_1 A0 A1 S1 N_1 Gnd Vdd 2x1
X2x1_2 A2 A3 S1 N_2 Gnd Vdd 2x1
X2x1_3 N_1 N_2 S0 Y Gnd Vdd 2x1

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V
|
Vin1 A0 Gnd pulse(0 5v 0 1n 1n 5n 10n)
Vin2 A1 Gnd pulse(0 5v 0 1n 1n 10n 20n)
Vin3 A2 Gnd pulse(0 5v 0 1n 1n 20n 35n)
Vin4 A3 Gnd pulse(0 5v 0 1n 1n 30n 60n)

Vin5 S0 Gnd pulse(0 5v 0 1n 1n 60n 100n)
Vin6 S1 Gnd pulse(0 5v 0 1n 1n 30n 80n)

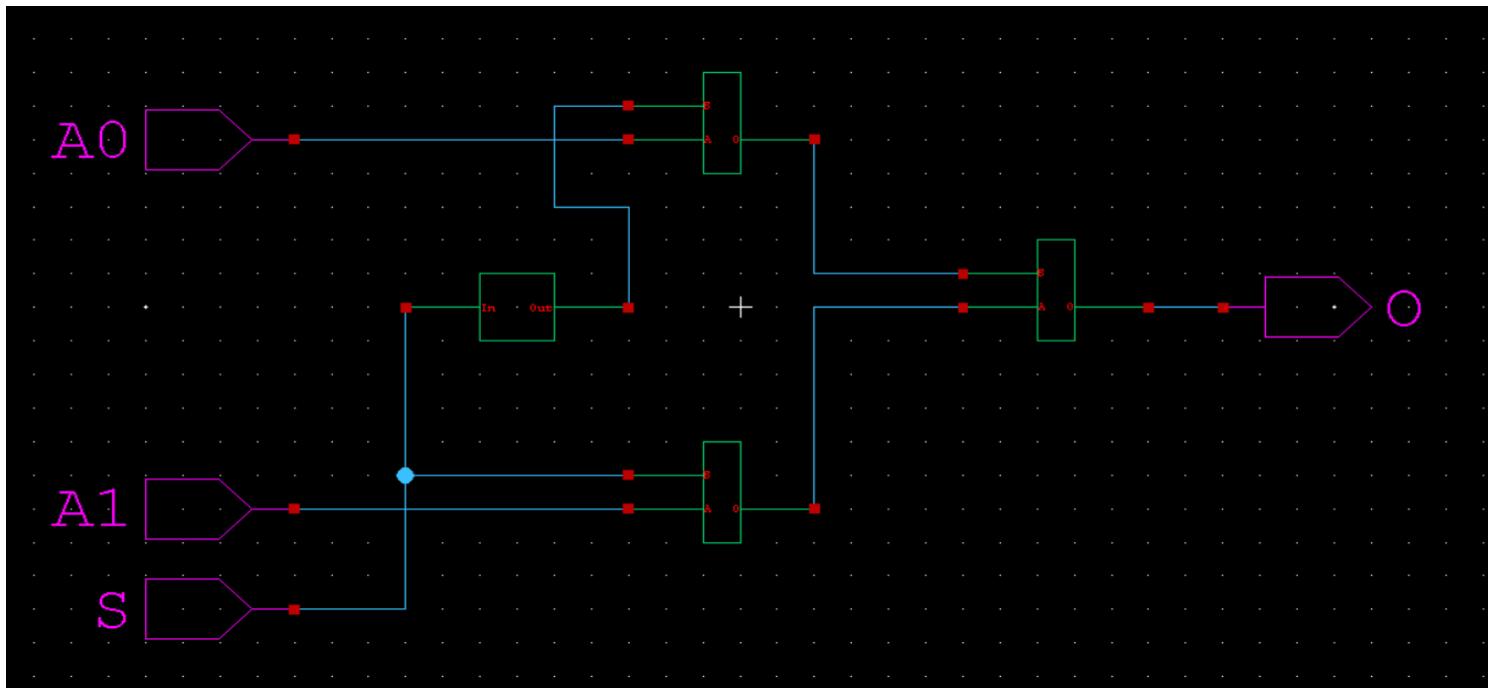
.Tran 1ns 100ns
**.power Vdd A 10000ns
.print V(Y) V(A7) V(A6) V(A5) V(A4) V(A3) V(A2) V(A1) V(A0) V(S0) V(S1) V(S3)
***** Simulation Settings - Additional SPICE commands *****
.end
```

## W-EDIT WAVEFORM

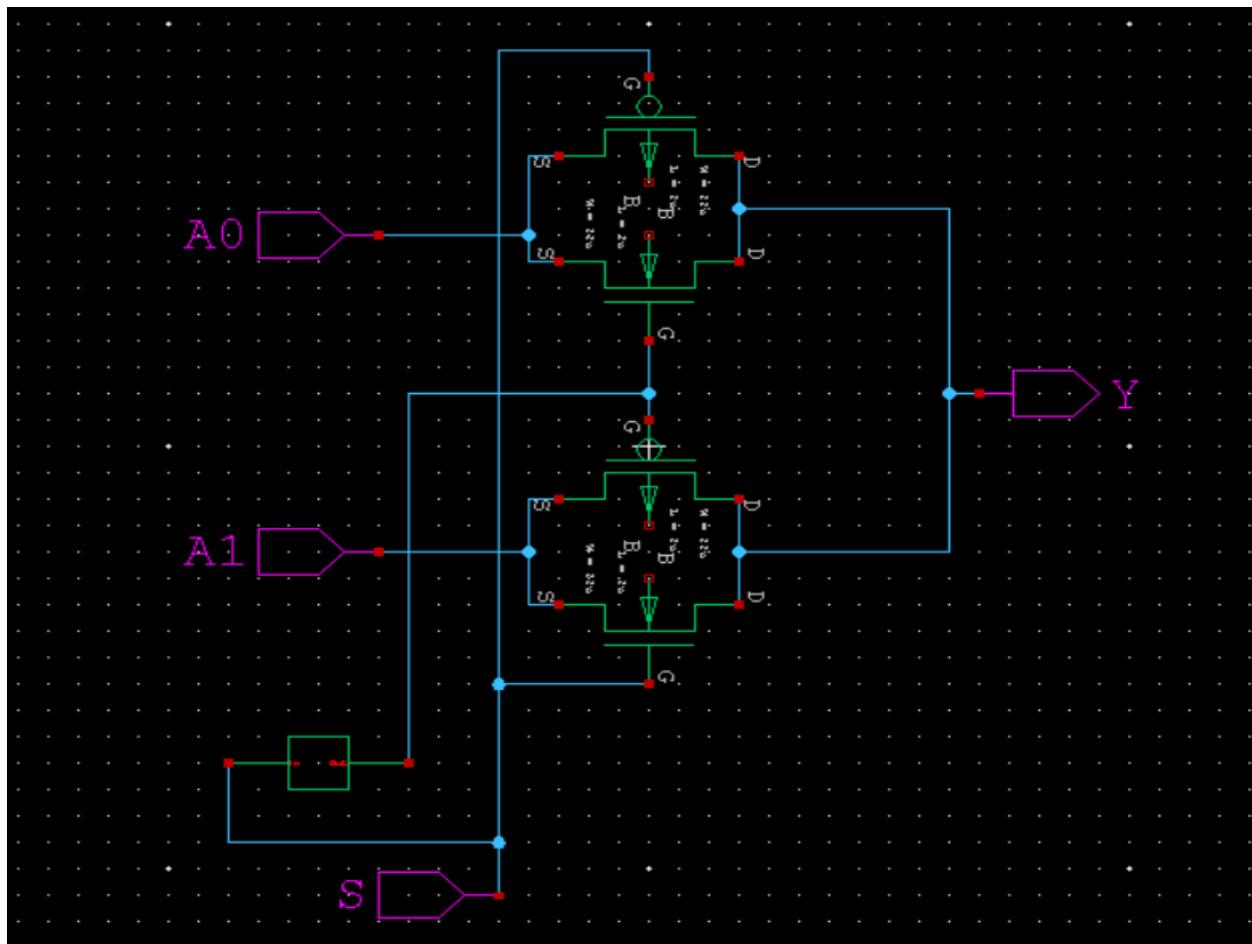


## 2X1 MUX

S-EDIT  
GATE MODEL



## TRANSITION MODEL



## T-SPICE

```
***** Simulation Settings - Parameters and SPICE Options *****

XNOT_1 S N_1 Gnd Vdd NOT
XOR_1 N_3 N_2 C Gnd Vdd OR
XAND_1 A0 N_1 N_2 Gnd Vdd AND
XAND_2 A1 S N_3 Gnd Vdd AND

***** Simulation Settings - Analysis section *****
.Model NMOS NMOS (Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V

Vin1 A0 Gnd pulse(0 5v 0 1n 1n 10n 20n)
Vin2 A1 Gnd pulse(0 5v 0 1n 1n 100n 200n)

Vin3 S Gnd pulse(0 5v 0 1n 1n 50n 100n)

.Tran 1ns 100ns
**.power Vdd A 10000ns
.print V(A0) V(A1) V(S) V(C)
***** Simulation Settings - Additional SPICE commands *****

.end
```

## W-EDIT WAVEFORM

