Optimal Structures for Voltage Controllers in Inverters

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Abstract— **Output voltage regulation is a primary performance objective in power electronics systems which are not supported by a stiff voltage source. In this paper, we pose an optimal voltage control problem for ac inverter systems and study the structure of the resulting feedback laws. Here, it is demonstrated that the solution to the optimal voltage regulation control problem exhibits an inner current-controller structure even though there are no explicit objectives on tracking current which are targeted. Furthermore, the outer-loop voltage control and inner-loop current control structure is insensitive to the weighting transfer functions used in the optimal control problem. Although the inner-outer structure has been used in prior works, the optimal nature of such a structure was not known. In deriving the optimal controller, we also present a systematic design framework which is cognizant of the physical properties of inverters. Case studies are used to study the optimal controller and its performance.**

I. INTRODUCTION

Voltage controllers form an integral component of microgrid systems, uninterruptible power supplies, dc-dc converters, and systems which are not supported by a stiff voltage source or grid. In so-called *master-slave* systems, the system voltage is supported by a single "master" power converter which typically acts on a fixed voltage reference and all remaining units regulate their currents [1]. In parallel converter systems, a centralized controller can be configured such that the voltage across a common load tracks a single reference [2], [3]. For decentralized implementations, *droop-controlled* inverters [4], [5] and dc-dc converters [6] each utilize an independent and variable voltage reference which depends on the output of each unit. Irrespective of how the voltage reference is generated, a voltage controller is needed to modulate the power electronics such that the output voltage tracks the reference. In this paper, we study the optimal structure of voltage controllers for ac inverter systems. In deriving the controller, we present a systematic design framework for designing multivariable voltage controllers with robust and optimal performance. The design framework provides a systematic means of targeting performance specifications that arise in typical ac power systems. As our main result, we show that the resulting optimal controller has an outer voltage controller and an inner current controller embedded in it. This result confirms that the inner-outer structure is optimal and substantiates the longstanding observation in conventional designs that inner-outer structures have superior performance [7]–[9].

Problems related to robust and optimal design of inverter controllers have received recent attention. In [10], [11], inverter controller parameters are obtained after solving a servomechanism robust optimization problem. The $\mathcal{H}_\infty$ framework and internal model principle were recently applied with the objective of rejecting periodic disturbances in microgrids [12], [13]. Along similar lines, optimal controllers for static VAR compensators have been investigated [14]. Here, our focus is on studying the structure of the optimal controller itself and outlining an unambiguous design procedure.

The outer-voltage inner-current control structure has a rich history in the power community and has been utilized extensively in single- and three-phase [8], [15] inverters as well as dc-dc converters [7], [9]. Going back several decades, some of the earliest uses of the inner-outer control structure are found in dc-dc converter applications [16] and was first employed due to its superior performance in comparison to single-loop controllers. Subsequent analysis and engineering judgment have indicated an inherent robustness to load variations and its application has become well-established in inverters for ac systems [8]. Despite its advantages over single-loop controllers, traditional inner-outer design methods are iterative in nature, are not tailored for multiple input systems, and do not offer performance guarantees. In contrast, the proposed method is well-suited for multivariable settings and guarantees optimality.

The main contributions of this paper are as follows: i) we demonstrate that that the optimal voltage controller has an inner-outer structure, and ii) in deriving the optimal controller, we describe a systematic design process which incorporates practical performance specifications in ac inverter systems.

The manuscript is organized in the following manner. In Section II we introduce the reader to the inverter system model, formulate the design problem, derive the plant model, and outline practical considerations for ac power electronics systems. The classical inner-outer structure is introduced and its correspondence with the optimal $\mathcal{H}_\infty$ is established in Section III. Concluding statements are in Section IV.

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Their work was supported by the Laboratory Directed Research and Development (LDRD) Program at the National Renewable Energy Laboratory and by the U.S. Department of Energy under Contract No. DE- AC36-08-GO28308.

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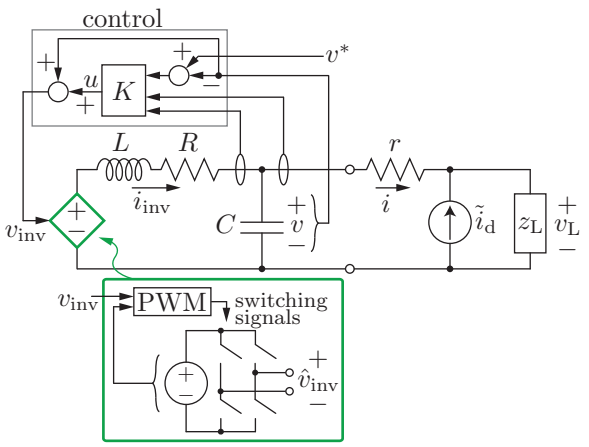

Fig. 1. A system consisting of a single-phase inverter connected across an impedance load with an LC filter and closed-loop controller. The unmodelled current source, $\tilde{i}_{\rm d}$, accounts for unknown sources and loads. The inverter hardware, shown on the bottom, produces an instantaneous switched voltage $\hat{v}_{\rm inv}$. Using averaging, the inverter is modeled as a controllable voltage source which follows the signal $v_{\rm inv}$.

II. System Model, Problem Formulation, and Control Design

A. Inverter System Description

Consider the system in Fig. 1 which consists of a power electronics inverter connected across an impedance load, $z_{\rm L}$. The inverter draws power from a dc source and generates a switched ac voltage, $\hat{v}_{\rm inv}$, which serves as a control variable. Using pulse width modulation (PWM) techniques and a high switching frequency, the switch cycle average of $\hat{v}_{\rm inv}$ follows the command $v_{\rm inv}$ [8]. The inductance, L, and capacitance, C, filter high-frequency harmonics generated by the switching action. R accounts for ohmic losses in the inductor and r is the branch resistance which interfaces the inverter terminals to the remaining system. $\tilde{i}_{\rm d}$ encapsulates the behavior of unknown loads and sources in the system and is treated as a disturbance. Since the switching period is typically much smaller than the filter time-constants, we model the switch terminals as a controllable voltage source which follows the control signal $v_{\rm inv}$. This averaged model facilitates design, modeling, and analysis.

We assume that the measured signals include the inductor current $i_{\rm inv}$, capacitor voltage v, and output branch current i. The objective is to design a feedback law that generates a voltage command, $v_{\rm inv}$, which ensures, i) v tracks v^*, ii) control performance is robust to parametric uncertainty, iii) the recovery time after disturbances and transients is small, and iv) the control signal, $v_{\rm inv}$, respects bandwidth limitations.

$\mathcal{H}_\infty$ methods provide a framework for addressing multiple objectives such as those in the previous paragraph. With this approach, a linear stabilizing control law is obtained by posing and solving an optimization problem. In the remainder of the paper, we apply the $\mathcal{H}_\infty$ framework to derive a controller $K(s)$ and subsequently show that the optimal design exhibits an inner-outer structure.

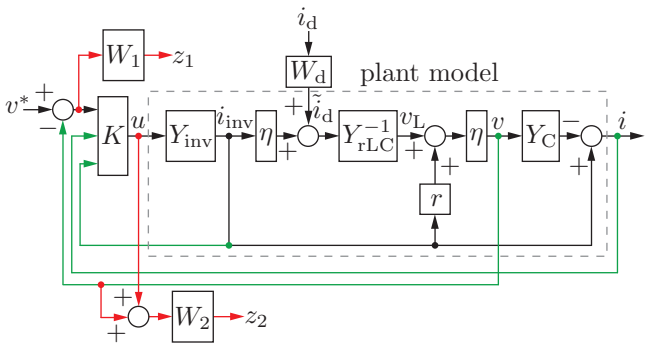

Fig. 2. Block-diagram of the inverter circuit. The regulated variables, z_1 and z_2, are shown in red and the measurements are shown in green.

B. Problem Formalization

We denote i) the *external input* as $w(s)$[1] where $w(s) = i_{\rm d}(s)$ for the system in Fig. 1, ii) the *control input* as $u(s) = v_{\rm inv}(s) - v(s)$ for the single inverter system, iii) the *regulated output* as $z(s)$ and we pick $z(s) = [W_1(s)(v^*(s) - v(s)), W_2(s)v_{\rm inv}(s)]^\top$ where $W_1(s)$ and $W_2(s)$ are user-defined weighting transfer functions, and iv) the *measured output* as $y(s)$ where $y(s) = [v^*(s) - v(s), i(s), i_{\rm inv}(s)]^\top$ for the inverter circuit. The physical configuration for this system is shown in Fig. 1.

The inductor current is given by

$$i_{\rm inv}(s) = Y_{\rm inv}(s)\left(v_{\rm inv}(s) - v(s)\right), \tag{1}$$

where $Y_{\rm inv}(s) := (sL + R)^{-1}$. The load voltage can be expressed as

$$v_{\rm L}(s) = \left(\eta(s) i_{\rm inv}(s) + \tilde{i}_{\rm d}(s)\right) Y_{\rm rLC}^{-1}(s), \tag{2}$$

where we define

$$\eta(s) := \frac{z_{\rm C}(s)}{z_{\rm C}(s) + r}, \tag{3}$$

$$Y_{\rm rCL}(s) := Y_{\rm C}(s)\eta(s) + Y_{\rm L}(s), \tag{4}$$

and $Y_{\rm C}(s) := z_{\rm C}^{-1}(s) = sC$. Along similar lines, the capacitor voltage can be written as

$$v(s) = \left(r i_{\rm inv}(s) + v_{\rm L}(s)\right)\eta(s). \tag{5}$$

Lastly, the capacitor state-equation can be rearranged to yield

$$i(s) = i_{\rm inv}(s) - Y_{\rm C}(s)v(s). \tag{6}$$

Using (1)–(6), recalling $u(s) = v_{\rm inv}(s) - v(s)$ and $z(s) = [W_1(s)(v^*(s) - v(s)), W_2(s)v_{\rm inv}(s)]^\top$, the block-diagram of the inverter circuit with the regulated variables is given in Fig. 2. Note that the transfer function, $W_{\rm d}(s)$ is a user-defined transfer function which defines the expected frequency range of disturbances.

[1]From here forward, $s = \sigma + {\rm j}\omega$ is a complex variable and proper transfer functions are assumed throughout.

The mapping from inputs $w(s)$ and $u(s)$ to outputs $z(s)$ and $y(s)$ is given as:

$$\begin{bmatrix} W_1(s)(v^*(s)-v(s)) \\ \hdashline \frac{W_2(s)v_{\rm inv}(s)}{v^*(s)-v(s)} \\ \hdashline i(s) \\ i_{\rm inv}(s) \end{bmatrix} = G(s) \begin{bmatrix} \frac{i_{\rm d}(s)}{v_{\rm inv}(s)-v(s)} \\ \hdashline \end{bmatrix}, \tag{7}$$

where, the generalized plant transfer matrix is

$$\underbrace{\left[\begin{array}{c|c} -\frac{W_1(s)W_{\rm d}(s)\eta(s)}{Y_{\rm rLC}(s)} & -\frac{W_1(s)\eta(s)(1+rY_{\rm L}(s))Y_{\rm inv}(s)}{Y_{\rm rLC}(s)} \\ \frac{W_2(s)W_{\rm d}(s)\eta(s)}{Y_{\rm rLC}(s)} & W_2(s)\left(1+\frac{\eta(s)(1+rY_{\rm L}(s))Y_{\rm inv}(s)}{Y_{\rm rLC}(s)}\right) \\ \hline -\frac{\eta(s)}{Y_{\rm rLC}(s)} & -\frac{\eta(s)(1+rY_{\rm L}(s))Y_{\rm inv}(s)}{Y_{\rm rLC}(s)} \\ -\frac{\eta(s)Y_{\rm c}(s)}{Y_{\rm rLC}(s)} & \frac{\eta(s)Y_{\rm L}(s)Y_{\rm inv}(s)}{Y_{\rm rLC}(s)} \\ 0 & Y_{\rm inv}(s) \end{array}\right]}_{=G(s)}. \tag{8}$$

The derivation of (8) is summarized in Appendix-A. Having obtained $G(s)$, the controller $K(s)$ can be found after specifying the user-defined transfer functions $W_1(s)$, $W_2(s)$, and $W_{\rm d}(s)$ and solving the $\mathcal{H}_\infty$ design problem.

Remark 1: Although the load is generally unknown and does not have static parameters, an estimate of the load admittance can be utilized in the plant model. Subsequently, we show robust performance to load variations.

C. Design of Weighting Transfer Functions

Here, we outline a set of guidelines for designing the cost transfer functions which encapsulate practical performance objectives and system properties.

1) Voltage regulation function $W_1(s)$: Referring to the first row in (7), it is apparent that $W_1(s)$ has a direct relationship on the voltage tracking error. Accordingly, $W_1(s)$ is designed such that tracking error at the nominal ac frequency, $\omega_{\rm o}$, is minimized, the resonant behavior of the inverter LC filter is damped by the controller, and performance within the inverter bandwidth is emphasized. Accordingly, $W_1(s)$ can be ascribed the following general form:

$$W_1(s) = \kappa_1 G_{\omega{\rm o}}(s) G_{\rm rlc}(s) G_{\rm bw}(s), \tag{9}$$

where κ_1 is an overall gain factor, $G_{\omega{\rm o}}(s)$ is tuned such that it has a large amplitude at $\omega_{\rm o}$, $G_{\rm rlc}(s)$ damps out the resonant behavior of the RLC elements in the filter, and $G_{\rm bw}(s)$ emphasizes performance within the inverter bandwidth.[2] $G_{\omega{\rm o}}(s)$ can be written as the superposition of a band-pass and notch filter with the following expression

$$G_{\omega{\rm o}}(s) = \frac{\kappa_{\rm N} s^2 + 2\kappa_{\rm BP}\zeta\omega_{\rm o} s + \kappa_{\rm BP}\omega_{\rm o}^2}{s^2 + 2\zeta\omega_{\rm o} s + \omega_{\rm o}^2}, \tag{10}$$

where $\kappa_{\rm N}$ and $\kappa_{\rm BP}$ are the gains of the notch and bandpass components, respectively, and ζ is the damping factor. Since we wish to emphasize performance at the rated frequency, $\omega_{\rm o}$, we must pick $\kappa_{\rm BP} > \kappa_{\rm N}$. For variable frequency ac systems, it may be necessary to increase ζ to broaden the frequency range where $G_{\omega{\rm o}}(s)$ is large. This approach of emphasizing the controller response at the rated system frequency is similar to the widely used *proportional-resonant* controller for ac systems [20], [21].

Undesired inverter filter resonance can be mitigated by including a model of the filter within $G_{\rm rlc}(s)$. Referring to Fig. 1, denote the parallel impedance of the RL branch and capacitor as $z_{\rm f}(s) := (R+sL)\,\|\,(sC)^{-1}$. We ascribe $G_{\rm rlc}(s)$ the following form:

$$G_{\rm rlc}(s) = (z_{\rm f}(s)+1)\,\frac{\rm den(z_f(s))}{\alpha(s)}. \tag{11}$$

In practice, the output filter is designed with minimal resistive losses such that high efficiency is maintained. Consequently, $z_{\rm f}(s)$ usually exhibits a tight peak at $1/\sqrt{LC}$ and small gain at all other frequencies. To provide robustness to parameter variations (typical filter component tolerances are $\pm 10\%$) we wish to damp frequencies around $1/\sqrt{LC}$ by tuning $G_{\rm rlc}(s)$. Towards that end, $\rm den(z_f(s))/\alpha(s)$ is selected to attain the desired response around $1/\sqrt{LC}$ and the addition of 1 in the first factor of (11) flattens the gain to unity at asymptotically high and low frequencies.

Reference tracking at frequencies within the inverter bandwidth can be further enhanced by including the transfer function, $G_{\rm bw}(s)$. Specifically, to ensure $W_1(s)$ does not emphasize high frequencies which cannot be realized by the hardware, $G_{\rm bw}(s)$ can be selected as a low-pass filter. Here, we pick

$$G_{\rm bw}(s) = \left(\omega_{\rm lpf}/\left(s+\omega_{\rm lpf}\right)\right)^2. \tag{12}$$

Lastly, the overall gain factor, κ_1, in (9) is proportional to the voltage regulation aggressiveness of the controller and can be tuned accordingly.

2) Inverter voltage control effort weighting function $W_2(s)$: Referring to (7), it follows that $W_2(s)$ corresponds to shaping the performance of $v_{\rm inv}$. Since there are no corresponding reference signals to track, $W_2(s)$ can be designed to suppress high-frequency control effort. Accordingly, a high-pass filter or a related variation can be used as given below

$$W_2(s) = W_3(s) = \frac{c_1 s + \omega_{\rm w}}{s + c_2\omega_{\rm w}}, \tag{13}$$

where c_1 and c_2^{-1} are the asymptotic gains at high frequencies and dc, respectively, and $c_1\omega_{\rm w}$ and c_2^{-1} are the frequency breakpoints.

3) Disturbance current transfer function $W_{\rm d}(s)$: The function, $W_{\rm d}(s)$, characterizes the response of expected disturbances. For systems with linear loads, we can assume that disturbance currents have components primarily at $\omega_{\rm o}$. However, if nonlinear disturbances, such as diode rectifier loads and switching power supplies, are anticipated, $W_{\rm d}(s)$ can be chosen to emphasize higher order harmonics. If the frequency content of unmodelled loads is anticipated, $W_{\rm d}(s)$ can be chosen accordingly. For instance, the harmonics of rectifier loads are well characterized in [18], [19]. Here, we choose this function as a low-pass filter (i.e., $W_{\rm d}(s) =$

[2] In practice, the inverter bandwidth is limited by the switching frequency, sampling frequency, and time-step size of the digital controller.

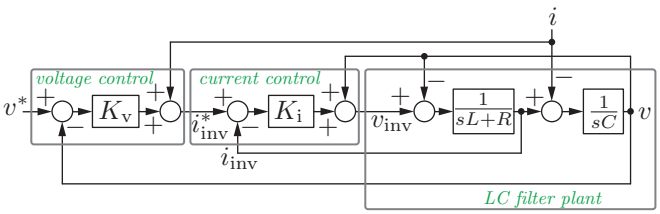

Fig. 3. Conventional voltage controller with an inner-outer structure.

$1/\left(\omega_\mathrm{d}^{-1}s+1\right)$) such that low-order harmonic rejection is emphasized.

III. Optimal Control Structure and Performance

In this section, we first introduce the classical voltage controller and subsequently demonstrate its correspondence with the proposed $\mathcal{H}_\infty$ design.

A. The Outer-Voltage Inner-Current Control Structure

Consider the well-known voltage controller in Fig. 3 which exhibits an inner-outer structure [7], [8], [15]. In this classical system, an outer voltage controller, $K_\mathrm{v}(s)$, generates a reference, $i^*_\mathrm{inv}(s)$, for an inner current controller, $K_\mathrm{i}(s)$. The feedforward terms, $i(s)$ and $v(s)$, are used to cancel signals which act as disturbances in the LC filter plant. The intuition behind this design is that the inner current controller allows for direct control of the energy delivered by the inductor without introducing delays from the capacitor. The architecture in Fig. 3 dates back several decades [16]. Referring to Fig. 3, the current controller output can be written as

$$\begin{aligned} &v_\mathrm{inv}(s)-v(s)\\ &=K_i(s)\left(i^*_\mathrm{inv}(s)-i_\mathrm{inv}(s)\right)\\ &=K_\mathrm{v}(s)K_i(s)\left(v^*(s)-v(s)\right)+K_\mathrm{i}(s)\left(i(s)-i_\mathrm{inv}(s)\right) \end{aligned} \quad (14)$$

Next, let's consider the $\mathcal{H}_\infty$ controller, $K(s)$, that we designed in Section II. This controller has inputs $[v^*(s)-v(s), i(s), i_\mathrm{inv}(s)]^\top$ and output signal is $u(s)=v_\mathrm{inv}(s)-v(s)$.[3] Denote the controller transfer matrix entries as $K(s)=[K_{ue}(s), K_{ui}(s), K_{u\mathrm{inv}}(s)]$, where $K_{ue}(s)$ is the transfer function between the voltage error and control signal, $K_{ui}(s)$ processes the output current measurement, and $K_{u\mathrm{inv}}(s)$ corresponds to the inverter inductor current. If $K_{ui}(s)\approx -K_{u\mathrm{inv}}(s)$, it follows that

$$\begin{aligned} u(s)&:=v_\mathrm{inv}(s)-v(s)\\ &=K_{ue}(s)\left(v^*(s)-v(s)\right)+K_{ui}(s)i(s)+K_{u\mathrm{inv}}(s)i_\mathrm{inv}(s)\\ &\approx K_{ue}(s)\left(v^*(s)-v(s)\right)+K_{ui}(s)\left(i(s)-i_\mathrm{inv}(s)\right). \end{aligned} \quad (15)$$

Comparing (15) and (14), it is apparent that if $K_{ui}(s)\approx -K_{u\mathrm{inv}}(s)$ holds, then the $\mathcal{H}_\infty$ controller, $K(s)$, has the same structure as the classical controller in Fig. 3. This leads us to the main result of the paper.

[3]The decision to pick $u(s)=v_\mathrm{inv}(s)-v(s)$ becomes clear since this provides an intrinsic voltage feedforward.

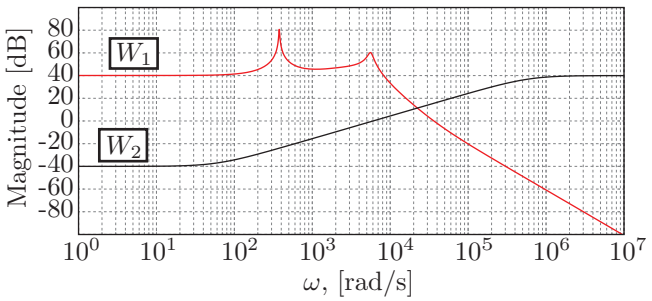

Fig. 4. The user-defined weights, as defined in Section II-C, are illustrated for the case $L=1\,\mathrm{mH}$, $C=22\,\mu\mathrm{F}$, and $R=10\,\mathrm{m}\Omega$. The peaks in $W_1(s)$ correspond to the rated system frequency and resonant frequency of the output filter. Here we illustrate the case when the performance coefficient is $\kappa_1=10^2$

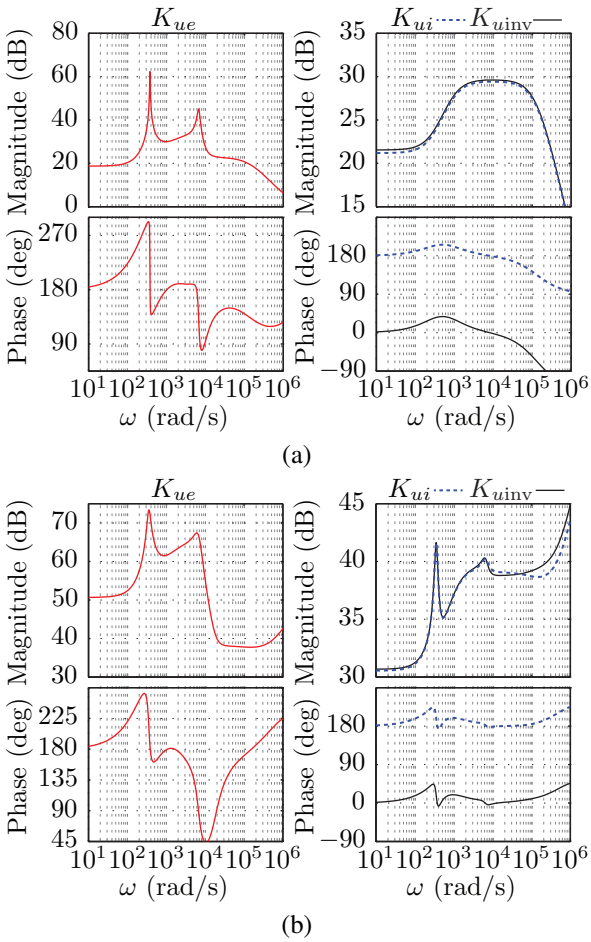

Fig. 5. Responses of the controller for filter parameters $L=1\,\mathrm{mH}$, $C=22\,\mu\mathrm{F}$, and $R=10\,\mathrm{m}\Omega$ when (a) $\kappa_1=10^2$, and (b) $\kappa_1=10^4$. The voltage tracking error to control signal transfer function is shown on the left. The responses from the output and inductor currents to control signal are given on the right. Note that the magnitudes of the currents-to-control transfer functions coincide over most of the frequency range and the phases are separated by 180°. Here, the optimality of a control architecture with an "outer" voltage controller and "inner" current controller is implied.

B. Optimality of inner current control and outer voltage control configuration

Given the generalized plant matrix in (8), the weighting transfer functions in (9)–(13), and the parameters in Table

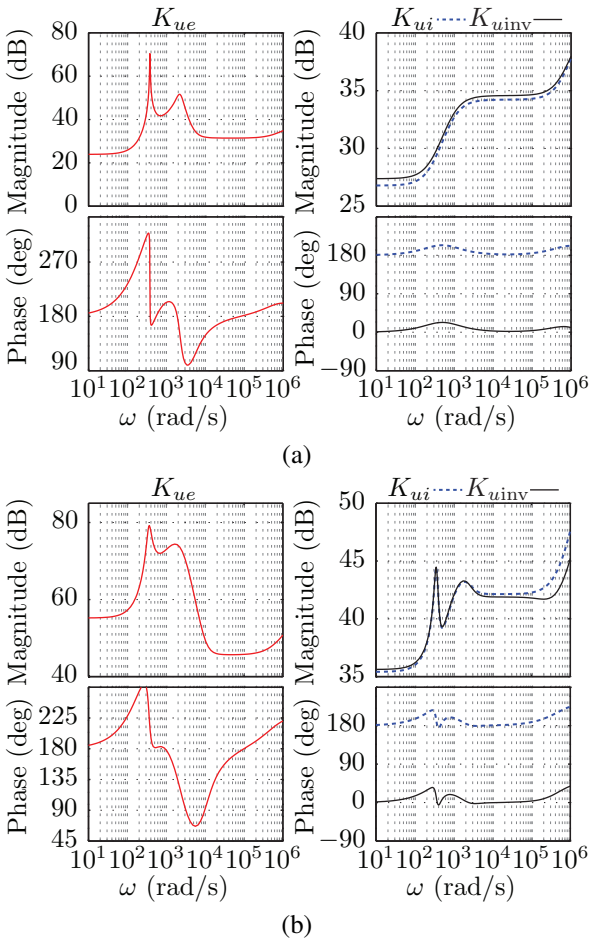

Fig. 6. Responses of the controller for filter parameters $L = 3\,\text{mH}$, $C = 66\,\mu\text{F}$, and $R = 30\,\text{m}\Omega$ when (a) $\kappa_1 = 10^2$, and (b) $\kappa_1 = 10^4$. As shown, the inner-outer structure remains despite variations in the filter parameters and control gains.

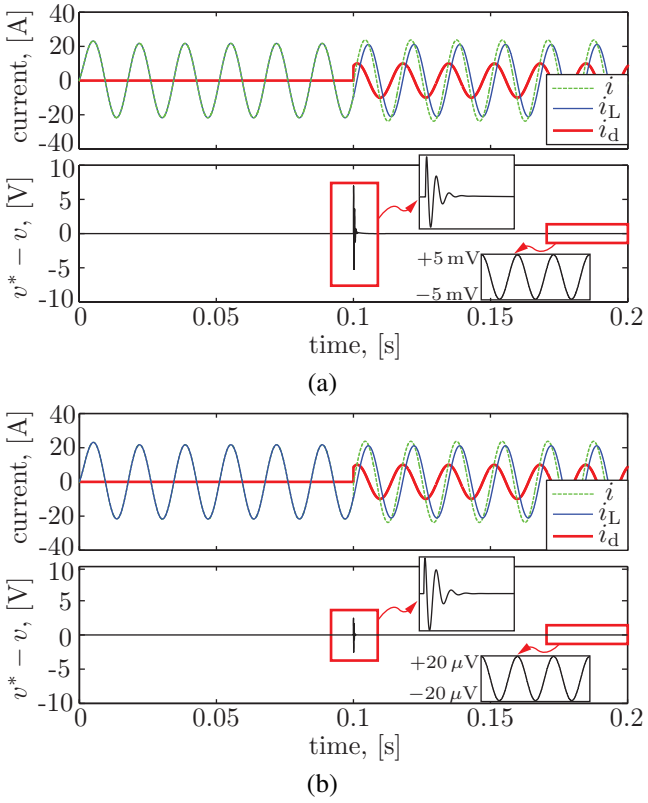

Fig. 7. A comparison of disturbance rejection for filter parameters $L = 1\,\text{mH}$, $C = 22\,\mu\text{F}$, and $R = 10\,\text{m}\Omega$ when, (a) the weighting coefficient $\kappa_1 = 10^2$, and (b) $\kappa_1 = 10^4$. In the simulation, a sinusoidal current disturbance is abruptly started at $t = 0.1\,\text{s}$. As illustrated, the controller with the larger coefficient in $W_1(s)$ reduces the error amplitude during transients and reaches a lower steady-state error. Note that the error during the transient exhibits oscillatory behavior at the filter resonant frequency.

1, the controller, $K(s)$, is obtained after solving the $\mathcal{H}_\infty$ design problem. As illustrated in Fig. 4, the voltage tracking weighting transfer function, $W_1(s)$, has peaks at $2\pi 60\,\text{rad/s}$ and $1/\sqrt{LC}$. The transfer function, $W_2(s)$, exhibits a high-pass characteristic. Having obtained the controller, we now study the responses of $K_{ui}(s)$ and $K_{uinv}(s)$.

As shown in, Figs. 5 and 6, the control response to both current measurements is similar in magnitude over a broad frequency range and they exhibit a 180^o phase shift between each other. This result confirms $K_{ui}(s) \approx -K_{uinv}(s)$ which implies the relationship in (15) and establishes a correspondence with the conventional inner-outer response in (14). This observation holds for parametric variations in the plant output filter and the controller gains. In particular, the L, C, and R filter values in Figs. 5 and 6 differ by a factor of 3 and the respective subplots utilize a weighting coefficient κ_1 that varies by a factor of 100. This provides strong evidence that $K_{ui}(s) \approx -K_{uinv}(s)$ holds over a broad set of conditions. *It is worth noting and especially interesting that the inner-current controller appears despite the exclusion of current as a regulated variable.*

C. Time-Domain Performance

Here we analyze the time-domain performance of the system in Fig. 1 with the optimal controller. In the generalized plant matrix, a nominal parallel RL load is assumed which consumes $1\,\text{kW}$ of real power with a power factor of 0.8. A sinusoidal voltage reference is utilized where $v^*(t) = 120\sqrt{2}\sin(\omega_\text{o} t)$.

We observe the case when a disturbance current, i_d, is injected into the load. Referring to Fig. 7, the inverter is initially delivering power to the nominal load. At $t = 0.1\,\text{s}$, a sinusoidal disturbance current with amplitude $10\,\text{A}$ and 120^o phase shift is initiated. To illustrate how controller performance is easily adjusted by tuning the weighting transfer functions, we compare voltage regulation when the performance coefficient κ_1 in (9) is adjusted. In Figs. 7(a) and 7(b), κ_1 is assigned a value of 10^2 and 10^4, respectively. In comparing the response of the two systems, it is evident that the controller with the larger value of κ_1 yields a smaller voltage tracking error during both transients and in steady-state.

IV. Conclusion

Here, we studied the optimal structure of voltage controllers for inverters. It was shown that the optimal con-

TABLE I

PLANT AND CONTROLLER PARAMETERS.

$R = 10\,\mathrm{m\Omega}, 30\,\mathrm{m\Omega}$	$r = 1\,\Omega$
$C = 22\,\mu\mathrm{F}, 66\,\mu\mathrm{F}$	$L = 1\,\mathrm{mH}, 3\,\mathrm{mH}$
$Y_{\mathrm{L(nom)}}^{-1} = 12\,\Omega + s(42.4\,\mathrm{mH})$	$\kappa_1 = 10^2, 10^4$
$\kappa_{\mathrm{N}} = 1$	$\kappa_{\mathrm{BP}} = 10^2$
$\zeta = 0.01$	$\alpha(s) = LCs^2 + 100RCs + 1$
$\omega_{\mathrm{lpf}} = 8\omega_{\mathrm{o}}$	$c_1 = c_2 = 0.01$
$\omega_{\mathrm{w}} = 4\omega_{\mathrm{o}}$	$\omega_{\mathrm{d}} = 3\omega_{\mathrm{o}}$

troller, obtained via $\mathcal{H}_\infty$ synthesis, contains outer-voltage and inner-current control loops embedded in it. This result is obtained despite variations in the design parameters and the intentional exclusion of current design specifications. This suggests that the optimality of the inner-outer structure holds over a wide parameter space and is generally applicable. As part of future efforts, an analytical proof of the inner-outer structure is in progress.

APPENDIX

A. Computation of $G(s)$

$v^*(s) - v(s)$ is given by

$$\begin{aligned} &v^*(s) - v(s) \\ &= v^*(s) - \left(\frac{\eta(s)}{Y_{\mathrm{rLC}}(s)}\right) i_{\mathrm{d}}(s) \\ &\quad - \left(\frac{\eta(s)\left(1 + rY_{\mathrm{L}}(s)\right) Y_{\mathrm{inv}}(s)}{Y_{\mathrm{rLC}}(s)}\right) \left(v_{\mathrm{inv}}(s) - v(s)\right), \end{aligned} \quad (16)$$

where the final expression follows from

$$r + \eta(s) Y_{\mathrm{rLC}}^{-1}(s) = Y_{\mathrm{rLC}}^{-1}(s)\left(1 + rY_{\mathrm{L}}(s)\right), \quad (17)$$

and $Y_{\mathrm{L}}(s) := z_{\mathrm{L}}^{-1}(s)$. (16) accounts for the first and third rows of $G(s)$ in (7).

The inverter voltage can be written in terms of $i_{\mathrm{d}}(s)$ and $(v_{\mathrm{inv}}(s) - v(s))$ as given below:

$$\begin{aligned} &v_{\mathrm{inv}}(s) \\ &= \frac{W_{\mathrm{d}}(s)\eta(s)}{Y_{\mathrm{rLC}}(s)} i_{\mathrm{d}}(s) + \\ &\left(1 + \frac{\eta(s)\left(1 + rY_{\mathrm{L}}(s)\right) Y_{\mathrm{inv}}(s)}{Y_{\mathrm{rLC}}(s)}\right) \left(v_{\mathrm{inv}}(s) - v(s)\right), \end{aligned} \quad (18)$$

The result in (18) corresponds to the second row of (7).

Along similar lines, the inverter output current can be expressed as

$$\begin{aligned} &i(s) \\ &= -\left(\frac{W_{\mathrm{d}}(s)\eta(s)Y_{\mathrm{c}}(s)}{Y_{\mathrm{rLC}}(s)}\right) i_{\mathrm{d}}(s) \\ &\quad + \left(\frac{\eta(s)Y_{\mathrm{L}}(s)Y_{\mathrm{inv}}(s)}{Y_{\mathrm{rLC}}(s)}\right) \left(v_{\mathrm{inv}}(s) - v(s)\right), \end{aligned} \quad (19)$$

where we utilized the fact that

$$1 - rY_{\mathrm{c}}(s)\eta(s) - \frac{\eta^2(s)Y_{\mathrm{c}}(s)}{Y_{\mathrm{rLC}}(s)} = \frac{\eta(s)Y_{\mathrm{L}}(s)}{Y_{\mathrm{rLC}}(s)}. \quad (20)$$

The fourth row of $G(s)$ is characterized using (19) and the last row is given by (1).

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