Robust Control Framework for Time-Varying Power-Sharing among Distributed Energy Resources

Mayank Baranwal[1,a] and Srinivasa M. Salapaka[1,b]

Abstract— One of the most important challenges facing an electric grid is to incorporate renewables and distributed energy resources (DERs) to the grid. Because of the associated uncertainties in power generations and peak power demands, opportunities for improving the functioning and reliability of the grid lie in the design of an efficient, yet pragmatic distributed control framework with guaranteed robustness margins. This paper addresses the problem of output voltage regulation for multiple DC-DC converters connected to a grid, and prescribes a robust scheme for sharing power among different sources. More precisely, we develop a control architecture where, unlike most standard control frameworks, the desired power ratios appear as reference signals to individual converter systems, and not as internal parameters of the system of parallel converters. This makes the proposed approach suited for scenarios when the desired power ratios vary rapidly with time. Additionally, the proposed control framework is suitable to both centralized and decentralized implementations, i.e., the same control architecture can be employed for voltage regulation irrespective of the availability of common load-current (or power) measurement, without the need to modify controller parameters. The control design is obtained using robust optimal-control framework. Case studies presented show the enhanced performance of prescribed optimal controllers for voltage regulation and power sharing.

I. INTRODUCTION

High environmental impact of fossil-based energy sources and demand for future energy sustainability have resulted in increased interest in the use of renewable energy resources such as solar and wind. Integration of renewable resources on the community level is achieved through smart microgrids. Microgrids are localized grid systems that are capable of operating in parallel with, or independently from, the existing traditional grid [1], [2]. Microgrid technology enables integration of renewable energy sources such as solar and wind energy, distributed energy resources (DERs), energy storage, and demand response. Fig. 1 shows a schematic of a microgrid with multiple DC sources providing power for AC loads. Although in most traditional grids that rely on conventional sources of *dispatchable* electric power, the power output of renewables can not be manipulated. Limited predictability with such resources result in intermittent power generation; moreover time-varying loads, practicability and economics factors pose additional challenges in efficient operation of microgrids. Thus it is required to develop efficient distributed control technologies for reliable operation of smart microgrids.

[1]Department of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, 61801 IL, USA
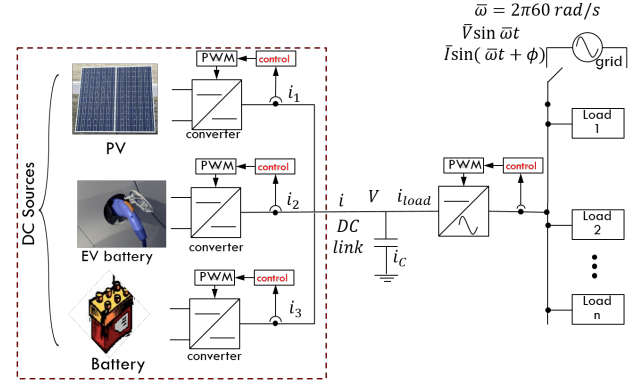[a]baranwa2@illinois.edu, [b]salapaka@illinois.edu

Fig. 1: A schematic of a microgrid. An array of DC sources provide power for AC loads. Power sources provide power at DC-link, their common output bus, at a voltage that is regulated to a set-point. The control system at the respective DC-DC converter that interfaces with a source is responsible for regulating the voltage at he DC-link. An inverter that connects to the DC-link converts the total current from the sources at the regulated voltage to alternating current (AC) at its output to satisfy the power demands of the AC loads. This paper describes an approach for control design of the multiple converters systems associated with power transfer from sources to the DC-link (shown by the dotted line).

In such smart grids, multiple DC power sources connected in parallel, each interfaced with DC-DC converter, provide power at their common output, the DC-link, at a regulated voltage; this power can directly feed DC loads or be used by an inverter to interface with AC loads. In this paper, we address the problem of distributed control of DC-DC converters for output voltage regulation, and time-varying power sharing (dictated by the economic layer) among multiple power sources. The main challenges arise from the uncertainties in the size and the schedules of loads, the complexity of a coupled multi-converter network, the uncertainties in the model parameters at each converter, and the adverse effects of interfacing DC power sources with AC loads, such as the 120 Hz ripple that has to be provided by the DC sources.

Problems pertaining to robust and optimal control of converters have received recent attention. Conventional PID-based controllers often to fail address the problem of robustness and modeling uncertainties. In [3], a linear-matrix-inequality (LMI) based based robust control design for boost converters has resulted in significant improvements over PID based control designs. In [4]–[6], robust $\mathcal{H}_\infty$-control framework is employed in the context of inverter systems. While the issue of current sharing is extensively studied [7], [8], most methods assume a single power source. A systematic

control design that addresses all the challenges and objectives for the multi-converter control is still lacking. The control architecture proposed in this paper addresses the following primary objectives - 1) voltage regulation at the DC-link with guaranteed robustness margins, 2) prescribed time-varying power sharing in a network of parallel converters, 3) controlling the trade-off between 120Hz ripple on the total current provided by the power sources and the ripple on the DC-link voltage. While these objectives are partially addressed in our prior work [9] on the robust control of DC-DC converters, a main drawback of the design proposed in [9] is that the control framework does not allow for time-varying power sharing requirements. In this work, we propose a novel control framework wherein the power requirements on each converter are imposed through external references, and thus the framework allows for time-varying power sharing by incorporating high-bandwidth robust controllers.

The control architecture proposed in this work exploits structural features of the paralleled multi-converter system, which results in a modular and yet coordinated control design. For instance, noting that the objective of voltage regulation is common to all converters; accordingly at each converter, it employs a nested (outer-voltage inner-current) control structure [10], where all converters share the same design for the outer-loop voltage controllers while the inner-loop current controllers are so chosen that the entire closed-loop multi-converter system can be reduced to an equivalent single-converter system in terms of the transfer function from the desired regulation setpoint V_{ref} to the voltage at the DC-link V_{dc}. The controllers are designed for fully *centralized* implementation with the instantaneous load current i_{load} measurement accessible to all converters; however, in practice i_{load} is often *estimated* through power calculations on the AC side and communicated to individual converters only at a rate slower than the sampling rate of the controllers. In the wake of this limitation, we propose a novel method for voltage regulation and power sharing that is inspired by conventional voltage droop method. An interesting aspect of the proposed implementation is that the same outer controllers K_v and K_r along with the shaped inner plant $\tilde{G}_{c,n}$ can be employed even for the scenario where i_{load} measurement is unavailable. Thus the proposed framework is applicable to both *centralized* and *decentralized* implementations. An important revelation provided by the application of $\mathcal{H}_\infty$ robust optimal control is the underlying optimal structure in the outer-loop controllers K_v and K_r. While we are yet to explore the reasoning behind the hidden optimal structure, it helps in further reduction of the overall complexity of the distributed control design from analysis and implementation points of view.

The rest of the paper is organized as follows. Sec. II describes the averaged modeling of DC-DC converters. We then describe the control design methodology for a single converter system in Sec. IV, followed by its extension to a network of parallel converters in Sec. V. The underlying theory is then corroborated by extensive simulations in Sec. VI, followed by some important conclusions and immediate
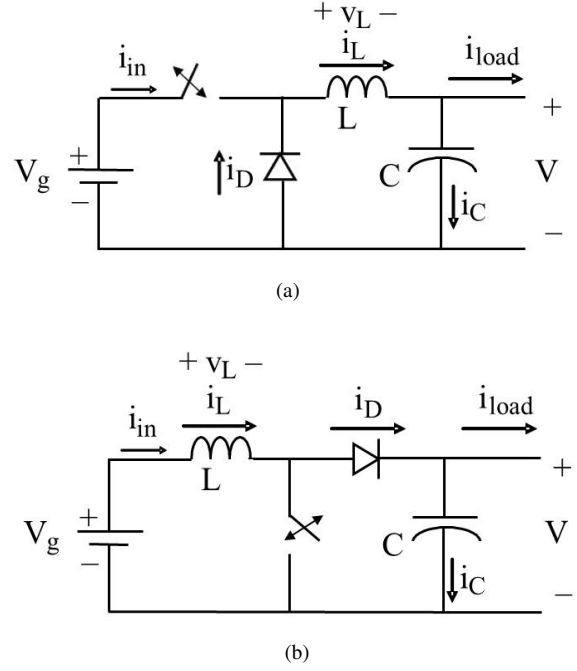

(a)

(b)

Fig. 2: Schematics for (a) Buck converter, (b) Boost Converter. The converters are assumed to operate in continuous-conduction-mode (CCM).

directions to future works.

II. MODELING OF CONVERTERS

In this section, we describe the differential equations that govern the dynamics of DC-DC converters. These converters belong to a class of switched-mode power electronics, where a semiconductor based high-frequency switching mechanism (and associated electronic circuit) connected to a DC power source enables changing voltage and current characteristics at its output. The models presented below depict dynamics for signals that are averaged over a switch cycle.

Fig. 2a shows a schematic of a Buck converter. Buck converter regulates a voltage at its output which is lower than the input voltage. The averaged dynamic model of a Buck converter is given by

$$L\frac{di_L(t)}{dt} = \underbrace{-V(t) + d(t)V_g}_{\tilde{u}(t):=-V(t)+u(t)} = \tilde{u}(t)$$
$$C\frac{dV(t)}{dt} = i_L(t) - i_{load}(t), \quad (1)$$

where $d(t)$ represents the duty-cycle (or the proportion of *ON* duration) at time t. Note that the prescribed averaged model does not explicitly require any information on the output load.

Similarly we can describe the averaged dynamics of a Boost converter (shown in Fig. 2b), given by

$$L\frac{di_L(t)}{dt} = \underbrace{V_g - d'(t)V(t)}_{\tilde{u}(t):=V_g-u(t)} = \tilde{u}(t)$$
$$C\frac{dV(t)}{dt} = \underbrace{\left(D' + \hat{d}'\right)}_{\approx D'}i_L(t) - i_{load}(t) \approx D'i_L(t) - i_{load}(t), \quad (2)$$
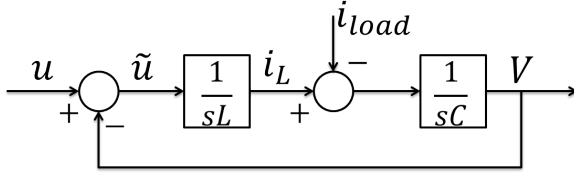
Fig. 3: Block diagram representation of a buck-type converter. The control signal $\tilde{u}$ is converted to an equivalent PWM signal to command the gate of the transistor acting as a switch.

where $d'(t) := 1 - d(t)$ and $D' = (V_g/V_{ref})$. Here V_{ref} represents the desired output voltage. Note that $\hat{d}(t) = d'(t) - D'$ is typically very small, and therefore allows for a linear approximation around the nominal duty-cycle, $D = 1 - D'$. We use both V and V_{dc} interchangeably to denote the output voltage at the DC-link.

III. PROBLEM FORMULATION

This paper addresses the following primary objectives *simultaneously* - (1) Output voltage regulation in presence of time-varying loads/generation and parametric uncertainties, (2) time-varying current (power) sharing among multiple sources, (3) $120Hz$ ripple current sharing between inductor current i_L and capacitor current i_C. The last two objective is dealt in our prior work [9] and is addressed by an appropriate design of inner-controller described in Sec. IV-A and V. In this paper, we primarily focus on achieving the first two objectives, while inheriting the properties of the inner-controller for ripple current sharing.

IV. CONTROL FRAMEWORK FOR SINGLE CONVERTER

In this section, we describe the *inner-outer* controller architecture for a single Buck converter system. The corresponding block diagram representation of the dynamical equations in 1 is shown in Fig. 3. While the design is easily extendable to include other converter types such as Boost and Buck-Boost, the discussion has been confined to Buck converters only for the sake of brevity. Unlike most other *outer*-controllers, the *outer*-controller proposed in this paper takes into account both DC-link voltage V and load current i_{load} measurements. The requirements on current sharing are imposed through this additional i_{load} measurement (as explained in Sec. V).

A. Design of the inner-loop controller

The design for the inner-loop controller K_c is inherited from our previous work [9]. The inner-loop controller K_c is designed as a 2nd-order controller to ensure a relatively low-order optimal controller $K_v = [K_v, K_r]^T$ (see Fig. 4). The main objective for designing the inner-loop controller K_c is to decide the trade-off between the 120Hz ripple on the capacitor current i_C (equivalently on the output voltage V_{dc}) and the inductor current i_L of the converter. Accordingly, K_c is designed such that the inner-shaped plant $\tilde{G}_c$ is given by

$$\tilde{G}_c(s) = \left(\frac{\tilde{\omega}}{s + \tilde{\omega}}\right)\left(\frac{s^2 + 2\zeta_1\omega_0 s + \omega_0^2}{s^2 + 2\zeta_2\omega_0 s + \omega_0^2}\right). \tag{3}$$
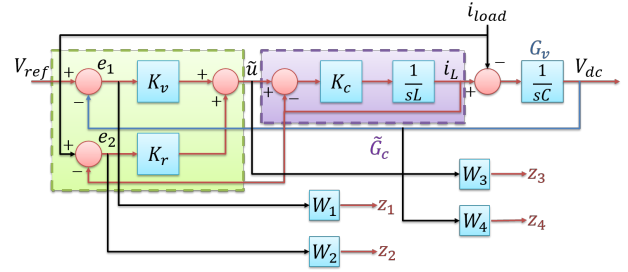

Fig. 4: Block diagram representation of the inner-outer control design. Exogenous signal V_{ref} represents the desired output voltage. The quantities V_{dc}, i_{load} and i_L represent the available measurements.

where $\omega_0 = 2\pi 120$rad/s and $\tilde{\omega}, \zeta_1, \zeta_2$ are design parameters. The parameter $\tilde{\omega} > \omega_0$ and it is used to implement a low-pass filter to attenuate undesirable frequency content in i_L beyond $\tilde{\omega}$. Thus, the bandwidth of the inner-shpaed plant is decided by the choice of $\tilde{\omega}$. The parameters ζ_1 and ζ_2 impart a notch-like behavior to $\tilde{G}_c$ at $\omega_0 = 120$Hz, and the size of the notch is determined by the ratio ζ_1/ζ_2. Note that $\tilde{G}_c$ represents the inner closed-loop plant from the output of the outer-loop controllers u to the inductor current i_L, and since $i_C = i_L - i_{load}$, the ratio ζ_1/ζ_2 can be appropriately designed to achieve a specified trade-off between 120Hz ripple on i_C and i_L. The stabilizing 2nd-order controller K_c that yields the aforementioned inner closed-loop plant $\tilde{G}_c$ is explicitly given by

$$K_c(s) = L\tilde{\omega}\frac{(s^2 + 2\zeta_1\omega_0 s + \omega_0^2)}{(s^2 + 2\zeta_2\omega_0 s + \omega_0^2 + 2(\zeta_2 - \zeta_1)\omega_0\tilde{\omega})}. \tag{4}$$

The readers are encouraged to refer to Sec. III in [9] for further details on the inner-loop control design.

B. Design of the outer-loop controller

For a given choice of inner-controller K_c, we present our analysis and design of controller in terms of transfer function block diagrams shown in Fig. 4. In this figure, $\tilde{G}_c$ represents the inner shaped plant. The outer controllers are denoted by K_v and K_r, and are designed to regulate the output DC voltage V_{dc} to the desired reference voltage V_{ref} and the inductor current i_L to the load current i_{load}, respectively. Note that from (1), i_L is equal to i_{load} at steady-state. The augmentation of controller K_r forms the basis for time-varying power sharing and is explained in the next section.

The performance of a Buck converter is characterized by its voltage and power reference tracking bandwidths, better voltage signal-to-noise-ratio (SNR), and robustness to modeling uncertainties. The main objective for the design of the controllers K_v and K_r is to make the tracking errors small and simultaneously attenuate measurement noise to achieve high resolution. This is achieved by posing a *model-based* multi-objective optimization framework, where the required objectives are described in terms of norms of the corresponding transfer functions, as described below. From Fig. 4, the transfer function from exogenous inputs $w = [V_{ref}, i_{load}, \tilde{u}]^T$ to regulated output $z = [z_1, z_2, z_3, z_4, e_1, e_2]$

is given by

$$
\begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ z_4 \\ e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} W_1 & W_1 G_v & -W_1 G_v \tilde{G}_c \\ 0 & W_2 & -W_2 \tilde{G}_c \\ 0 & 0 & W_3 \\ 0 & -W_4 G_v & W_4 G_v \tilde{G}_c \\ 1 & G_v & -G_v \tilde{G}_c \\ 0 & 1 & -\tilde{G}_c \end{bmatrix} \begin{bmatrix} V_{ref} \\ i_{load} \\ \tilde{u} \end{bmatrix}. \quad (5)
$$

The optimization problem is to find stabilizing controllers $K_{outer} = [K_v, K_r]^T$ such that the $\mathcal{H}_\infty$-norm of the above transfer function from w to z is minimized. Here the weights W_1, W_2, W_3 and W_4 are chosen to reflect the design specifications of robustness to parametric uncertainties, tracking bandwidth, and saturation limits on the control signal. More specifically, the weight functions $W_1(j\omega)$ and $W_2(j\omega)$ are chosen to be large in frequency range $[0, \omega_{BW}]$ to ensure small tracking errors $e_1 = V_{ref} - V_{dc}$ and $e_2 = i_{load} - i_L$ in this frequency range. The design of weight function $W_3(j\omega)$ entails ensuring that the control effort lies within saturation limits. The weight function W_4 is designed as a high-pass filter to ensure that the transfer function from i_{load} to V_{dc} is small at high frequencies to provide mitigation to measurement noise.

Current droop compensation for voltage regulation without i_{load} measurement: So far in our analysis, we assume that i_{load} is available for direct measurement for all converters. However in practice, while the converters can measure their common DC-link voltage V_{dc}, i_{load} is only *estimated* through power calculations on the AC side and communicated to individual converters only at a rate slower than the sampling rate of the controllers. In the wake of this limitation, we propose a novel method for voltage regulation and power sharing that is inspired by conventional voltage droop method. An interesting aspect of the proposed implementation is that the same outer controllers K_v and K_r along with the shaped inner plant $\tilde{G}_{c,n}$ can be employed even for the scenario where i_{load} measurement is unavailable. In this case, the outer controller K_r regulates the inductor current i_L to $i_{ref} + f(\cdot) * (V_{ref} - V_{dc})$, where $f(\cdot)$ represents an LTI filter and $*$ is the convolution operator. This can be understood as follows. Let us suppose that $i_{ref} > i_{load} = (V_{ref}/R)$, where R is the output load resistance. This in turn implies that $V_{dc} = i_{ref} R$ is bigger than V_{ref}. Thus the compensation term $(V_{ref} - V_{dc}) < 0$ and the reference to the outer-loop controller K_r becomes smaller than i_{ref}, as required. A similar inference can be drawn when $i_{ref} < i_{load}$. The corresponding block diagram is shown in Fig. 5.

Extension to Boost Converters: The extension of the proposed control design to Boost and Buck-Boost DC-DC converters is easily explained after noting that their averaged models are structurally identical to Buck converters, except that the dependence of duty cycles on the control signal u or constant parameter D' are different. The differences in how duty cycles depend on $u(t)$ do not matter from the control design viewpoint since duty cycles for pulse-width modulation are obtained only after obtaining the control designs (that use the averaged models). Fig. 6 shows the
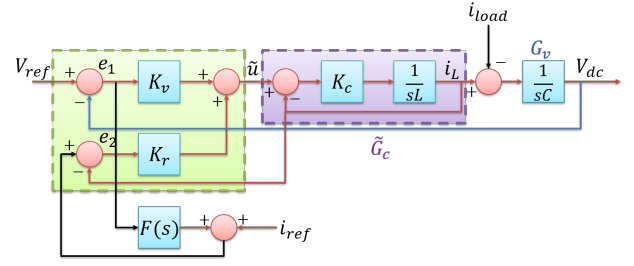

Fig. 5: Modified architecture for *decentralized* implementation. $F(s)$ represents the Laplace transform of the corresponding LTI filter $f(\cdot)$. The reference to the outer controller K_r is $i_{ref} + f(\cdot) * (V_{ref} - V_{dc})$.
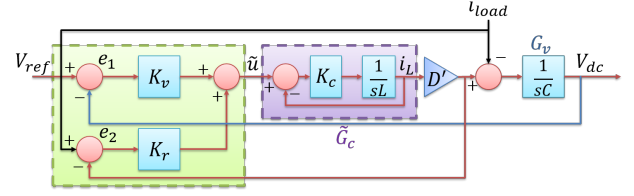

Fig. 6: Block diagram representation of the inner-outer control design for boost-converter. Note that this representation differs from that of the buck converter only in terms of the constant parameter D' and the expression that is used to obtain the duty-cycle from the control signal $\tilde{u}$.

equivalent schematic of the proposed control framework for a Boost converter system.

V. EXTENSION TO A SYSTEM OF PARALLEL CONVERTERS

In this section we extend our control framework for a single converter to a system of DC-DC converters connected in parallel in the context of power sharing, keeping in mind the practicability and robustness to modeling and load uncertainties.

Fig. 7a represents an inner-outer control framework for a system of m parallel connected converters. Note that instead of feeding i_{load} directly to the kth outer controller K_{r_k}, the measurement signal is prescaled by a time-varying multiplier $\gamma_k, 0 \leq \gamma_k \leq 1$. The choice of γ_k dictates the power sharing requirements on the kth converter. In fact, we later show that the proposed implementation distributes the output power in the ratios $\gamma_1 : \gamma_2 : .. : \gamma_m$. After noting that the voltage-regulation and current reference tracking is common to all the outer controllers, in our architecture, we impose the same design for outer-controllers for all the converters, i.e., $K_{v_1} = K_{v_2} = .. = K_{v_m}$ and $K_{r_1} = K_{r_2} = .. = K_{r_m}$. This imposition enables significant reduction in the overall complexity of the distributed control design for a parallel network of converters and power sources, thus ensuring the practicability of the proposed design which allows integration of power sources of different types and values.

We design inner-controllers K_{c_k} such that the inner-shaped plants from $\tilde{u}_k$ to i_{L_k} are same and given by,

$$
\tilde{G}_{c,n}(s) = \left(\frac{\tilde{\omega}}{s + \tilde{\omega}} \right) \left(\frac{s^2 + 2\zeta_{1,n}\omega_0 s + \omega_0^2}{s^2 + 2\zeta_{2,n}\omega_0 s + \omega_0^2} \right), \quad (6)
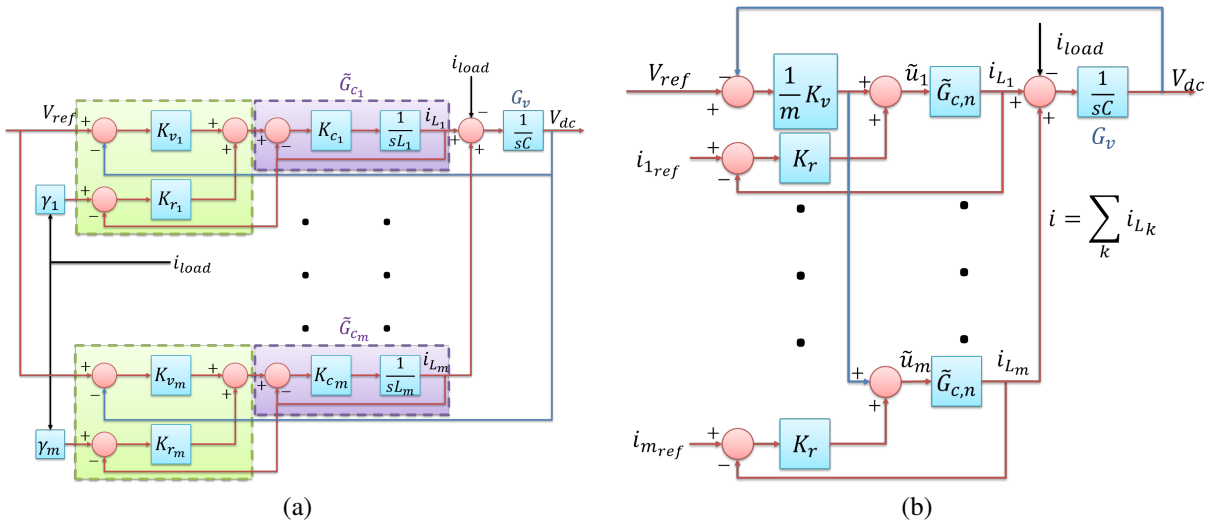$$

Fig. 7: (a) Control framework for a network of m parallel converters. Here γ_k represents the proportion of power demanded from the kth source. (b) A multiple-converters system with shaped inner plants $\tilde{G}_c$. In the proposed implementation, we adopt the same outer controller for different converters, i.e., $K_{v_1} = K_{v_2} = .. = K_{v_m} = \frac{1}{m}K_v$ and $K_{r_1} = K_{r_2} = .. = K_{r_m} = K_r$.

where the ratio $\zeta_{1,n}/\zeta_{2,n}$ determines the tradeoff of 120Hz ripple between the total inductor current $i_L = \sum_{k=1}^{m} i_{L_k}$ and the capacitor current i_C. Note that for given values of $\zeta_{1,n}, \zeta_{2,n}$ and inductance L_k, explicit design of K_{c_k} exists and is given by (4). After noting that $K_{v_k} = \frac{1}{m}K_v$ and $K_{r_k} = K_r$, the system in Fig. 7a can be simplified to Fig. 7b.

Indeed, by our choice of inner and outer controllers, the transfer functions from external references V_{ref} and $i_{k_{ref}}$ to the desired output V_{dc} are identical for all converters. Hence the entire network of parallel converters can be analyzed in the context of an equivalent single converter system. This implies that K_{v_k} and K_{r_k} can be computed by solving $\mathcal{H}_\infty$-optimization problem (as discussed in the previous section) similar to the *single* converter case. We make these design specifications more precise and bring out the equivalence of the control design for the single and multiple converter systems in the following theorem.

We say that the system representation in Fig. 4 is *equivalent* to that in Fig. 7b, when the transfer functions from reference voltage V_{ref} and load current i_{load} to the DC-link voltage V_{dc} (and therefore the total current sourced $i = i_L$) in Fig. 4 are identical to the corresponding transfer functions in Fig. 7b. In the following theorem, we denote the outer-voltage sensitivity transfer function in Fig. 4 from V_{ref} to V_{dc} by $S_1 = \left(\frac{1}{1+\tilde{G}_{c,n}K_r+G_v\tilde{G}_{c,n}K_v}\right)$ and the corresponding complementary sensitivity transfer function by $T_1 = G_v\tilde{G}_{c,n}K_vS_1$. Similarly, we denote the outer-current sensitivity transfer function by $S_2 = \left(\frac{1}{1+\tilde{G}_{c,n}K_r}\right)$ and the corresponding complementary transfer function by $T_2 = 1 - S_2$. Moreover, we define $H = \tilde{G}_{c,n}K_vS_1$.

Theorem 1: Consider the single-converter system in Figure 4 with inner-shaped plant $\tilde{G}_{c,n}(s)$ as given in (6), outer controllers K_v, K_r and external references V_{ref}, i_{load}; and the multi-converter system described in Figures 7a and 7b

with inner-shaped plants $\tilde{G}_{c_k} = \tilde{G}_{c,n}(s)$ and outer controllers $K_{v_k} = \frac{1}{m}K_v$; $K_{r_k} = K_r$, and external references $V_{ref}, i_{k_{ref}}$ for $1 \le k \le m$.
1. [System Equivalence]: If $\sum_{k=1}^{m} i_{k_{ref}} = i_{load}$, then the system representations in Fig. 4 and Fig. 7b are *equivalent*.
2. [Power Sharing]: If controllers K_v and K_r are designed such that $|H(j\omega)| < \epsilon$, $|S_2(j\omega)| < \epsilon$ and the total current mismatch $|\sum_k i_{k_{ref}}(j\omega) - i_{load}(j\omega)| < \Delta$ at frequncy ω for some $\epsilon > 0$ and $\Delta > 0$, then $|i_{L_k}(j\omega) - i_{k_{ref}}(j\omega)| < \frac{\epsilon(|V_{ref}(j\omega)|+m|i_{k_{ref}}(j\omega)|+(1+\epsilon)|i_{load}(j\omega)|)}{m} + \frac{(1+\epsilon)^2\Delta}{m}$.

Remark 1: Since the system representations in Figs. 4 and 7b are equivalent, the analysis and design of the entire multi-converter system can be done using an equivalent single converter system, where the multi-converter system inherits the performance and robustness achieved by a design for the single-converter system.

Remark 2: While the sensitivity transfer functions S_1 and S_2 can be made sufficiently small by designing appropriate high DC-gain controllers, the transfer function H is also small at sufficiently low-frequencies. In fact, it can be easily shown that $|H(j0)| = 0$, since $|\tilde{G}_{c,n}(j0)| = 1$ and $G_v(s) = 1/(sC)$, which has infinite DC-gain.

Remark 3: Note that from power-sharing result in the above theorem, if $i_{k_{ref}} = \gamma_k i_{load}$, where $\sum_k \gamma_k = 1, \gamma_k \ge 0$, then the output current at the DC-link gets divided approximately in the ratio $\gamma_1 : \gamma_2 : \cdots : \gamma_m$; more precisely the *low-frequency* components (and thus the steady-state) $i_{L_1} : i_{L_2} : \cdots : i_{L_m} \approx \gamma_1 : \gamma_2 : \cdots : \gamma_m$.
Proof: See Appendix.

VI. CASE STUDIES: SIMULATIONS AND DISCUSSIONS

In this section, we report some simulation studies that cover different aspects of the proposed distributed control design. All simulations are performed in MATLAB/Simulink using SimPower/SimElectronics library. Note that the experiments are underway and therefore not reported in this paper.

In order to include nonlinearities associated with real-world experiments, and effects of switching frequencies on voltage regulation and power sharing, we use *non-ideal* components (such as diodes with non-zero forward-bias voltage, IGBT switches, stray capacitances, parametric uncertainties) and switched level implementation.

A. Robustness to Modeling Parameters

Traditional control techniques such as proportional-integral (PI) based control designs exhibit satisfactory performance when the actual converter system parameters (L, C) lie *close* to the nominal system parameters for which the controllers are to be designed. A slight deviation from the nominal values may result in rapid degradation in the tracking performance and power sharing. The issue is particularly critical in power electronic systems where individual component values have large tolerance about the nominal values. The lack of robustness is addressed through $\mathcal{H}_\infty$ robust control framework, where an optimizing controller with guaranteed margins of robustness to modeling uncertainties is sought.

Fig. 8a shows the tracking performance of the proposed robust inner-outer controllers for 20% uncertainty in indcutance (L) and capacitance (C) values. The actual converter parameters are chosen as:
$C = 500\mu$F, $L = 1.2$mH, Switching-frequency $f_s = 50$kHz, Input voltage $V_g = 480V$, Desired output voltage $V_{ref} = 240V$, Load-current $i_{load} = 20 + 0.4\sin(2\pi120t)$
The design parameters for the inner-controller K_c are:
Damping factors $\zeta_1 = 1.2$, $\zeta_2 = 2.1$, and $\tilde{\omega} = 2\pi200$rad/s.
The outer controllers K_v and K_r are obtained by solving the stacked $\mathcal{H}_\infty$ optimization problem (see Eq. (5)) [11] with the weighting functions:

$$W_1 = \frac{0.5(s + 502.7)}{(s + 2.513)}, W_2 = \frac{0.5(s + 628.3)}{(s + 3.142)}, W_3 = 0.1$$

The resulting outer-controllers are reduced to sixth-order using balanced reduction [12] and are given by,

$$
\begin{aligned}
K_v &= -0.0076\frac{(s - 8.69e5)}{(s + 2.73e4)}\frac{(s + 2.01e4)}{(s + 1.07e4)}\frac{(s + 2577)}{(s + 433.9)} \\
&\quad \frac{(s + 194.2)}{(s + 2.498)}\frac{(s^2 + 0.02s + 0.0001)}{(s^2 + 0.01978s + 0.0008)} \\
K_r &= 0.065\frac{(s + 4.07e5)}{(s + 1.15e4)}\frac{(s + 2474)}{(s + 422.4)}\frac{(s + 191.7)}{(s + 3.11)} \\
&\quad \frac{(s + 3.20)}{(s + 2.03)}\frac{(s + 0.01)(s + 0.0099)}{(s^2 + 0.01978s + 0.0008)}
\end{aligned}
$$

Optimal structure of outer-loop controllers: For the stacked $\mathcal{H}_\infty$ problem, the outer-loop controllers K_v and K_r are observed to be constant multiples of each other for a number of choices of weighting functions W_1 and W_2. While we are yet to explore the reasons for the underlying optimal structure, the optimal structure significantly reduces the complexity of the distributed control design by allowing to get rid of the controller K_r from the outer-loop and modifying the input of the controller K_v to $V_{ref} - V_{dc} + \alpha(i_{load} - i_L)$. Here $\alpha > 0$ is an appropriate constant which captures the relationship between the outer-loop controllers K_v and K_r. We believe that the constant α is related to the

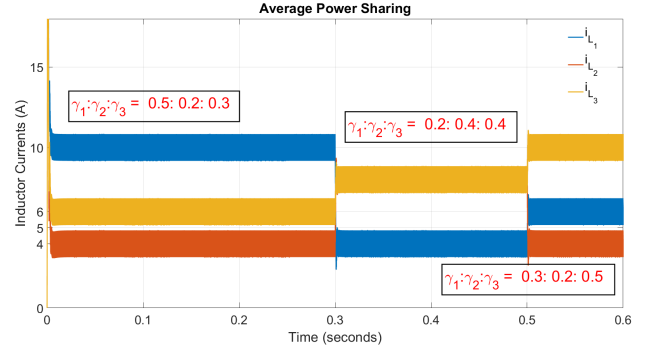

Fig. 9: Power sharing among three buck-converters for $V_{ref} = 240V$ and $R = 12\Omega$ in the prescribed ratios. The controllers allow for rapidly varying power-sharing requirements.

system parameters L and C, however, this is something we would definitely like to explore in our future work.

B. Current Sharing among Converters

Fig. 9 shows the system performance for time-varying output current sharing among three Buck converters. The following parameters are assumed for the three converters - $L_1 = 1.2$mH, $V_{g_1} = 480V$; $L_2 = 1.6$mH, $V_{g_2} = 460V$; $L_3 = 1.9$mH, $V_{g_3} = 480V$. Clearly, the total load current is 20A. The converters divide the load current in the ratios $10 : 4 : 6$ for $t \in [0, 0.3s]$; $4 : 8 : 8$ for $t \in [0.3s, 0.5s]$ and $6 : 4 : 10$ for $t \in [0.5s, 0.6s]$, as required.

C. Current Sharing and Voltage Regulation without i_{load} measurement

We now consider the scenario when i_{load} measurement is unavailable. In this case, the input to the outer-loop controller K_r is some nominal reference current i_{ref} plus a compensation term which is a manifestation of error in voltage reference tracking. This can be understood as follows. Fig. 10 shows the system performance for voltage reference tracking for the proposed *decentralized* implementation. Note that despite the unavailability of load current measurement, the controller regulates the DC-link voltage to the desired reference voltage, albeit with relatively larger overshoot.

VII. CONCLUSIONS AND FUTURE WORKS

In this work, we propose a distributed control architecture for voltage tracking and power sharing for a network of DC-DC converters connected in parallel. The proposed design is capable of achieving multiple objectives such as robustness to modeling uncertainties, reference DC voltage generation and output power sharing among multiple DC sources. The controllers are designed using a robust optimal control framework. We also propose a novel approach for *decentralized* implementation, where the load current is not available for measurement. We are currently setting up the experiments to demonstrate the effectiveness of the proposed implementation. Moreover, the optimal structure of the outer-loop controllers K_v and K_r needs to be analyzed in full details to gain further insights into the problem of voltage control of DC-DC converters.

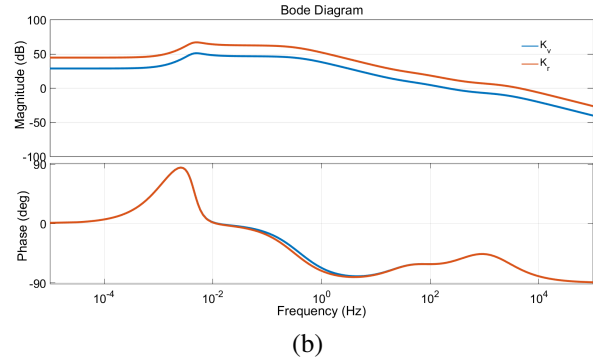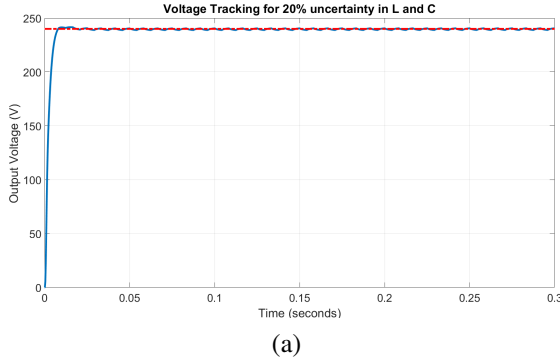(a)   (b)

Fig. 8: (a) Robustness to model parameters. The proposed controller tracks the desired voltage in presence of parametric uncertainties and ripple in load current. (b) Bode plots of the outer-loop controllers. It can be observed that the two controller transfer functions are constant multiples of one-another.
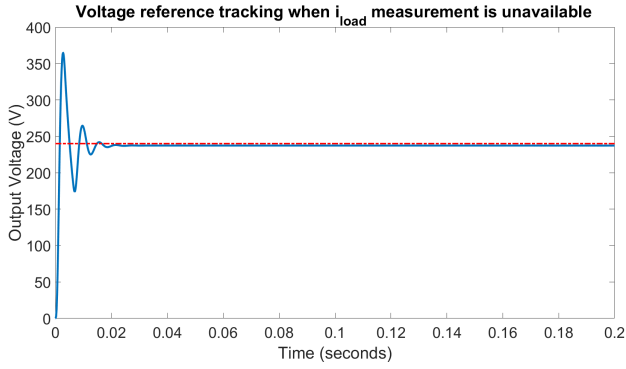

Fig. 10: A droop-like approach for voltage regulation in the absence of i_{load} measurement. The converter is required to regulate the output voltage to $240V$. The load R is chosen to be 12Ω. This corresponds to an $i_{load} = 20A$. However, in the absence of i_{load} measurement, we assume $i_{ref} = 16A$. The filter transfer function is chosen as $F(s) = \frac{376.99}{s+314.16}$.

APPENDIX

Proof of Theorem 1: System Equivalence

Proof: The underlying equivalence is straightforward to derive. From Fig. 4, with $\tilde{G}_c(s) = \tilde{G}_{c,n}(s)$, the output DC-link voltage in terms of the exogenous signals V_{ref} and i_{load} is given by

$$V_{dc} = \left(\frac{1}{1+\tilde{G}_{c,n}K_r+G_v\tilde{G}_{c,n}K_v} \right) \left(G_v\tilde{G}_{c,n}K_v V_{ref} - G_v i_{load} \right) \tag{7}$$

However, from Figs. 7a and 7b, we obtain

$$V_{dc} = G_v \left(-i_{load} + \tilde{G}_{c,n} \sum_{k=1}^{m} \tilde{u}_k \right)$$

$$\tilde{u}_k = \left(\frac{1}{1+\tilde{G}_{c,n}K_r} \right) \left(\frac{1}{m}K_v(V_{ref} - V_{dc}) + K_r i_{k_{ref}} \right) \tag{8}$$

From Eq. (8) and using the fact that $\sum_{k=1}^{m} i_{k_{ref}} = i_{load}$ we recover Eq. (7), which establishes the required equivalence. ∎

Proof of Theorem 1: Power Sharing

Proof: From Fig. 8b, it can be shown that the difference between the inductor current i_{L_k} and the reference current

$i_{k_{ref}}$ for the kth converter (in terms of signals V_{ref}, i_{load} and $i_{k_{ref}}$) is given by

$$i_{L_k} - i_{k_{ref}} = \quad \frac{1}{m}HV_{ref} - \frac{1}{m}T_1T_2 \left(\sum_k i_{k_{ref}} - i_{load} \right)$$
$$+ \frac{1}{m}T_1S_2 i_{load} - S_2 i_{k_{ref}} \tag{9}$$

Moreover, we have $|T_1(j\omega)| < 1 + \epsilon$ and $|T_2(j\omega)| < 1 + \epsilon$. Thus from (9) and conditions of the theorem, we get

$$|i_{L_k}(j\omega) - i_{k_{ref}}(j\omega)| < \frac{\epsilon}{m}|V_{ref}(j\omega)| + \frac{\epsilon(1+\epsilon)}{m}|i_{load}(j\omega)|$$
$$+ \frac{(1+\epsilon)^2\Delta}{m} + \epsilon|i_{k_{ref}}(j\omega)| \tag{10}$$

Additionally, if $i_{k_{ref}} = \gamma_k i_{load}$, then the total current mismatch term in (9) is zero. Moreover, through an appropriate design of high DC-gain controllers, we have that there exists a sufficiently small $\epsilon > 0$ such that for $\omega << \omega_{BW}$, where ω_{BW} is bandwidth of the closed-loop system, $|H(j\omega)| < \epsilon$ and $|S_2(j\omega)| < \epsilon$. Then from (10) we obtain,

$$|i_{L_k}(j\omega) - \gamma_k i_{load}(j\omega)| < \frac{\epsilon}{m}|V_{ref}(j\omega)| + \frac{\epsilon}{m}|i_{load}(j\omega)|$$
$$+ \epsilon|i_{k_{ref}}(j\omega)| \tag{11}$$

Thus $|i_{L_k}(j\omega) - \gamma_k i_{load}(j\omega)|$ is small for $\omega << \omega_{BW}$ and therefore, the load current gets approximately divided in the ratio $\gamma_1 : \gamma_2 : \cdots : \gamma_m$. ∎

REFERENCES

[1] R. H. Lasseter, "Microgrids," in *Power Engineering Society Winter Meeting, 2002. IEEE*, vol. 1. IEEE, 2002, pp. 305–308.

[2] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, "Microgrids," *Power and Energy Magazine, IEEE*, vol. 5, no. 4, pp. 78–94, 2007.

[3] C. Olalla, R. Leyva, A. El Aroudi, P. Garces, and I. Queinnec, "Lmi robust control design for boost pwm converters," *IET Power Electronics*, vol. 3, no. 1, pp. 75–85, 2010.

[4] G. Weiss, Q.-C. Zhong, T. C. Green, and J. Liang, "H repetitive control of dc-ac converters in microgrids," *Power Electronics, IEEE Transactions on*, vol. 19, no. 1, pp. 219–230, 2004.

[5] T. Hornik and Q.-C. Zhong, "A current-control strategy for voltage-source inverters in microgrids based on and repetitive control," *Power Electronics, IEEE Transactions on*, vol. 26, no. 3, pp. 943–952, 2011.

[6] S. Salapaka, B. Johnson, B. Lundstrom, S. Kim, S. Collyer, and M. Salapaka, "Viability and analysis of implementing only voltage-power droop for parallel inverter systems," in *Decision and Control (CDC), 2014 IEEE 53rd Annual Conference on*. IEEE, 2014, pp. 3246–3251.

[7] Y. Panov, J. Rajagopalan, and F. C. Lee, "Analysis and design of n paralleled dc-dc converters with master-slave current-sharing control," in *Applied Power Electronics Conference and Exposition, 1997. APEC'97 Conference Proceedings 1997., Twelfth Annual*, vol. 1. IEEE, 1997, pp. 436–442.

[8] R.-H. Wu, T. Kohama, Y. Kodera, T. Ninomiya, and F. Ihara, "Load-current-sharing control for parallel operation of dc-to-dc converters," in *Power Electronics Specialists Conference, 1993. PESC'93 Record., 24th Annual IEEE*. IEEE, 1993, pp. 101–107.

[9] M. Baranwal, S. M. Salapaka, and M. V. Salapaka, "Robust de-centralized voltage control of dc-dc converters with applications to power sharing and ripple sharing," in *American Control Conference (ACC), 2016 - To Appear*. IEEE, 2016, http://web.engr.illinois.edu/~baranwa2/ACC2016/2016ACC_1392_FI.pdf.

[10] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[11] S. Skogestad and I. Postlethwaite, *Multivariable feedback control: analysis and design*. Wiley New York, 2007, vol. 2.

[12] G. E. Dullerud and F. Paganini, *A course in robust control theory: a convex approach*. Springer Science & Business Media, 2013, vol. 36.