VLSI   FISAC-2

Q15

$$V_{out} = \overline{A \cdot B \cdot C}$$

⇒ **Rise Delay** :

$$\tau_{Rise} = 6RC \quad \{Best \; case\}$$
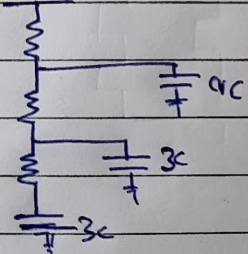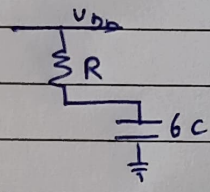
$$\tau_{Rise} = 9RC + 3RC + 3RC$$

$$= 15 \; RC \quad \{worst \; case\}$$

⇒ **Fall Delay :**
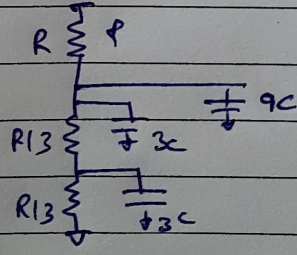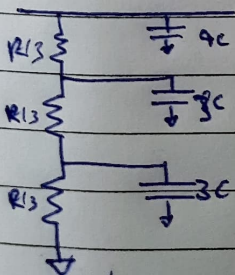
$$\tau_{Fall} = 9RC + 2RC + RC$$

$$= 12 \; RC \quad \{worst\}$$

$$\tau_{Fall} = 9C \cdot \frac{2R}{3} + \frac{3R + 2R}{3} + 3C \cdot R_{17}$$

$$\tau_{Fall} = 9 RC \quad (Best)$$

Q2

$P_1 = \frac{10}{10} = 1$

$y_1 = 1$

$n_1^2 x_1 = \frac{2}{10} \cdot \frac{2}{10}$

$P_2 = 2$

$g_2 = 5|3$

$h_2 = y/x$

$P_8 = 2$

$g_3 = 4|_8$

$n_3 = 24$

$P_4 = 1$

$g_4 = 1$

$h_4 = 40/2$

$40C$
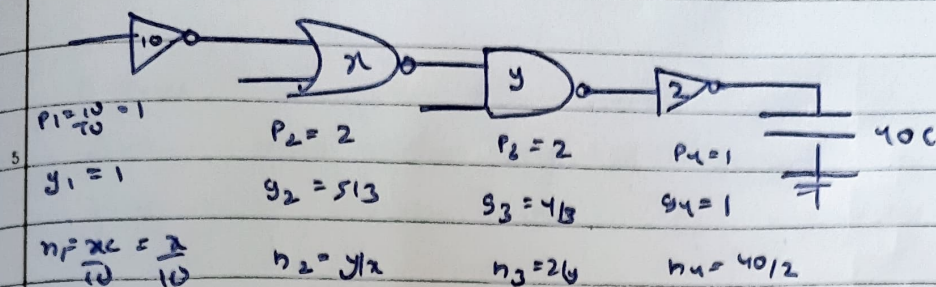
$\rightarrow G = g_1 \cdot g_2 \cdot g_3 \cdot g_4 = \frac{20}{9}$

$M = \frac{C_{out}}{C_{in}} = \frac{40}{10} = 4$

$\therefore$ Total path effort $= G \cdot M = \frac{20}{9} \times 4 = \frac{80}{9} = 8.89$

$\rightarrow f = (F)^{1/N} = (8.89)^{1/4} = 1.23$

$\rightarrow g_i \cdot h_i = F \qquad g_1 h_1 = 1.73$

$x = 10 \times 1.73 = 17.3 C$

$y = \frac{1.73 \times 17.3}{(5|3)} = 18 C$

$2 = \frac{1.73 \times 18}{(4|2)} = 23.36C$

$2 = 40 / 1.73 = 23.12 C$

Q3

minimum delay $= \sum_{i=1}^{h} P_i + \sum_{i=1}^{h} g_i \cdot h_i$

$= 6 + 4 \times 1.73$

$d_{min} = 12.92$

Q⁴   **3-T DRAM :**

(1)   **ALL ~~write~~ operation :**

Operation	Conditions	Result on Bit-line
write 1	Data = 1, WEϕ_2=1, wϕ_2=1	stores 1 at node
write 0	Data=0, WEϕ_2=1, wϕ_2=1	stores 0 by discharging
Read 1	Rϕ_2=1, Node=1 → T$_3$ on	Bit line pulled low
Read 0	Rϕ_2=1, Node=0 → T$_3$ off	Bitline pulled high

(2)   **Stick diagram :**

$\boxed{\text{⬚⬚⬚⬚}}$ = Red
$\boxed{\text{· · · ·}}$ = Green
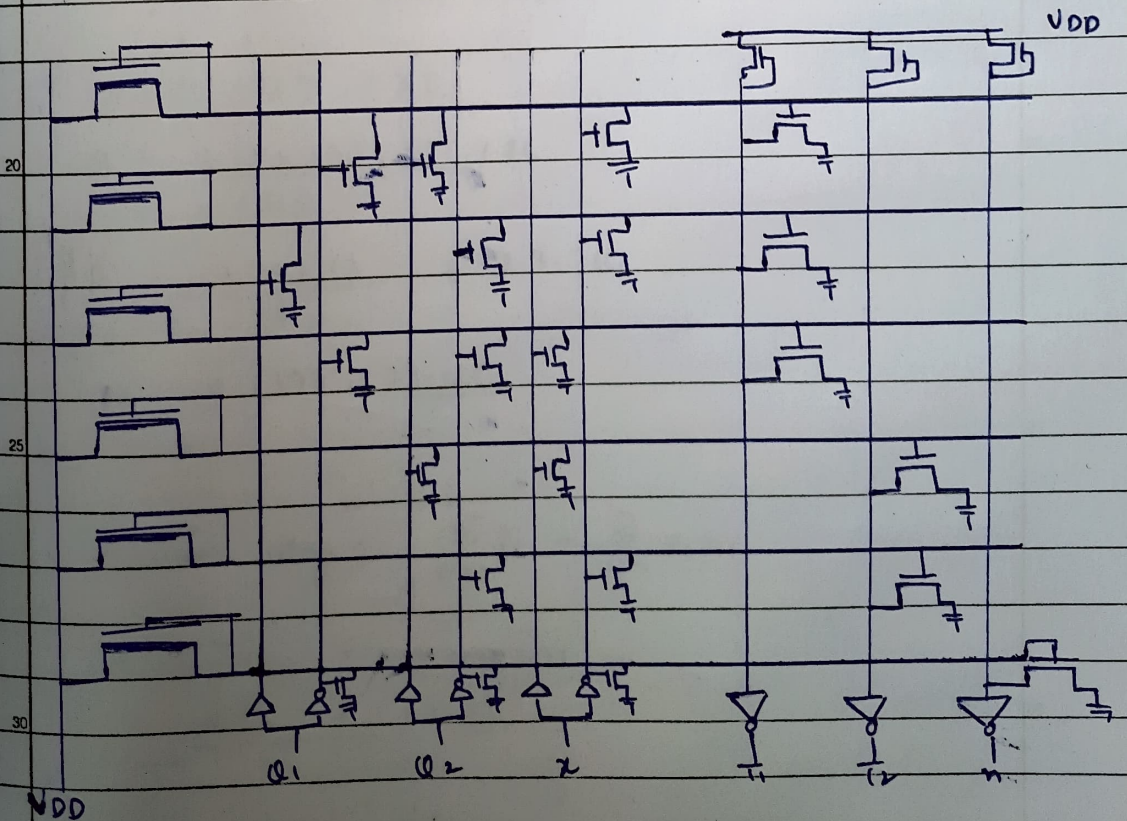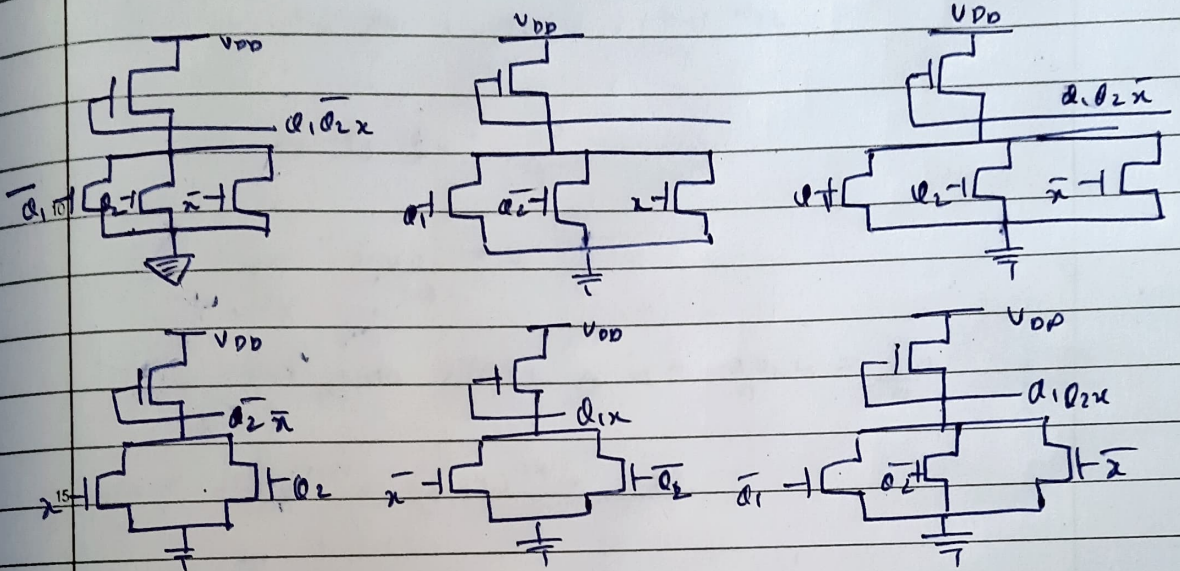$\boxed{\text{- - -}}$ = Blue

Date : _____

Q5
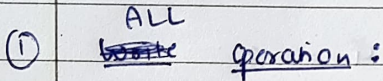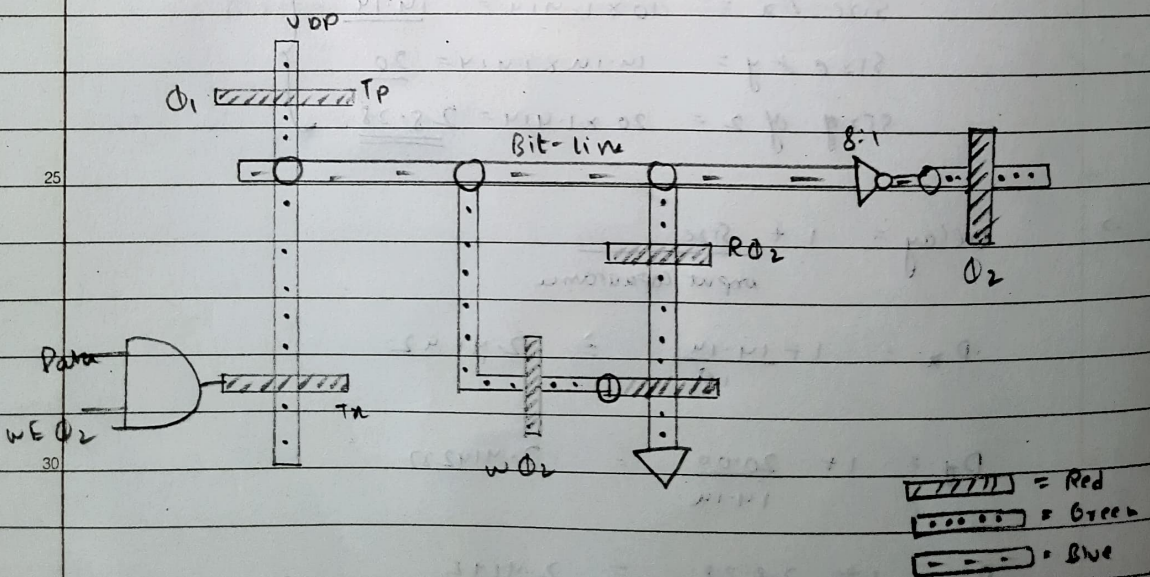
0101 sequence detector using NMOS PLA & T-Flip flops

$$T_1 = Q_1 Q_2' x + Q_1' Q_2 x + Q_1 Q_2 x'$$
$$T_2 = Q_2' x' + Q_2 x$$
$$n = Q_1 Q_2 x$$

NMOS PLA