Type: MCQ

Q1. What is the primary advantage of using CMOS technology in VLSI design?(0.5)

1. **Lower power consumption
2. Higher speed operation
3. Higher breakdown voltage
4. Lower tolerance to noise

Q2. Which parameter in MOSFET models accounts for channel length modulation? (0.5)

1. **Early voltage (VA)
2. Threshold voltage (VT)
3. Mobility (μ)
4. Subthreshold slope (SS)

Q3. In Pseudo NMOS logic, what is the required number of transistors to implement an N-input function? (0.5)

1. N
2. **N+1
3. 2N
4. 3N+3

Q4. What is the minimum dimension of channel implant for Depletion MOSFET (0.5)

1. 2λ×2λ
2. 4λ×4λ
3. **6λ×6λ
4. 8λ×8λ

Q5. What is the main drawback of dynamic CMOS logic? (0.5)

1. Higher power consumption
2. Slower switching speed
3. Complexity in design
4. **Charge leakage

Q6. Domino effect problem associated with which of the following logic (0.5)

1. Static CMOS
2. **Dynamic CMOS
3. Pseudo NMOS
4. DOMINO

Q7. What happens if the clock width (W) in a sequential circuit is greater than the minimum delay through the network? (0.5)

1. It improves the performance of the combinational logic
2. **It causes a multistepping or race condition

3. It reduces the overall circuit complexity
4. It increases the propagation delay

Q8. Minimum number of NMOS pass transistor needed to implement 4 to 1 MUX (0.5)

1. 8
2. **6
3. 4
4. 12

Q9. What is the minimum separation needed between n diffusion and polysilicon(0.5)

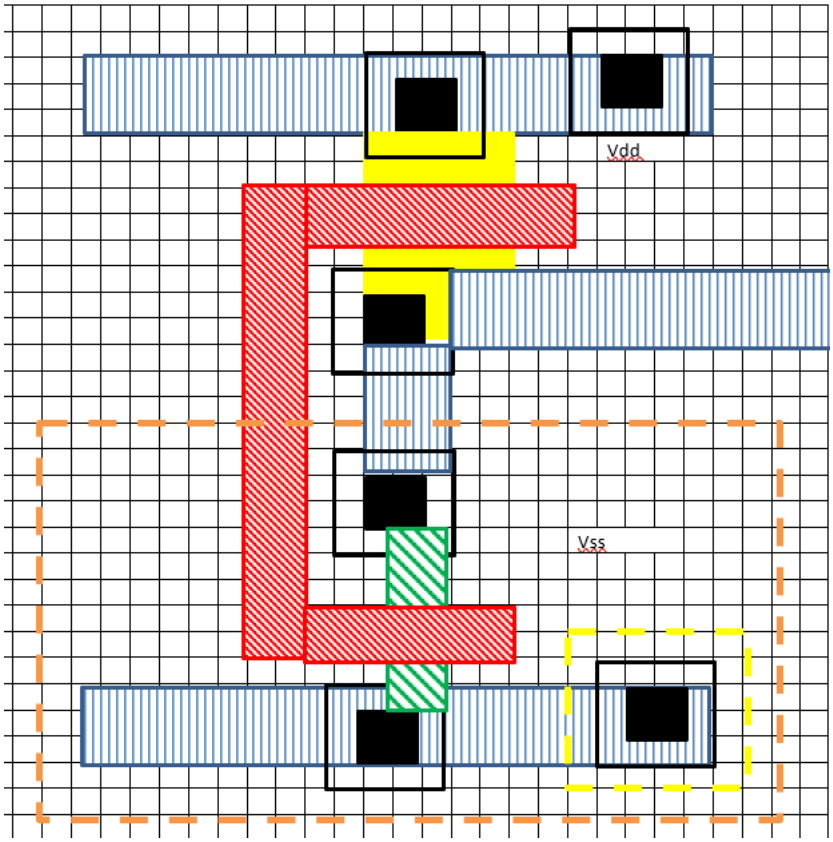
1. **λ
2. 2 λ
3. 3 λ
4. 4 λ

Q10. Depletion type NMOS transistor is fabricated on (0.5)

1. Polysilicon Substrate
2. **P-type substrate
3. N-type substrate
4. Silicon Nitride Substrate

Type: DES

Q11. Draw the layout of CMOS inverter using λ based design rule. (4)



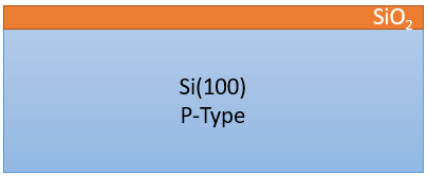
V_{DD} and Vss Contact—1 Marks

P-Well – 0.5 Marks

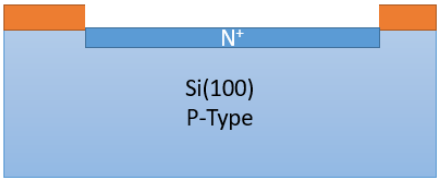
Remaining Layout 2.5 Marks

Q12. Describe the steps involved in the fabrication of Depletion NMOS transistor with neat diagram. (4)

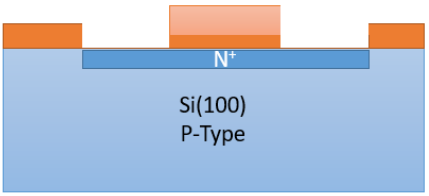
1. Substrate Selection and oxidation



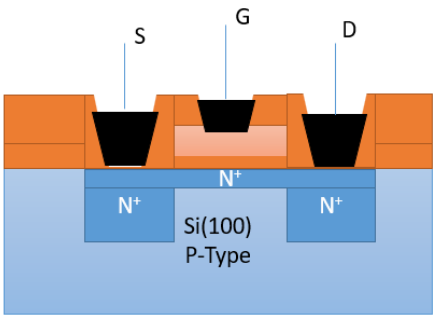
2. Oxide Patterning and Channel implant



3. Gate Oxide and poly-Si deposition and patterning



4. Source & Drain wion implantation and Metallaization & patterning



1×4=4Marks

Q13. A 0.18-μm fabrication process is specified to have t_{ox}= 4nm, μ_n=450cm^2/Vs and V_T=0.5V. Find the value of $\mu_n C_{ox}$(Also known as kn'processtransconductance) For a N-channel MOSFET with minimum length fabricated in this process, find the required value of W so that the device exhibits a channel resistance r_{DS} of 1K at V_{GS}=1V. Given E_{ox}=3.45×10^{-11} F/m^2. (3)

Answer:

The permittivity of silicon dioxide is,

$$\varepsilon_{ox} = 3.45 \times 10^{-11} F/m$$

The oxide capacitance is,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Substitute $3.45 \times 10^{-11} F/m$ for ε_{ox} and 4 nm for t_{ox} in the equation.

$$C_{ox} = \frac{3.45 \times 10^{-11}}{4 \times 10^{-9}}$$

$$= 0.8625 \times 10^{-2} F/m^2$$

The Trans conductance parameter is,

$$k_n' = \mu_n C_{ox}$$

Substitute $450 cm^2/Vs$ for μ_n and $0.8625 \times 10^{-2} F/m^2$ for C_{ox} in the equation.

$$k_n' = (450 \times 10^{-4})(0.8625 \times 10^{-2})$$

$$= 388.125 \mu A/V^2$$

Hence, the value of process transconductance parameter is $k_n' = 388.125 \mu A/V^2$

1.5 Marks

The relation for the linear resistance is,

$$r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GD} - V_t)}$$

Substitute 1 kg for r_{DS} , $450 cm^2/Vs$ for μ_n , $0.8625 \times 10^{-2} F/mz$ for C_{ox}, , 0.18 μm for L , 1V for V_{GS} and 0.5V for V_t, in the equation.

$$1 \times 10^3 = \frac{1}{450 \times 10^{-4}(0.8625 \times 10{-}2)\frac{W}{.18 \times 10^{-6}}(1 - .5)}$$

(k_n')

$$W = \frac{.18 \times^{-6}}{194.0625 \times 10^{-3}}$$

$$W = 0.93 \times 10^{-6}$$

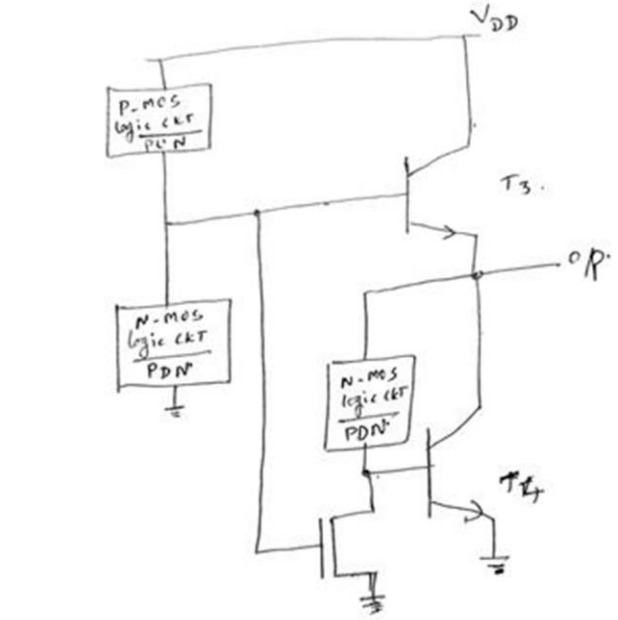
Hence, value of W is,0.93μm **1.5 Marks**

Mistakes in the units: 2.5 M

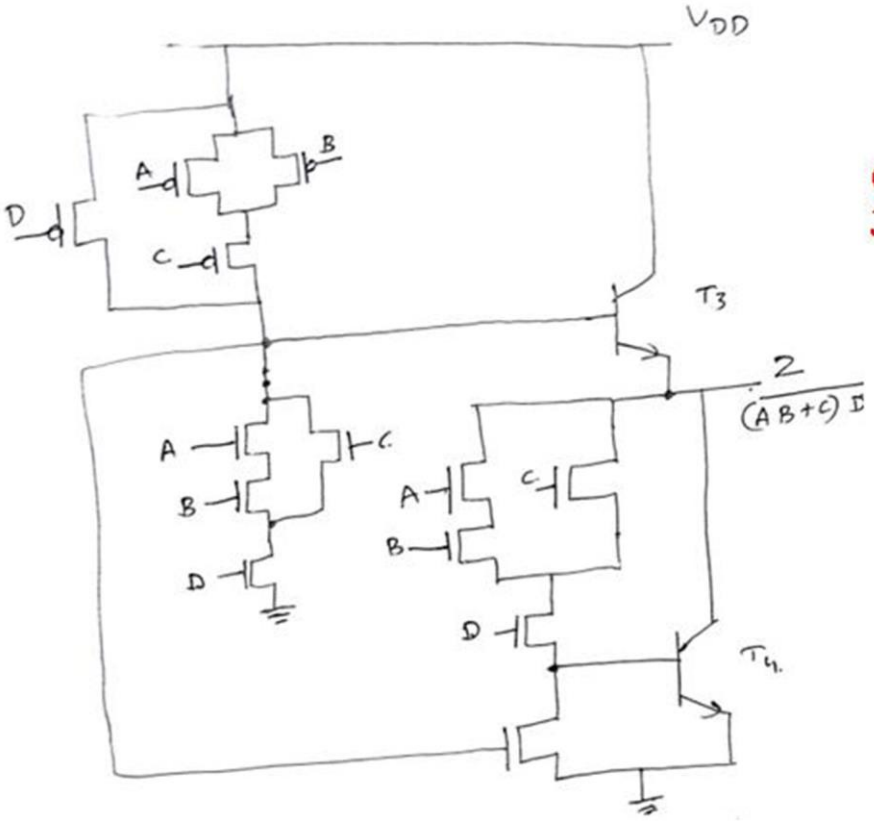
W calculation formula/procedure wrong but k_n' is correct: 1.5 M

Q14. Implement $Z = \overline{(A.B + C).D}$ using Bi-CMOS logic. (3)

Implement $Z = \overline{(AB+C)_D}$ **using Bi-CMOS logic.**



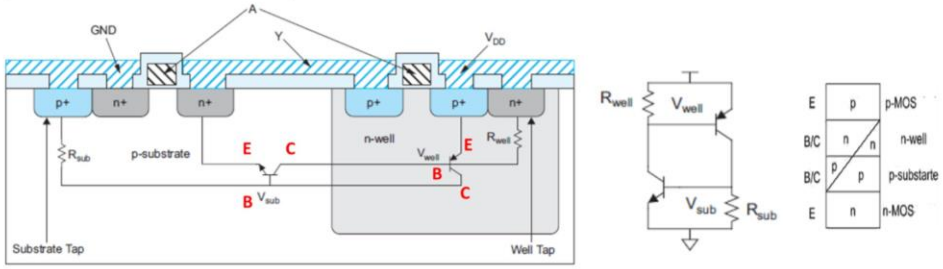
Marks will be awarded based on the mistakes 0M or 0.5M or 1M



Correct 3 Marks

Q15. Describe latch-up problem in CMOS and suggest solutions.(3)

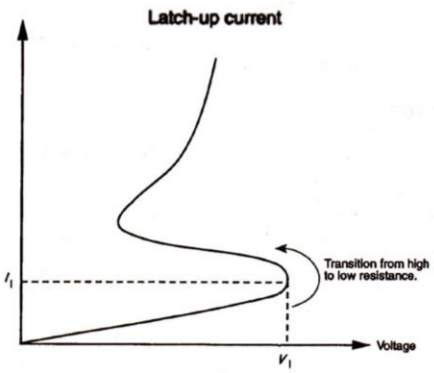
Tendency of CMOS to develop low-resistance path between *VDD* and VSS because of parasitic BJT is called Latch up.



Reason:
1. glitches on the supply rails
2. incident radiation

These BJTs form pnpn structure with positive feedback and virtually short circuit the power rail to ground, thus causing excessive current flows and even permanent device damage.

- PNP transistor whose base is formed by the n-well with its base-to-collector current gain (β1) as high as several hundreds.
- NPN transistor with its base formed by the p-type substrate. The base-to-collector current gain β2 of this lateral transistor may range from a few tenths to tens.
- *Rwell* represents the parasitic resistance in the n-well structure with its value ranging from 1 kΩ to 20 kΩ.
- *Rsub* can be as high as several hundred ohms.
- If the collector current of one of the transistors is temporarily increased by an external disturbance, however, the resulting feedback loop causes this current perturbation to be multiplied by *(*β1 β2*)*. This event is called the *triggering* of the pnpn.



Once triggered, each transistor drives the other transistor with positive feedback, eventually creating and sustaining a low impedance path between the power and the ground rails, resulting in latch-up.

$$\beta_1 \cdot \beta_2 \geq 1$$

Once latched-up, this condition will be maintained until the latch-up current drop below I1.

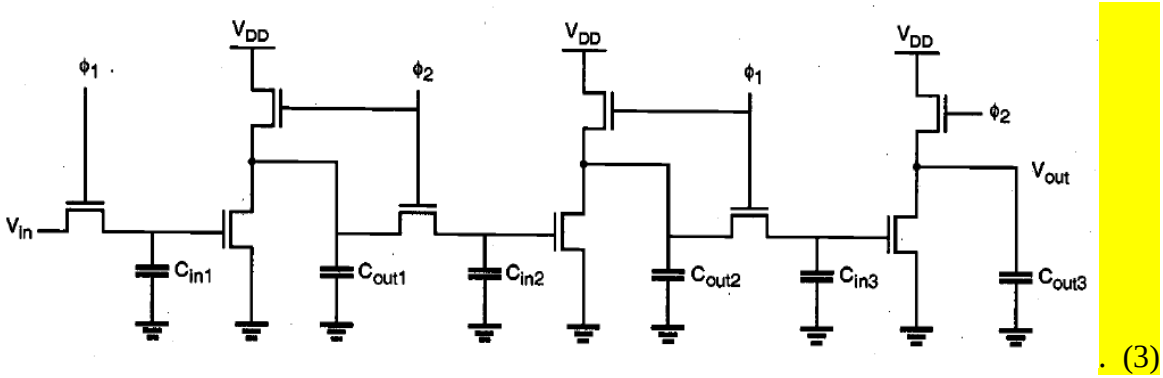
It is thus essential for a CMOS process to ensure that *V1* and *11* are not readily achieved in any normal mode of operation. **1.5 Marks**

Technique to overcome Latch-up

- an increase in substrate doping levels with a consequent drop in the value of *Rwell* .
- reducing *Rsub* by control of fabrication parameters and by ensuring a low contact resistance to *Vss.*
- Use of Trench Isolation.

1.5 Marks

Q16. Determine whether the dynamic shift register circuit depicted in the figure employs ratioed or ratioless logic. Provide reasoning to support your conclusion.

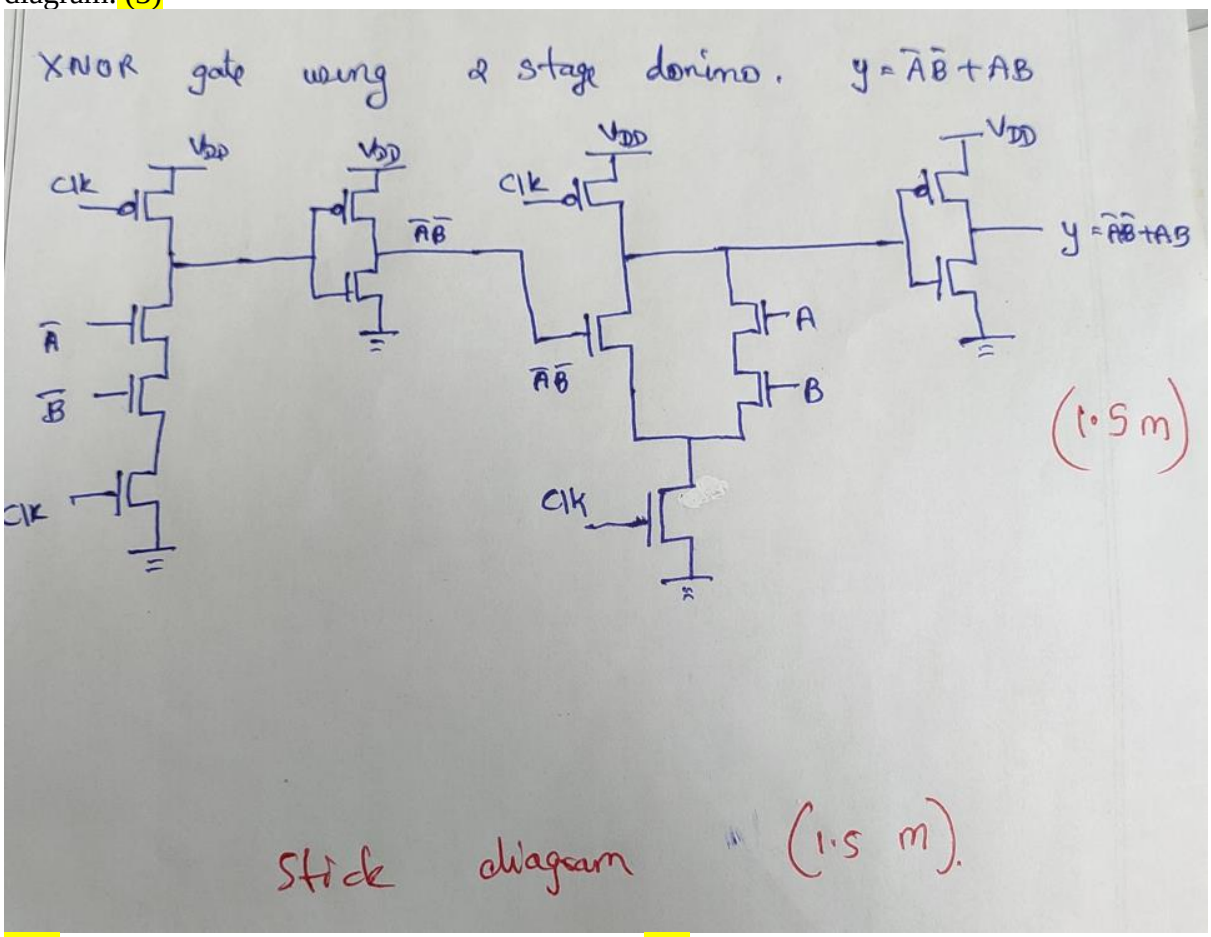


. (3)

The circuit is ratioed logic. (1 Mark)

When clock 1 is active, Cin1 is charged to logic 1 through pass transistor. When clock 2 is active, the load nMOS of 1st inverter will be turned on. Since, Cin1 is still in logic 1, the output of first inverter stage attains its valid logic level. This continues for the next stage of the circuit. The valid VOL (low output level) of each stage is strictly determined by driver-to-load ratio. Therefore, this is ratioed dynamic shift register. (2 marks)

Q17. Implement 2 input XNOR gate using 2 stage domino CMOS logic and draw its stick diagram. (3)



Q18. Why MOSFET is a self aligned technology? (2)

Explanation for bi-directional property of MOSFET i.e., drain and source terminals can be interchanged. (2 marks)