

VLSI:

Wednesday, 29 January 2025 12:10 AM

Moor's law :

predicts a steady decrease in gate length. IC densities have been doubling approximately every 18 months. And this doubling in size is accompanied by a similar exponential increase in circuit speed.

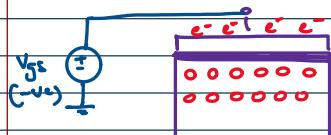
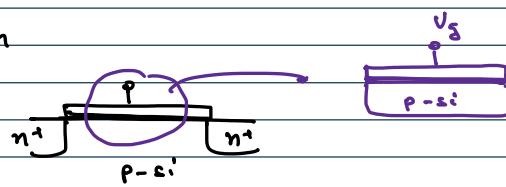
MOS vs BJT :

MOS BJT

Static power dissipation	: ↓	↑
Input impedance	: ↑	↓
Noise margin	: ↑	↓
Packing density	: ↑	↓
Fanout	: ↓	↑
Direction	: Bi	uni

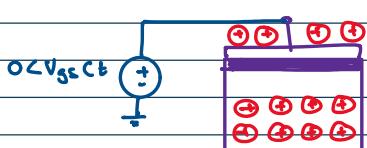
MOS Capacitance

i) Accumulation



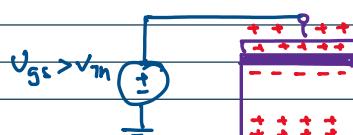
- on applying -ve potential at gate gate we can see that electron come up to gate.
- This e- attract holes from the body and hence holes come up to region beneath gate.

ii) Depletion:



- small positive charge at i/p
- holes are repelled from the region beneath the gate, creating depletion region.
 - positive charge not strong enough to attract e- to the region.

iii) Inversion:

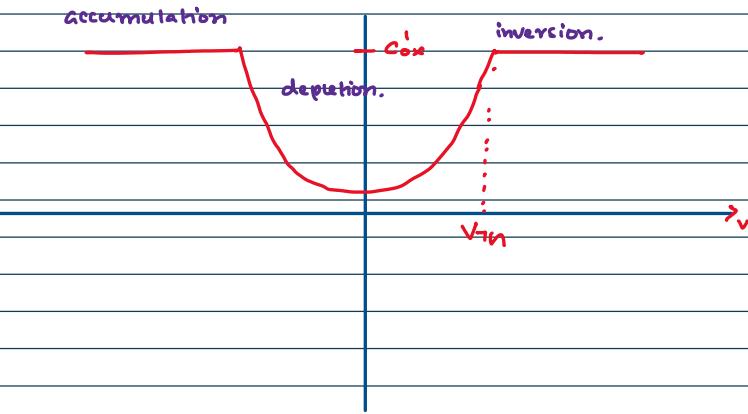


- higher voltage at input
- e- get attracted to the surface.
 - surface as higher concn. of e- compare to bulk.
Surface is more than n-type than bulk.
- ↳ Inversion.
and layer of e- formed is called inversion layer.

accumulation

inversion.

is called inversion layer.



MOSFET

Depletion Type
n-MOS p-MOS

Enhancement Type
n-MOS p-MOS

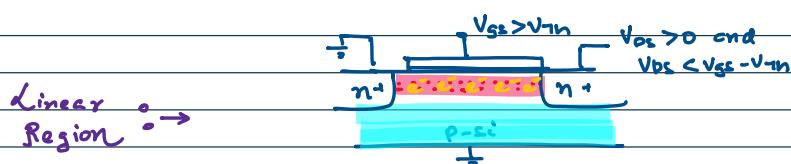
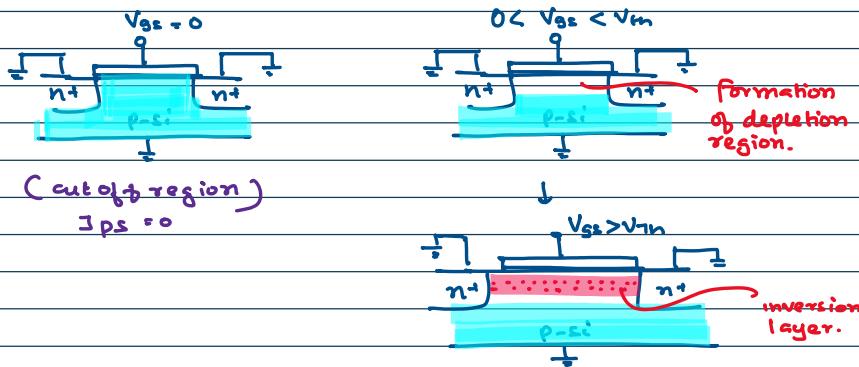
Enhancement NMOS

Regions of Operations :

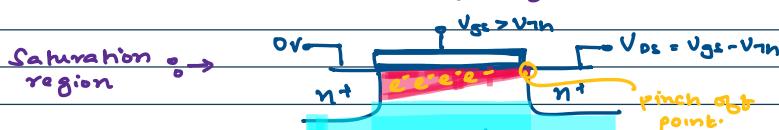
(a) Cutoff : $V_{GS} < V_m \rightarrow$ channel not formed
Thus $I_{DS} = 0$. (Accumulation region)

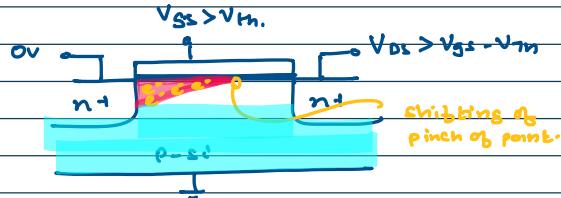
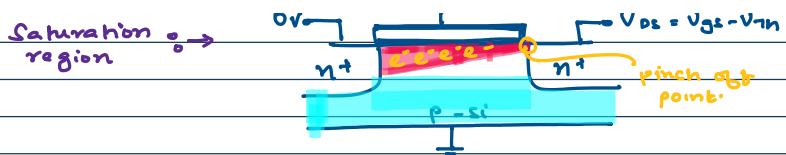
(b) Linear region : (weak inversion) region, drain current depends on gate and drain voltage

(c) Saturation region : (strong inversion region) drain current independent of drain source voltage

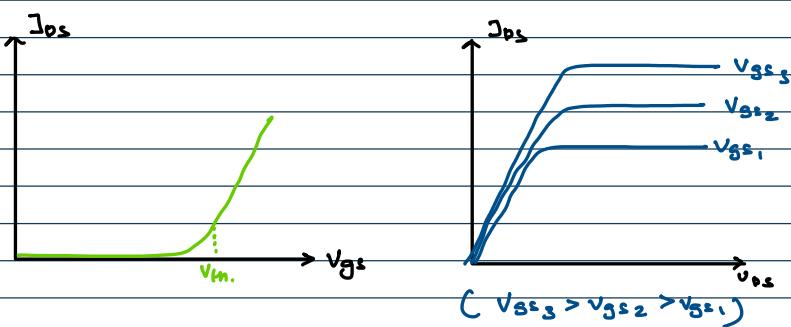
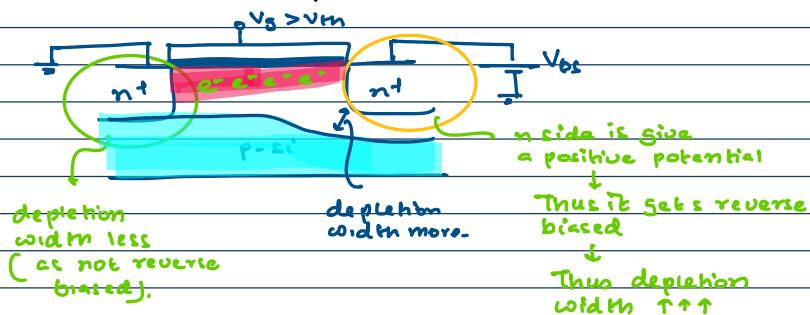


(potential difference created b/w drain and source and current starts flowing).

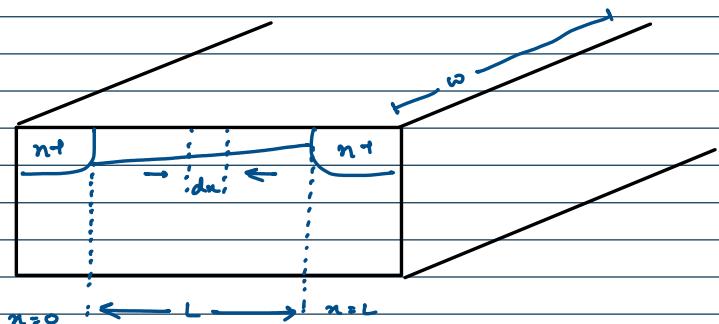




Q Drain side has more depletion region width ??



Q Drain to Source Current (I_{DS}) :



at small dx we have charge dQ

$$\therefore Q = CV$$

$$\text{or } Q = C_{ox} V$$

at $x=0$:

at source $V_S = 0$, $V_G = V_{GS}$

Out of V_{GS} , V_{TH} is used for channel formation

$$\therefore (V_c)_{x=0} = V_{GS} - V_{TH}$$

at $x=L$: $V_D = V_{GS} - V_{TH} - V_{DS}$

at any point x let $(V_D)_x = V_{SS} - V_{DS} - V_x$

$$\therefore d\theta = -CV = -Cox [V_{GS} - V_{TH} - V_n] / \text{unit area.}$$

area = $w \cdot dn$

$$\text{or, } d\theta = -Cox w \cdot [V_{GS} - V_{TH} - V_n] dn$$

$$\therefore J = \frac{d\theta}{dt} = -Cox w [V_{GS} - V_{TH} - V_n] \frac{dx}{dt}$$

$$\text{or, } J = -Cox w [V_{GS} - V_{TH} - V_n] v_d \quad \text{drift velocity.}$$

$$\text{or, } J = -Cox w [V_{GS} - V_{TH} - V_n] \mu E$$

$$= -Cox w [V_{GS} - V_{TH} - V_n] \mu \left(-\frac{dv}{dx} \right)$$

$$= \mu Cox w [V_{GS} - V_{TH} - V_n] \frac{dv}{dn}$$

$$\text{on } \int_0^L J dn = \mu Cox w \int_0^{V_{DS}} [V_{GS} - V_{TH} - V_n] dv$$

$$\text{or, } J [n]_0^L = \mu n Cox w [V_{GS} - V_{TH}] v \Big|_0^{V_{DS}} - \frac{V^2}{2}$$

$$\text{or, } J_L = \mu n Cox w (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}$$

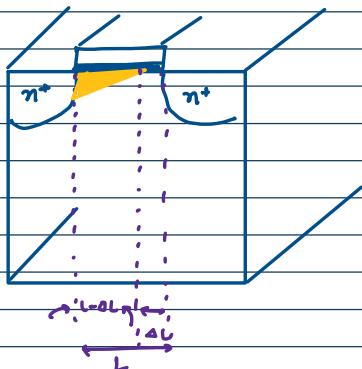
$$\text{or, } J = \frac{1}{2} \mu n Cox \frac{w}{L} (2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2)$$

at saturation region we have

$$\textcircled{1} \quad V_{DS} = V_{GS} - V_{TH}$$

$$\therefore J_{DS} = \frac{1}{2} \mu n Cox \frac{w}{L} (V_{GS} - V_{TH})^2$$

channel length modulation



At Saturation

$$J_{DS} = \frac{1}{2} \mu n Cox \frac{w}{L} (V_{GS} - V_{TH})^2$$

$$\text{or, } J_{DS} = \frac{1}{2} \mu n Cox \frac{w}{L - \alpha L} (V_{GS} - V_{TH})^2$$

$$\text{or, } J_{DS} = \frac{1}{2} \mu n Cox \frac{w}{L} \left(\frac{V_{GS} - V_{TH}}{1 - \frac{\alpha L}{L}} \right)^2$$

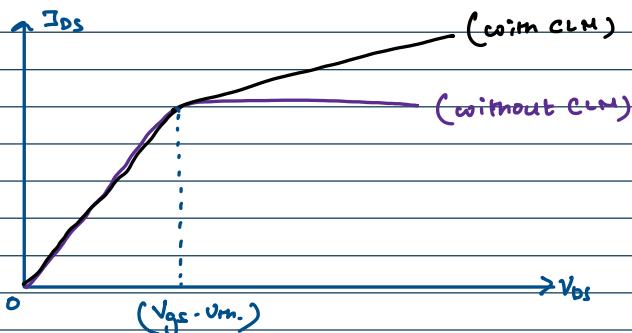
$$\text{or, } J_{DS} = \frac{1}{2} \mu n Cox \frac{w}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{\alpha L}{L} \right)^{-2}$$

$$\text{or, } J_{DS} = \frac{1}{2} \mu n Cox \frac{w}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{\alpha L}{L} \right)$$

$$\Delta L \propto V_{DS}$$

$$\text{or, } \frac{\Delta L}{L} = \lambda V_{DS}$$

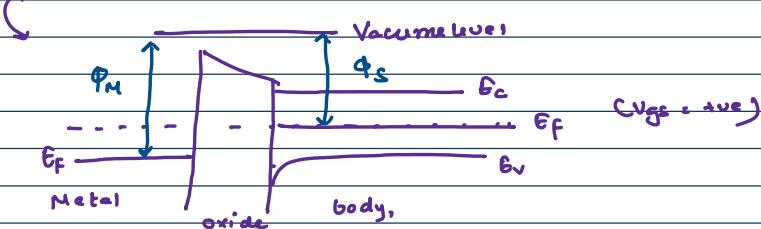
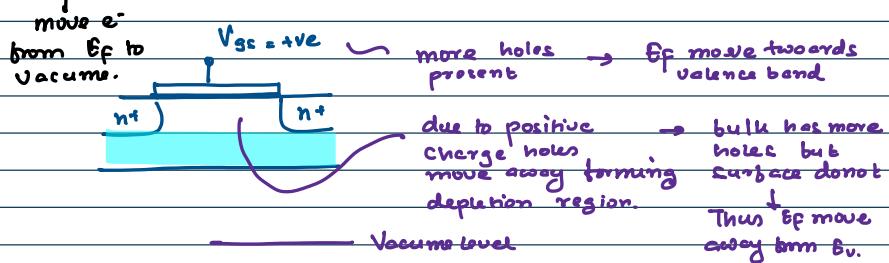
$$\therefore I_{DS} = \frac{1}{2} \sinh \frac{q}{L} (V_{GS} - V_m)^2 (1 + \lambda V_{DS})$$



Threshold Voltage

↓
is defined by
four parameters.

(a) Work function difference b/w channel and gate.



Φ_M : work function of metal. Φ_S : work function of silicon } Clearly there is a mismatch.

(b) The gate voltage component to change surface potential:

→ Fermi potential of substrate surface should change from Φ_F to $-\Phi_F$ for generation of inversion layer.

(c) The gate voltage component to offset the depletion region charge.

(d) The voltage component to offset the fixed charge in gate oxide and silicon oxide interface.

work function Φ_{MS} is given as

$$\circ \quad \Phi_{MS} = \Phi_{substrate} - \Phi_{Metal}$$

for surface inversion, surface potential should be changing from Φ_F to $-\Phi_F$. So net charge will be $-\Phi_F - \Phi_F = -2\Phi_F$.

On applying voltage at gate holes are repelled inside substrate forming depletion region. The Region is now left with ions which forms offset voltage due to charges of ions.

$$V_{BD} = -\sqrt{2qN_A\epsilon_{Si}|-2\Phi_F|}$$

If substrate bias is present then we need to add it as well.

$$\therefore V_B = -\sqrt{2qN_A\epsilon_{Si}|-2\Phi_F + V_{SB}|}$$

Thus to nullify this we need to apply $-\frac{\Phi_B}{C_{ox}}$; where C_{ox} is gate oxide capacitance per unit area.

Also there is a fixed positive charge density ρ_{ox} due to lattice imperfection at interface. Thus to nullify this we need to apply $-\frac{\rho_{ox}}{C_{ox}}$.

$$\therefore V_{Th} = \Phi_{MS} - 2\Phi_F - \frac{\rho_A}{C_{ox}} - \frac{\rho_{ox}}{C_{ox}}$$

Second Order Effects :

1) Velocity saturation

$$V_d = VE$$

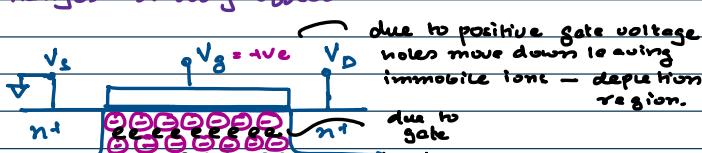
$$\text{as } E \propto V_d \propto I$$

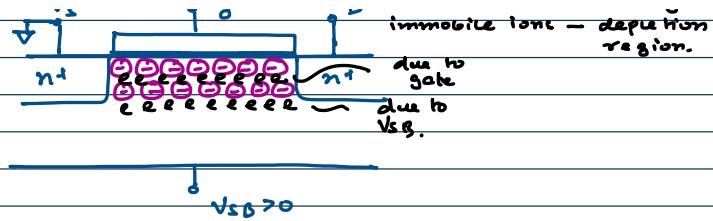
But at particular velocity \rightarrow Velocity becomes constant \rightarrow saturation.

2) Mobility degradation :

due to strong electric field it causes carrier to scatter against the surface and hence it reduces carrier mobility.

3) Body Effect : when potential difference b/w source and body i.e. V_{SB} \rightarrow threshold voltage of MOSFET changes \rightarrow body effect.





$$V_{CB} > 0$$

or, $V_E - V_B > 0$

or, $V_B < 0 \therefore V_B$ is negative.

a layer of e^- gets formed near the channel.
(similar phenomenon to gate)
 $\hookrightarrow (V_{in} ++)$

charge in depletion region is different.

$$\therefore V_{in} = \Phi_{MS} - 2\Phi_F - \frac{\Phi_D}{C_{ox}} - \frac{\Phi_{SB}}{C_{ox}}$$

new depletion region charge.

Constant values.

$$\text{or, } V_{in} = \text{const} - \frac{\Phi_D}{C_{ox}}$$

$$\Delta V_{in} = V_{in} - V_{in}' = -\frac{\Phi_D}{C_{ox}} - \left(-\frac{\Phi_D'}{C_{ox}} \right)$$

$$\text{or, } \Delta V_{in} = -\frac{\Phi_D}{C_{ox}} + \frac{\Phi_D'}{C_{ox}} = \frac{1}{C_{ox}} (\Phi_D' - \Phi_D)$$

$$\text{or, } \Delta V_{in} = \frac{1}{C_{ox}} \left[-\sqrt{2qN_A\epsilon_{Si}[-2\Phi_F + V_{SB}]} + \sqrt{2qN_A\epsilon_{Si}[-2\Phi_F]} \right]$$

$$\text{or, } \boxed{\Delta V_{in} = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}} \left[\sqrt{2\Phi_F} - \sqrt{2\Phi_F + V_{SB}} \right]}$$

$$\text{or, } V_{in} - V_{in}' = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}} \left[\sqrt{2\Phi_F} - \sqrt{2\Phi_F + V_{SB}} \right]$$

Let $\gamma = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}}$ = Body effect coefficient.

$$\therefore V_{in}' = V_{in} - \gamma \left[\sqrt{2\Phi_F} - \sqrt{2\Phi_F + V_{SB}} \right]$$

$$= V_{in} - \gamma \sqrt{2\Phi_F} + \gamma \sqrt{2\Phi_F + V_{SB}}$$

$$\Rightarrow \boxed{V_{in}' = V_{in} + \gamma \left[\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right]}$$

New threshold voltage considering body effect.

Threshold voltage without body effect

Body effect coefficient

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}}$$

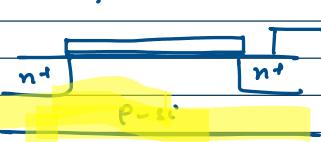
$$q_F = \frac{kT}{q} 2n \left(\frac{N_A}{N_D} \right)$$

- o k : Boltzmann const.
- o T : Temp. in Kelvin
- o N_A : doping level of substrate
- o N_D : doping level of wells.

for $T = 300K$

we have $\frac{kT}{q} = 26mV$.

4. Drain punch through:

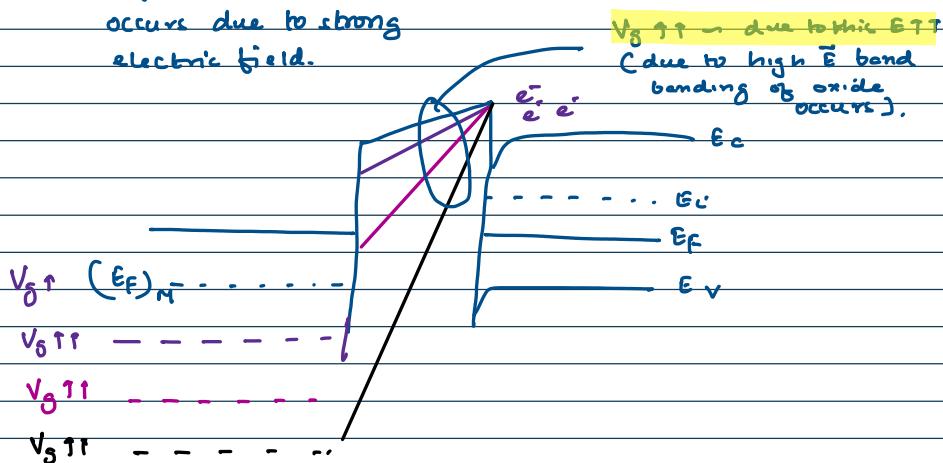


- o $V_{DS} \uparrow\uparrow$
- o drain side get more reverse biased
- o depletion width $\uparrow\uparrow$
- o At a time, depletion layer will punch through source

5. Tunneling :

(a) F-N tunneling (Fowler-Nordheim):

occurs due to strong electric field.



(b) Direct tunneling:

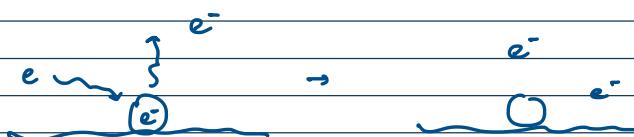
- o Occur at lower voltage
- o Mainly due to thin thickness layer of MOSFET's present.

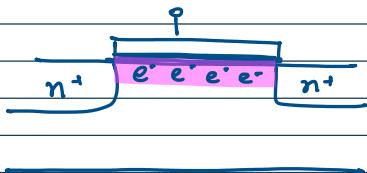
6. Hot Carrier effect

$E \uparrow\uparrow \sim$ due to strong electric field energy of electrons increase very much
 ↓
 (Hot carrier electron)

effect :

(i) Impact ionization:





- This electrons due to high energy and speed may collide with lattice creating e⁻-hole pair.

Thus hole starts moving towards body.

- This e⁻ generated thus move towards the drain, but holes experience a strong repulsive force.

This causes a small current flow due to drain and body. (drain body current)

② Gate Current



due to high energy and velocity they may penetrate through SiO₂ oxide layer causing a current to flow in opposite direction - gate current.

Inverter Circuit

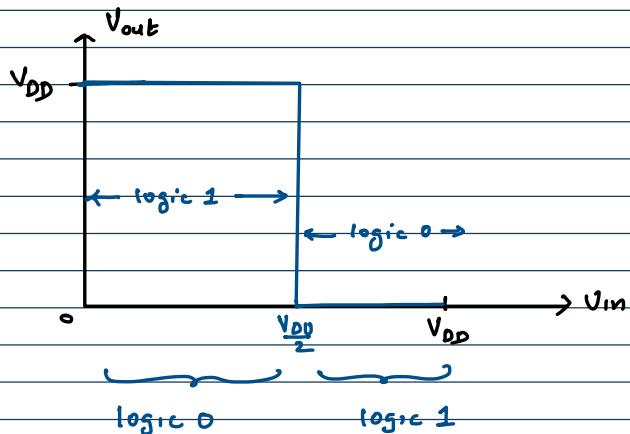
1. Ideal inverter
2. Resistive load inverter
3. n-MOS inverter
 - (a) enhancement load
 - (b) depletion load
4. C-MOS inverter.

• Ideal inverter :



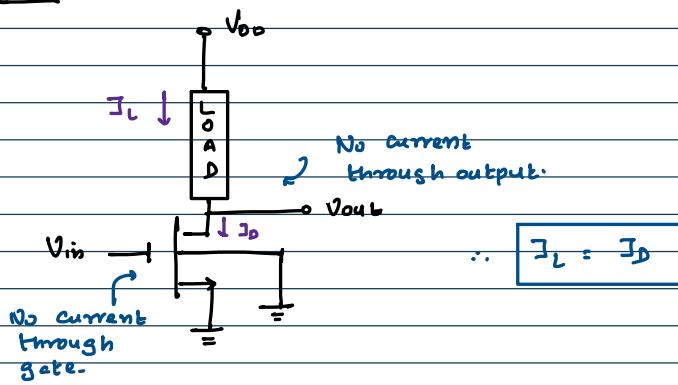
Truth table	
A	Y
0	1
1	0

logic '1' : V_{DD}
logic '0' = gnd.



2. n-Mos inverter





Case : If V_{in} is less ($V_{in} < V_{th}$) : No inversion layer.

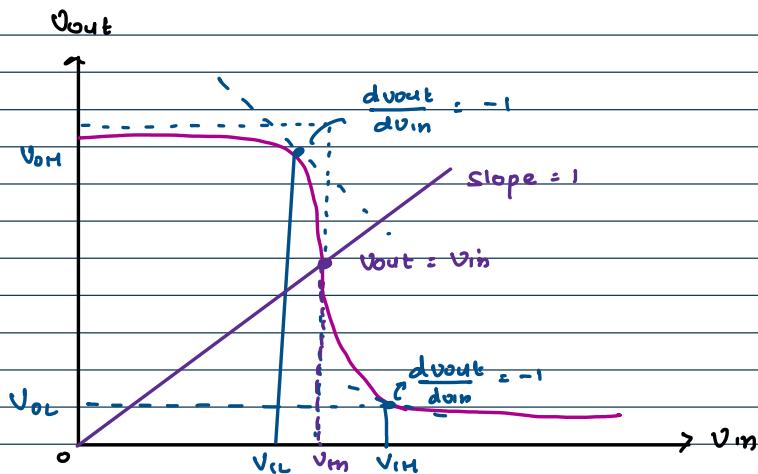
\therefore No drain current (I_D very very small)

$$\therefore V_{out} = V_{DD} - I_D R_L$$

$$\text{or, } V_{out} \approx V_{DD}$$

Case : On increasing V_{in} further — inversion layer starts forming and hence $I_D = I_L$ current starts increasing.

$$\therefore V_{out} = V_{DD} - I_L R_L \quad \text{and hence } V_{out} \downarrow$$



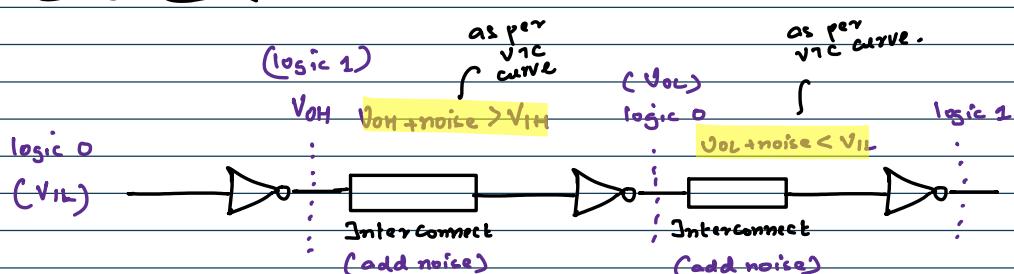
o V_{OH} : high o/p voltage when o/p is logic 1

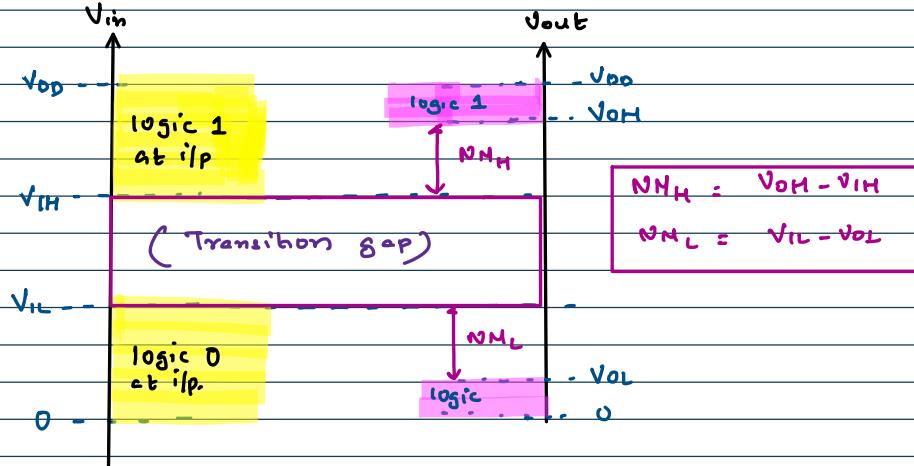
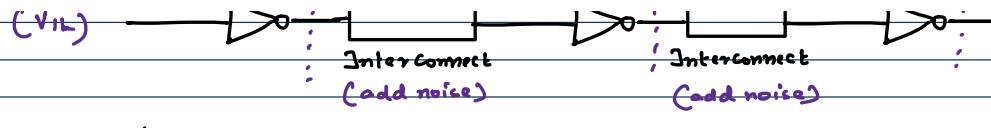
o V_{OL} : low o/p voltage when o/p is logic 0

o V_{IL} : Maximum i/p voltage upto which o/p is logic 1.

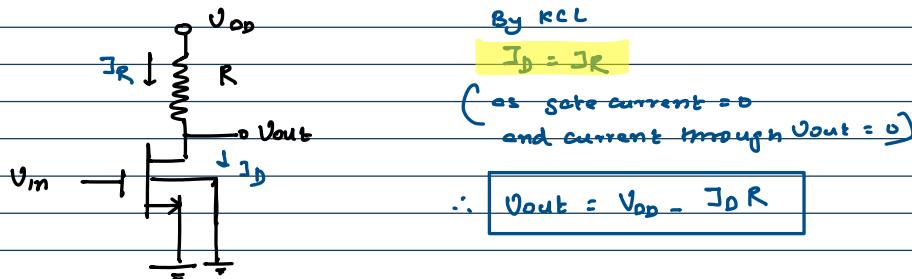
o V_{IH} : Minimum i/p voltage for which o/p is logic 0.

Noise margin %





Resistive load inverter :

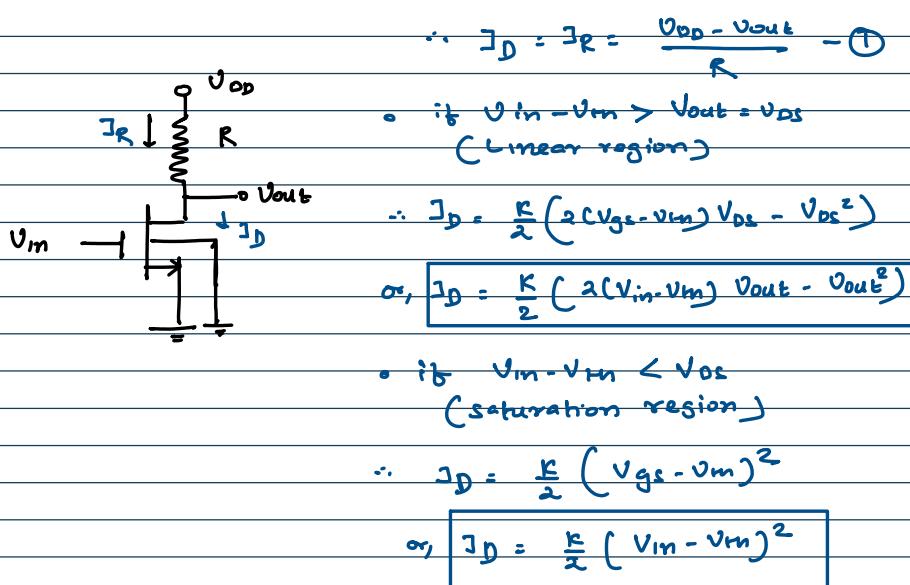


(o) If input voltage is logic 0 then inversion layer will not be formed and hence $I_D = 0$.

$$\therefore V_{out} = V_{DD}$$

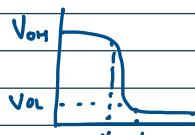
(o) If input voltage is logic 1, then inversion layer will be formed and hence I_D will increase and at a point output will be logic 0.

$$\therefore V_{out} = 0$$



$$\text{or } I_D = \frac{k}{2} (V_{in} - V_{th})^2$$

V_{OH} = ?

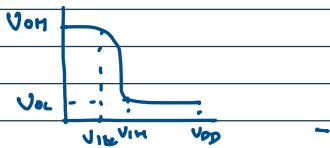


when $V_{in} = 0$; $V_{out} = V_{OH}$
 \therefore MOSFET \rightarrow cut-off region

$$\therefore V_{out} = V_{DD} - I_D R_L$$

$$\text{or } V_{OH} = V_{DD}$$

V_{OL} = ?



when $V_{in} = V_{DD}$, $V_{out} = V_{OL}$

\therefore clearly $V_{in} - V_{th} > V_{out}$
 (Thus mosfet in linear region)

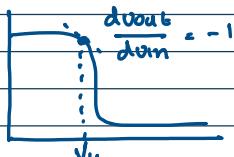
$$\therefore \frac{V_{DD} - V_{out}}{R} = \frac{k}{2} [2(V_{GS} - V_{th})^2 / K * R_L - V_{DS}^2]$$

$$\Rightarrow \frac{V_{DD} - V_{OL}}{R} = \frac{k}{2} [2(V_{DD} - V_{th})^2 / K * R_L - V_{OL}^2]$$

$$\Rightarrow V_{OL}^2 - 2(V_{DD} - V_{th} + \frac{1}{KR})V_{OL} + \frac{2}{KR}V_{DD} = 0$$

$$\therefore V_{OL} = V_{DD} - V_{th} + \frac{1}{KR} - \sqrt{(V_{DD} - V_{th} + \frac{1}{KR})^2 - \frac{2V_{DD}}{KR}}$$

V_{IL} = ?



at point V_{IL} we have

$$V_{out} = V_{OH} \quad (\text{logic 1})$$

$$V_{in} = V_{IL}$$

$\therefore V_{out} > V_{in} - V_{th}$
 (MOSFET in saturation region)

$$\therefore \frac{V_{DD} - V_{out}}{R} = \frac{k}{2} (V_{in} - V_{th})^2$$

differentiating w.r.t to V_{in}

$$\frac{d}{dV_{in}} \left(\frac{V_{DD} - V_{out}}{R} \right) = \frac{d}{dV_{in}} \frac{k}{2} (V_{in} - V_{th})^2$$

$$\text{or, } \frac{dV_{DD}/R}{V_{in}} - \frac{1}{R} \frac{dV_{out}}{dV_{in}} = \frac{k}{2} 2(V_{in} - V_{th})$$

$$\text{or, } \frac{dV_{out}}{dV_{in}} - \frac{1}{R} \frac{dV_{out}}{dV_{in}} = \frac{K}{2} (V_{in} - V_m)$$

$$\text{or, } -\frac{1}{R} \frac{dV_{out}}{dV_{in}} = K (V_{in} - V_m)$$

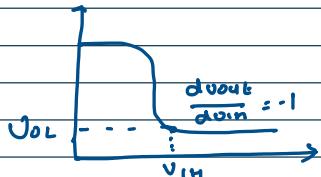
$$\text{or, at } V_{in} = V_{IL} \text{ we have } \frac{dV_{out}}{dV_{in}} = -1$$

$$\therefore \frac{1}{R} = K (V_{IL} - V_m)$$

$$\text{or, } V_{IL} - V_m = \frac{1}{KR}$$

$$\text{or, } V_{IL} = V_m + \frac{1}{KR}$$

V_{OL} ?



at $V_{in} = V_m$ we have $V_{out} = V_{OL}$

$$\therefore V_{out} < V_{in} - V_m \quad (\text{Linear region})$$

$$\therefore \frac{V_{DD} - V_{out}}{R} = \frac{K}{2} \left(2(V_{in} - V_m) V_{out} - V_{out}^2 \right)$$

or, differentiating w.r.t to V_{in}

$$-\frac{1}{R} \frac{dV_{out}}{dV_{in}} = \frac{K}{2} \left[2(V_{in} - V_m) \frac{dV_{out}}{dV_{in}} - 2V_{out} \frac{dV_{out}}{dV_{in}} \right]$$

$$\text{or, } \frac{1}{R} = \frac{K}{2} \left[2(V_{in} - V_m) + 2V_{out} \right]$$

$$\text{or, } \frac{1}{R} = -K(V_m - V_m) + KV_{out}$$

$$\text{or, } \frac{1}{R} = -K(V_{IH} - V_m) + KV_{out}$$

$$\text{or, } V_{IH} = V_m + 2V_{out} - \frac{1}{KR}$$

$$\text{or, } V_{IH} = V_m + \sqrt{\frac{8}{3} \frac{V_{DD}}{KR} - \frac{1}{KR}}$$

H Avg. DC power consumption

$$P = V \times I$$

for 50% duty cycle

$$V = \frac{V_{DD}}{2}$$

$$I = \frac{V_{DD} - V_{OL}}{R}$$

$$\therefore P = \frac{V_{DD}}{2} \left(\frac{V_{DD} - V_{OL}}{R} \right)$$

Q. Design a resistive load inverter with $P_L = 1k\Omega$ such that $V_{OL} = 0.6V$
The enhancement type driver transistor has the following parameters

$$V_{DD} = 5V, V_{TH} = 1V, \gamma = 0.1V^{1/2}, R = 0, \mu nCox = \frac{224A}{V^2}$$

Determine : (i) ω/L ratio (ii) V_{IH} and V_{IL} (iii) Noise margin.

$$\rightarrow V_{OL} = 0.6V$$

$$\therefore \frac{V_{DD} - V_{OL}}{R} = \frac{k}{2} [2(V_{GS} - V_{TH}) V_{OL} - V_{OL}^2]$$

$$\text{or, } \frac{5 - 0.6}{1000} = \frac{22 \times 10^{-6}}{2} \times \frac{\omega}{L} [2(V_{DD} - V_{TH}) V_{OL} - V_{OL}^2]$$

$$\text{or, } \frac{4.4}{1000} = 11 \times 10^{-6} \frac{\omega}{L} [2(5 - 1) 0.6 - 0.6^2]$$

$$\therefore \frac{\omega}{L} = 90$$

$$(i) V_{IL} = V_{TH} + \frac{1}{kR} = 1 + \frac{1}{22 \times 10^{-6} \times 90 \times 10^3}$$

$$\Rightarrow V_{IL} = 1.505V.$$

$$V_{IH} = V_{TH} + \sqrt{\frac{8}{3} \frac{V_{DD}}{kR}} - \frac{1}{kR}$$

$$\Rightarrow V_{IH} = 1 + \sqrt{\frac{8}{3} \frac{5}{1.98}} - \frac{1}{1.98}$$

$$\Rightarrow V_{IH} = 3.08V$$

$$(iii) NMH = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

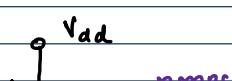
$$\text{or, } NMH = 5 - 3.08 = 1.92V.$$

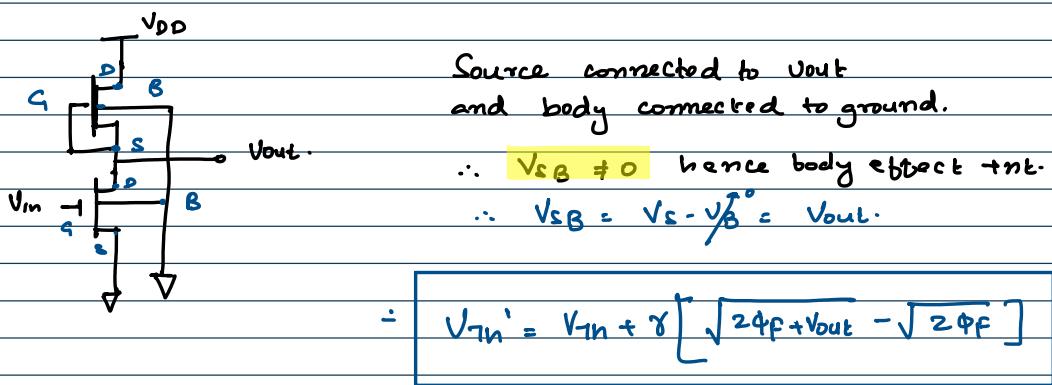
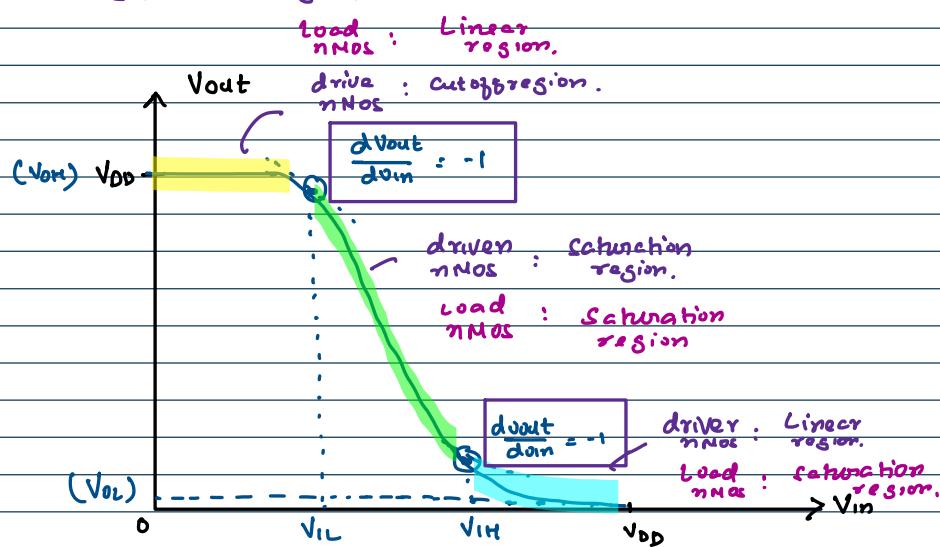
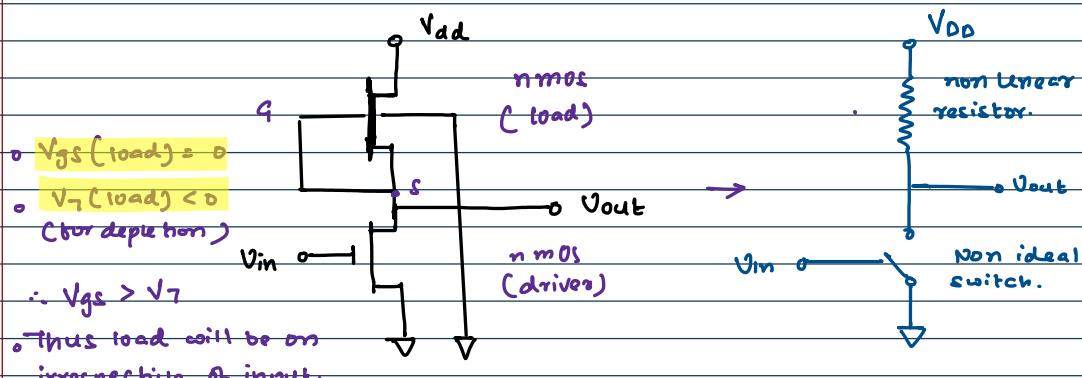
$$NML = V_{IL} - V_{OL}$$

$$\text{or, } NML = 1.505 - 0.6 = 0.905V$$

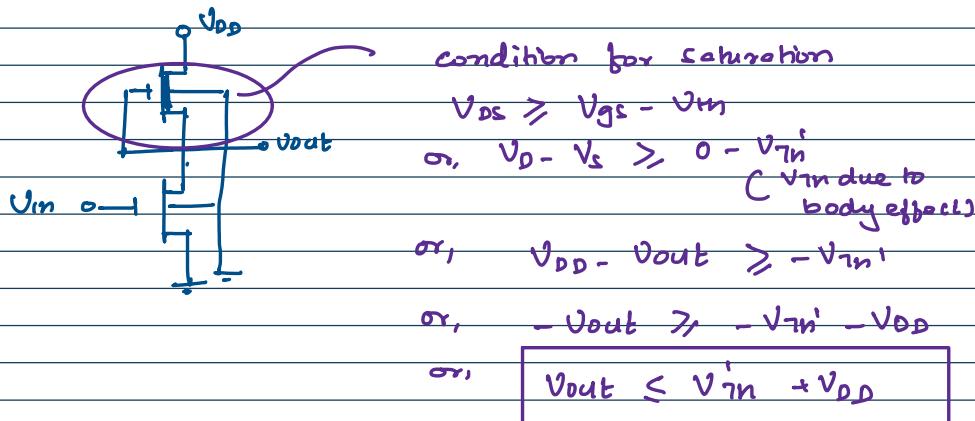
Depletion load nMOS inverter :

- o It has sharper better VTC transition
- o Better noise margin
- o single power supply.
- o smaller overall layout area.
- o It has reduced standby leakage current.





Operating region



$$\therefore I_{DS} = \frac{k}{2} (V_{GS} - V_m)^2$$

$$\text{on } I_{DS} = \frac{k}{2} (0 - V_{Th})^2$$

$$\text{or, } I_{DS} = \frac{k}{2} (-V_{Th})^2$$

(V_{Th} is a function of V_{out})

$$\therefore V_{out} \leq V_{DD} + V_{Th}$$

(V_{Th} is always negative)

when V_{out} is very large \Rightarrow Depletion load in linear region.

$$\therefore (I_D)_{load} = \frac{k_{load}}{2} \left[2 (V_{GS}^0 - V_{Th,load}) V_{DS} - V_{DS}^2 \right]$$

$$\text{on } (I_D)_{load} = \frac{k_{load}}{2} \left[2 |V_{Th,load}| (V_D - V_S) - (V_D - V_S)^2 \right]$$

$$\text{or } (I_D)_{load} = \frac{k_{load}}{2} \left[2 |V_{Th,load}| (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

V_{in}	V_{out}	Driver operating region	Load operating region
V_{OL} ($V_{OL} < V_m$)	V_{OH}	Cutoff region	Linear region
V_{IL} ($V_{IL} > V_m$)	$\approx V_{OH}$	Saturation region	Linear region
V_{IH}	V_{OL}	Linear region	Saturation region
V_{OH}	V_{OL}	Linear region	Saturation region.

$$\frac{V_{OH} - ?}{t}$$

Output voltage when input is 0 or V_{OL} .

Driver NMOS : cutoff

Load NMOS : linear

$$\therefore I_D = 0 = I_L = \frac{k_{load}}{2} \left[2 |V_{in}| (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

For equation to be 0 we should have

$$V_{DD} - V_{OH} = 0 \quad \left\{ \begin{array}{l} \therefore k_{load} \neq 0 \\ V_{in} \neq 0 \end{array} \right.$$

or, $V_{OH} = V_{DD}$

$$\underline{\underline{V_{OL}}} = ??$$

↓
output voltage when $V_{in} = V_{OH} \rightarrow V_{out} = V_{OL}$

Driver : linear region

Load : saturation region

$$\therefore I_D = \frac{k_{Driver}}{2} \left[2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 \right] = I_L = \frac{k_{load}}{2} (V_{SS} - V_{in})^2$$

$$\text{or, } \frac{k_{Driver}}{2} \left[2(V_{OH} - V_{TH}) V_{OL} - V_{OL}^2 \right] = \frac{k_{load}}{2} (-V_{in})^2$$

$$\therefore \underline{\underline{V_{OL} = V_{OH} - V_{TH} - \sqrt{(V_{OH} - V_{TH})^2 - \left[\frac{k_{load}}{k_{Driver}} \right] \cdot V_{in}^2}}}$$

depends on
 $V_{out} = V_{OL}$

$$\underline{\underline{V_{IL}}} = ??$$

↓
minⁿ. input voltage for which $V_{out} = V_{OH}$.

Driver : saturation region

Load : linear region.

$$\therefore I_{Driver} = I_{load}$$

$$\text{or, } \frac{k_{\text{driver}}}{2} \left[(V_{IL} - V_{IN})^2 \right] = \frac{k_{\text{load}}}{2} \left[2(V_{GS} - V_{TH}) (V_{OD} - V_{OUT}) - (V_{OD} - V_{OUT})^2 \right]$$

or, at $V_{IN} = V_{IL}$ we have $\frac{dV_{OUT}}{dV_{IN}} = -1$

$$\therefore V_{IL} = V_{TH} + \left(\frac{k_{\text{load}}}{k_{\text{driver}}} \right) \left[V_{OUT} - V_{OD} + |V_{IN}'| \right]$$

$$\underline{\underline{V_{IH}}} = ?$$

↓
minimum V_{IN} for after which $V_{OUT} = V_{OD}$.

Driver : Linear region.

Load : Saturation region.

$$\therefore I_{\text{Driver}} = I_{\text{load}}$$

$$\text{or } \frac{k_{\text{driver}}}{2} \left[2(V_{GS} - V_{TH}) V_{OUT} - V_{OUT}^2 \right] = \frac{k_{\text{load}}}{2} \left[V_{SS} - V_{TH} \right]^2$$

$$\text{or } \frac{k_{\text{driver}}}{2} \left[2(V_{IH} - V_{TH}) V_{OUT} - V_{OUT}^2 \right] = \frac{k_{\text{load}}}{2} \left[-V_{TH} \right]^2$$

at $V_{IN} = V_{IH}$ we have $\frac{dV_{OUT}}{dV_{IN}} = -1$

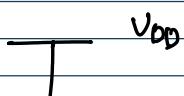
$$\therefore V_{IH} = V_{TH} + 2V_{OUT} + \left(\frac{k_{\text{load}}}{k_{\text{driver}}} \right) \left[-V_{TH}' \right] \frac{dV_{TH}'}{dV_{OUT}}$$

$$V_{TH}' = V_{TH} + \gamma \left[\sqrt{2\phi_F + V_{OUT}} - \sqrt{2\phi_F} \right]$$

$$\therefore \frac{dV_{TH}'}{dV_{OUT}} = \frac{d}{dV_{OUT}} V_{TH} + \gamma \frac{d}{dV_{OUT}} \sqrt{2\phi_F + V_{OUT}} - \frac{d}{dV_{OUT}} \sqrt{2\phi_F}$$

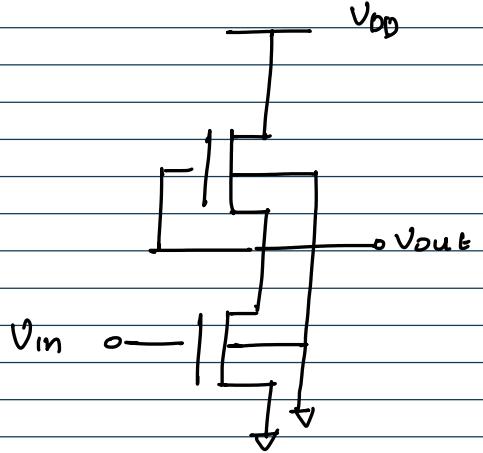
$$\text{or, } \frac{dV_{TH}'}{dV_{OUT}} = \frac{\gamma}{2\sqrt{2\phi_F + V_{OUT}}}$$

Q Calculate critical voltages ($V_{OL}, V_{OH}, V_{IL}, V_{IH}$) and find noise margin of following depletion load inverter.



$$\circ V_{DD} : 5V$$

.. 1.01



- $V_{DD} = 5V$
- $V_{TH\text{ driver}} = 1.0V$
- $V_{TH\text{ load}} = -3.0V$.
- $(W/L)_{\text{driver}} = 2 \quad (W/L)_{\text{load}} = 1/3$
- $U_{\text{driver}} = U_{\text{load}} = 25 \mu A/V^2$
- $\gamma = 0.4 V^{1/2}$
- $q_y = -0.3V$.

$$(i) \quad V_{DD} = V_{DD} = 5V$$

$$(ii) \quad V_{OL} = V_{DD} - V_{TH} - \sqrt{(V_{DD} - V_{TH})^2 - \left(\frac{U_{\text{load}}}{U_{\text{driver}}} \right) \cdot \left| V_{TH\text{ load}} \right|^2}$$

$$\Rightarrow V_{OL} = 5 - 1 - \sqrt{(5-1)^2 - \frac{25 \mu A \times 4/3}{25 \mu A \times 2} \cdot 3^2}$$

$$= 4 - \sqrt{4^2 - \frac{9}{6}}$$

$$= 4 - \sqrt{16 - 9/6} = 4 - \sqrt{\frac{87}{6}}$$

$$= 0.192V.$$

Now using V_{OL} we can calculate $V_{TH\text{ (load)}}$ again

$$\therefore V_{TH'} = V_{TH} + \gamma \left(\sqrt{|2\Phi_f| + V_{OL}} - \sqrt{|2\Phi_f|} \right)$$

$$\text{or, } V_{TH'} = -3 + 0.4 \left(\sqrt{0.6 + 0.192} - \sqrt{0.6} \right)$$

$$\text{or, } V_{TH'} = -2.95V.$$

Using this $V_{TH'}$ we can calculate again V_{OL}

$$\therefore V_{OL} = 0.186V$$

$$3) \quad V_{IL} = V_{TH} + \frac{U_{\text{load}}}{U_{\text{driver}}} \left[V_{out} - V_{DD} + |V_{TH\text{ load}}| \right]$$

$$\text{or, } V_{IL} = 1 + \frac{1}{6} (V_{out} - 5 + 2.36)$$

$$\text{or, } V_{IL} = 0.167 V_{out} + 0.56$$

$$\therefore V_{out} = 6 V_{IL} - 3.36$$

Substitution equation in 1st eqn

$$\therefore V_{out} = 6V_{IL} - 3.35$$

Substituting equation in KCL eqn

$$\frac{k_{load}}{2} \left[2(V_{GS} - V_{TH}) (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right] =$$

$$\frac{k_{driver}}{2} [V_{GS} - V_{TH}]^2$$

$$\Rightarrow \frac{25 \mu A}{k} \times \frac{1}{2} \left[2 |V_{TH, load}| (5 - 6V_{IL} + 3.35) - (5 - 6V_{IL} + 3.35)^2 \right]$$

$$= \frac{25 \mu A}{k} \times 2 [V_{IL} - 1]^2$$

$$\therefore V_{IL} = \begin{cases} 0.98V \\ 1.36V. \end{cases}$$

V_{IL} should always be higher than V_{TH} of driver MOSFET and hence $V_{IL} = 1.36V$.

$$V_{TH} = V_{DD}$$

$$V_{OL} = V_{DD} - V_{TH} - \sqrt{(V_{DD} - V_{TH})^2 - \frac{k_{load}}{k_{driver}} |V_{TH, load}|^2}$$

$$\text{ideally } V_{OL} = V_{DD} = \checkmark$$

$V_{OL} = 0 = \text{as low as possible}$

$$V_{OL} = V_{DD} - V_{TH} - \sqrt{(V_{DD} - V_{TH})^2 - \frac{k_{load}}{k_{driver}} |V_{TH, load}|^2}$$

fixed \rightarrow *This should be as max. as possible*

$\therefore \frac{k_{load}}{k_{driver}} \uparrow \uparrow \uparrow \text{ should be high as possible}$

Most important parameter.
(Known as k_R)

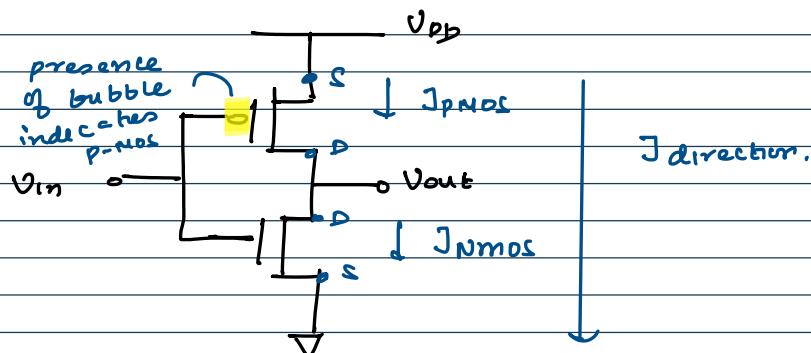
$$\cdot k_R \cdot \frac{k_{load}}{k_{driver}} = \frac{m_{max}(V_{IL})}{V_{IL}}$$

$$K_R = \frac{k_{load}}{k_{driver}} = \frac{W_{load} C_{ox} (\omega_L)_{load}}{W_{driver} C_{ox} (\omega_L)_{driver}}$$

$$\Rightarrow K_R = \frac{(\omega_L)_{load}}{(\omega_L)_{driver}}$$

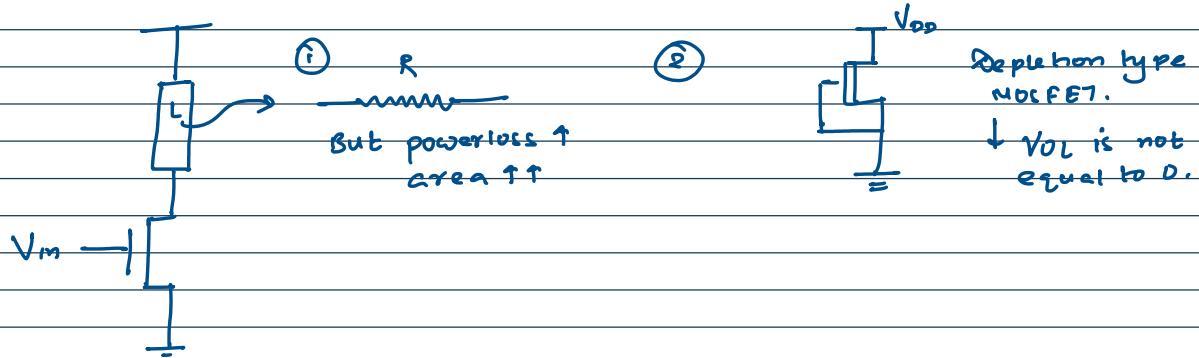
CMOS Inverter

Complementary metal oxide semiconductor.



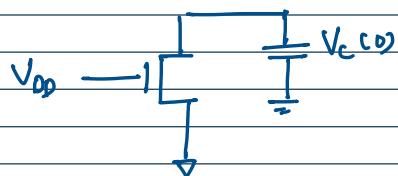
Operations :

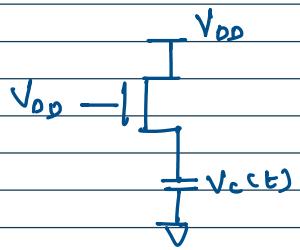
V_{in}	p-MOS	n-MOS	Output
0	on (short)	off (open)	V_{DD}
1	off (open)	on (short)	0



V_{DD} turns off the mosfet by forming inversion layer and hence capacitor starts discharging to 0.

\Rightarrow Strong logic 0.





$$V_{gs} = V_g - V_s = V_{dd} - V_c(t)$$

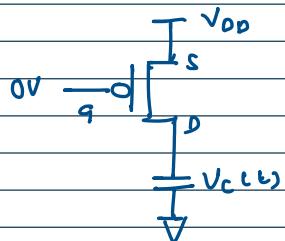
Initially $V_c(0) = 0$ and hence $V_{gs} = V_{dd}$
 which will be more than V_{thn} and
 current starts flowing from drain
 to source which will charge the
 capacitor.

Thus $V_c(t) \uparrow \uparrow \therefore V_{dd} - V_c(t) \downarrow \downarrow$ and
 $t = t_0$ a point

$$V_{gs} = V_{dd} - V_c(t) < V_{thn}$$

(MOSFET will be turned off)
 Weak logic 1

P-MOS



$$V_{gs} = V_g - V_s = 0 - V_{dd} = -V_{dd}$$

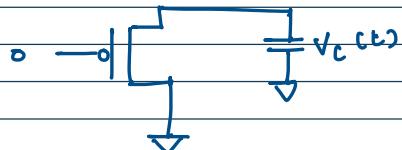
$$\therefore (V_{gs} < V_{thn})$$

Thus transistor will always remain
 open as $V_{gs} < V_{thn}$

Hence current starts flowing from
 source to drain and hence $V_c(t)$
 starts charging to V_{dd}

Strong logic 1

$$V_{gs} = V_g - V_s = -V_c(t)$$



Let initially $V_c(0) = V_{dd}$

$$\therefore V_{gs} = -V_{dd} < V_{thn}$$

and hence p-mos on and
 capacitor starts discharging.

$V_c(t)$ value starts decreasing
 from V_{dd} and at a point

$V_c(t) > V_{thn}$ and hence
 MOSFET will be off.

Weak logic 0

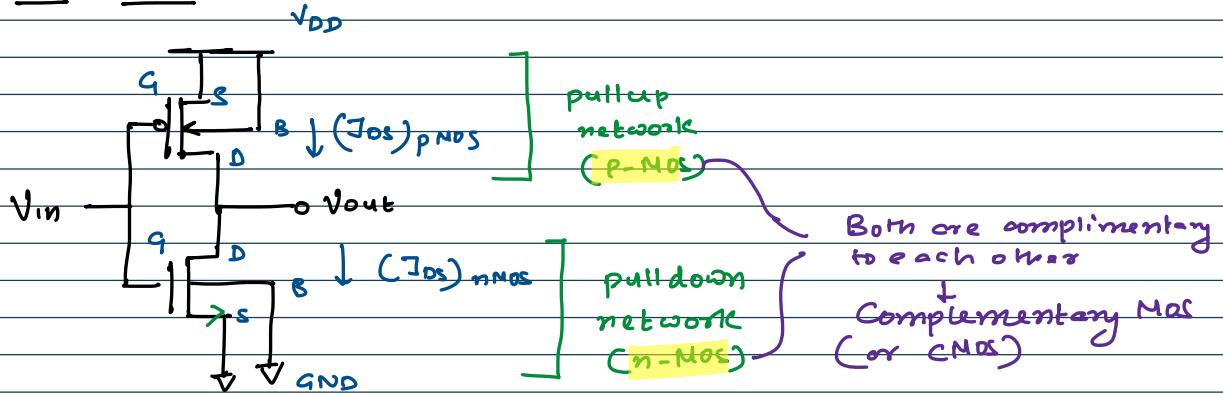
Observation

i) n-MOS pulled down o/p voltage to 0. \rightarrow pull-down / pdN device

ii) p-MOS pulled up o/p voltage to 1 \rightarrow pull-up / puN device

CNOS inverter

CMOS inverter

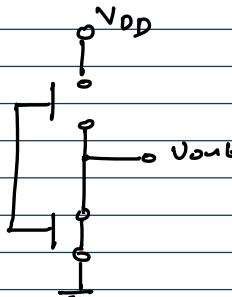


when $V_{in} = \text{logic 1}$ (i.e., $V_{in} = V_{DD}$)

$$\therefore (V_{gs})_n = (V_g)_n - (V_s)_n = V_{DD} > (V_{in})_n \quad (\text{functional})$$

$$(V_{gs})_p = (V_g)_p - (V_s)_p = V_{DD} - V_{DD} = 0 > (V_{in})_p \\ (\text{hence in cut off})$$

\therefore Equ. Circuit



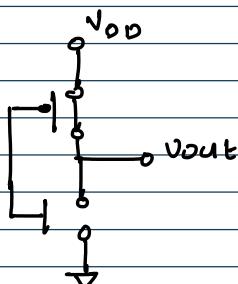
$\therefore V_{out} = 0$
when $V_{in} = \text{high}$

By when $V_{in} = \text{logic 0}$ (0V)

$$\therefore (V_{gs})_n = (V_g - V_s)_n = 0 - 0 = 0V \quad \begin{matrix} \text{cutoff} \\ \text{clearly } 0 < (V_{in})_n \end{matrix}$$

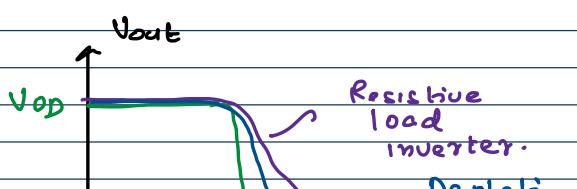
$$(V_{gs})_p = (V_g)_p - (V_s)_p = 0 - V_{DD} = -V_{DD} < (V_{in})_p \\ \text{L short circuit}$$

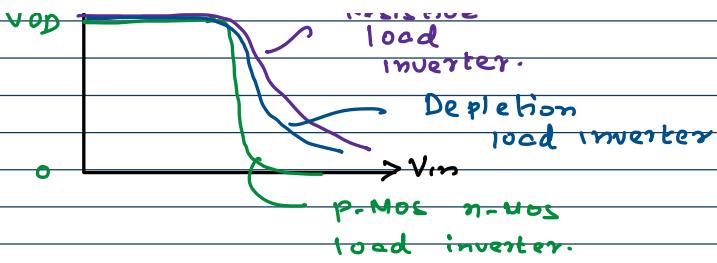
\therefore Equ. Circuit



$\therefore V_{out} = V_{DD}$
when $V_{in} = 0V$

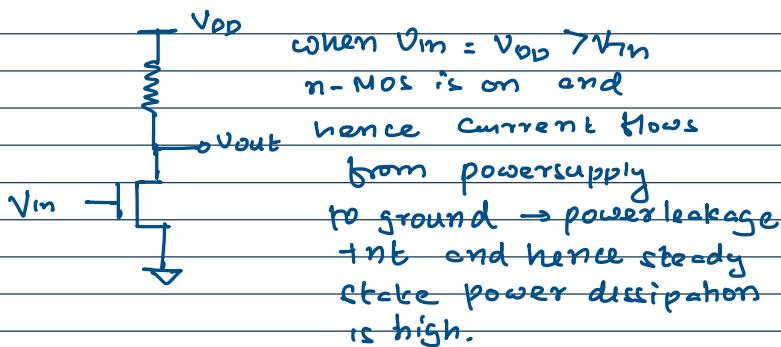
Thus in CMOS inverter what is happening is V_{out} switches from 0V to V_{DD} i.e. full power supply.





→ Steady state power dissipation in case of C-MOS is 0.

power leakage
when circuit is
complete



However in CMOS
inverter there is
no connection b/w
 V_{DD} to ground

↓
power dissipation
steady state is
0.

- $(V_{gs})_n = (V_g)_n - (V_s)_n = V_{in}$
- $(V_{gs})_p = (V_g)_p - (V_s)_p = V_{in} - V_{DD}$
- $(V_{os})_n = (V_o)_n - (V_s)_n = V_{out}$
- $(V_{os})_p = (V_o)_p - (V_s)_p = V_{out} - V_{DD}$.

n-MOS saturation

$$(V_{os})_n \geq (V_{gs})_n - (V_{th})_n$$

or, $V_{out} \geq V_{in} - (V_{th})_n$

p-MOS saturation

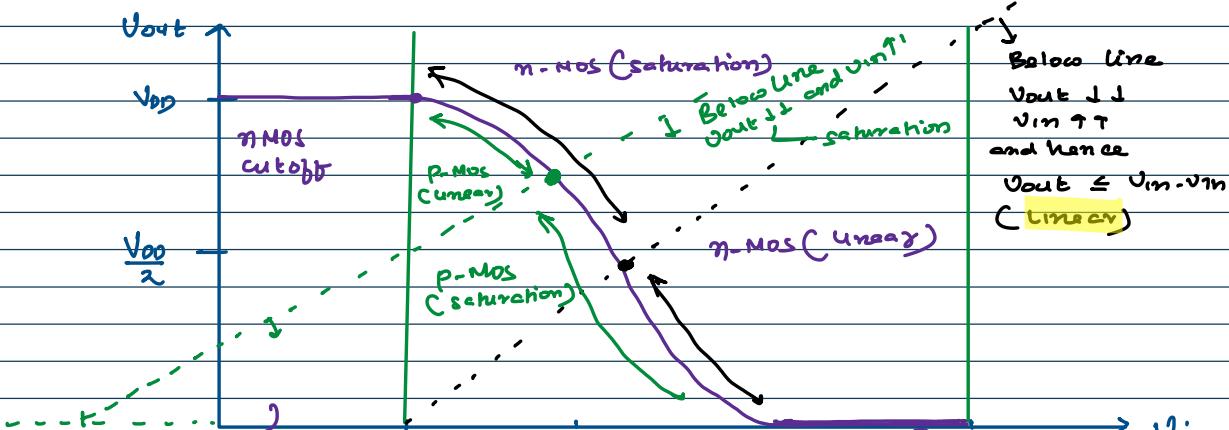
$$(V_{os})_p \leq (V_{gs})_p - (V_{th})_p$$

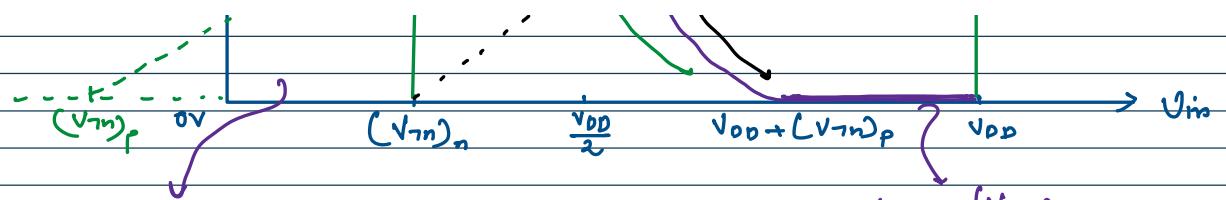
or, $V_{out} - V_{DD} \leq V_{in} - V_{DD} - (V_{th})_p$

or, $V_{out} \leq V_{in} - (V_{th})_p$

• CMOS inverter V_{TC}

above line
 $V_{out} \uparrow \uparrow \therefore V_{out} \rightarrow V_{in}, V_{in}$
 $V_{in} \downarrow \downarrow$ and hence saturation.





$$\text{m-MOS} \quad V_{GS} = V_{IN} = 0 \quad V_{DS} = V_{OUT} = V_{DD}$$

$V_{GS} < (V_{tn})_n$
Cutoff

P-MOS $V_{GS} = V_{IN} - V_{DD} = -V_{DD}$
 $-V_{DD} < (V_{tn})_p$ and
hence not in cutoff.

$V_{OUT} = V_{DD} \geq V_{IN} - (V_{tn})_p$
and hence (Linear region) (Clearly born $\propto mV + c$
with $(V_{tn})_p$ being -ve)

$$\text{for n-MOS Saturation} \quad (V_{DS})_n \geq (V_{DD} - V_{IN})_n$$

$$\text{or, } V_{OUT} \geq V_{IN} - (V_{tn})_n$$

$$\text{let } V_{OUT} = V_{IN} - (V_{tn})_n \quad \text{n-MOS} \quad V_{IN} = V_{DD} \times (V_{tn})_n \\ \text{Cub born } y = mx + c \\ \text{with } m = 1$$

$$V_{DD} + (V_{tn})_p = V_{DD} \quad \text{as } (V_{tn})_p \text{ is -ve}$$

$$\downarrow \quad \text{at } V_{IN} = V_{DD}, V_{OUT} = 0$$

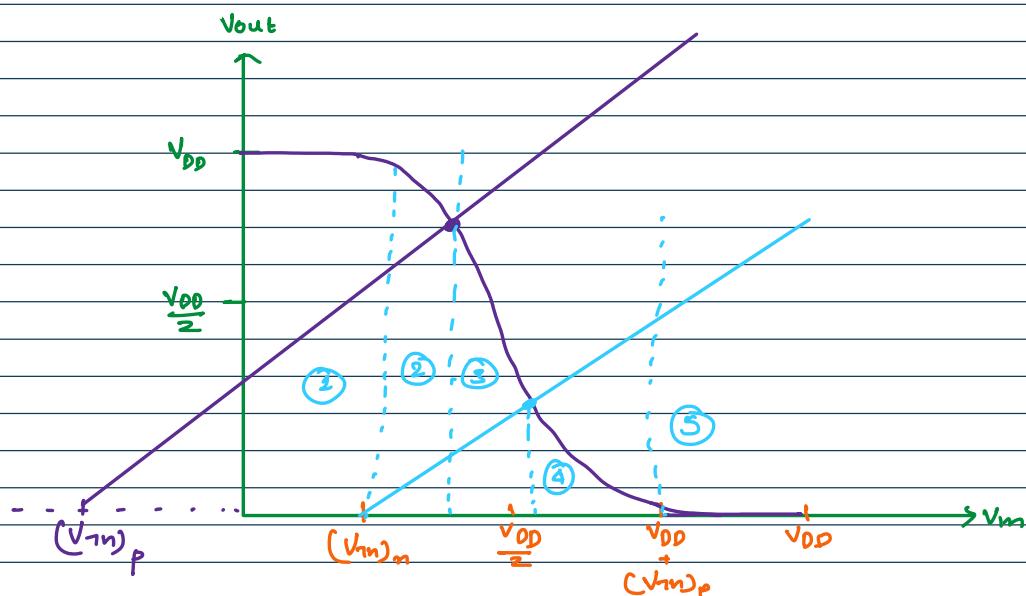
$$\therefore 0 \leq V_{DD} - (V_{tn})_n \quad \text{(Linear region)}$$

for p-MOS saturation we have

$$V_{OUT} \leq V_{IN} - (V_{tn})_p$$

$$\text{P-MOS } (V_{GS}) = V_{IN} - V_{DD} = 0$$

$$V_{GS} \geq (V_{tn})_p \quad (\text{Hence cutoff})$$

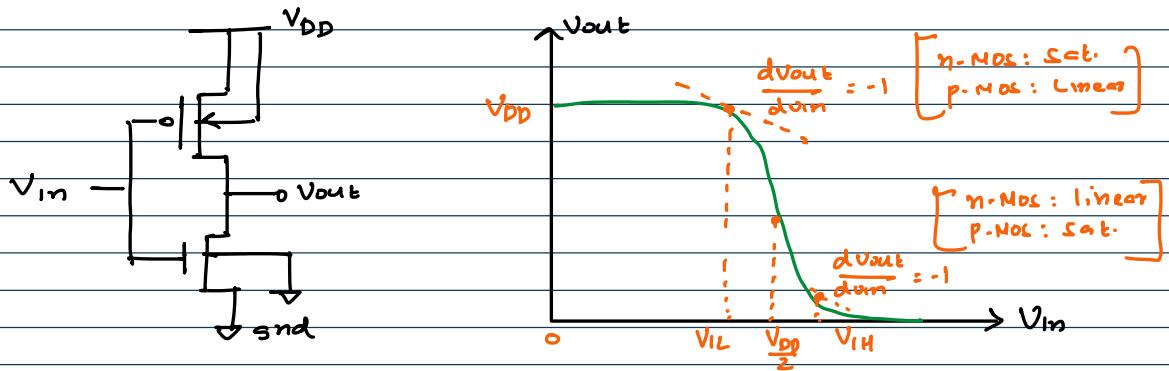


Region	n-MOS	p-MOS
1	Cutoff	Linear
2	Saturation	Linear
3.	Saturation	Saturation
4.	Linear	Saturation
5.	Linear	Cutoff

CMOS parameters $(V_{L}, V_{H}, V_{OL}, V_{OH}) \approx$



$$\frac{dV_{OUT}}{dV_{IN}} = -1 \quad \begin{cases} \text{n-MOS: Sat.} \\ \text{p-MOS: Linear} \end{cases}$$



$$V_{IL} = ? \quad (\underline{I_D})_{n\text{-MOS}} = (\underline{I_D})_{p\text{-MOS}}$$

$$\text{or, } \frac{k_n}{2} \left[(V_{SS})_n - (V_{IN})_n \right]^2 = \frac{k_p}{2} \left[2 \left((V_{SS})_p - (V_{IN})_p \right) (V_{DS})_p - (V_{DS})_p^2 \right]$$

$$(V_{SS})_n = V_{in} = V_{IL} \quad (V_{SS})_p = V_{in} - V_{DD} = V_{IL} - V_{DD}$$

$$(V_{DS})_p = V_D - V_S = V_{out} - V_{DD}$$

$$\therefore \frac{k_n}{2} \left[V_{IL} - (V_{IN})_n \right]^2 = \frac{k_p}{2} \left[2 \left(V_{IL} - V_{DD} - (V_{IN})_p \right) (V_{out} - V_{DD}) - (V_{out} - V_{DD})^2 \right]$$

at point V_{IL} we have $\frac{dV_{out}}{dV_{in}} = -1$, hence differentiating
above eqn. w.r.t to V_{in}

$$\therefore \frac{k_n}{2} \cancel{x} \left[V_{IL} - (V_{IN})_n \right] = \frac{k_p}{2} \left[\cancel{x} \left(V_{IL} - (V_{IN})_p - V_{DD} \right) \frac{dV_{out}}{dV_{in}} + \cancel{x} (V_{out} - V_{DD}) - \cancel{x} (V_{out} - V_{DD}) \frac{dV_{out}}{dV_{in}} \right]$$

$$\Rightarrow k_n \left(V_{IL} - (V_{IN})_n \right) = k_p \left[- \left(V_{IL} - (V_{IN})_p - V_{DD} \right) + (V_{out} - V_{DD}) + (V_{out} - V_{DD}) \right]$$

$$\Rightarrow V_{IL} = \frac{2V_{out} + (V_{IN})_p - V_{DD} + k_R (V_{IN})_n}{1 + k_R}$$

$$\text{where } k_R = \frac{k_n}{k_p}$$

$$V_{IH} = ?? \Rightarrow \frac{dV_{out}}{dV_{in}} = -1$$

\hookrightarrow n-MOS: linear
p-MOS: saturation

$$\therefore (\underline{I_D})_n = (\underline{I_D})_p$$

$$\text{or, } \frac{k_n}{2} \left[2 \left((V_{SS})_n - (V_{IN})_n \right) (V_{DS})_n - (V_{DS})_n^2 \right] = \frac{k_p}{2} \left[(V_{SS})_p - (V_{IN})_p \right]^2$$

$$\text{or, } \frac{k_n}{2} \left[2((V_{SS})_n - (V_{IN})_n)(V_{DS})_n - (W_{DS})_n^2 \right] = \frac{k_p}{2} \left[(V_{SS})_p - (V_{IN})_p \right]$$

$$\text{or, } \frac{k_n}{2} \left[2(V_{IH} - (V_{IN})_n) V_{out} - V_{out}^2 \right] = \frac{k_p}{2} \left[V_{IL} - V_{DD} - (V_{IN})_p \right]^2$$

Differentiating w.r.t to V_{in} we have

$$\frac{k_n}{2} \left[2(V_{IH} - (V_{IN})_n) \frac{dV_{out}}{dV_{in}} + V_{out} - V_{out} \frac{dV_{out}}{dV_{in}} \right]$$

$$= \frac{k_p}{2} \left[2(V_{IL} - V_{DD} - (V_{IN})_p) \right]$$

$$\text{on } k_n \left(-(V_{IH} - (V_{IN})_n) \rightarrow V_{out} - V_{out} \right) = k_p \left(V_{IL} - V_{DD} - (V_{IN})_p \right)$$

$$\therefore V_{IH} = \frac{V_{DD} + (V_{IN})_p + k_R (2V_{out} + (V_{IN})_n)}{1 + k_R}$$

where $k_R = k_n/k_p$

- o $V_{OH} = V_{DD}V$
- o $V_{OL} = 0V$

$V_{IN} = ??$ Both nMOS and pMOS in transition.

Transition point where $V_{IN} = V_{out}$

$$\frac{k_n}{2} \left[(V_{GS})_n - (V_{IN})_n \right]^2 = \frac{k_p}{2} \left[(V_{SS})_p - (V_{IN})_p \right]^2$$

$$\Rightarrow k_n \left[V_{in} - (V_{IN})_n \right]^2 = k_p \left[V_{in} - V_{DD} - (V_{IN})_p \right]^2$$

at $V_m = V_{in} = V_{out} = V_m$.

$$\therefore k_n \left[V_m - (V_{IN})_n \right]^2 = k_p \left[V_m - V_{DD} - (V_{IN})_p \right]^2$$

on

$$V_m = \frac{(V_{IN})_n + \sqrt{\frac{1}{k_R}} (V_{DD} + (V_{IN})_p)}{\left(1 + \sqrt{\frac{1}{k_R}} \right)}$$

$\therefore k_R = k_n/k_p$

transconductance ratio.

- o L Ideal inverter $V_m = V_{DD}/2$

ratio.

o for ideal inverter $V_{in} = V_{DD}/2$

$$\therefore \sqrt{\frac{1}{K_R}} = \frac{V_{in} - (V_{in})_n}{V_{DD} + (V_{in})_p - V_{in}}$$

$$\text{or, } K_R = \left[\frac{V_{DD} + (V_{in})_p - V_{in}}{V_{in} - (V_{in})_n} \right]^2$$

or, ideally $V_{in} = V_{DD}/2$

$$\therefore K_R = \left[\frac{V_{DD} + (V_{in})_p - 0.5V_{DD}}{0.5V_{DD} - (V_{in})_n} \right]^2$$

$$\text{on } K_R = \left[\frac{0.5V_{DD} + (V_{in})_p}{0.5V_{DD} - (V_{in})_n} \right]^2$$

p-MOS and n-MOS are symmetrical to each other

$$\text{if } |(V_{in})_n| = |(V_{in})_p|$$

$$\therefore K_R = \left[\frac{0.5V_{DD} - (V_{in})_p}{0.5V_{DD} - (V_{in})_n} \right]^2 \because (V_{in})_p \text{ will be negative only}$$

$$\text{on } K_R = 1$$

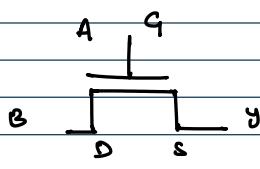
$$K_R = \frac{k_n}{k_p} = \frac{\mu_n C_{ox} (\omega_L)_n}{\mu_p C_{ox} (\omega_L)_p}$$

$$\text{or, } K_R = \frac{\mu_n}{\mu_p} \frac{(\omega_L)_n}{(\omega_L)_p} = 1$$

$$\text{or, } \frac{(\omega_L)_n}{(\omega_L)_p} = \frac{\mu_p}{\mu_n} \Rightarrow \frac{230 \text{ cm}^2/\text{V.s}}{580 \text{ cm}^2/\text{V.s}} = \frac{1}{2.5}$$

$$\therefore (\omega_L)_P = 2.5 (\omega_L)_N$$

Pass Transistor logic : Transistor that passes logic signal (I/O)



• $A = 1$ (V_{DD}) \rightarrow nMOS on (drain connected to ground)

• if $B = 1$ then $y = 1$

• if $A = 0$ or $B = 0$ $\rightarrow y = 0$

(open circuit) (no potential diff.)

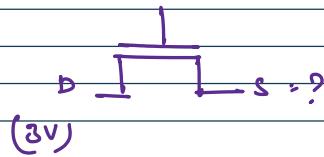
A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

$(V_{DD}) \quad (V_{DD}) \quad (V_{DD}) \approx V_{DD}$

$G = 3V$

AND gate

$$Y = A \cdot B$$



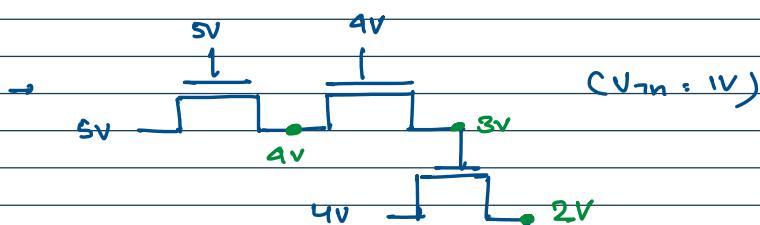
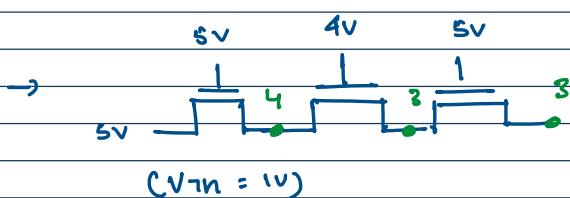
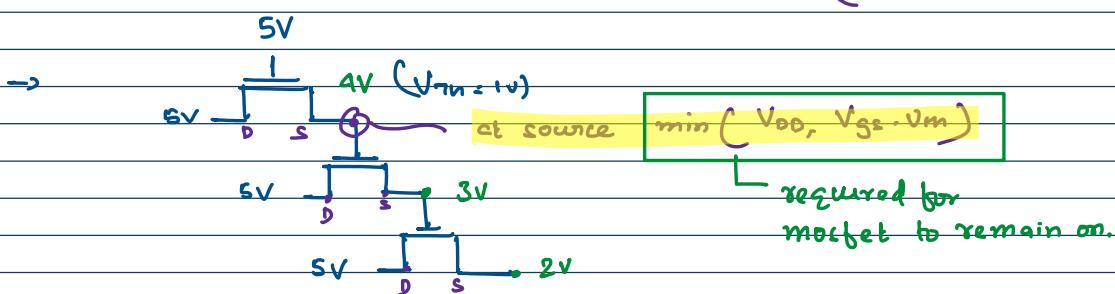
$$V_{GS} > V_{TH} \quad (\text{let } V_{TH} = 1V)$$

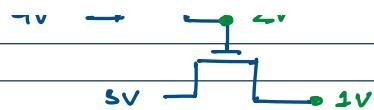
$$\therefore V_G - V_S > V_{TH}$$

$$\text{or, } 3 - V_S > 1$$

$$\text{or, } -V_S > -2$$

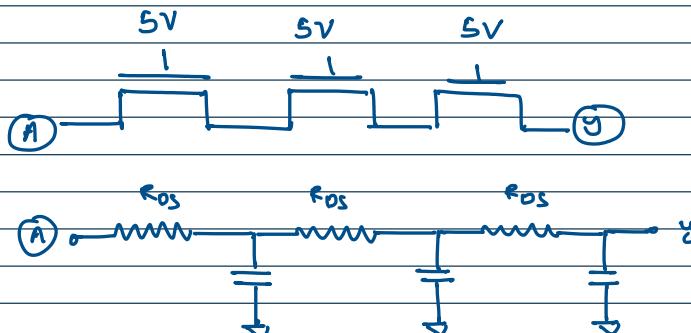
or, $V_S < 2V$ — Thus it is not getting charged upto 3V.
(weak logic 1).





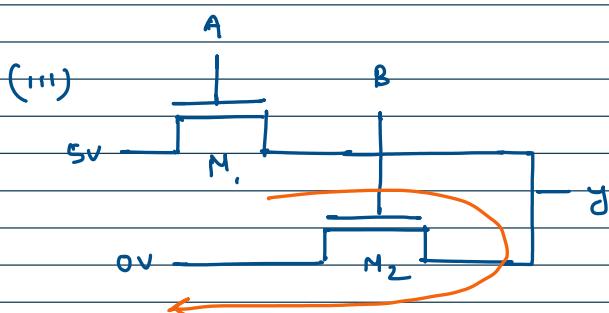
Problems :

i) $V_{GS} - V_m$ at o/p. (Threshold voltage drop)



(ii) Because R and C we have delay in the o/p.

(RC delay)

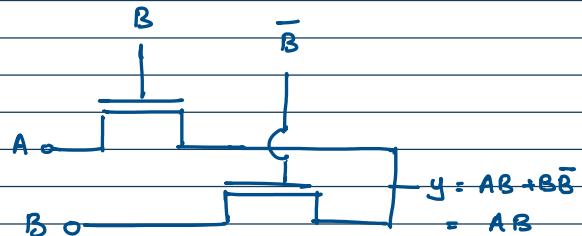


Leakage / Sneak path :

If $A = B = V_{DD}$ both M_1 and M_2 are on and as a result instead of getting connected to y it connects to $0V$.

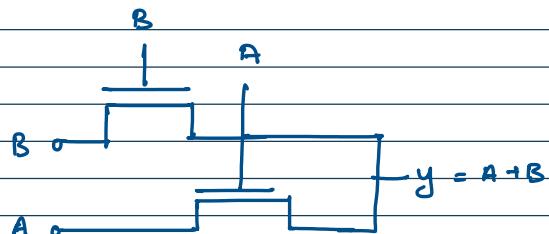
And gate (using PTL)

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1



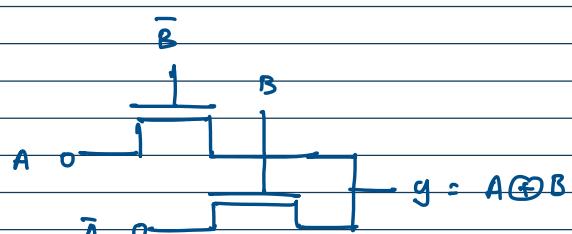
OR gate

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1



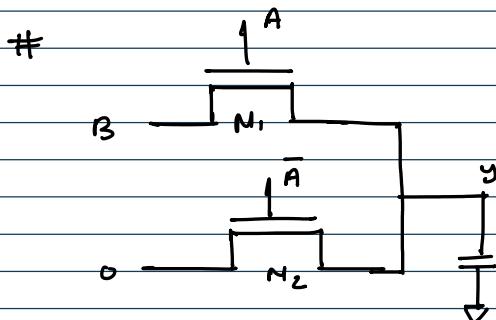
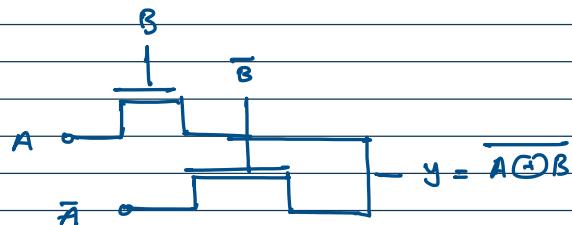
XOR gate

A	B	y
0	0	0
0	1	1

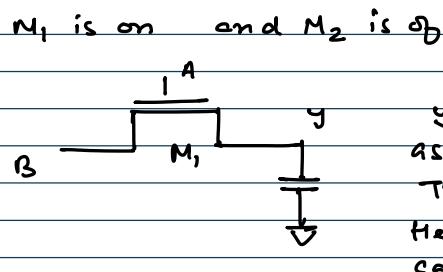


0	0	0	B
0	1	1	
1	0	1	
1	1	0	\bar{B}

XNOR gate
 $(y = AB + \bar{A}\bar{B})$

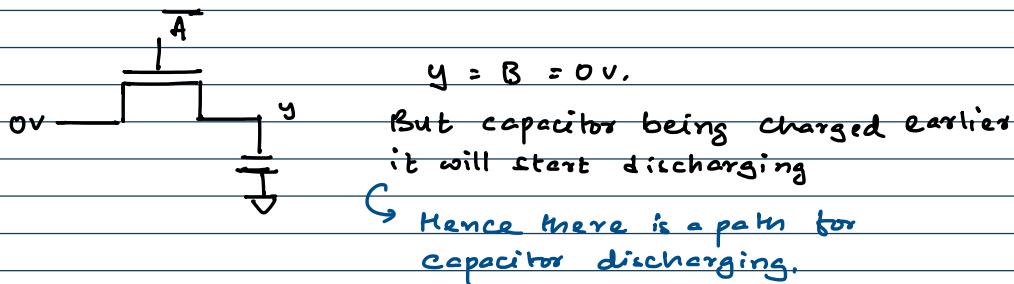


when $A=1$

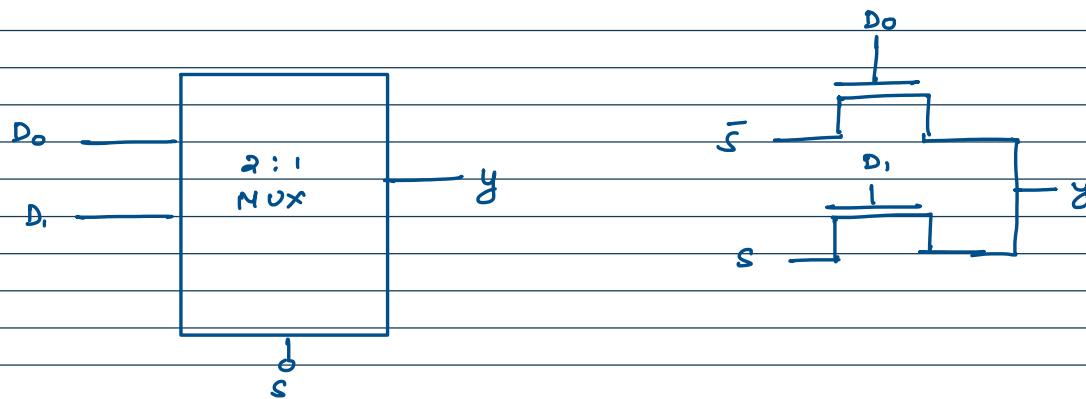


$y = B$
 assuming B to be logic 1
 Thus $y = 1$.
 Hence it charges the capacitor.

When $A=0$ N_1 is off and M_2 is on.

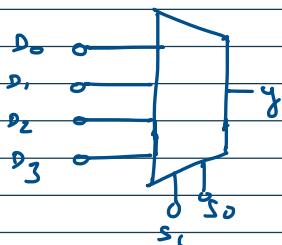


NUX using Pass Transistor logic

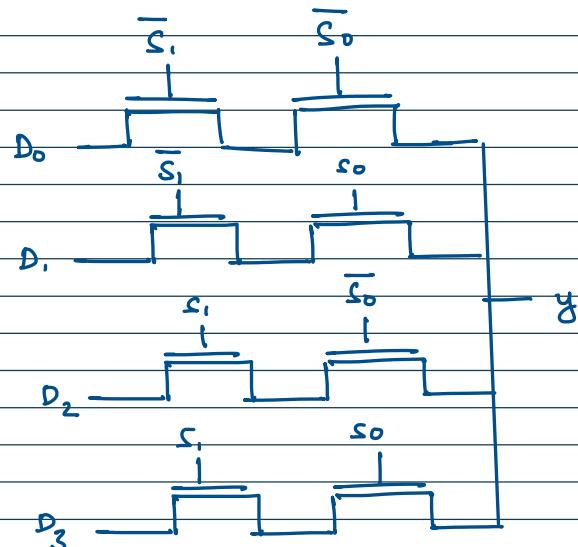


$$y = \bar{s}_1 D_0 + s_1 D_1$$

4:1 MUX



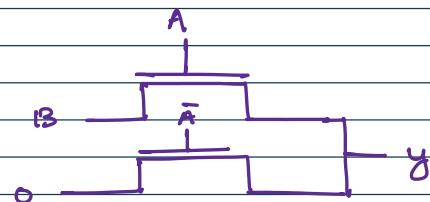
$$y = \bar{s}_1 \bar{s}_0 D_0 + \bar{s}_1 s_0 D_1 + s_1 \bar{s}_0 D_2 + s_1 s_0 D_3$$



Logic gates using PTL :

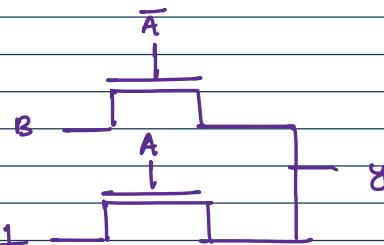
① AND gate

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1



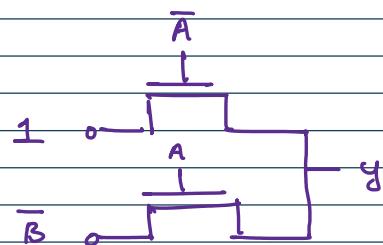
② OR gate

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1



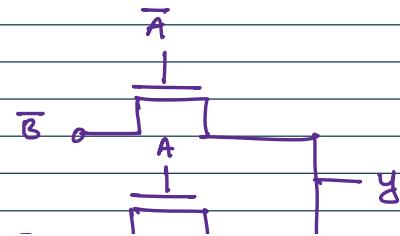
③ NAND gate

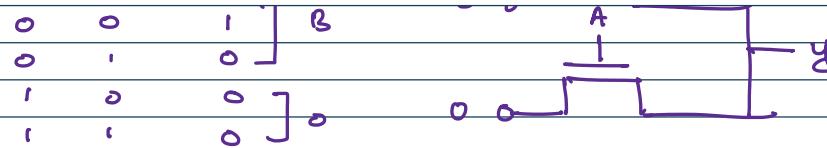
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0



④ NOR gate

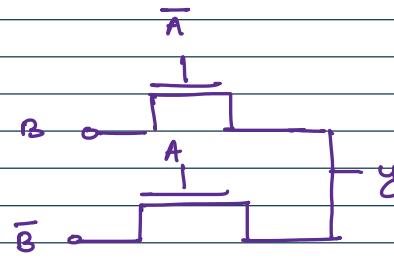
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0





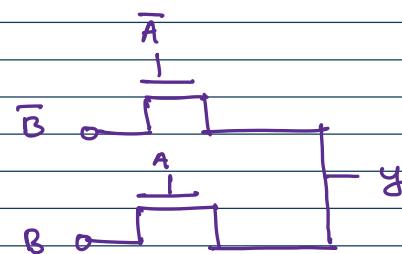
(5) XOR gate

A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

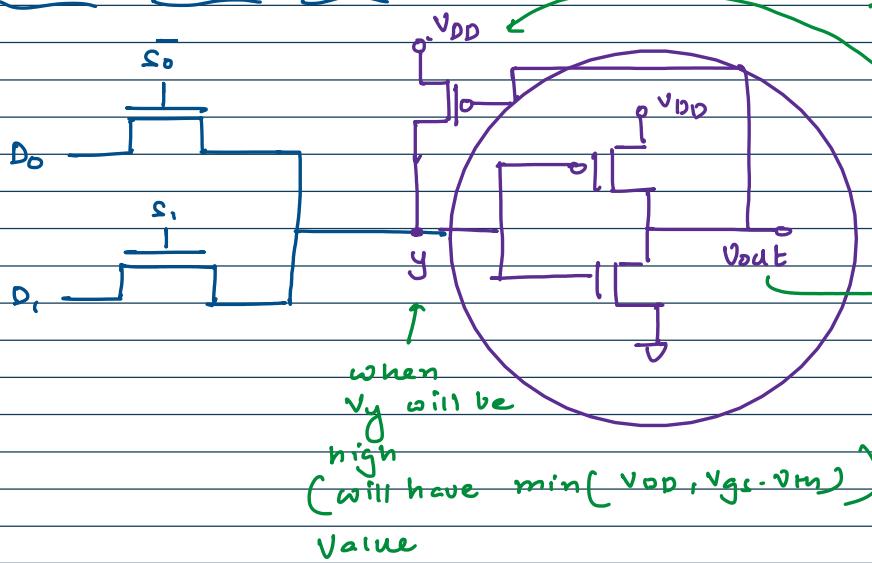


(6) X-NOR gate

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

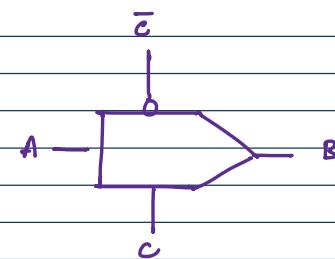
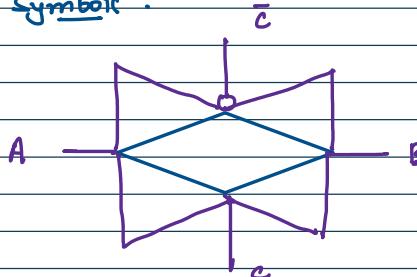


Logic level restoration



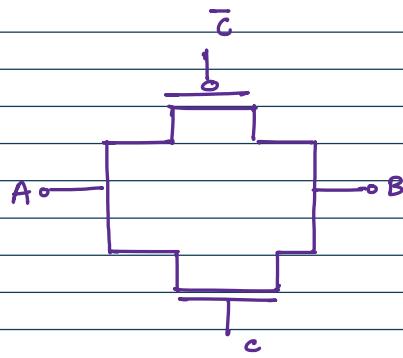
C MOS transmission gate :

Symbol :



Circuit :

Circuit :

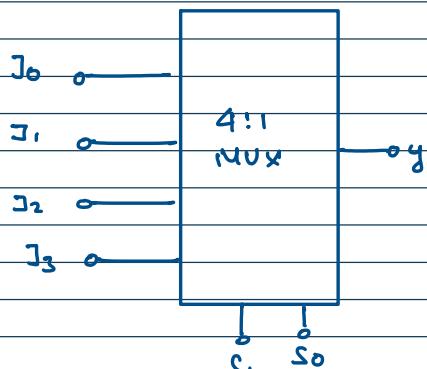


- One p-MOS and one c-MOS in parallel to each other.
- Gate is complementary to both transistors.

Working and Truth table

<u>Input</u>	<u>o/p</u>
C A	B
0 0	high impedance { o/p not connected to o/p }
0 1	high impedance
1 0	0 (will pass through \rightarrow strong logic 0)
1 1	1 (will pass through \rightarrow strong logic 1)

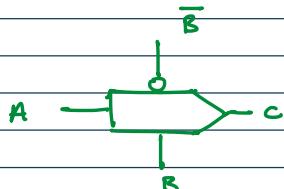
4:1 Mux using TG logic :



S ₁	S ₀	y
0	0	J ₀
0	1	J ₁
1	0	J ₂
1	1	J ₃

$$y = \bar{S}_1 \bar{S}_0 J_0 + \bar{S}_1 S_0 J_1 + S_1 \bar{S}_0 J_2 + S_1 S_0 J_3$$

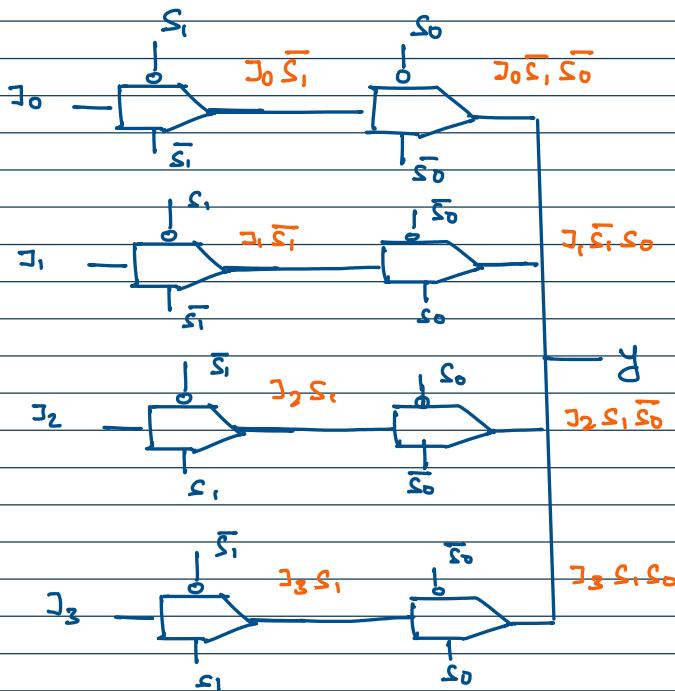
Transmission gate :



A	B	C
0	0	H1
0	1	0
1	0	H1
1	1	1

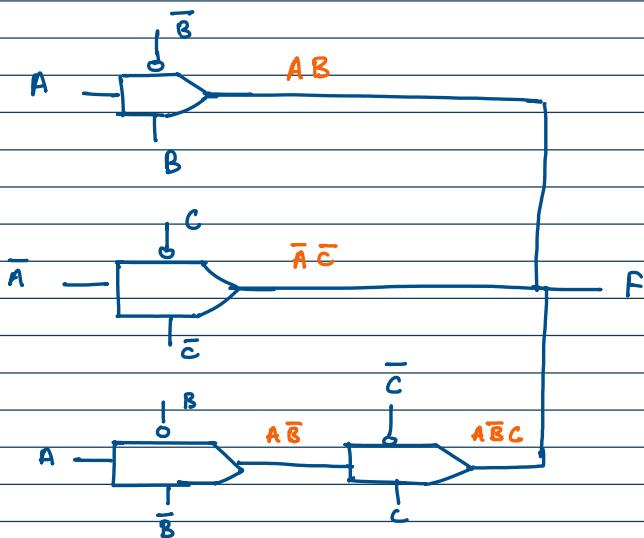
Thus it acts like a and gate.

$$4:1 \text{ Mux} : \bar{s}_1 \bar{s}_0 s_0 + \bar{s}_1 s_0 s_1 + s_1 \bar{s}_0 s_2 + s_1 s_0 s_3$$



Q Implement following function using TG logic

$$F = AB + \bar{A}\bar{C} + A\bar{B}C$$



BJT



→ speed is higher in BJT :-

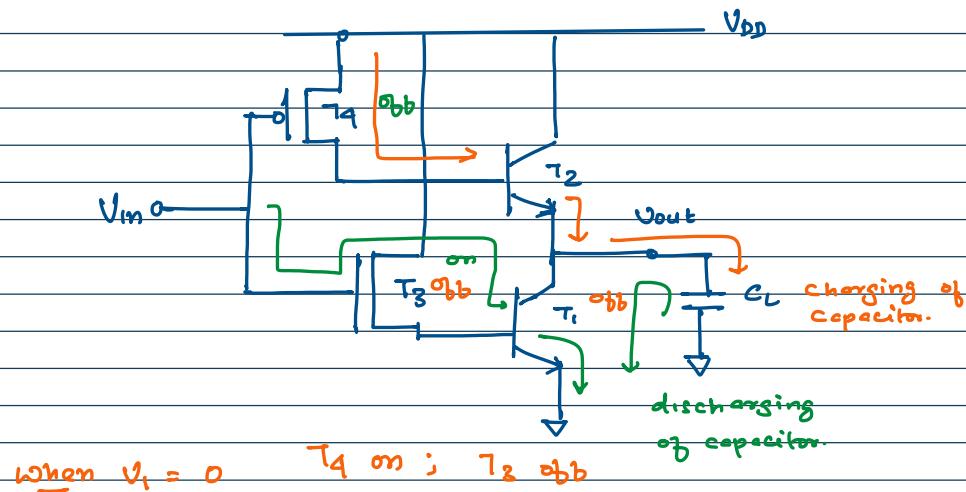
{) capacitances in MOSFET more and hence RC delay.

→ But CMOS has 0 static power dissipation

→ Scalability of MOSFET is more.

→ But CMOS has 0 static power dissipation
 → Scalability of MOSFET is more.

Combine MOSFET and BJT → BiCMOS

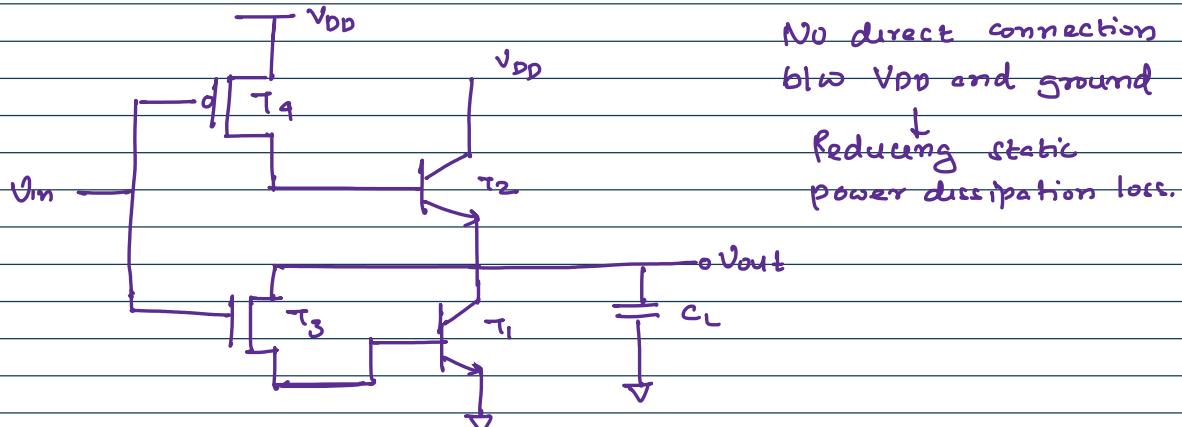


$V_i = 1 \quad T_4$ off, T_3 on

(But problem is when $V_{DD} = 1$ we can see there is a direct connection b/w V_{DD} and ground)

↳ Hence there will be static power dissipation.

↓
Modified circuit



Combinational logic implementation using CMOS

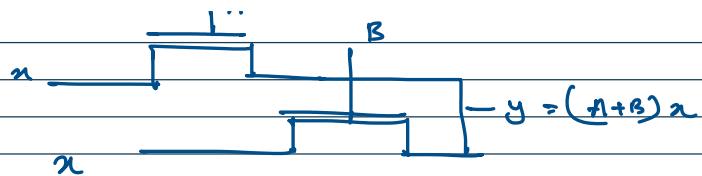
$$x \rightarrow \begin{cases} 1 & \text{if } x = 1 \\ 0 & \text{if } x = 0 \end{cases} \quad y = Ax$$

$$x \rightarrow \begin{cases} 1 & \text{if } A \\ 0 & \text{if } B \end{cases} \quad y = ABx$$

$$x \rightarrow \begin{cases} 1 & \text{if } A \\ 0 & \text{if } B \end{cases} \quad y = \bar{A}\bar{B}x$$

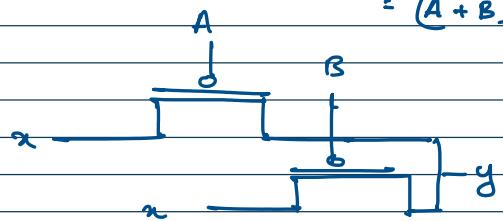
$$x \rightarrow \begin{cases} 1 & \text{if } A \\ 0 & \text{if } B \end{cases} \quad y = \bar{A}x$$

$$y = \bar{A}\bar{B}x \\ = (A+B)x$$



$$V - V_{DD} = V$$

$$= (\bar{A} + \bar{B})x$$



$$\therefore y = \bar{A}x + \bar{B}x$$

$$= (\bar{A} + \bar{B})x$$

$$= \bar{A}\bar{B}x$$

* n-MOS and p-MOS circuit complement each other.

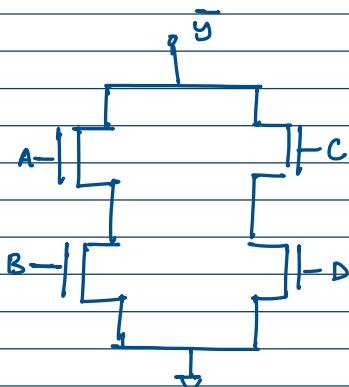
ex: n-MOS in series \rightarrow and gate
p-MOS in series \rightarrow nand gate.

* nMOS and pMOS circuits \rightarrow duality in nature.

$y = \overline{AB + CD}$

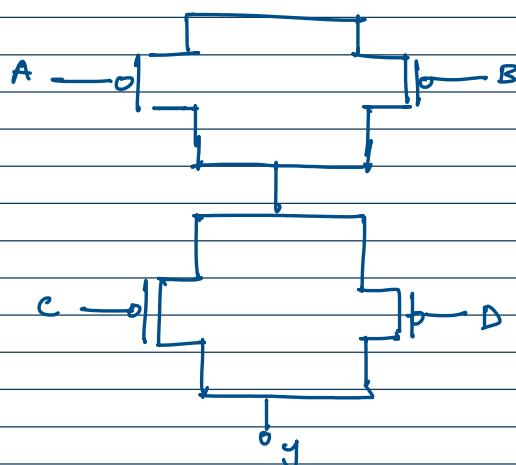
(i) nMOS can't have complement.

Thus we implement $AB + CD$.



(ii) p-MOS we can implement complement

$$y = \overline{AB + CD} = \overline{AB} \cdot \overline{CD} = (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D})$$



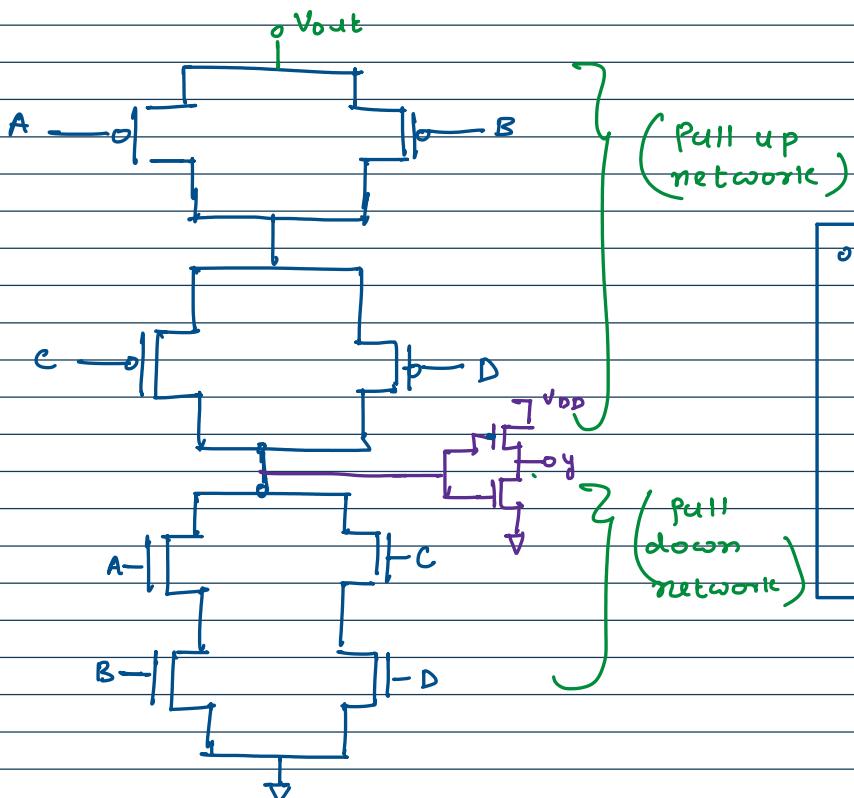
• When n-MOS network is giving high impedance state, p-MOS network connects o/p. to V_{DD}.

• Ily when p-MOS network is giving high impedance nMOS connect o/p to GND

$\therefore y = \overline{AB + CD}$ can be formed by connecting both nMOS and p-MOS network.

o V_{out}

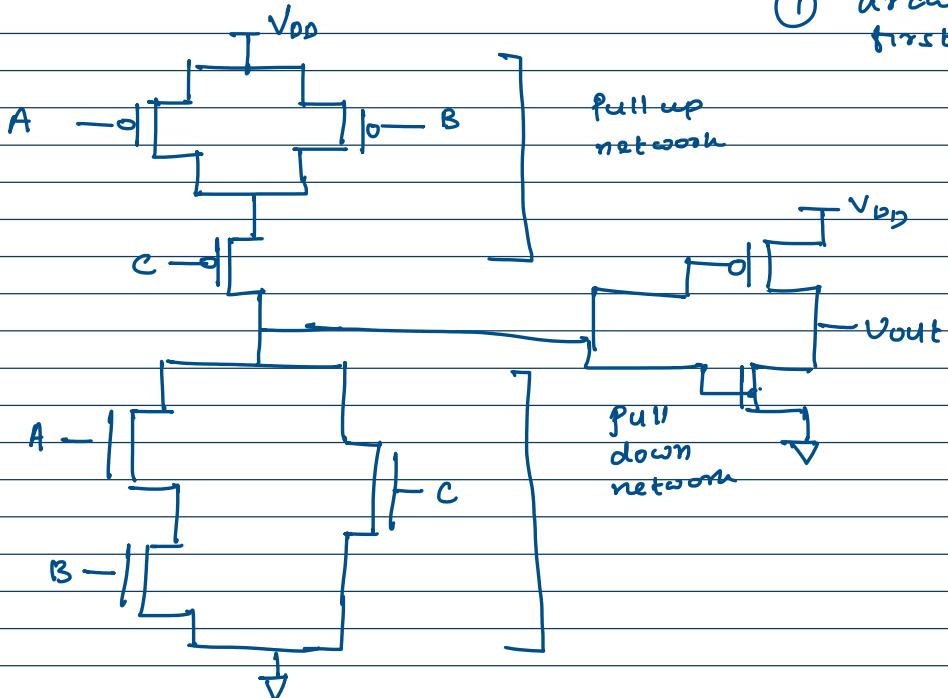
pull up network



- o CMOS circuit implements complement network
- o n-MOS series up p-MOS parallel (vice versa)

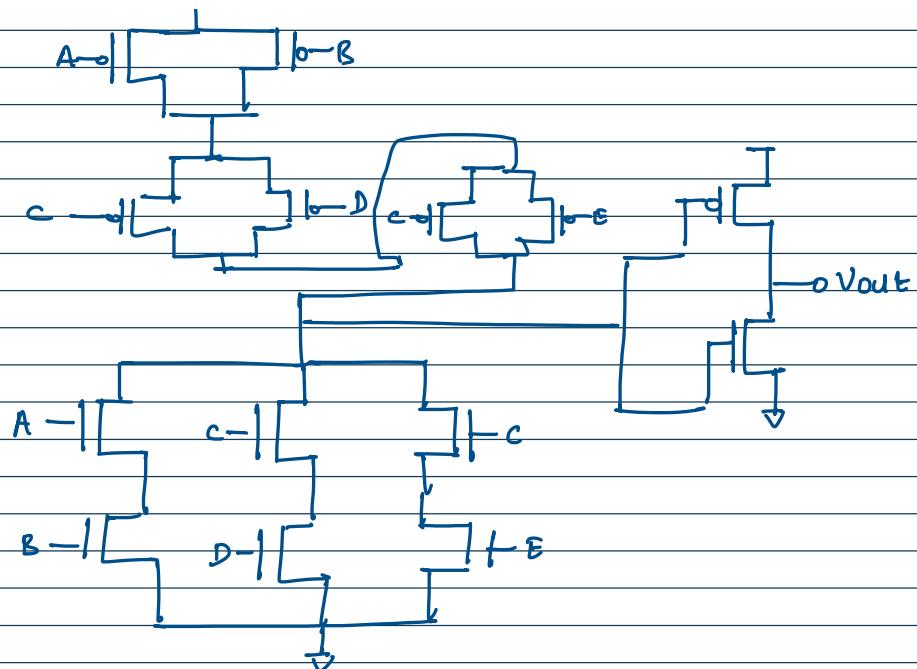
Q $y = \overline{AB + C} \rightarrow$ since it is already complement \rightarrow we can implement directly.

① draw nMOS first.



Q $y = \overline{AB + C(D+E)} = \overline{AB} + \overline{C(D+E)}$





Boolean Implementation using CMOS Transistor

i) For (\ominus) operation

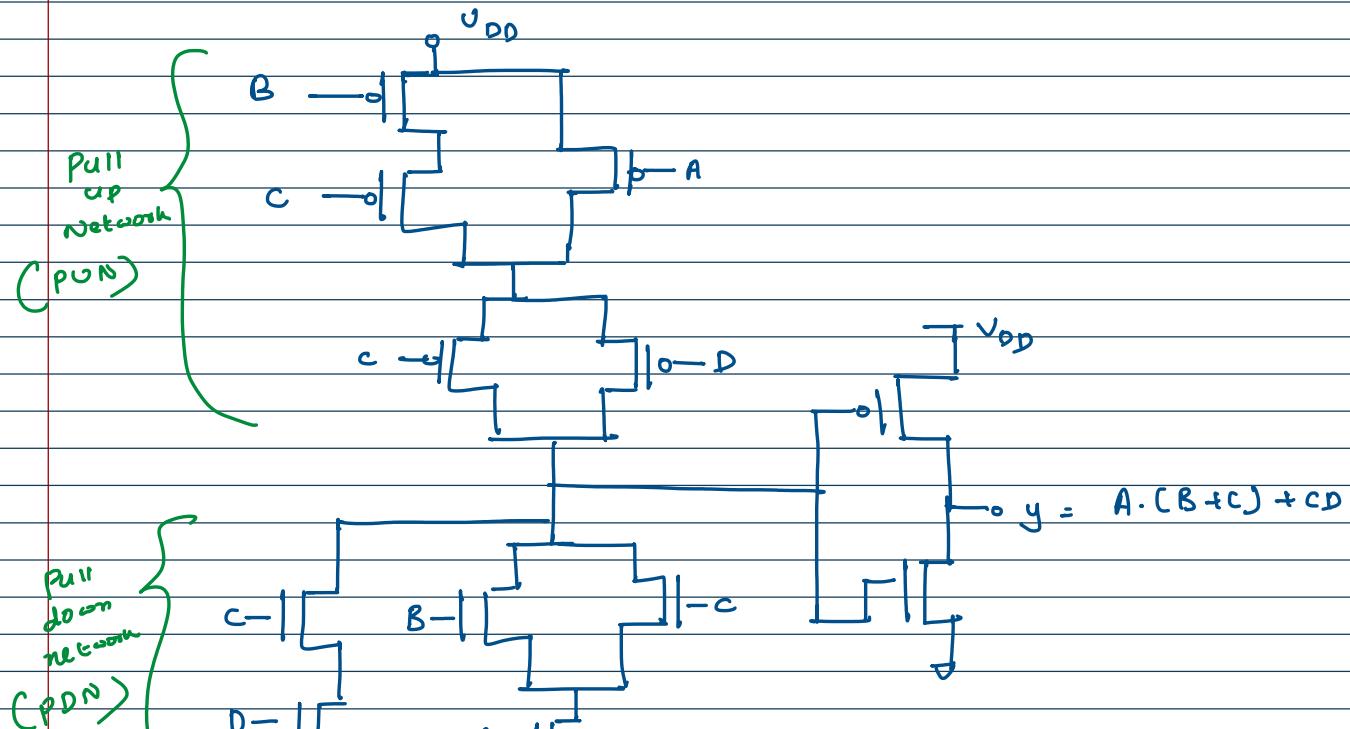
- n-MOS : Series
- p-MOS : parallel

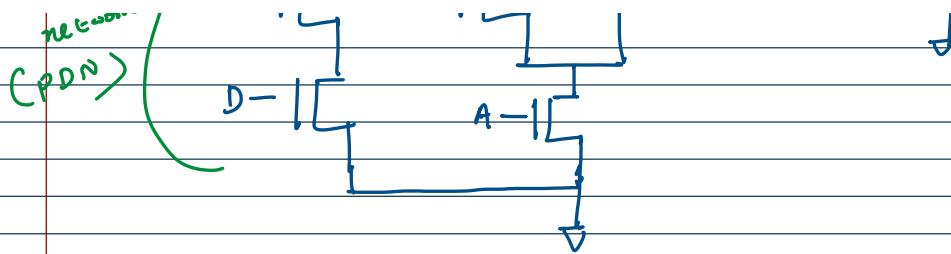
ii) At last we need to invert the given funcn.

ii) For ($+$) operation

- nMOS: parallel
- pMOS: series.

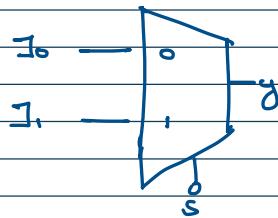
Implement $y = A \cdot (B+C) + CD$ using CMOS.



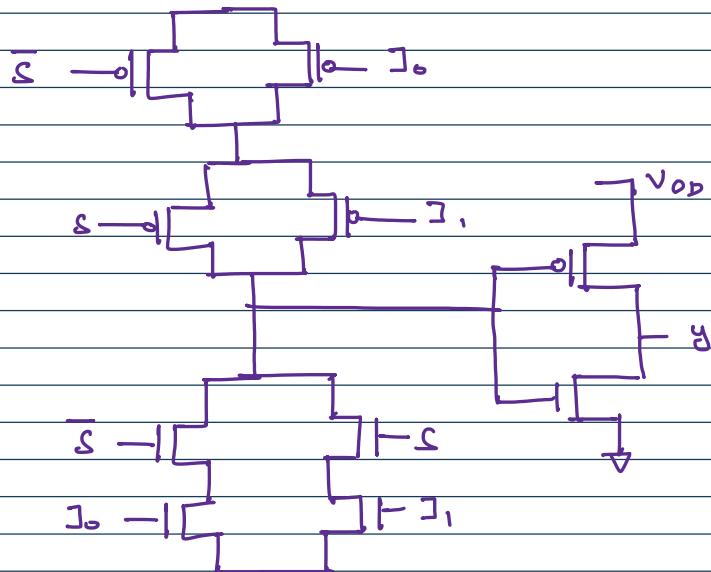


CMOS multiplexer

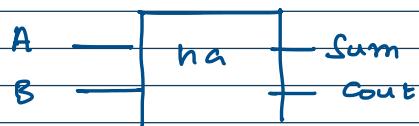
e.g: 2×1 Multiplexer



$$g = \bar{s}j_0 + s j_1$$



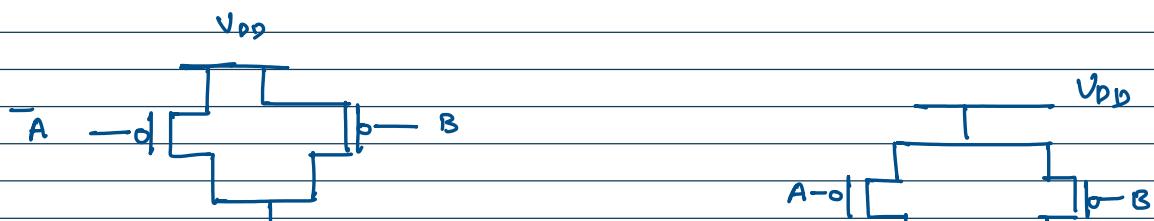
Implement half adder using CMOS logic

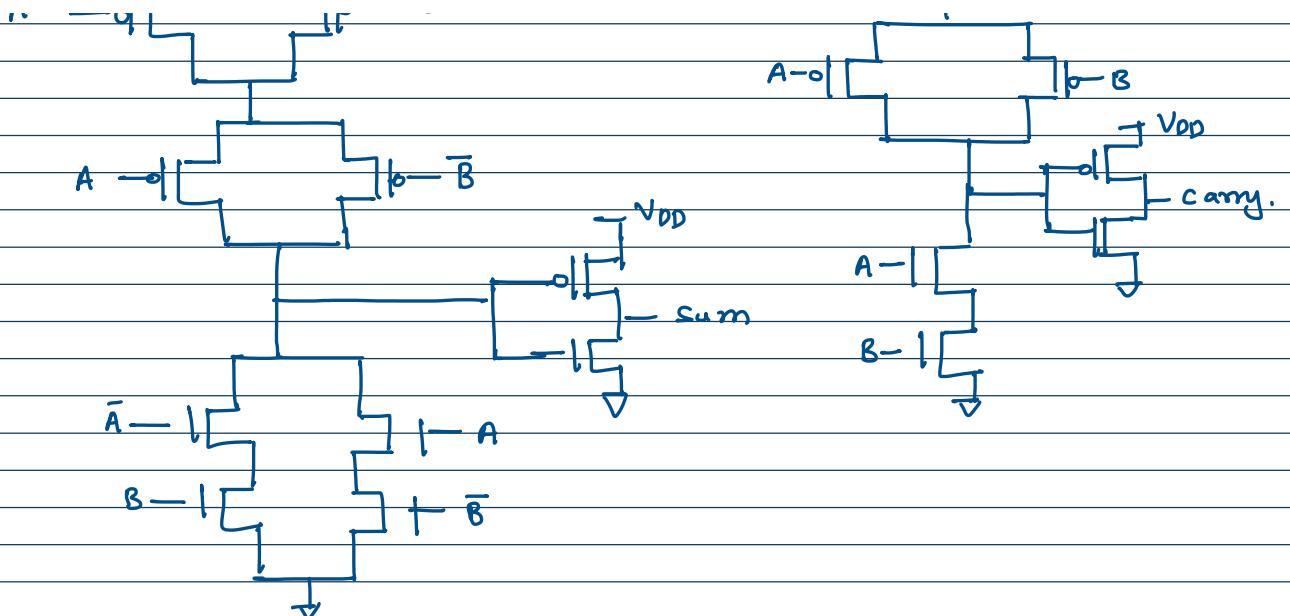


A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{Sum} = A \oplus B = \bar{A}B + A\bar{B}$$

$$\text{Carry} = AB$$

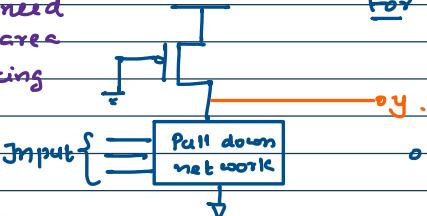




If N inputs \Rightarrow n -NOS
 \downarrow
 N n-NOS transistor
 \downarrow
 $n-p$ NOS transistor
 \downarrow
Total : $2N$ transistors

Pseudo n-NOS:

useful when need to smaller area while sacrificing small power dissipation.



Total transistor: $N+1$

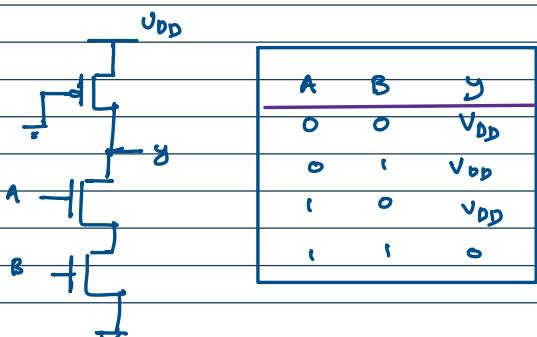
For p-NOS

$$(V_{GS})_P < (V_{TH})_P \text{ always on.}$$

- If pull down network is on output gets connected to ground.

- Elsewise output = V_{DD} .

e.g.:



As p-NOS is always on and thus when pull down network is on V_{DD} gets connected to ground.

Static power ↑↑ dissipation.

$$\circ V_{OH} = V_{DD}$$

$$\circ V_{OL} \approx 0 \text{ but not } 0 \quad (\because \text{p-NOS is always on})$$

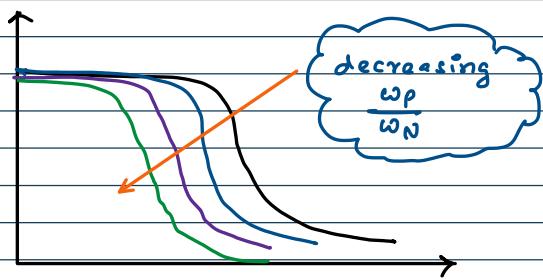
$$\left(\frac{W_P}{W_N} \downarrow \downarrow \right) \sim \frac{W_N \uparrow \uparrow}{W_P \downarrow \downarrow}$$

$$V_{OL} \approx \frac{W_P}{2W_N} \mid \frac{W_P}{2W_N} \mid \frac{V_{DD} - V_{OL}}{I_{const}}$$

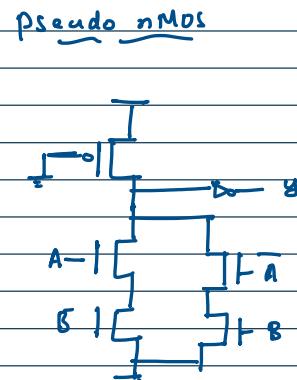
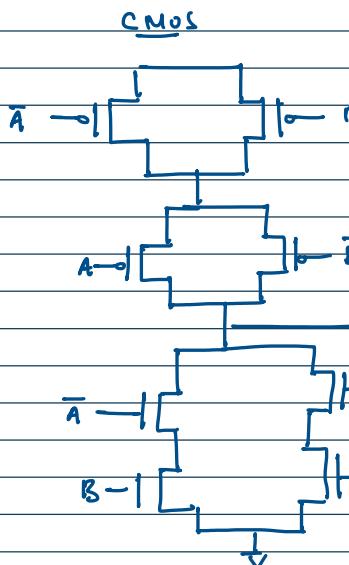
Constant

(4.8.5) $\frac{W_P}{2W_N} + \downarrow$

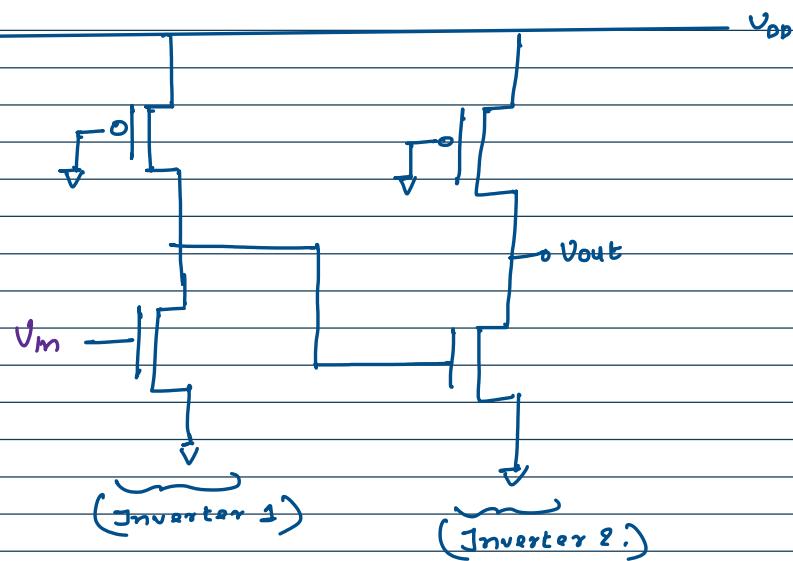
$\therefore (V_{OL} \downarrow)$ \rightarrow approaches to 0.



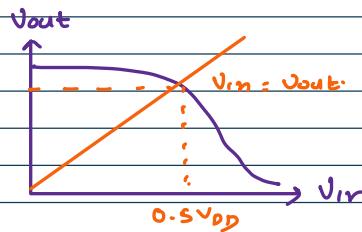
Q Design an XOR using CMOS and pseudo nMOS logic and differentiate b/w 2 implementation.



Pseudo nMOS 2



for nMOS analysis let $V_{INV} = \frac{V_{DD}}{2}$
 \downarrow
 a point where
 $V_{IN} = V_{OUT} = \underline{\underline{V_{DD}}}$



a point where
 $V_{in} = V_{out} = \frac{V_{DD}}{2}$

for NMOS

$$V_{gs} = V_g - V_s = \frac{V_{DD}}{2}$$

$$V_{ds} = \frac{V_{DD}}{2} - V_{ds}$$

$$\therefore V_{ds} > V_{gs} - V_m$$

(saturation region)

for PMOS

$$V_{gs} = V_g - V_s = -\frac{V_{DD}}{2}$$

$$V_{ds} = V_D - V_s = -\frac{V_{DD}}{2} - V_{ds}$$

$$= -1.5V_{DD}$$

$$\therefore V_{ds} < V_{gs} - V_m$$

(resistive region)

\therefore equating currents we have,

$$V_{inv} = V_m + \left(\frac{2\mu_p}{\mu_n} \right)^{1/2} \frac{\left[- (V_{DD} - V_m) (V_{ds})_p - (V_{ds})_p^2 \right]}{\left(Z_{pu}/Z_{pd} \right)^{1/2}}$$

where,

- $Z_{pu} = \left(\frac{L_{pu}}{W_{pu}} \right)$ pullup

- $Z_{pd} = \left(\frac{L_{pd}}{W_{pd}} \right)$ pulldown

for, $V_{inv} = 0.5V_{DD}$

$$(V_m)_n = (V_m)_p = 0.2V_{DD}$$

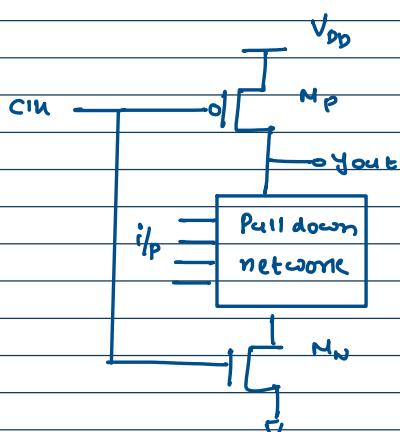
$$V_{DD} = 5V \quad \text{and} \quad \mu_n = 2.5\mu_p$$

we have

$$\left(\frac{Z_{pu}}{Z_{pd}} \right) = \frac{3}{1}$$

for a ideal inverter
 it should have a
 ratio of 3:1

Clocked CMOS



$C_{th} = 0$:
 P-MOS off
 n-nMOS off
 \therefore output gets charged to V_{DD} .

$C_{th} = 1$:
 P-MOS off.
 n-nMOS on.
 Now depends on pull down
 network whether it will be
 logic 1 or logic 0.



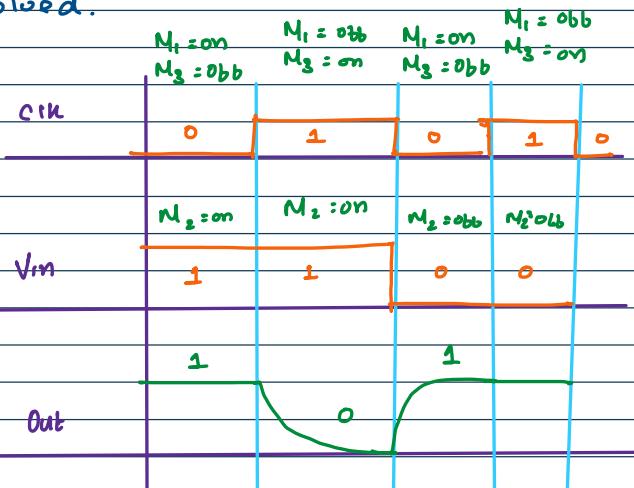
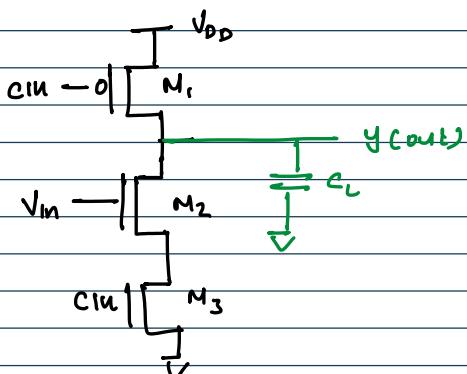
evaluation stage

Now y depends on pull down network whether it will be logic 1 or logic 0.

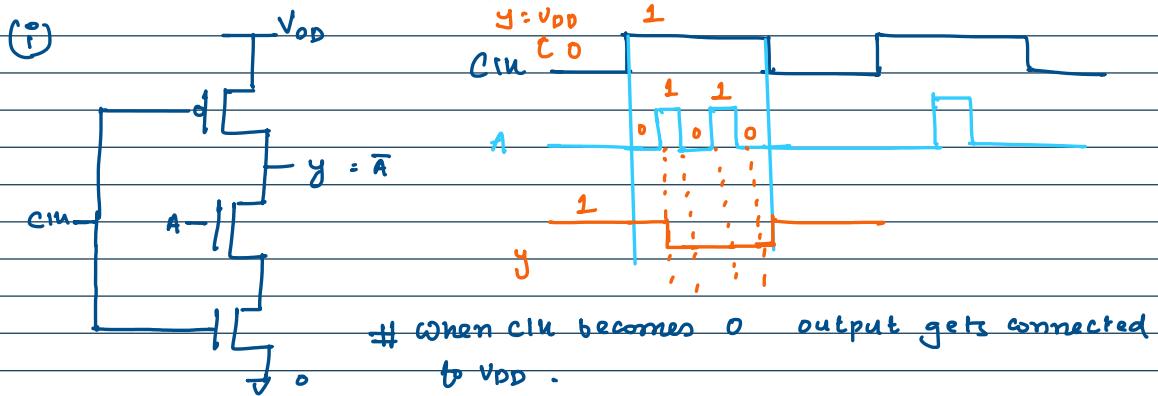
advantage :

- less number of transistors compared to CMOS

- static power dissipation issue of pseudo nMOS is solved.



Challenges :



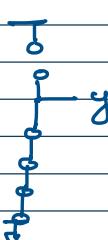
Clu = 1 :

when A = 0 :



output does not have any closed path
L remains same.

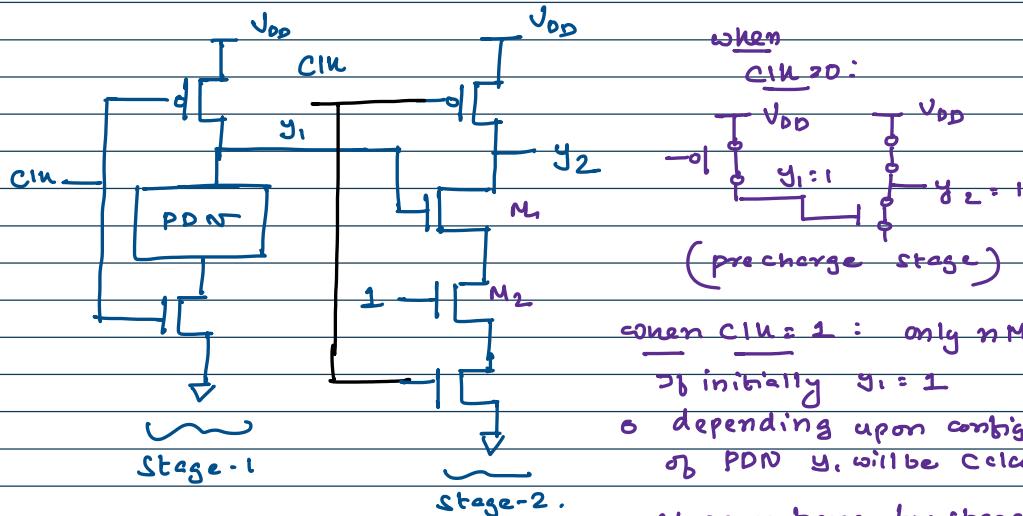
when A = 1 :



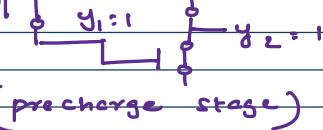
output has a path to discharge
L thus it becomes logic 0.

But problem! After one transition no further transitions are allowed within same clock pulse.

(II) Cascading of dynamic CMOS ?



when $C1n = 0$:



when $C1n = 1$:

- o initially $y_1 = 1$
- o depending upon configuration of PDN y_1 will be calculated

At some time for stage 2

will be calculated for $y_1 = 2$

M_1 on, M_2 on and hence y_2 will discharge to 0.

- o But if y_1 will be 0 y_2 will still remain at 1 as M_1 off.

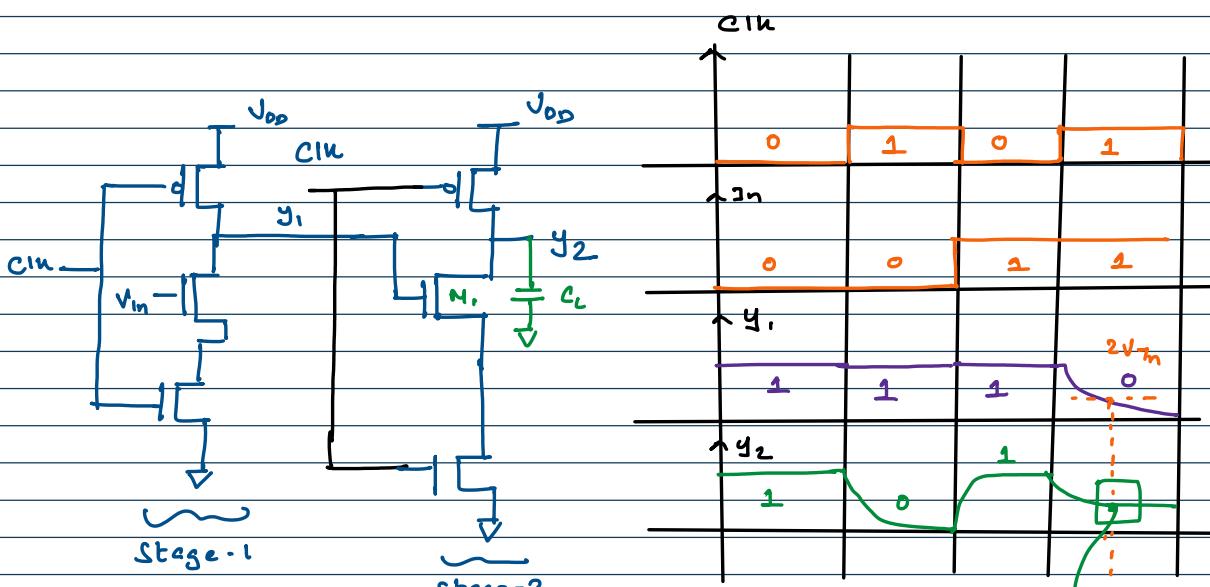


error output ??

here stage 1 output has logic 1 and PDN network complete to discharge to 0.
But this transition will take some time.

But stage 2 will not wait for y_1 to become 0 it will treat $y_1 = 1$ as 1p and discharge to 0.

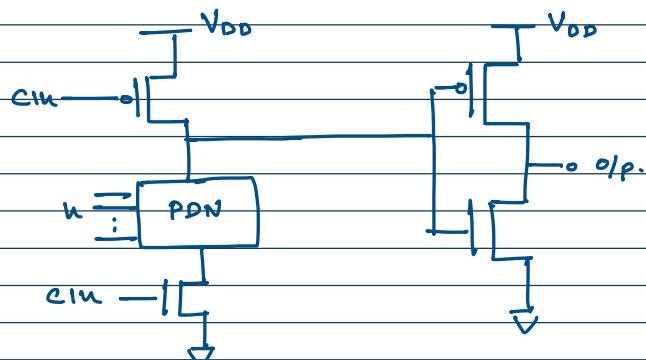
[And as only one transition allowed
Nothing further will affect it.]



Stage-1

Stage-2

Domino logic CMOS



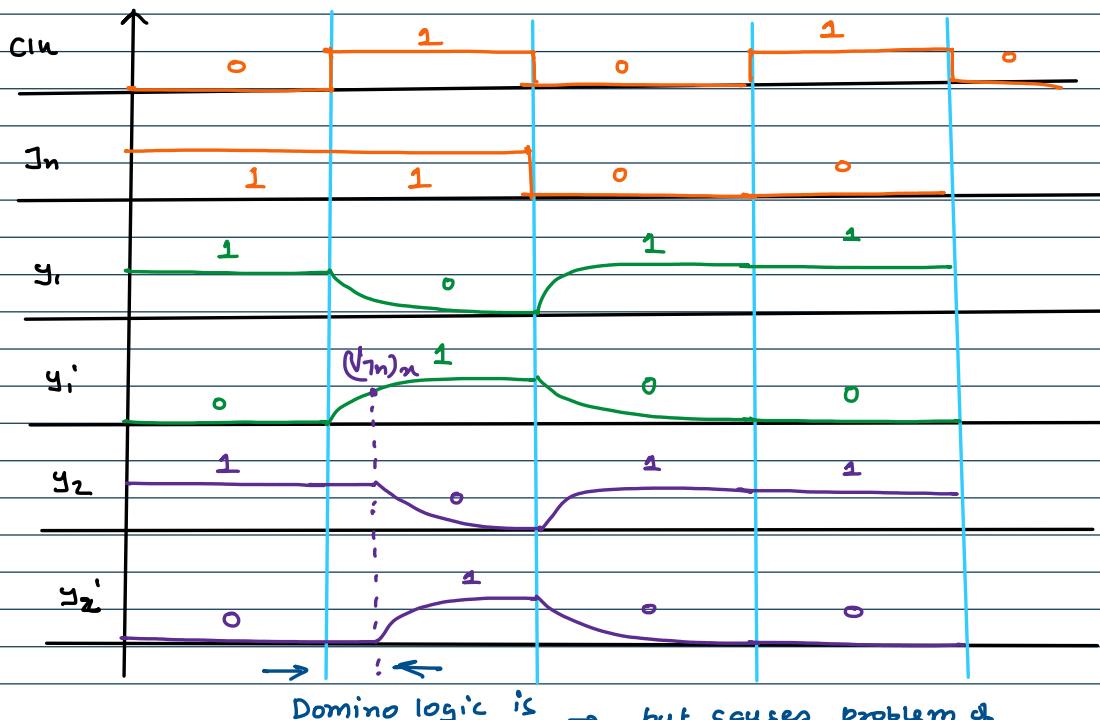
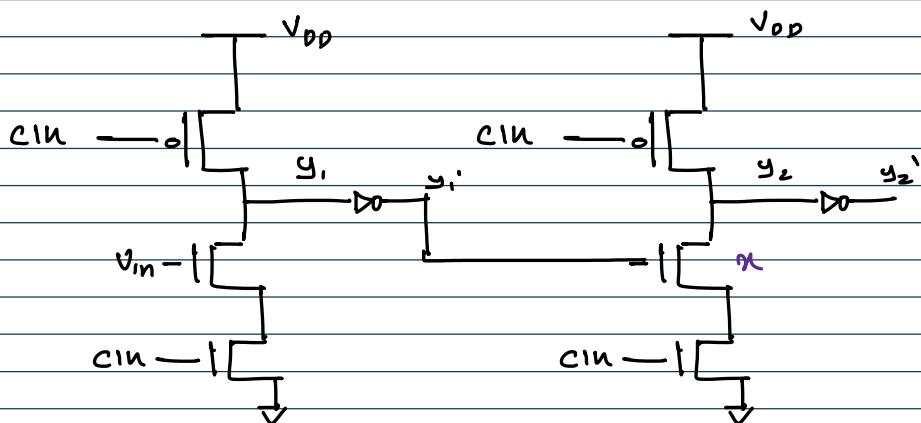
Total transistors used: $(n+2)_{NMOS} + 2_{PMOS}$

after this

M₁ gets switched off

and it remains in high impedance state.

Cascading of domino logic



\rightarrow ! \leftarrow
Domino logic is solving problem

but causes problem of RACE.

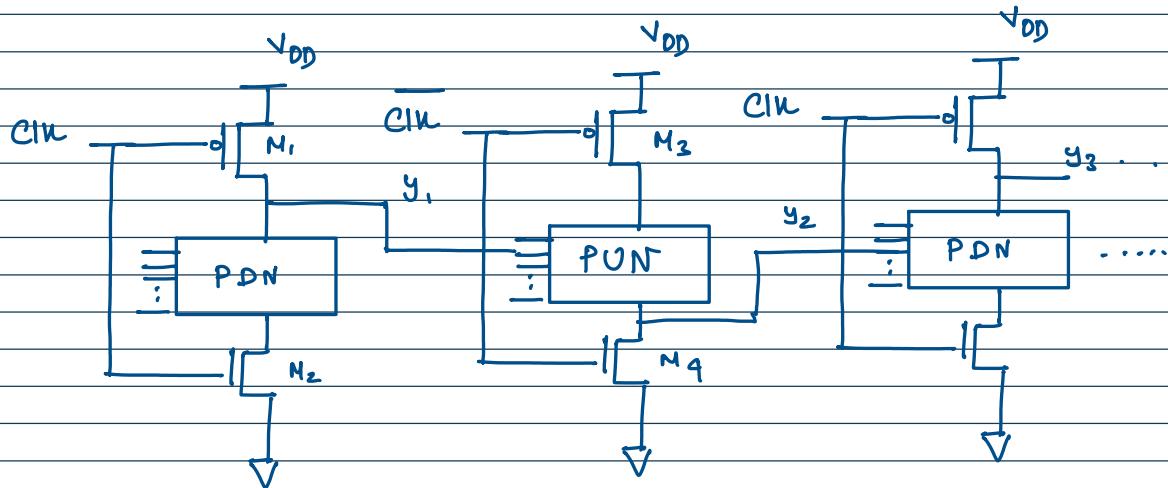
$(V_{in})_x$

\vdash threshold voltage of transistor x

$V < (V_{in})_n \Rightarrow (M)_n$ off and hence o/p constant

$V > (V_{in})_n \Rightarrow (M)_n$ on and o/p starts discharging to gnd.

n-p logic (NOR logic)



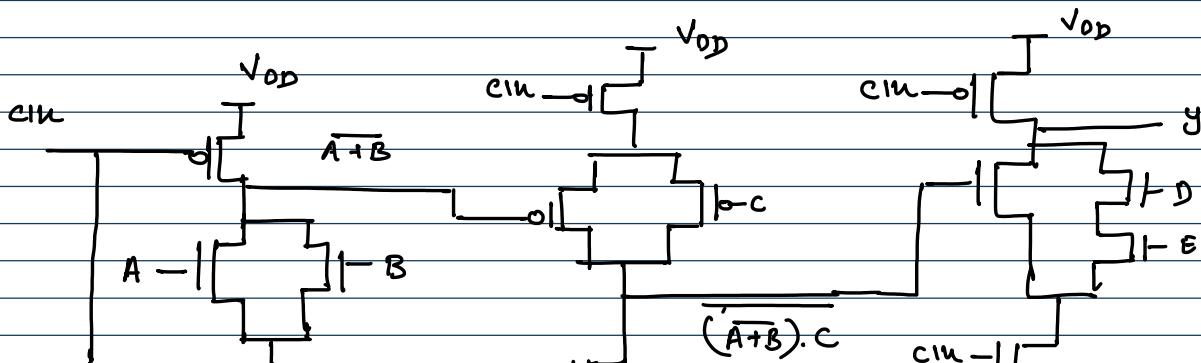
$CIN = 0 \Rightarrow M_1 = \text{on}$ and $M_2 = \text{open}$
 $\therefore y_1$ is charged to V_{DD}

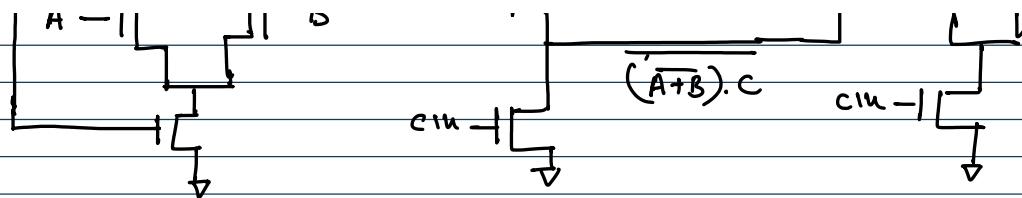
also $M_3 = \text{open}$ and $PUN = \text{off}$.
 $\therefore y_2 = 0$

$CIN = 1$: M_1 open \rightarrow depends upon boolean function present inside PUN or PDN

eg: $y = \overline{(A+B)} \cdot C + (\overline{D} \cdot E)$

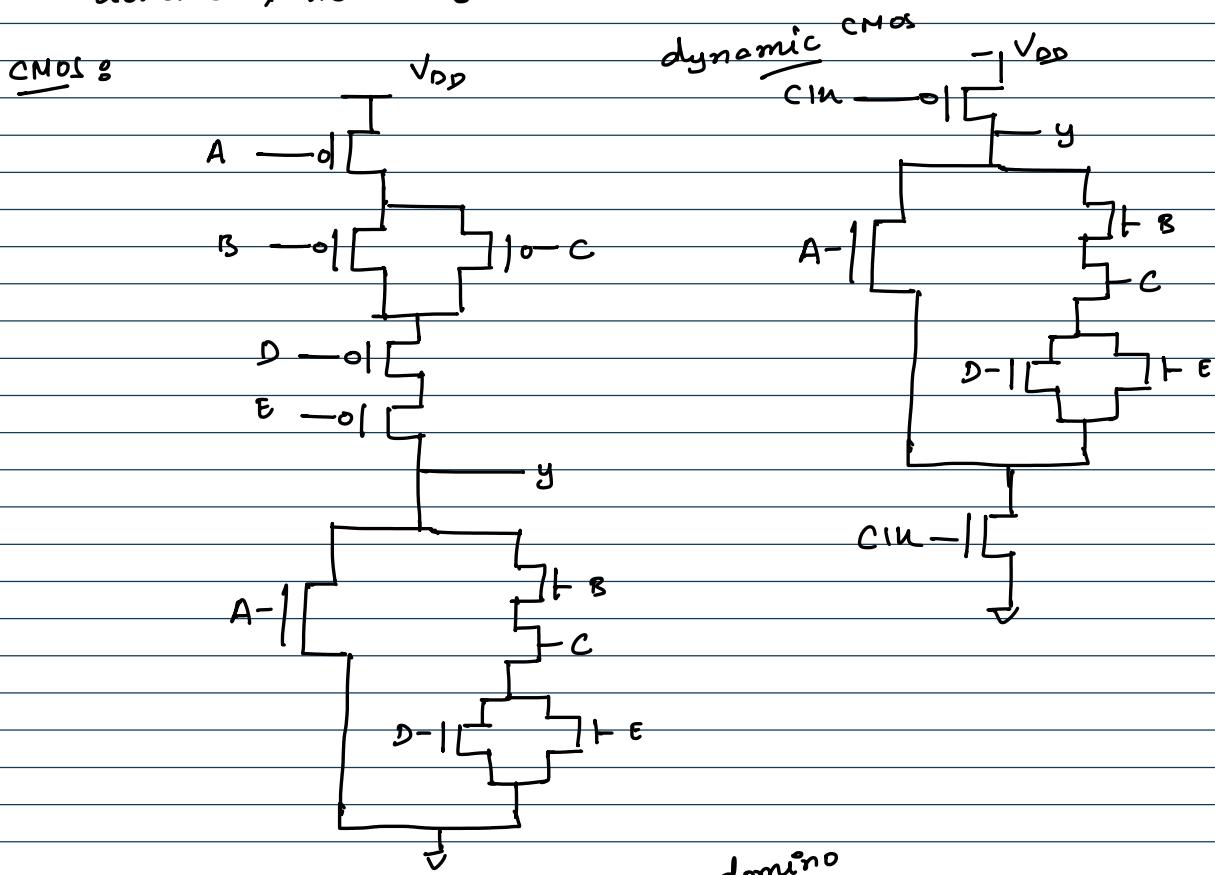
Implement in PDN
 output + next in PUN
 output + next in PDN.



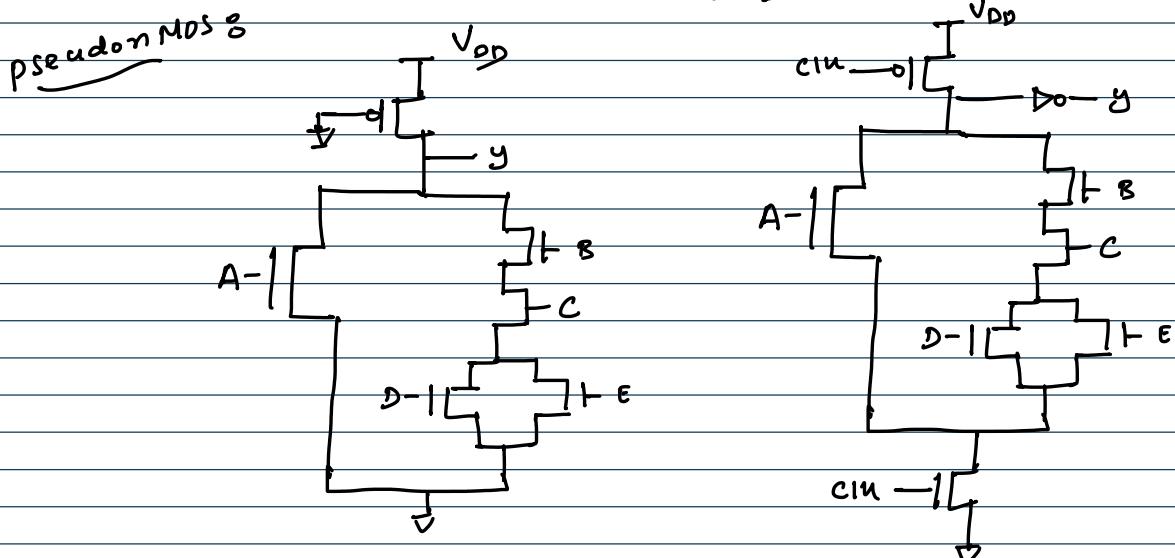


$$Q \quad y = \overline{A + BC} (D + E)$$

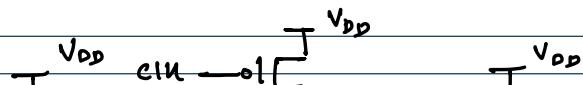
Implement using CMOS, pseudonmos, dynamic, domino, nor-a logic



domino



nora logic



nor logic

