ECE2243 FPGA BASED SYSTEM DESIGN [3 0 0 3]

Total number of lecture hours: 36

Course Learning Outcomes:

At the end of the course, the student will be able to:

CLO1	Explain the various modelling style in Verilog
CLO2	Explain the various FPGA architecture and technologies
CLO3	Develop the ability to model combinational and sequential digital circuits using Verilog HDL
CLO4	Implementation of the combinational and sequential digital circuits in FPGA
CLO5	Design and implement a system using FPGAs for real-world applications like a traffic light controller or real-time clock.

Course Description

Verilog HDL

Coding Style: Lexical Conventions - Ports and Modules – Operators - Structural Modeling, Data Flow Modeling - Behavioral level Modeling -Tasks & Functions. System Tasks & Compiler Directives - Test Bench. **[10]**

Verilog Modelling of Combinational and Sequential Circuits:

Behavioral, Data Flow and Structural Realization – Adders – Multipliers- Comparators - Flip Flops - Realization of Shift Register - Realization of a Counter- Synchronous and Asynchronous. **[8]**

Synchronous Sequential Circuit:

State diagram-state table –state assignment-choice of flipflops – Timing diagram –One hot encoding Mealy and Moore state machines – Design of serial adder using Mealy and Moore state machines - State minimization – Sequence detection- Design examples: Sequence detector, Serial adder, Vending machine using One Hot Controller. **[8]**

Overview of FPGA Architectures and Technologies

FPGA Architectural options, coarse vs fine-grained, vendor-specific issues (emphasis on Xilinx FPGA), Antifuse, SRAM and EPROM-based FPGAs, FPGA logic cells, interconnection network, and I/O Pad. **[5]**

System Design Examples using Xilinx FPGAs

Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD, Embedded Processor Hardware Design. **[5]**

***Self-directed Learning:** Simulation of various designs using Xilinx Software.

References:

1. M.J.S. Smith, *"Application Specific Integrated Circuits"*, Pearson, 2000.
2. Peter Ashenden, *"Digital Design using Verilog"*, Elsevier, 2007.
3. Clive Maxfield, *"The Design Warriors' Guide to FPGAs"*, Elsevier, 2004
4. Samir Palnitkar, *"Verilog HDL: A Guide to Digital Design and Synthesis"* Prentice Hall, Second Edition, 2003.
5. Wayne Wolf, *"FPGA Based System Design*", Prentices Hall Modern Semiconductor Design Series, Pearson, 2004.