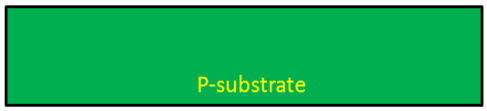
NMOS FABRICATION PROCESS

Step 1

- Processing is carried on single crystal silicon of high purity on which required P impurities are introduced as crystal is grown. Such wafers are about 75 to 150 mm in diameter and 0.4 mm thick and they are doped with say boron to impurity concentration of 10 to power 15/cm3 to 10 to the power 16 /cm3.



Clean substrate

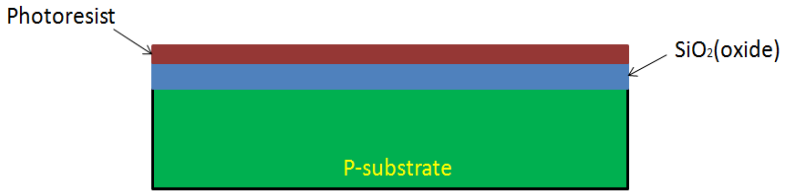
Step 2

- A layer of silicon dioxide (SiO_2) typically 1 micrometer thick is grown all over the surface of the wafer to protect the surface, acts as a barrier to the dopant during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.

Silicon dioxide(SiO_2) grown at the surface of the wafer

Step 3

- The surface is now covered with the photoresist which is deposited onto the wafer and spun to an even distribution of the required thickness.



substrate surface covered with photoresist

Step 4

- The photo resist layer is then exposed to ultraviolet light through masking which defines those regions into which diffusion is to take place together with transistor channels.
- The opaque region at the mask allow the ultraviolet light to hit the surface of the photoresist at the substrate and making it dissolve.

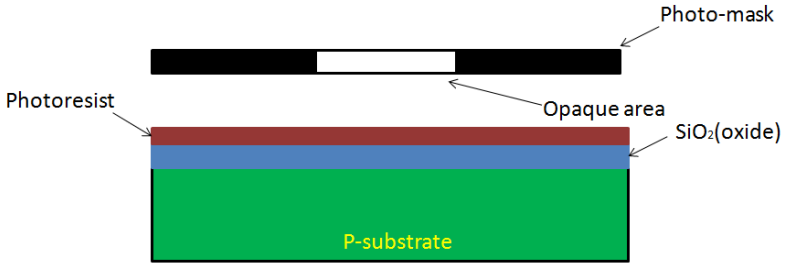
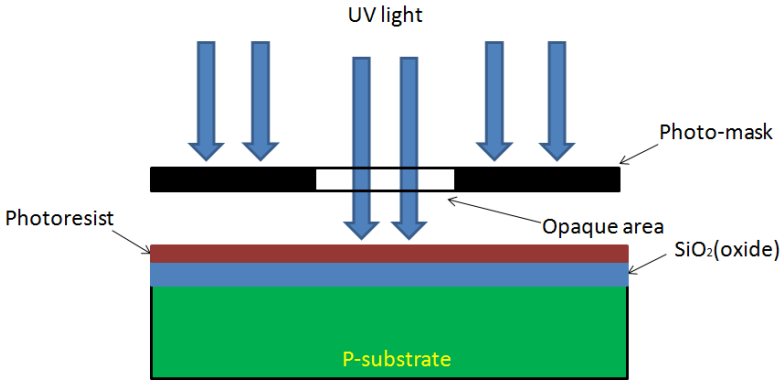
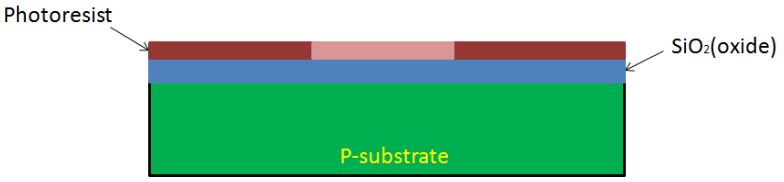


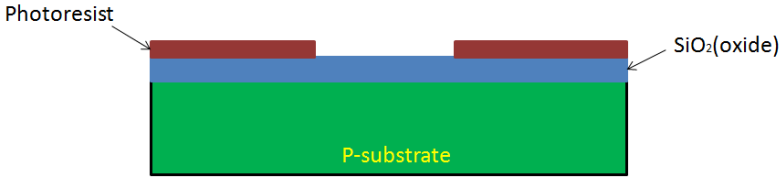
Photo-mask is in position for patterning



UV light exposed to the substrate



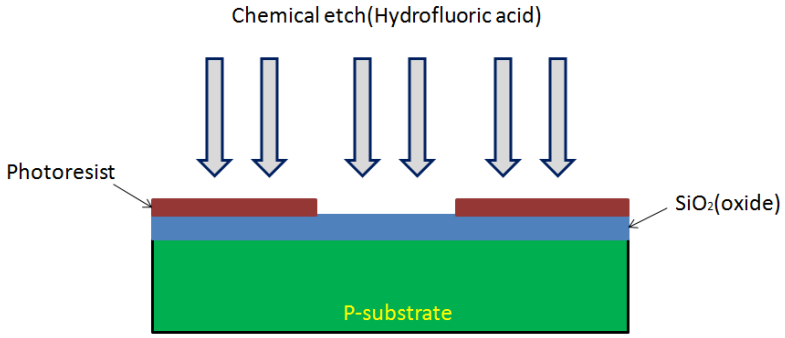
Photoresist surface that hit by the UV light dissolve



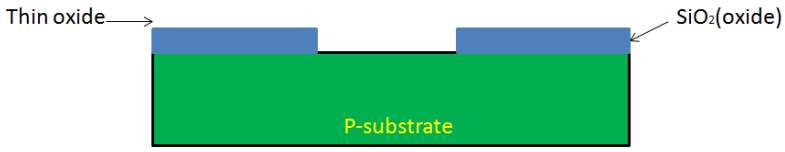
The uncovered dissolve while the covered region remain

Step 5

- The substrate now is ready to be etched to remove the remaining photoresist at the substrate and to create an opening at the substrate. In this process, Hydrofluoric acid is used as its etch acid.



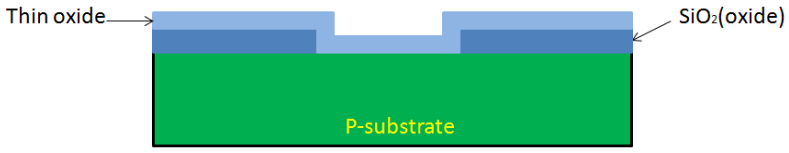
hydrofluoric acid used as etch acid



the remaining photoresist removed and an opening to the substrate created.

Step 6

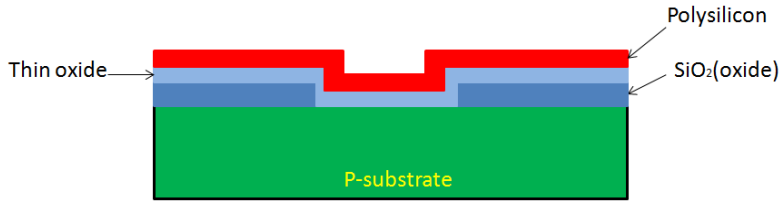
- A layer of the thin oxide is form SiO_2 (0.1 micrometer typical) is grown over the entire chip surface at high temperature.



A layer of thin oxide grown at the surface of the substrate

Step 7

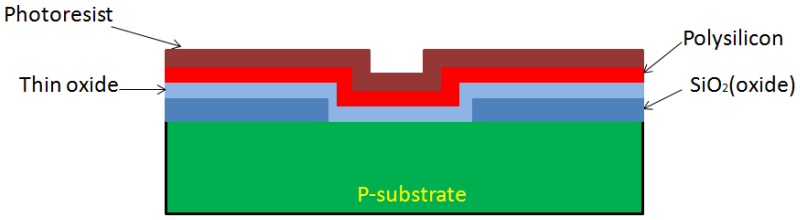
- The polysilicon layer consists of heavily doped polysilicon deposited at the surface of the substrate by chemical vapor deposition (CVD).



Polysilicon is deposited at the surface of the substrate.

Step 8

- Photoresist is done for the second time at the surface of the substrate.



Substrate is coated with photoresist

Step 9

- The photolithography process also done for the second time. The process is done to create a new pattern to make a polysilicon gate at the center of the substrate.

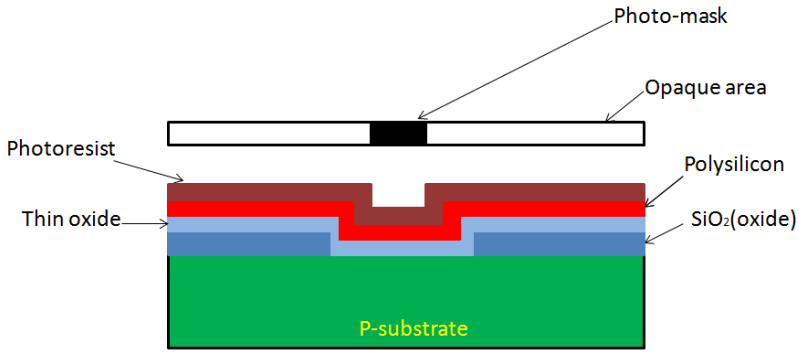
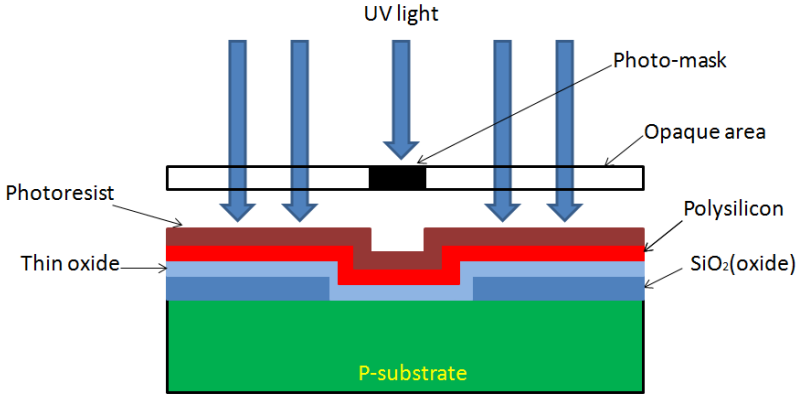
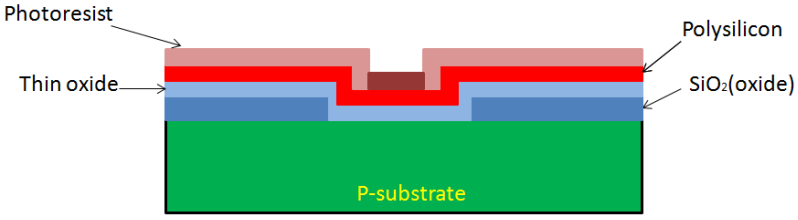


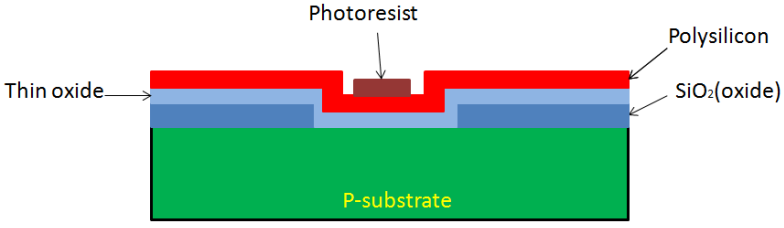
Photo-mask is in position for patterning



UV light exposed to the substrate



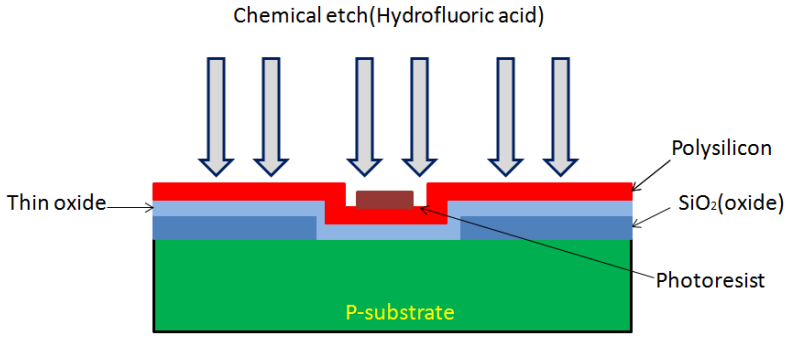
Photoresist surface that hit by the UV light dissolve



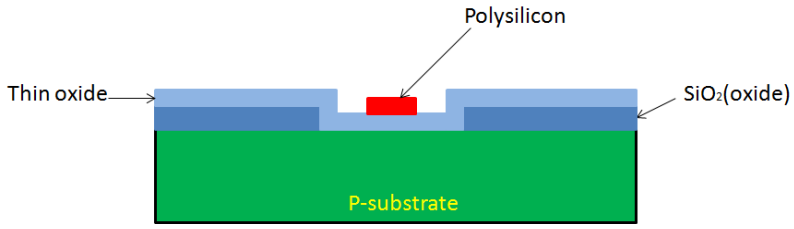
The uncovered dissolve while the covered region remain

Step 10

- The substrate is now etch with hydrofluoric acid to remove the remaining photoresist and polysilicon. As a result , a polysilicon gate is formed at the center of the substrate.



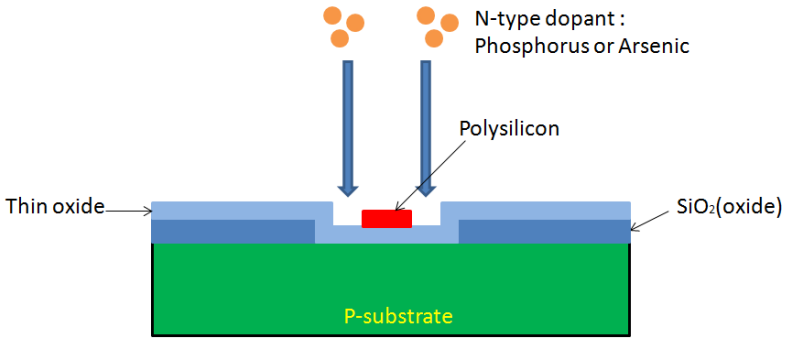
hydrofluoric acid used as etch acid



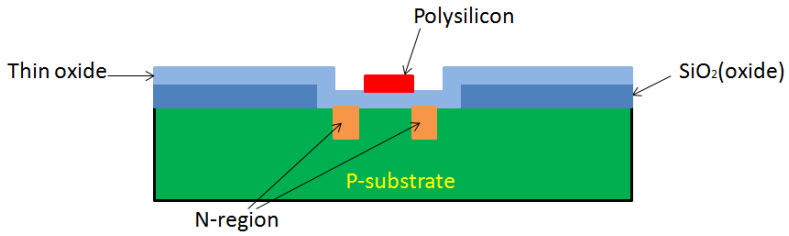
polysilicon gate created

Step 11

- In this process, Substrate is bombarded by an amount of arsenic or phosphorus electron to create N region to form drain and source.



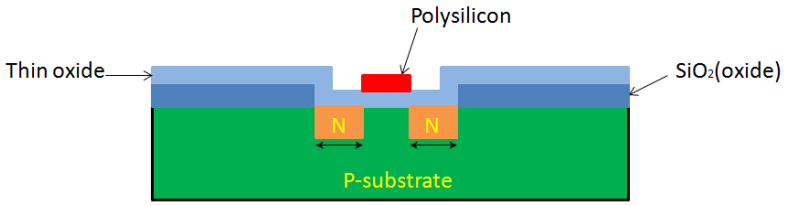
Arsenic or phosphorus ion bombarded at the substrate.



N region formed at the substrate representing source and drain

Step 12

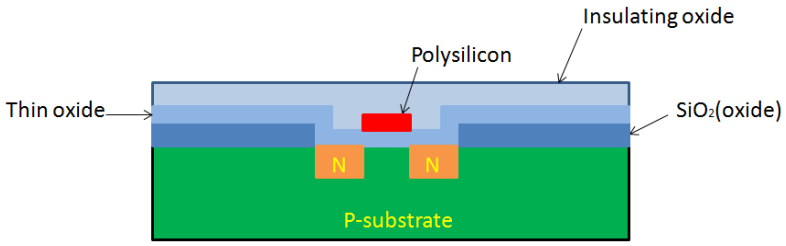
- After the ion implantation done, the annealing process is conducted to repair the single crystal structure of the substrate and active the dopant.



The annealing process done to repair the single crystal structure

Step 13

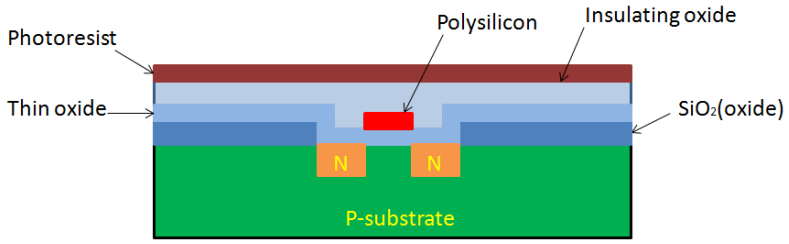
- Oxidation process is conducted once more to grow an insulating oxide at the substrate



The growth of insulating oxide

Step 14

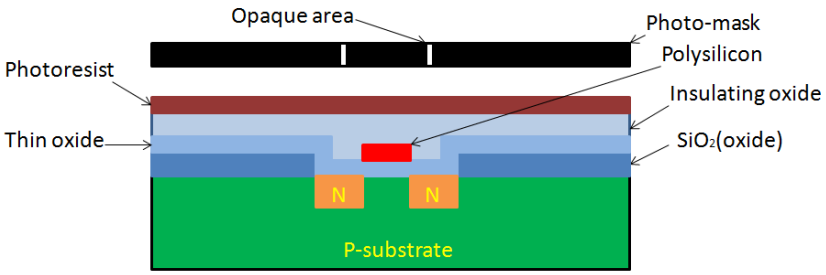
- Photoresist is conducted once more at the surface of the substrate.



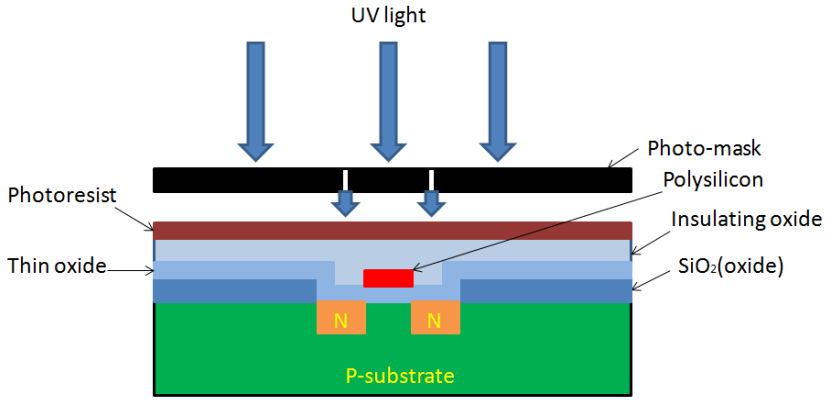
Photoresist coated the substrate

Step 15

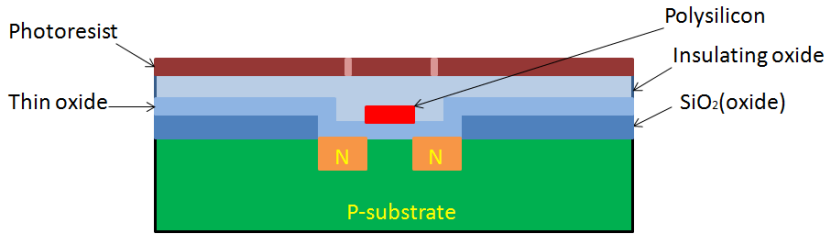
- Another photolithography is done to create an opening to metallization process



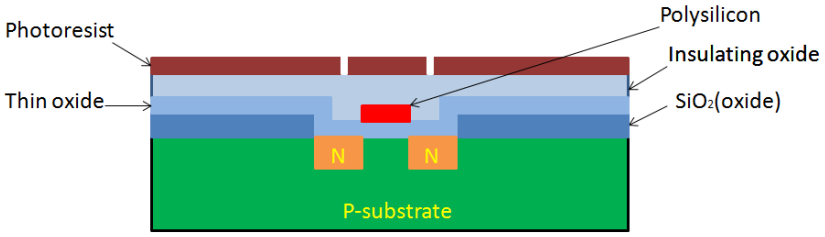
Masking process



UV light exposed to the substrate



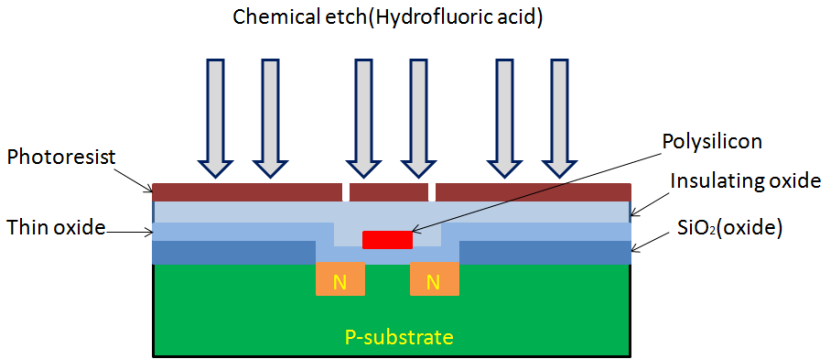
Photoresist surface that hit by the UV light dissolve



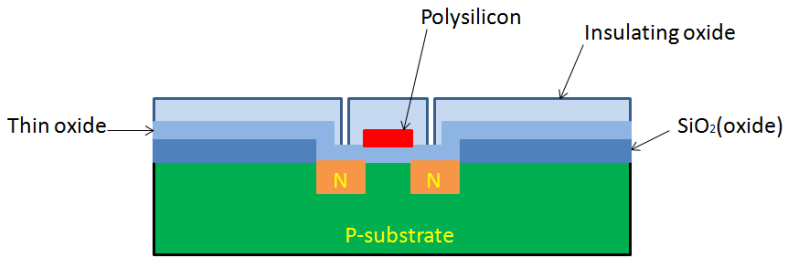
The uncovered dissolve while the covered region remain

Step 16

- The substrate is now etched remove the remaining photoresist. As a result creating an opening for metallization process.



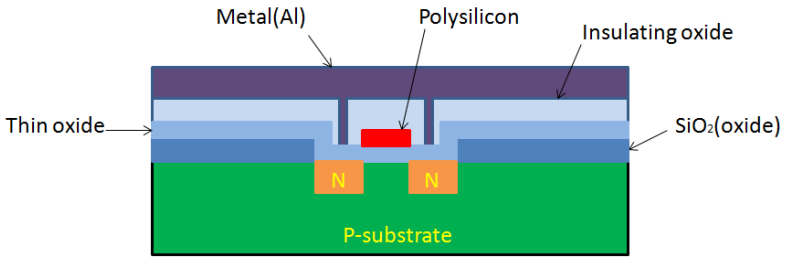
Etching process to remove photoresist and create an opening



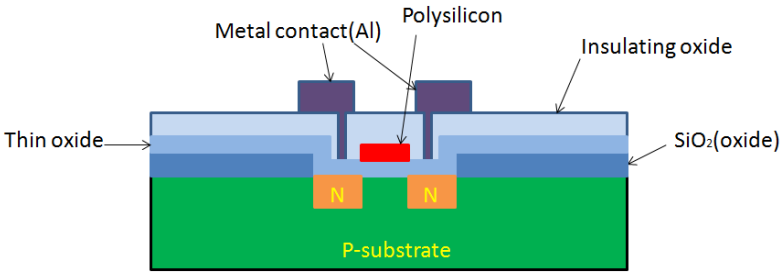
An opening created through etching

Step 17

- The substrate then has metal (aluminum) deposited over its surface to a thickness typically of 1 micrometer. Aluminum evaporated to cover surface. This metal layer is then masked and etched to form the required interconnection pattern.



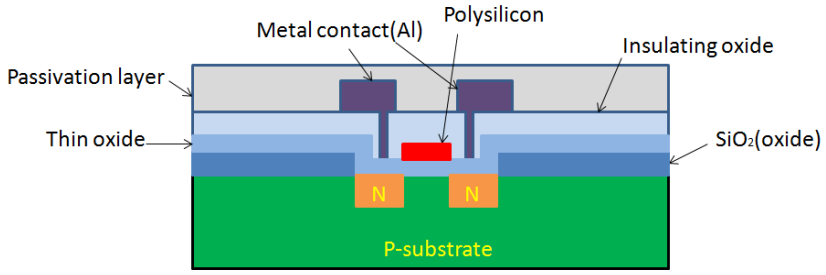
Aluminum evaporated to cover the surface of the surface



Aluminum etched to form Metal contact

Step 18

- Then passivation layer is created with an oxide layer to protect against contamination and increase electrical stability at the substrate.



The substrate then coated by the passivation layer