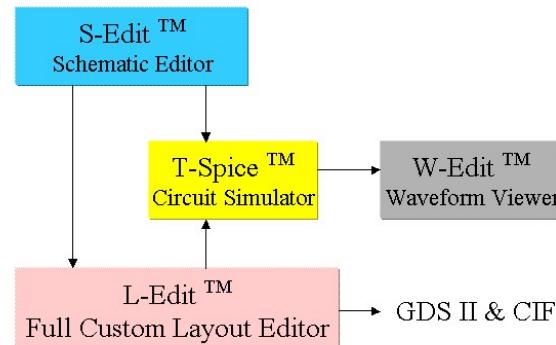


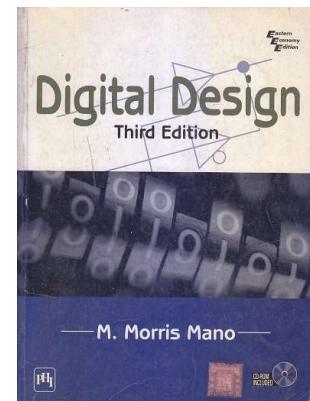
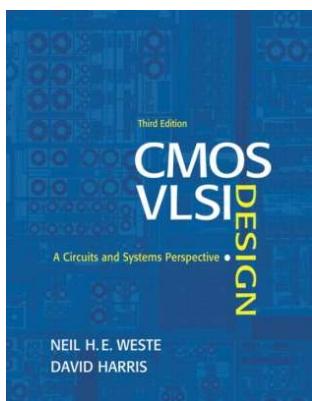
VLSI Design (ECE2221)



Instructor: Dr. Amit Kumar Goyal

Office: AB5/Ground Floor/Room-3/FC43

Contact: amit.goyal@manipal.edu



BTech in Electronics Engineering (VLSI Desing and Technology)

OBJECTIVES and OUTCOME

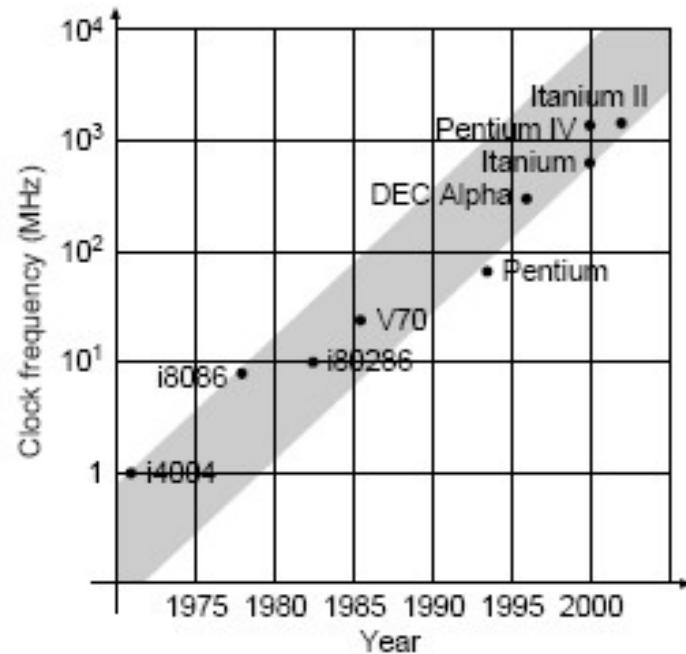
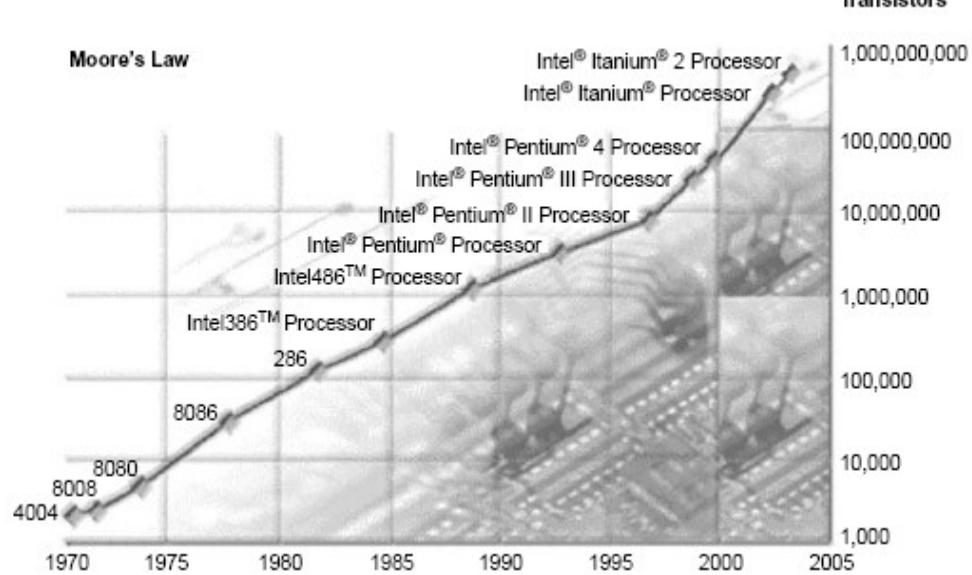
1. This course provides an introduction to the fundamental principles of VLSI circuit design.
2. Emphasis is placed on the design of basic building blocks of large-scale digital integrated circuits and systems.
3. Understand the concept behind ASIC Design.
4. Implement a complete digital system on silicon using state-of-the-art CAD tools.
5. Understand the consequence of scaling down the dimensions of transistors and its effect on device speed and density....
6. Have the necessary background to complete CMOS designs and assess which particular design style to use on a given design, from FPGA to Full custom design.

OBJECTIVES and OUTCOME

1. Analyze NMOS & CMOS inverter circuits.
2. Analyze and Design combinational and sequential circuits using MOS devices.
3. Describe the process of fabrication of NMOS and CMOS devices.
4. Draw the stick diagrams and layouts for different MOS circuits.
5. Describe various issues involved in subsystem design and estimate performance parameters.
6. Analyze the impact of interconnects on the circuit performance.

Moore's law

The evolution of MOS technology has followed the famous Moore's law that predicts a steady decrease in gate length. As predicted by Gordon Moore in the 1960s, integrated circuit (IC) **densities have been doubling** approximately **every 18 months**, and this doubling in size has been accompanied by a similar exponential increase in circuit speed (or more precisely, clock frequency).



On-chip transistor count increase for the Intel processors (Source: Intel).

What is expected?

Complexity → ∞

Intel 4004 Processor: 2300 Transistor → 10µm Technology

Intel i7 Processor : 3,200,000,000 Transistors → 14nm Technology

Power → Min

Intel 4004 Processor: 1 W

Intel i7 Processor : 47W

Cost → Min

Intel 4004 Processor: \$60

Intel i7 Processor : \$366

Delay → Min

Intel 4004 Processor: 740KHz

Intel i7 Processor : 3.6 GHz

Size → Min

Intel 4004 Processor: 12 mm²

Intel i7 Processor : 246 mm²

VLSI : Very Large Scale Integration

- Integration: Integrated Circuits
 - multiple devices on one substrate
- How large is Very Large?
 - SSI (small scale integration)
 - 7400 series, 10-100 transistors
 - MSI (medium scale)
 - 74000 series 100-1000
 - LSI 1,000-10,000 transistors
 - VLSI > 10,000 transistors
 - ULSI (some disagreement)

WHY VLSI?

Integration Improves the Design

- Lower parasitics, higher clocking speed
- Lower power
- Physically small

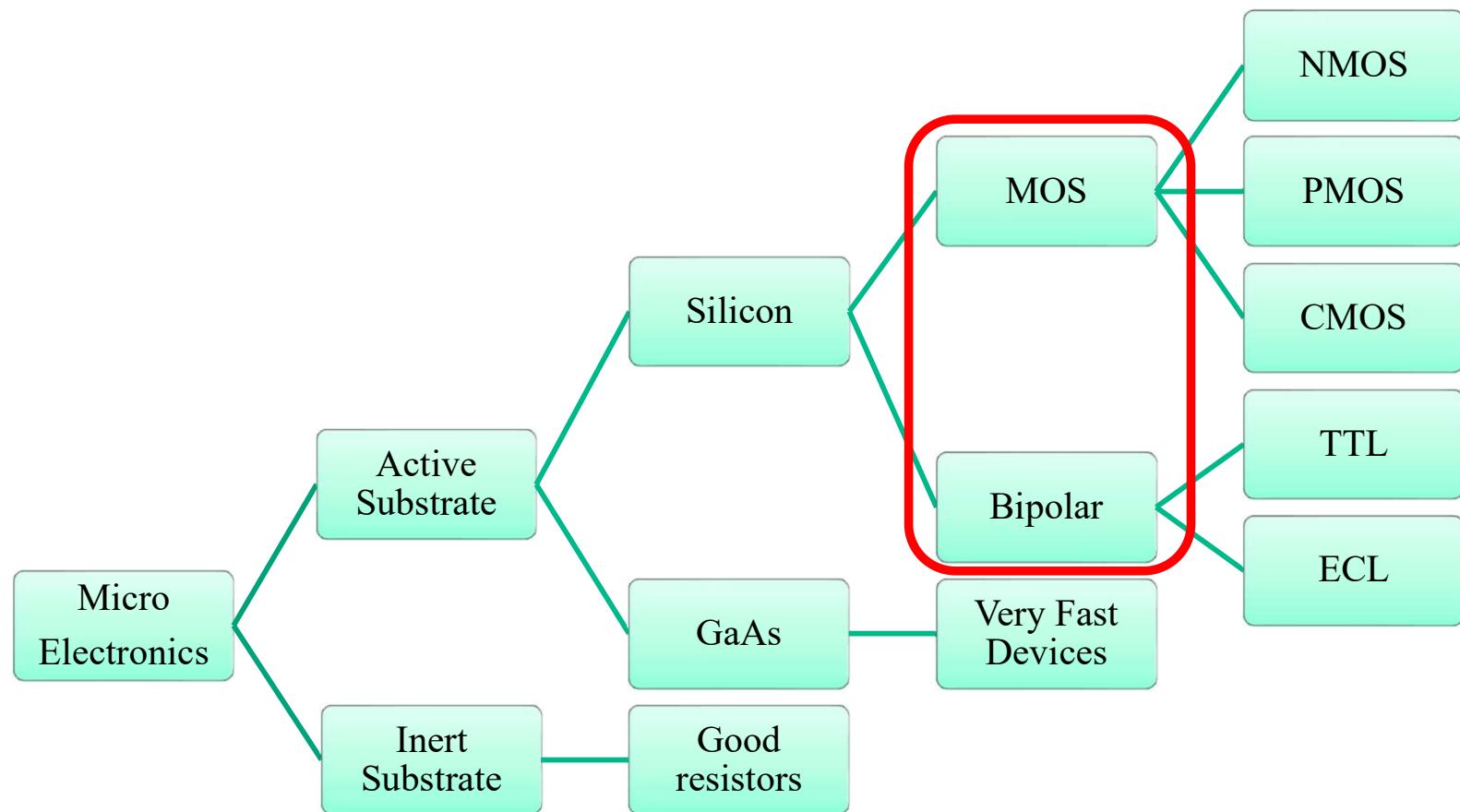
Integration Reduces Manufacturing Costs

- (almost) no manual assembly
- About \$1-5 billion/fab
- Typical Fab \approx 1 city block, a few hundred people
- Packaging is largest cost
- Testing is second largest cost
- For low volume ICs, Design Cost may swamp all manufacturing costs

What is “CMOS VLSI”?

- MOS = Metal Oxide Semiconductor (This used to mean a Metal gate over Oxide insulation)
- Now we use polycrystalline silicon which is deposited on the surface of the chip as a gate. We call this “poly” or just “red stuff” to distinguish it from the body of the chip, the substrate, which is a single crystal of silicon.
- We do use metal (aluminum) for interconnection wires on the surface of the chip.

Microelectronics Technology



MOS Vs. BJT

Factors	CMOS	Bipolar
Static Power Dissipation	Low	High
Input Impedance	High	Low
Noise Margin	High	Low
Packing Density	High	Low
Fan-out	Low	High
Direction	Bidirectional	Unidirectional

CMOS is superior!

VLSI Design

- The real issue in VLSI is about designing systems on chips.
- The designs are complex, and we need to use structured design techniques and sophisticated design tools to manage the complexity of the design.
- We also accept the fact that any technology we learn the details of will be out of date soon.
- We are trying to develop and use techniques that will transcend the technology, but still respect it.
- The real issue in VLSI is about designing systems on chips.

Design Styles

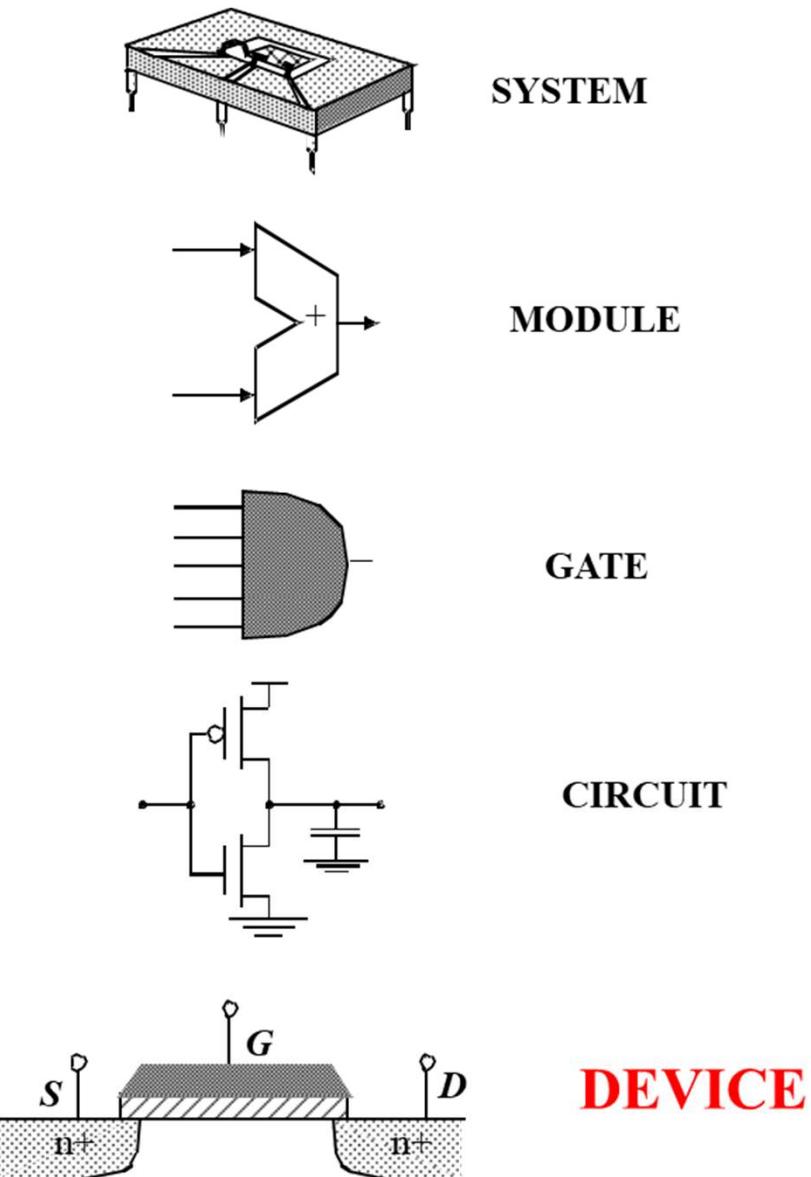
- Full custom
- Standard cell
- Gate-array
- Macro-cell
- “FPGA”
- Combinations

Comparison

	FPGA	Gate array	Standard cell	Full custom	Macro cell
Density	Low	Medium	Medium	High	High
Flexibility	Low (high)	Low	Medium	High	Medium
Analog	No	No	No	Yes	Yes
Performance	Low	Medium	High	Very high	Very high
Design time	Low	Medium	Medium	High	Medium
Design costs	Low	Medium	Medium	High	High
Tools	Simple	Complex	Complex	Very complex	Complex
Volume	Low	Medium	High	High	High
Device cost	High	Medium	Low	Low	Low

Levels of Design

- Specifications
 - IO, Function, Costs
- Architectural Description
 - VHDL, Verilog, Behavioral, Large Blocks
- Logic Design
 - Gates plus Registers
- Circuit Design
 - Transistors sized for power and speed
 - Discrete Logic, Technology Mapping
- Layout
 - Size, Interconnect, Parasitics



Design Methodology

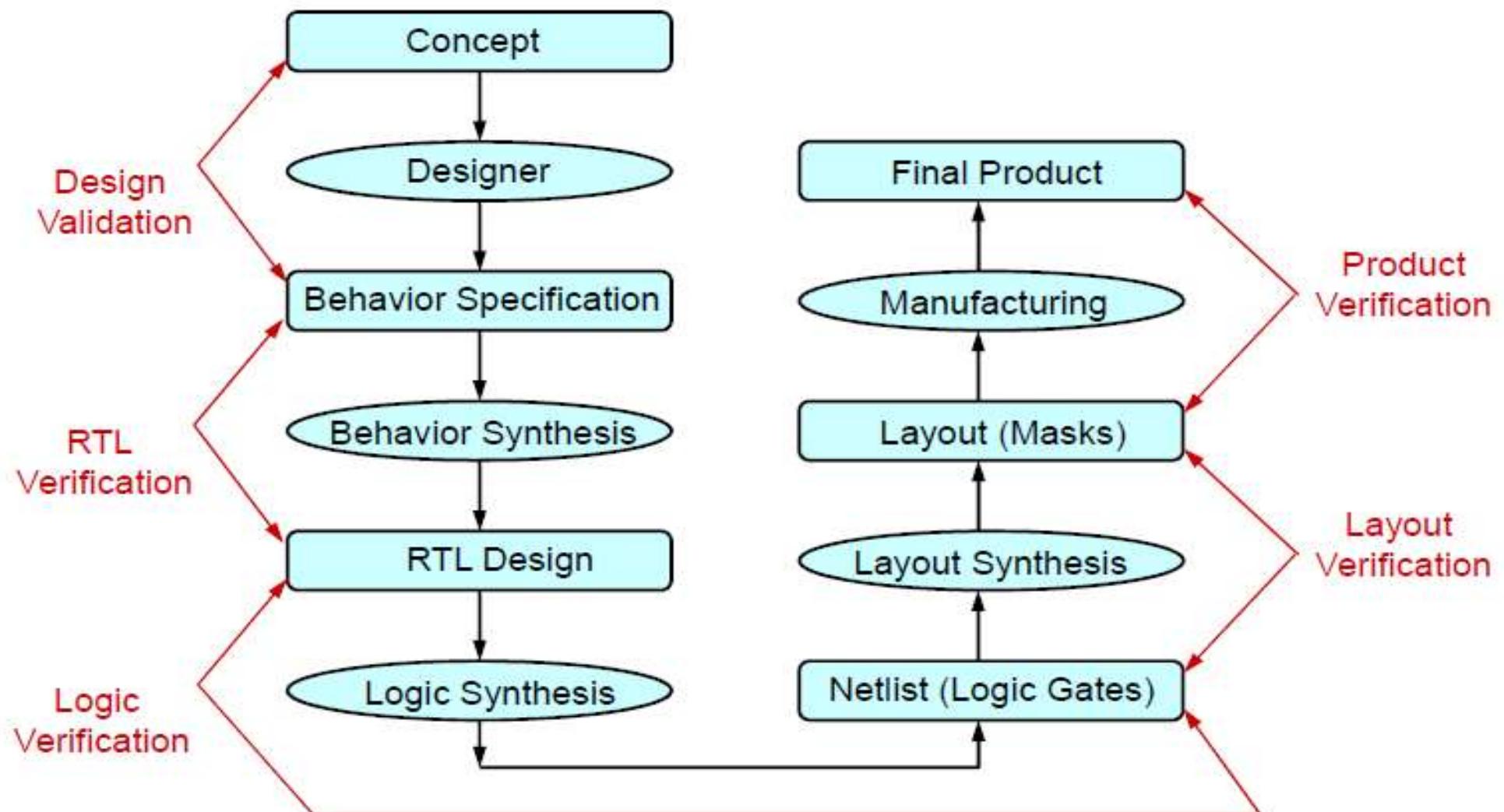
➤ **Design methodology**

- Process for creating a design

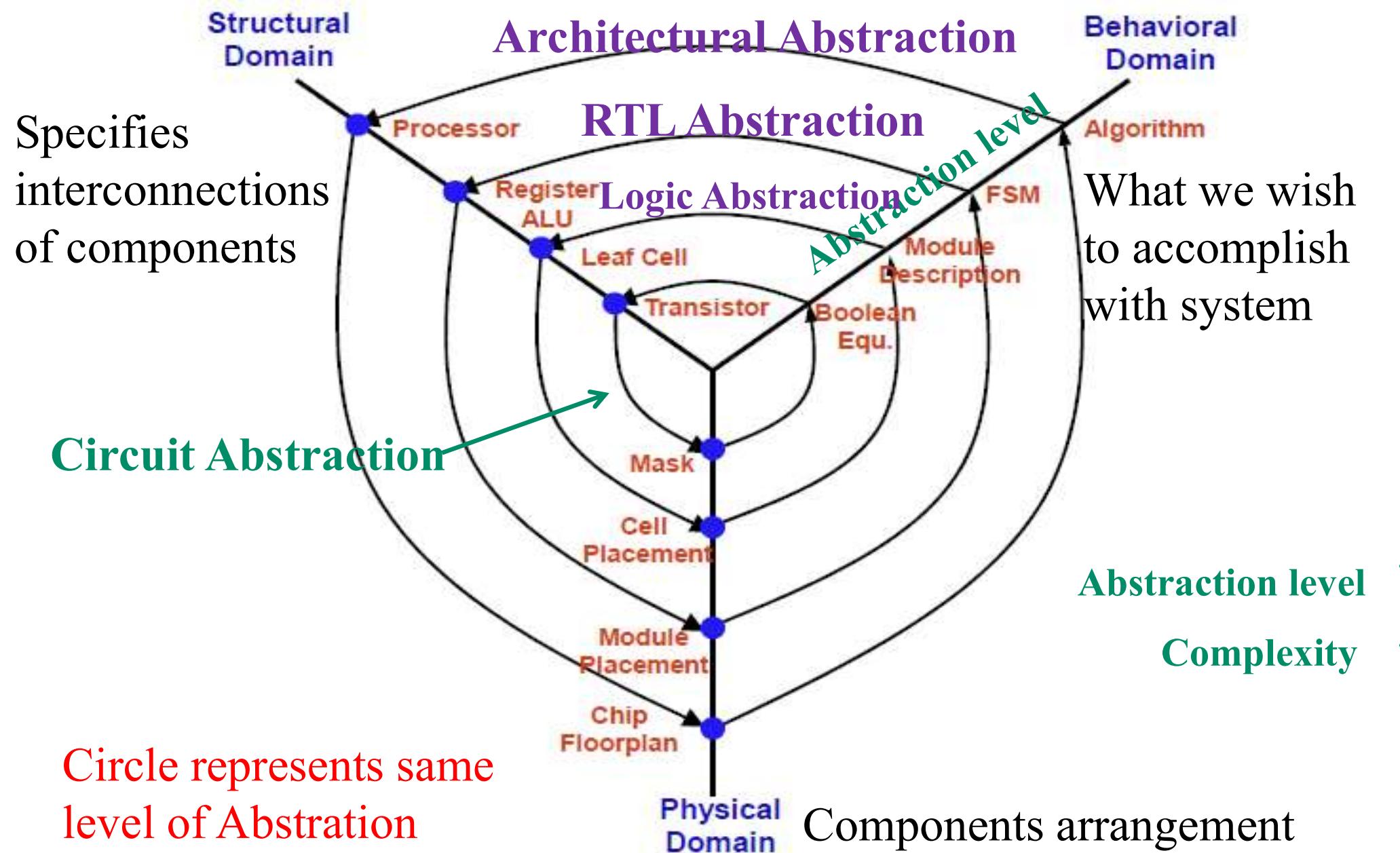
➤ **Methodology Goals**

- Design cycle
- Complexity
- Performance
- Reuse
- Reliability

VLSI Design Flow



Gajski Y Chart



VLSI Design Hierarchy

Works on Divide and Conquer

- Regularity
- Modularity
- Locality

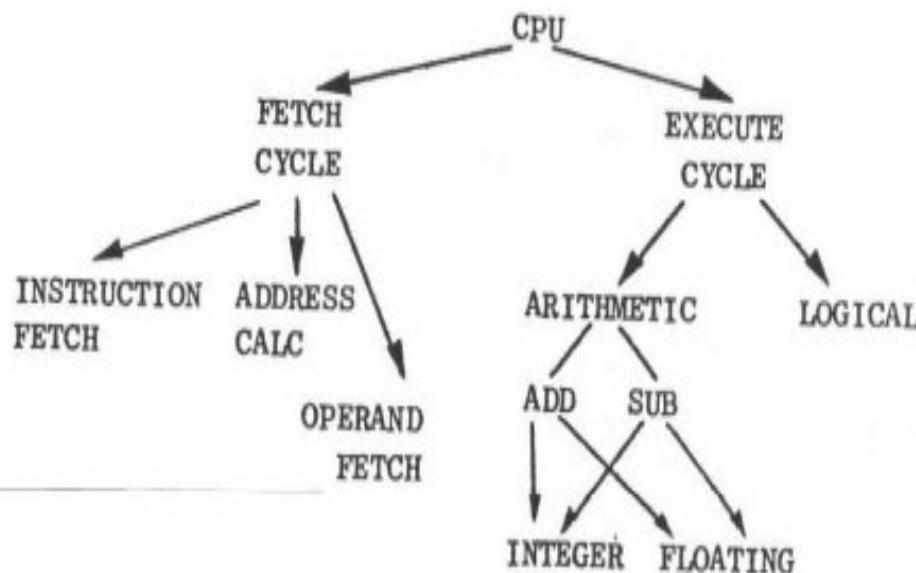
Hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible

Various functional blocks which make up the larger system must have well-defined functions and interfaces. **Independent of each other**

Internals of each module become unimportant to the exterior modules. **Internal details remain at the local level.**

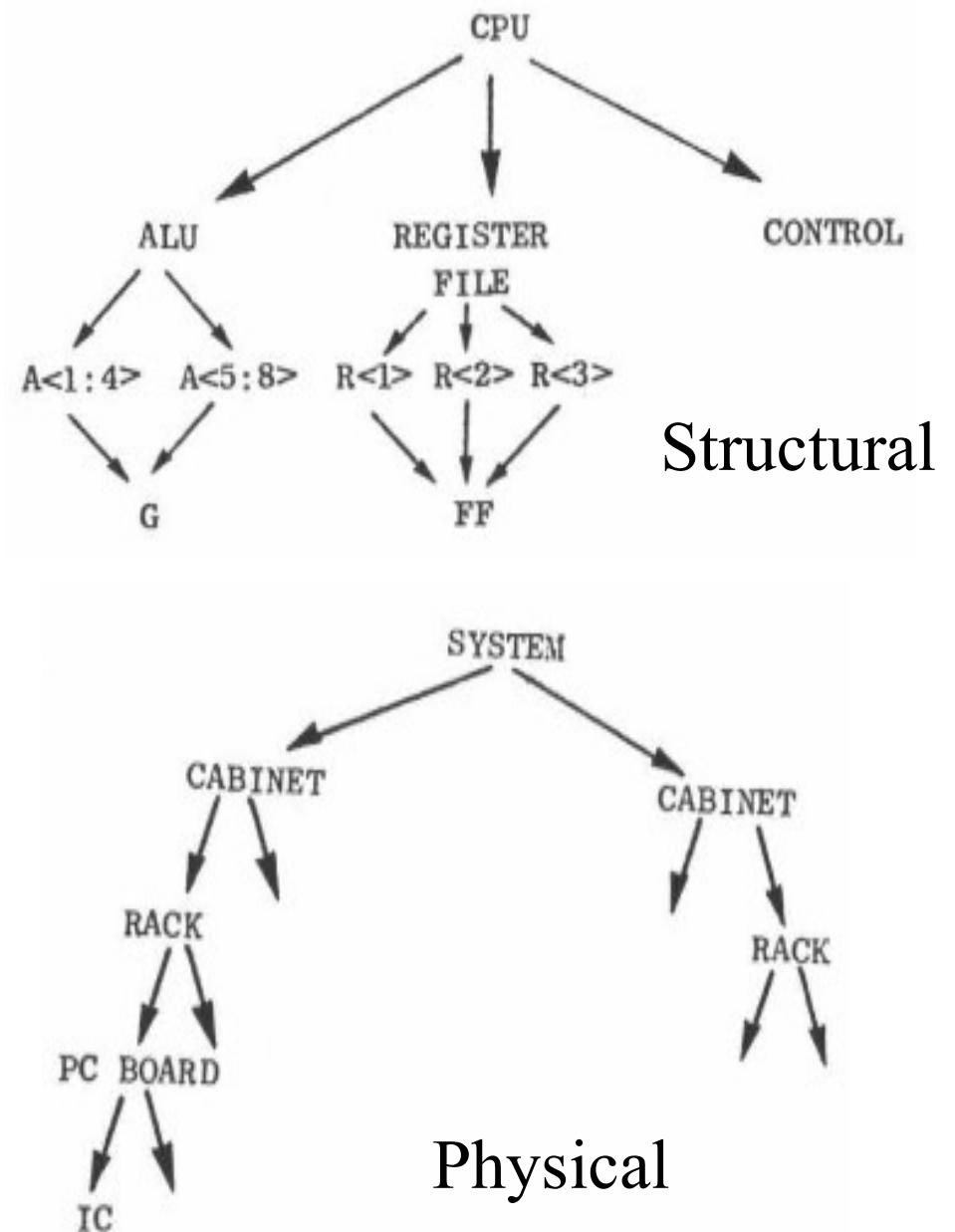
VLSI Design Hierarchy

Exist at all level of Abstraction



Behavioral

Example of a Computer



VLSI Design Hierarchy

Regularity exist at all level of Abstraction

- Transistor Level: All are of same size
- Logic Level : All Gate are of same type

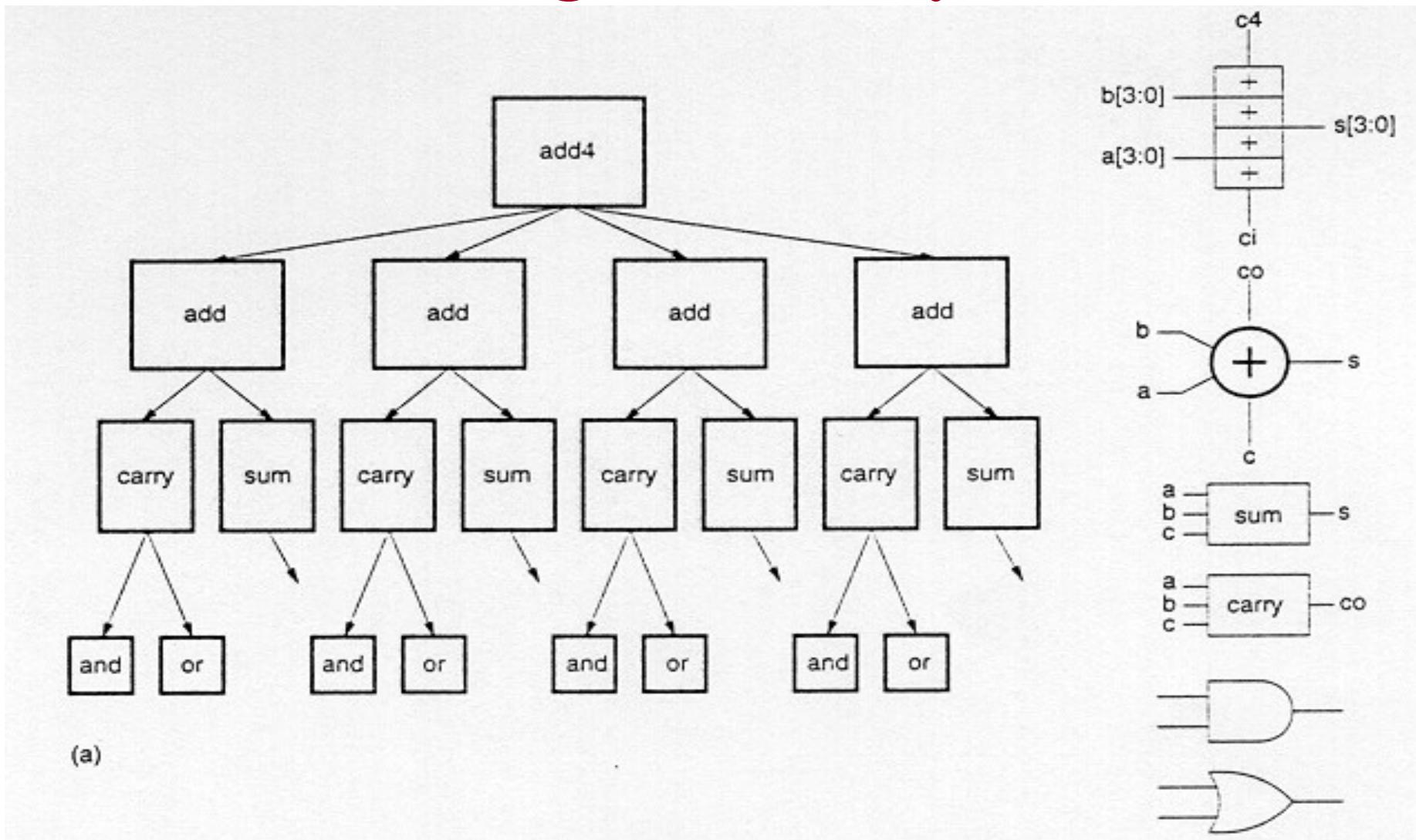
VLSI Design Hierarchy (Advantage)

Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

Modularity enables the parallelization of the design process. It also allows the use of generic modules in various designs.

Time-critical operations should be performed locally, without the need to access distant modules or signals.

VLSI Design Hierarchy (Example)



Structural decomposition of a CMOS four-bit adder into its components

COURSE INFORMATION

B.Tech. Electronics and Communication Engineering

COURSE PLAN: THEORY COURSE

Department :	Electronics and Communication Engineering			
Course Name & code :	VLSI Design & ECE-2221			Core
Semester & branch :	IV		ECE & EE(VLSI Design and Technology)	
Name of the faculty :	Dr. Amit Kumar Goyal			
No of contact hours/week:	L 4	T 0	P 0	C 4

COURSE INFORMATION

Introduction to MOS transistor: MOS Transistor, CMOS logic, Inverter, Long-Channel I-V and CV Characteristics, Non ideal I-V Effects, DC-Transfer characteristics, Noise Margin. Second order effects, MOS parasitic capacitance, Power: Dynamic Power, Static Power. Introduction to MOS spice models and Scaling of MOS circuits. [10]

Fabrication of ICs: Fabrication of MOS transistor, Latch-up in CMOS, Stick Diagrams, Layout Design Rules. [8]

Combinational and sequential MOS logic circuits: Static CMOS, Ratioed Circuits, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, with examples, Domino, Dual Rail Domino, CPL, Cascode Voltage Switch Logic, Bi-CMOS inverter circuits. Static latches and Registers, Dynamic latches and Registers, Sense Amplifier Based Register, clocking strategies. [12]

COURSE INFORMATION

Subsystem design: Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, Designing Memory and Array structures, Memory Core, Memory Peripheral Circuitry. Design of RAM, ROM, EPROM, EEPROM and flash memory with examples. [10]

Sheet resistance and delay models: Sheet resistance, standard unit of capacitance, Estimation of delays in NMOS and CMOS inverters, driving of large capacitive loads, super buffers, RC Delay Model, Elmore Delay, Linear Delay Model, Parasitic Delay, Delay in Logic Gate. | [8]

***Self-directed Learning:**

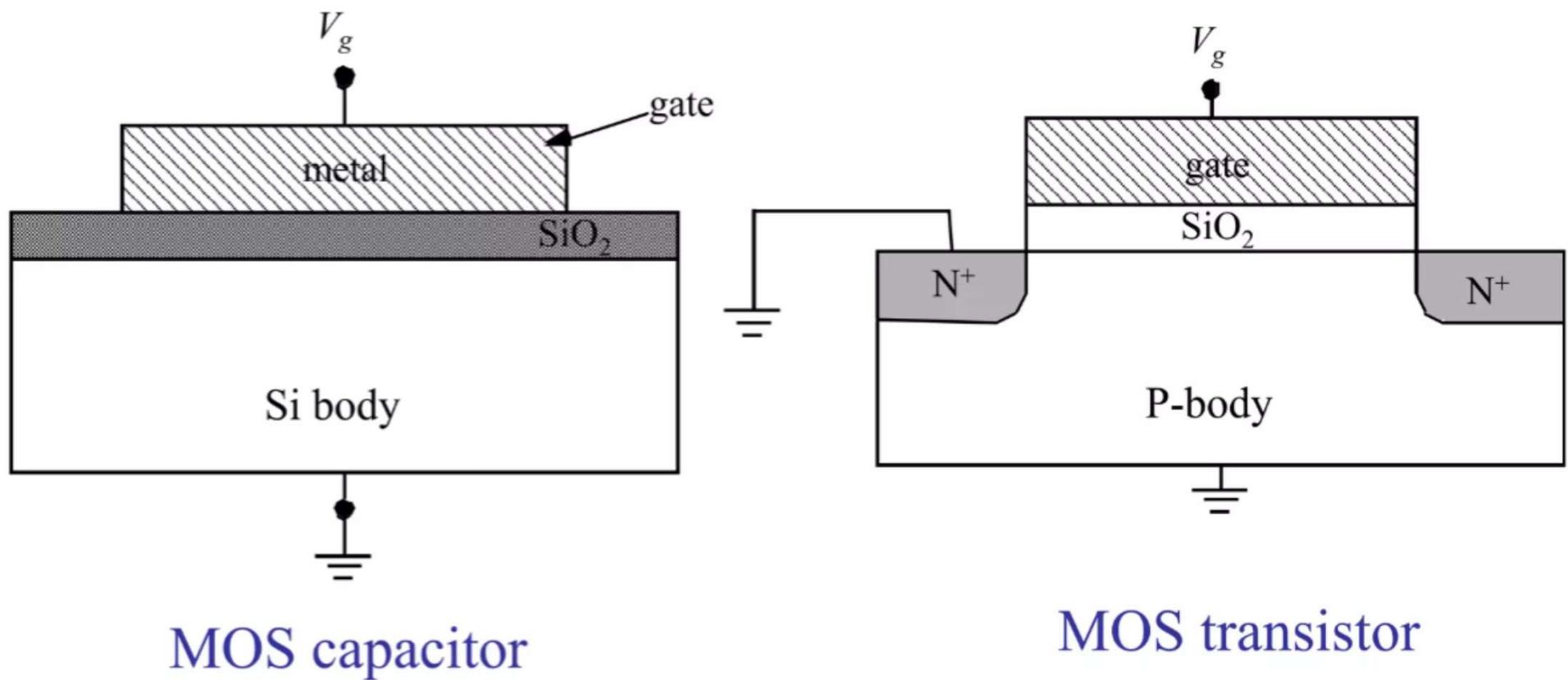
Simulation of MOSFET based logic circuits using LTSPICE

Course Books

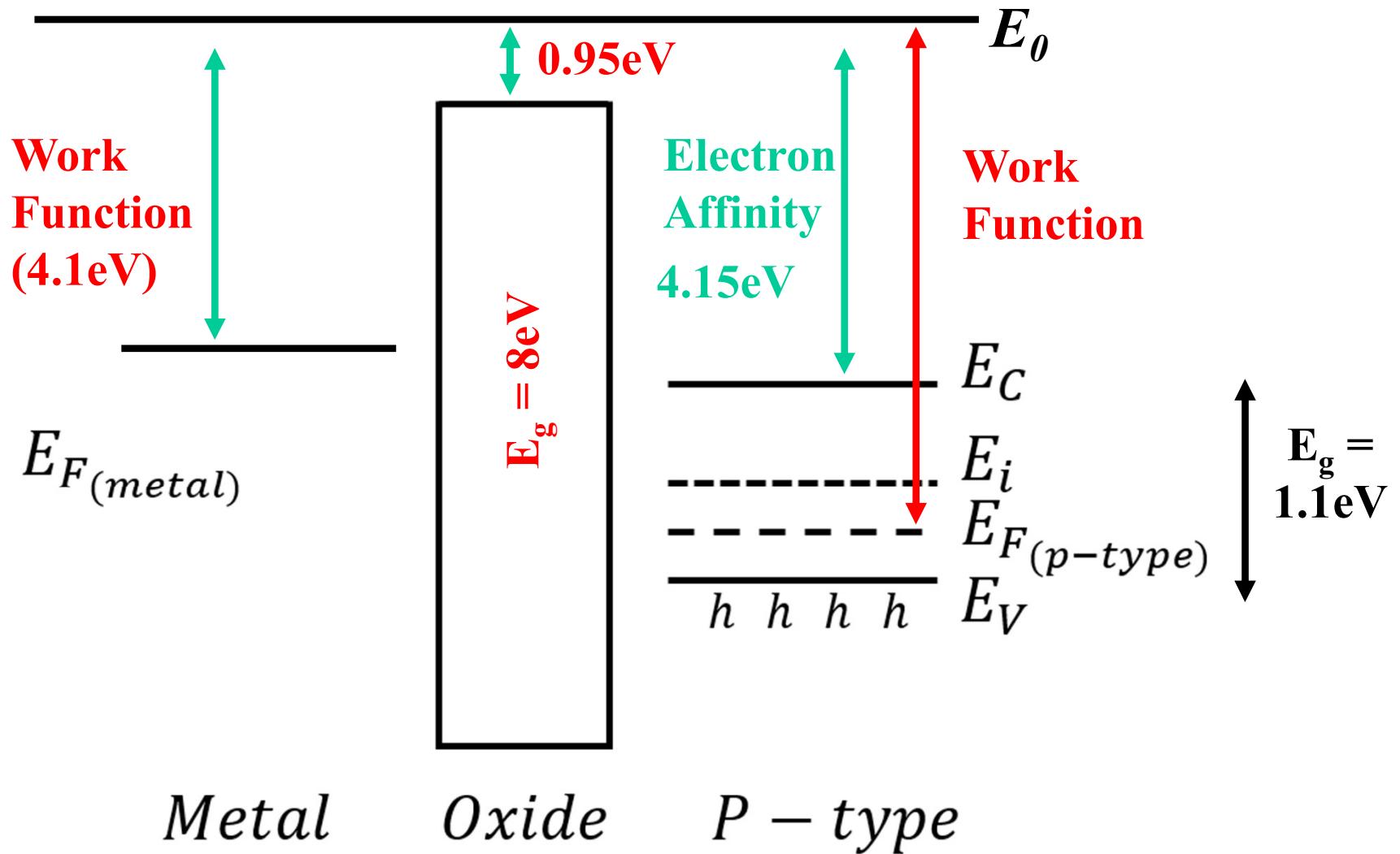
Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

- | | |
|----|--|
| 1. | Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3 rd Edition, Tata McGraw-Hill Publication, 2003. |
| 2. | J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits: A Design Perspective", 2 nd Edition, Pearson Education Inc., 2003. |
| 3. | Neil Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 3 rd Edition, Addison Wesley, 2005. |
4. D. A. Pucknell and K. Eshraghian, "*Basic VLSI Design*", PHI publication, 2009.
5. John P Uyemura, "*Introduction to VLSI Circuits and Systems.*" Wiley, 2002.

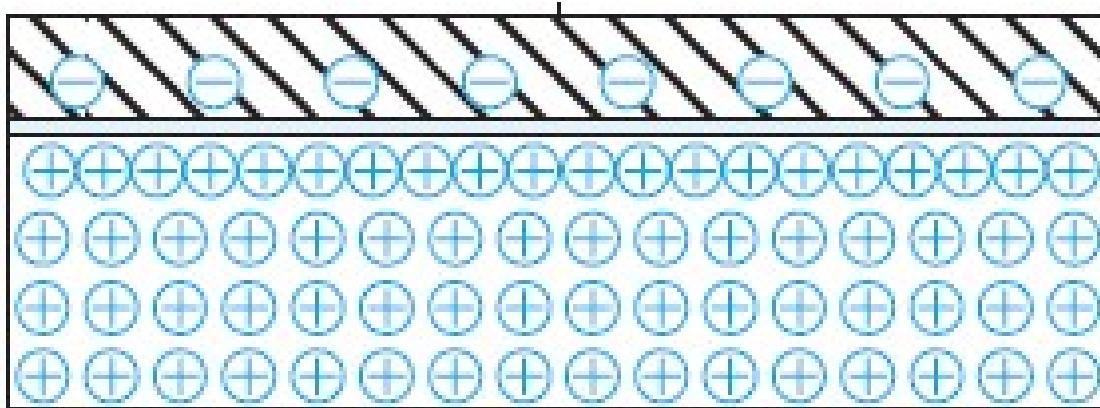
MOS: Metal-Oxide-Semiconductor



MOS Capacitor



MOS Capacitor

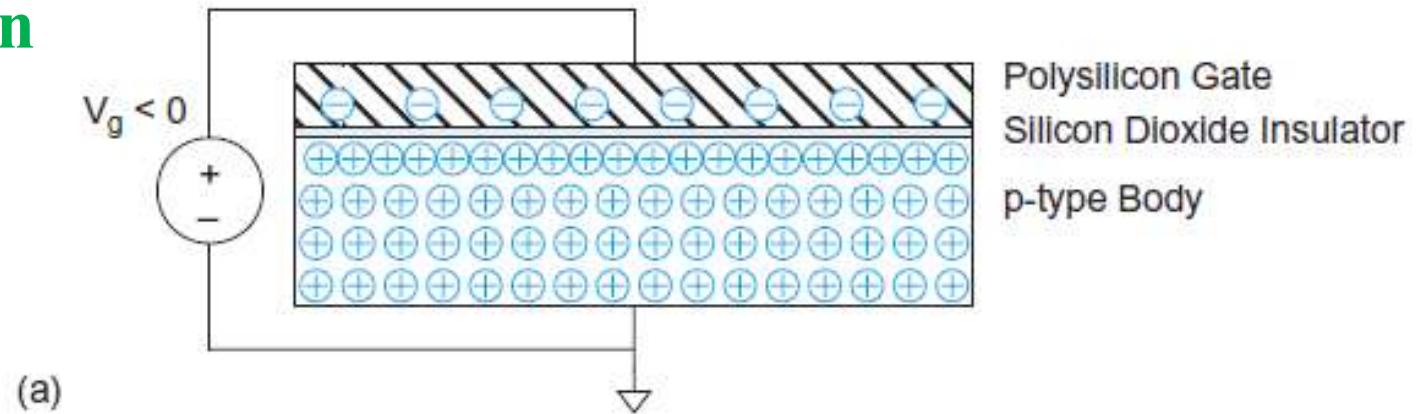


Oxide thickness, Threshold voltage, and Doping levels, depend on the fabrication process, and cannot be changed by design; they are technology parameters.

MOS Capacitor

$$C_g = \frac{\epsilon_{ox}}{t_{ox}}$$

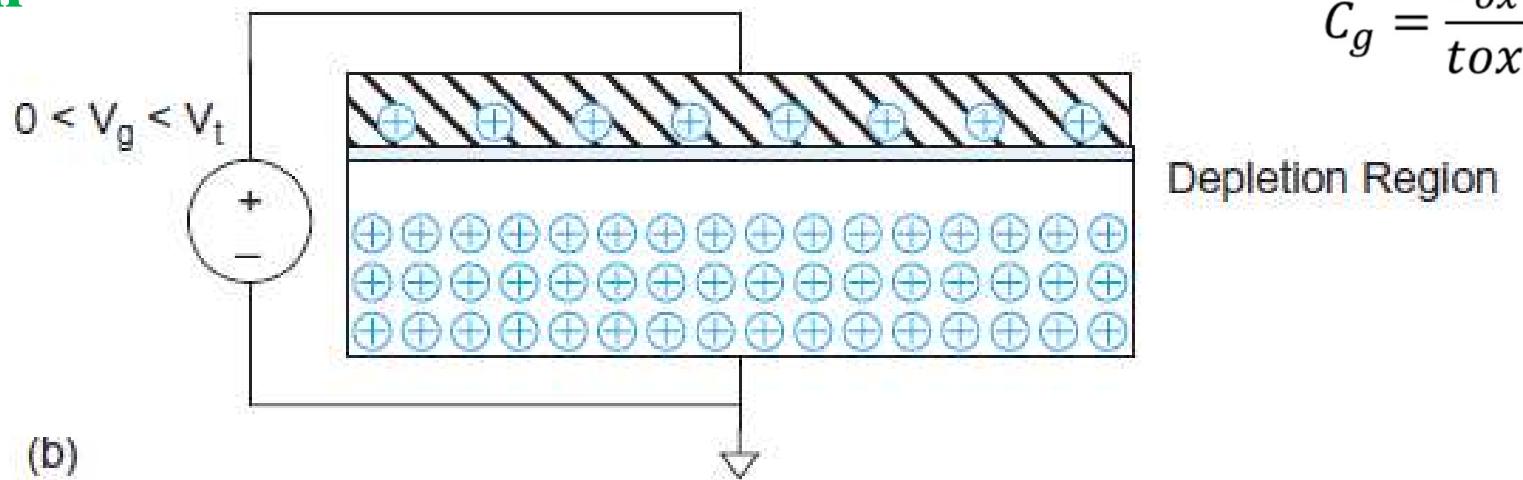
i. Accumulation



A negative voltage is applied to the gate, so there is negative charge on the gate. The mobile positively charged holes are attracted to the region beneath the gate. This is called the *accumulation* mode

MOS Capacitor

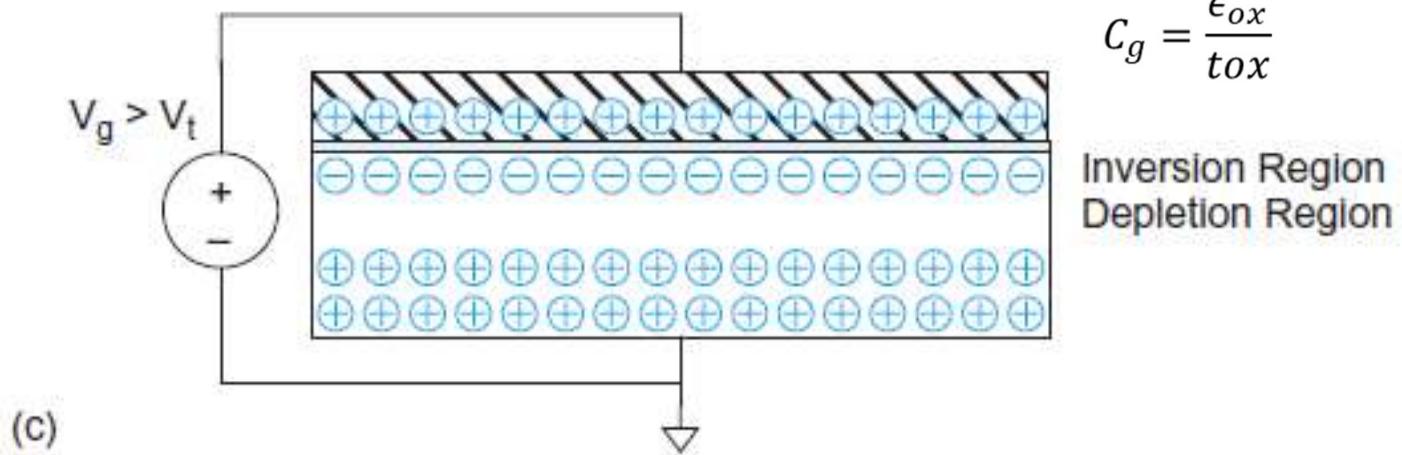
ii. Depletion



A small positive voltage is applied to the gate, resulting in some positive charge on the gate. The holes in the body are repelled from the region directly beneath the gate, resulting in a *depletion* region forming below the gate.

MOS Capacitor

iii. inversion

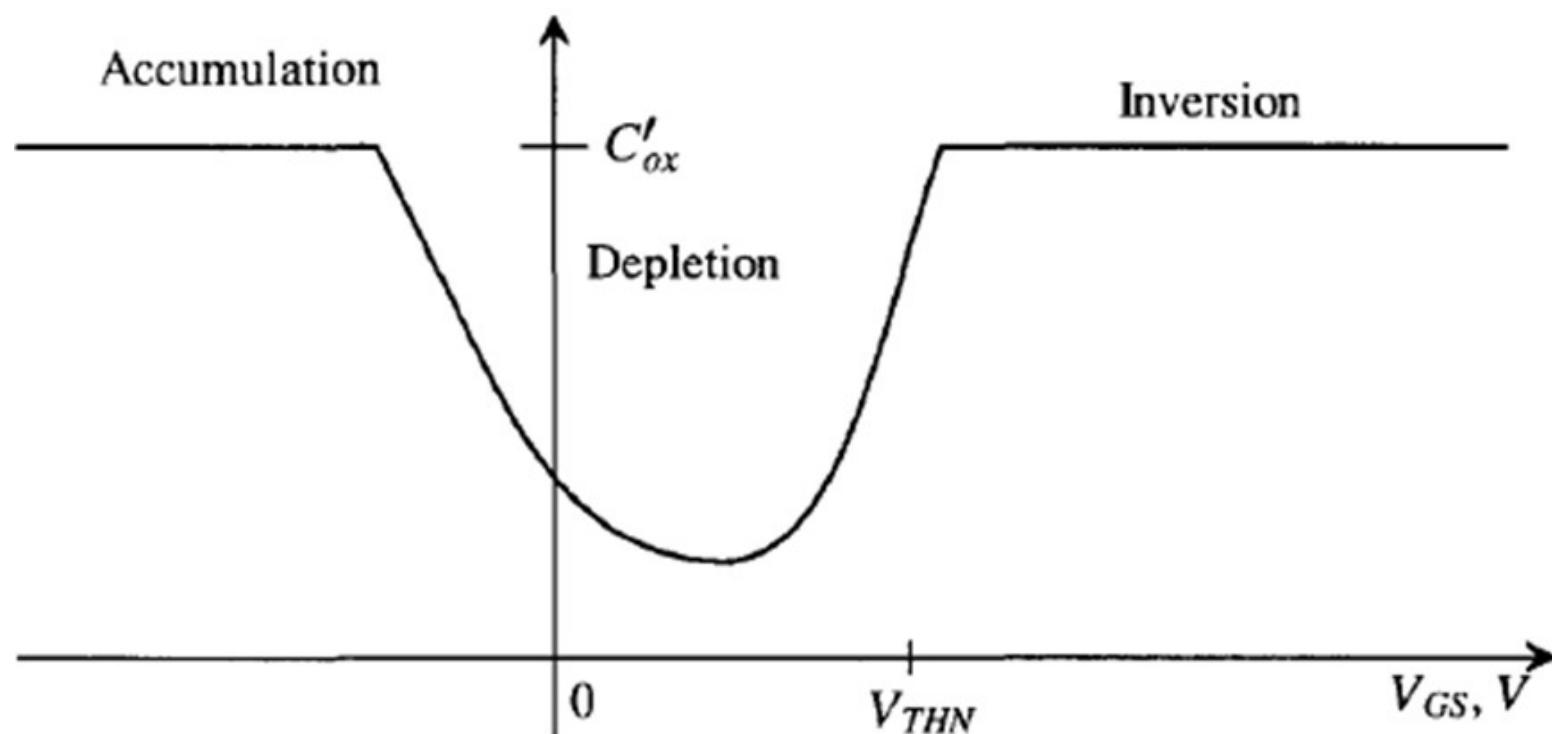


$$C_g = \frac{\epsilon_{ox}}{t_{ox}}$$

Inversion Region
Depletion Region

A higher positive potential exceeding a critical threshold voltage V_t is applied, attracting more positive charge to the gate. The holes are repelled further and some free electrons in the body are attracted to the region beneath the gate. This conductive layer of electrons in the p-type body is called the *inversion* layer

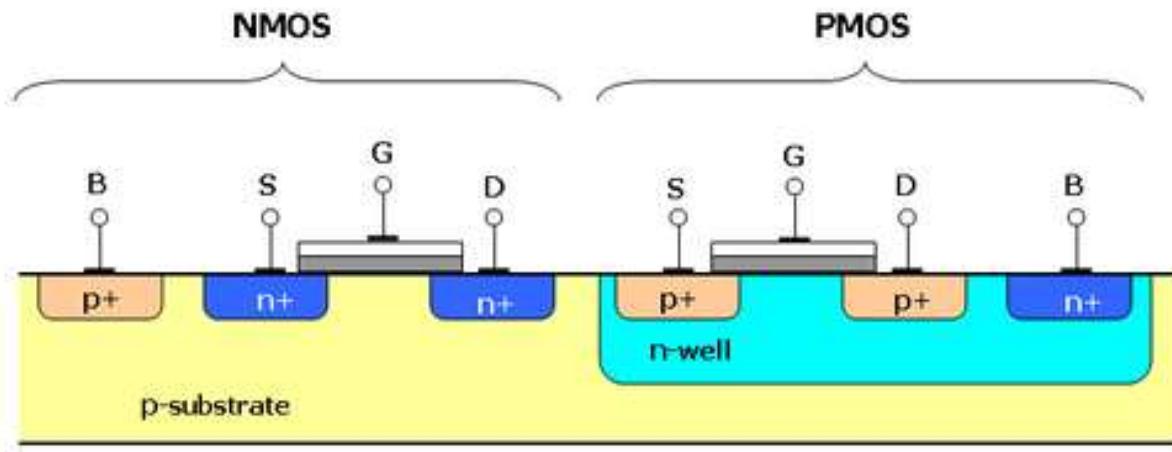
MOS Capacitor



MOSFET

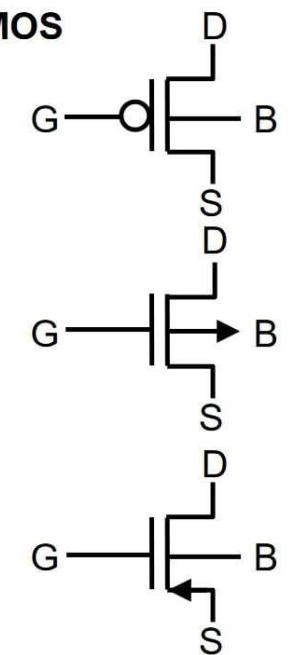
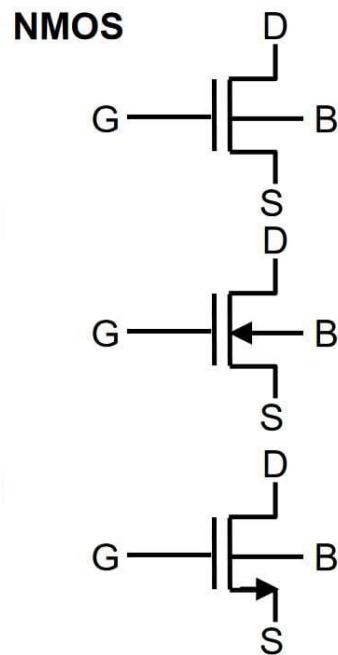
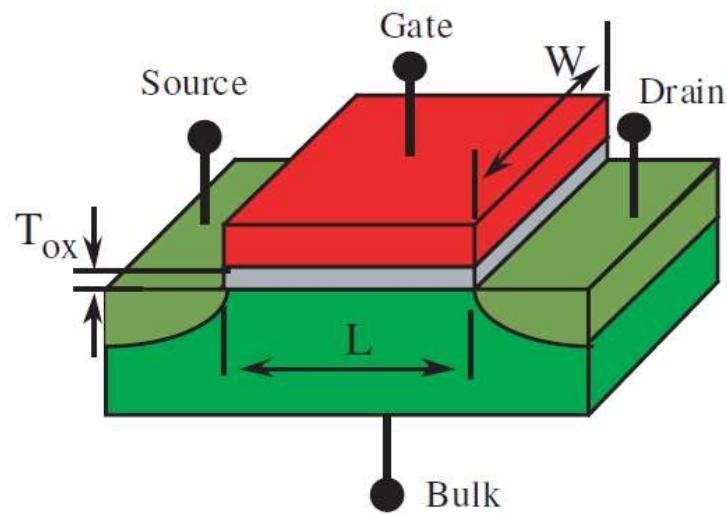
- Enhancement type MOSFET
 1. N-Channel MOSFET
 2. P-Channel MOSFET

Device Structure



- Depletion type MOSFET
 1. N-Channel MOSFET
 2. P-Channel MOSFET

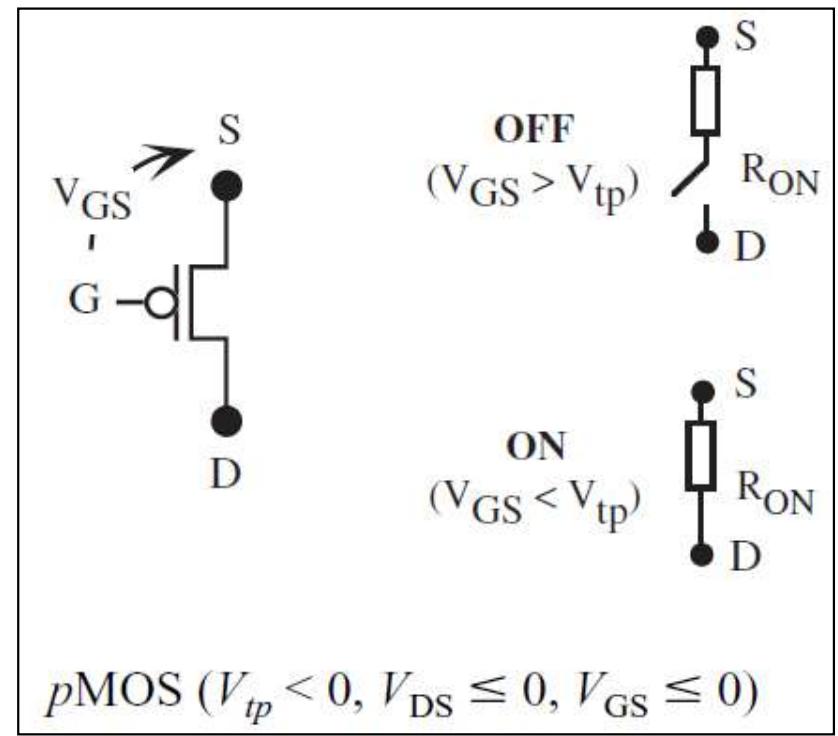
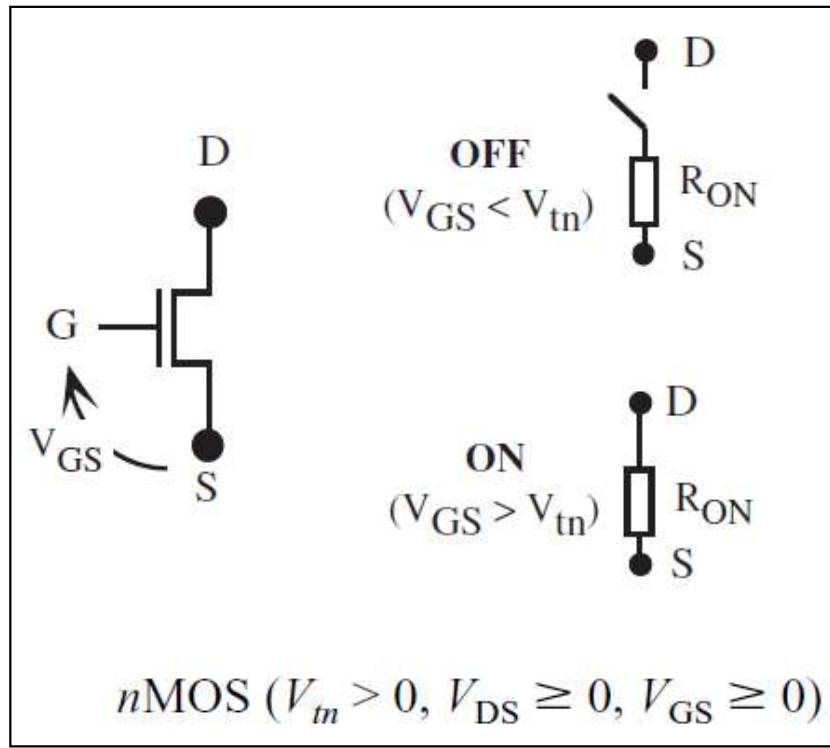
Enhancement MOSFET



$T_{ox} = 15\text{\AA}$ to 100\AA (Diameter of SiO_2 molecule is about 3.2\AA)

Arrows always point from P to N, so an NMOS (N-channel in P-well or P-substrate) has the arrow pointing in (from the bulk to the channel)

Enhancement MOSFET



V_{Th} is fixed for NMOS and PMOS devices for given fabrication process

Operation Of N-MOS Transistor

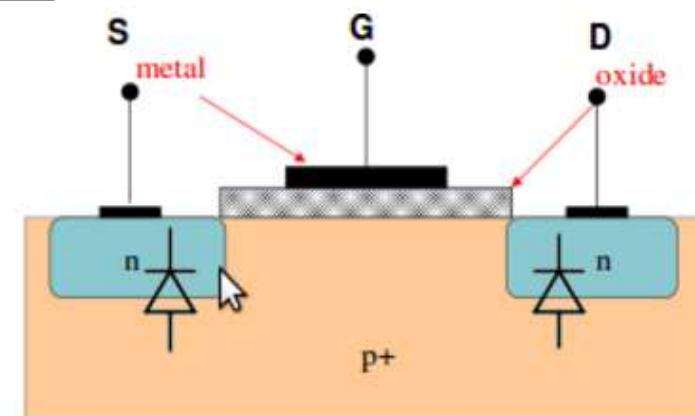
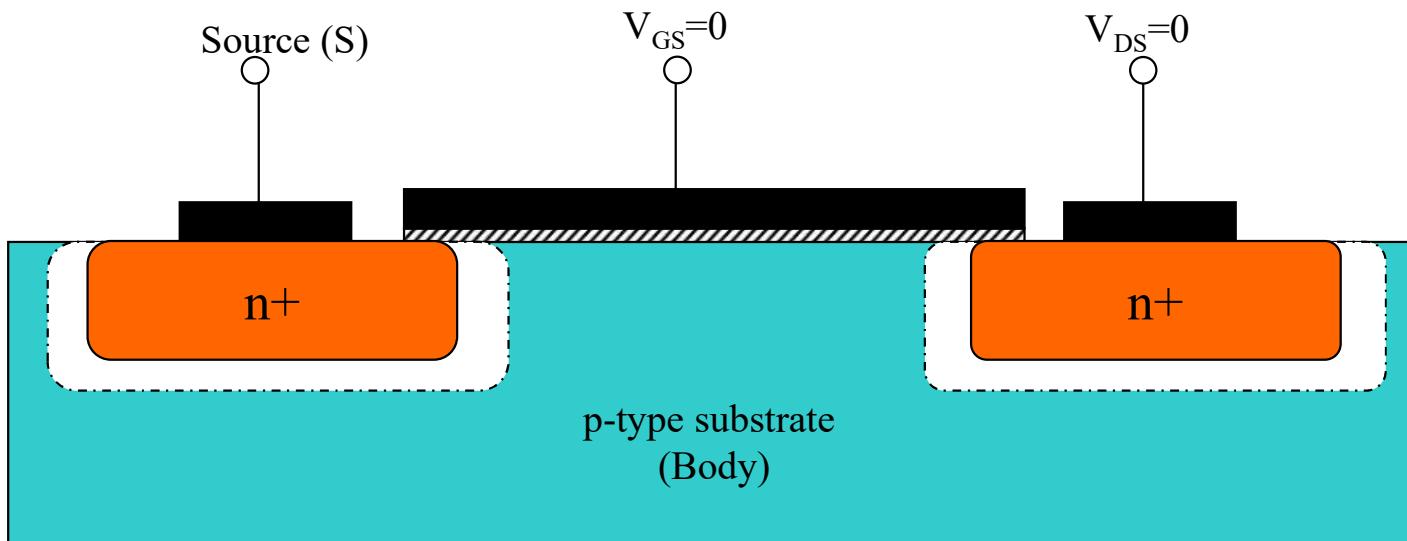
Depending on the relative voltages of the source, drain and gate, the NMOS transistor may operate in any of three regions viz :

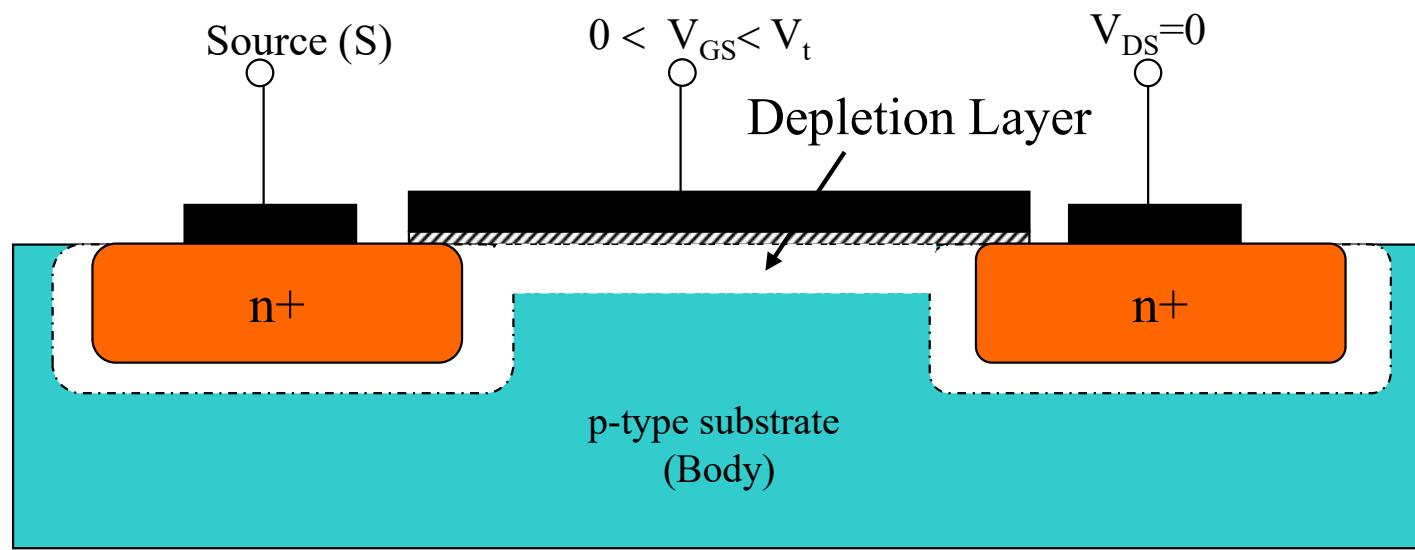
Cut off : Current flow is essentially zero (also called accumulation region)

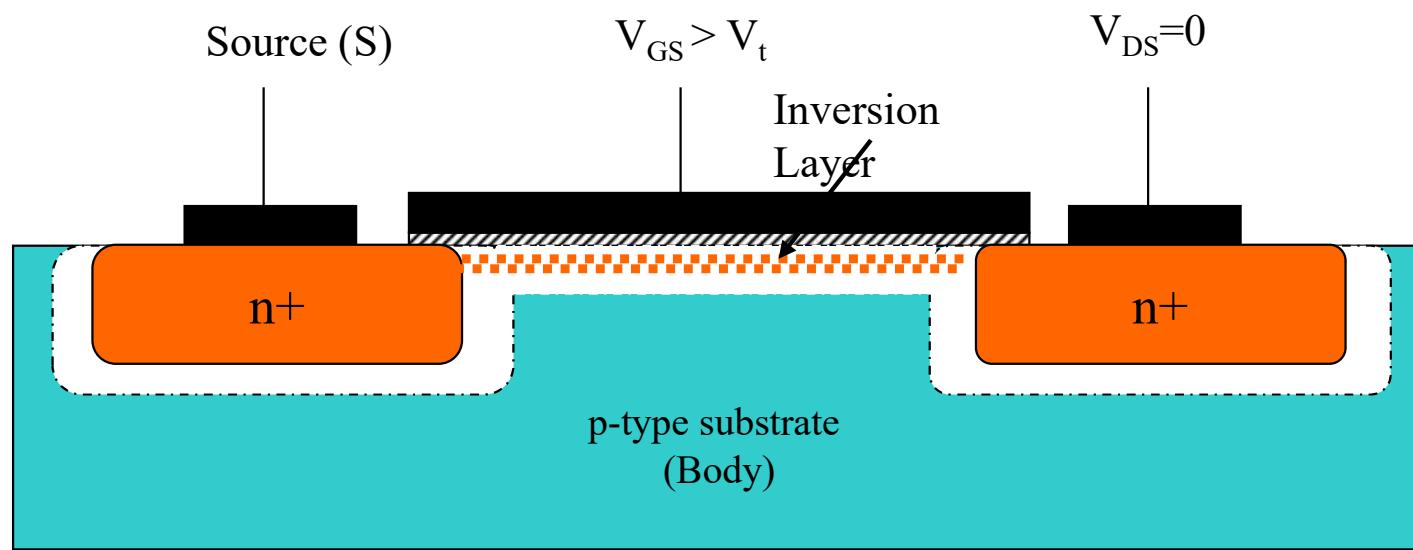
Linear :(Non saturated region)-It is weak inversion region drain current depends on gate and drain voltage.

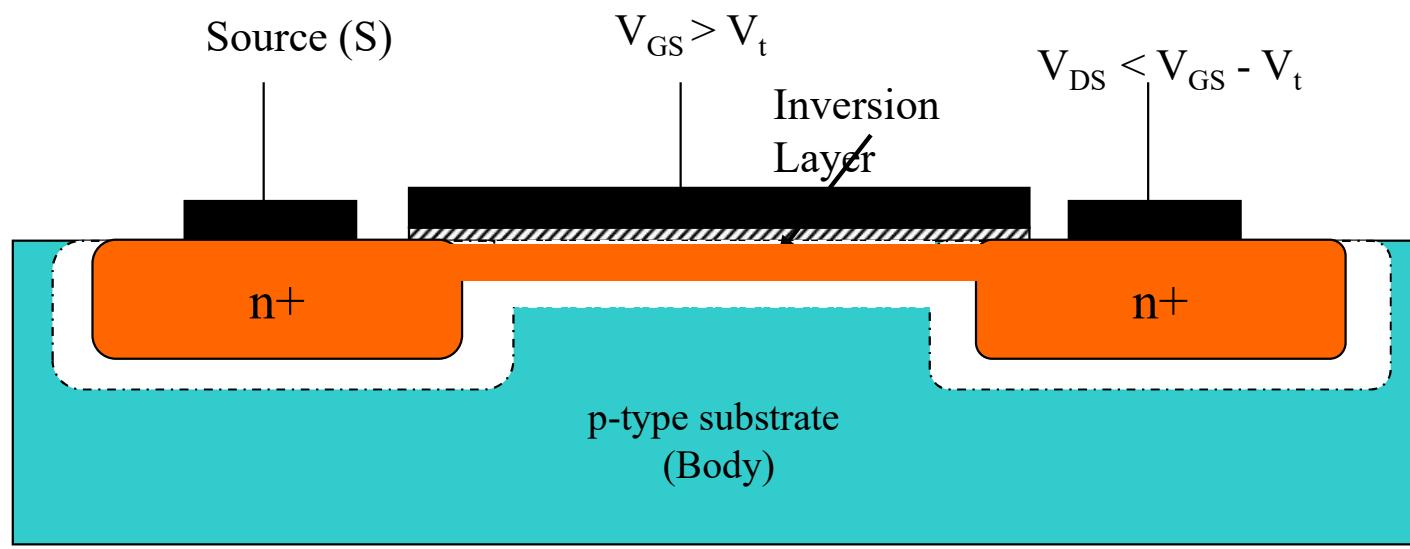
Saturation : It is strong inversion region where drain current is independent of drain-source voltage.

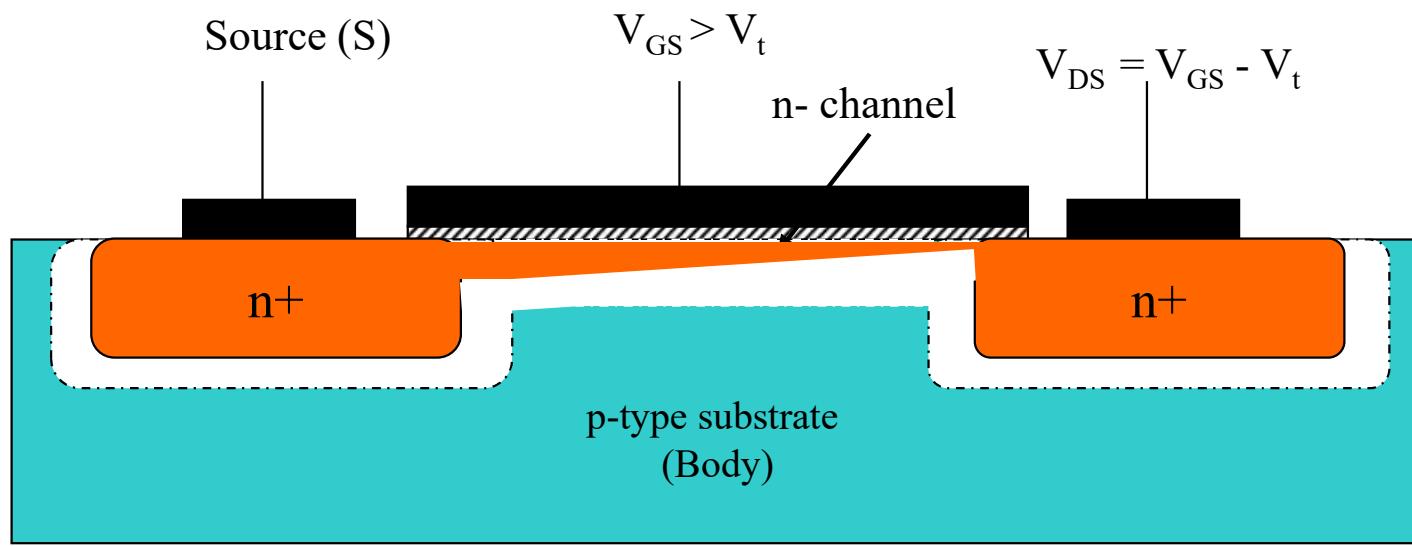
Cut-off Region



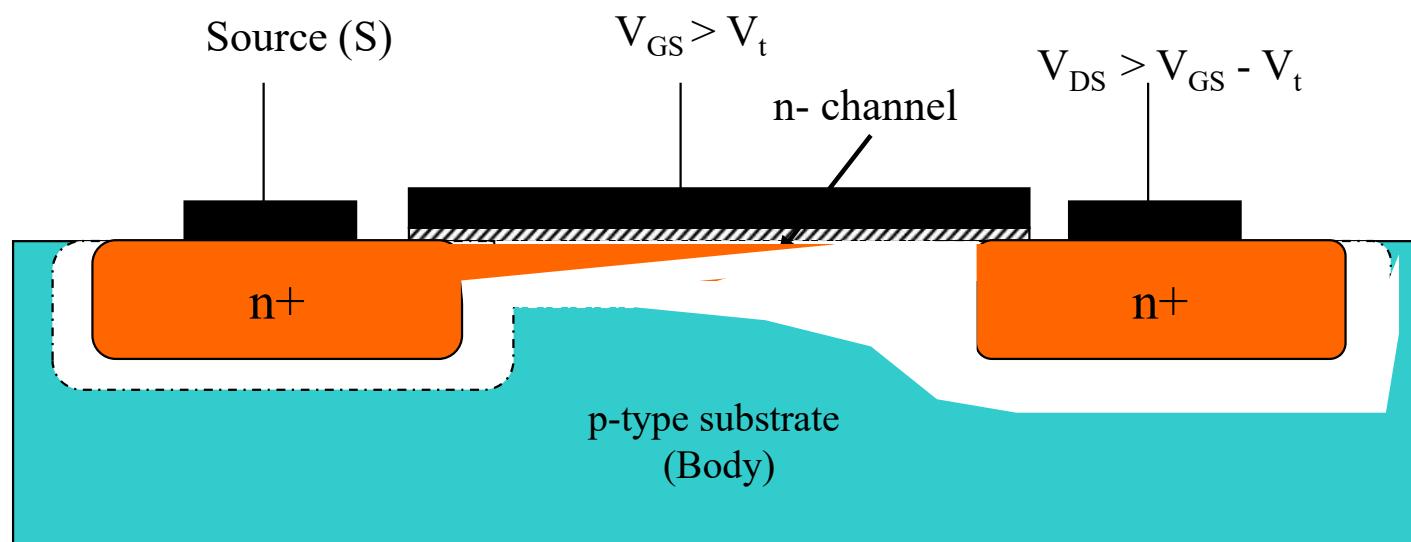








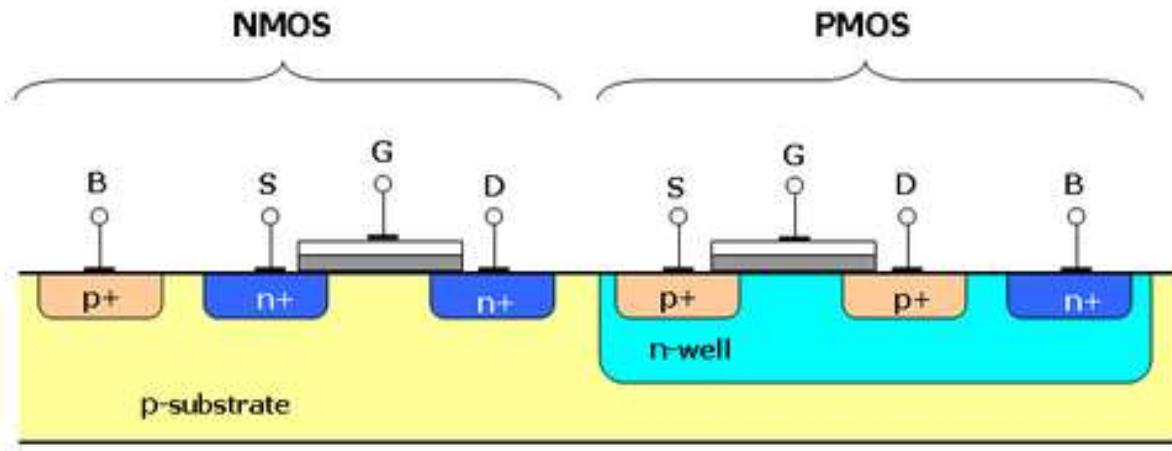
Saturation Region



MOSFET

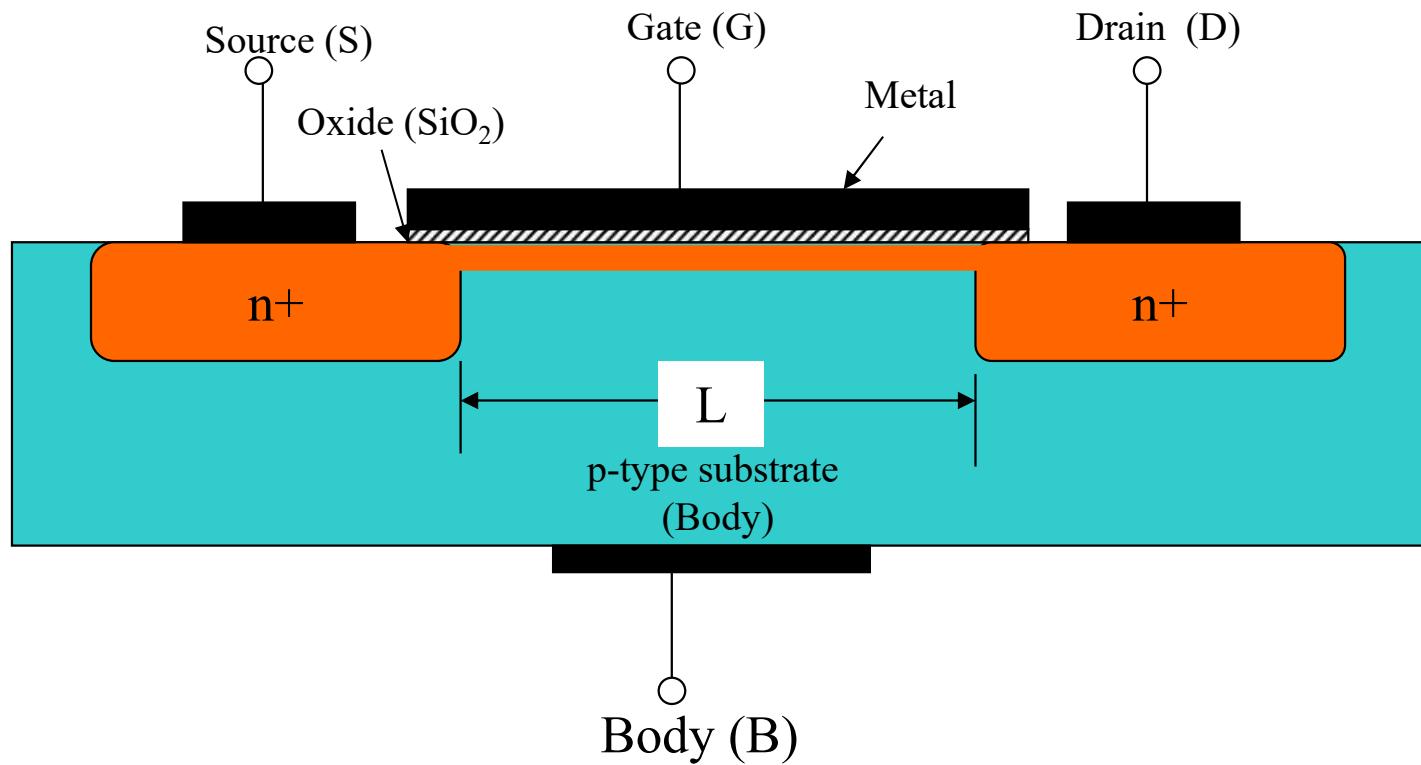
- Enhancement type MOSFET
 1. N-Channel MOSFET
 2. P-Channel MOSFET

Device Structure

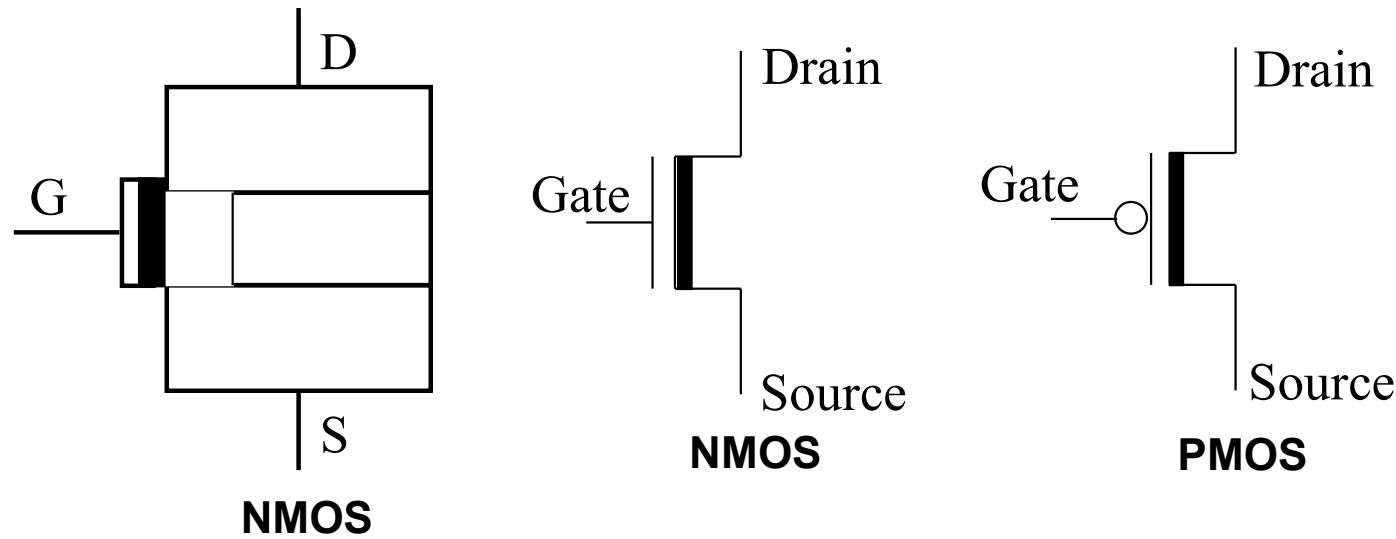


- Depletion type MOSFET
 1. N-Channel MOSFET
 2. P-Channel MOSFET

Depletion Type MOS

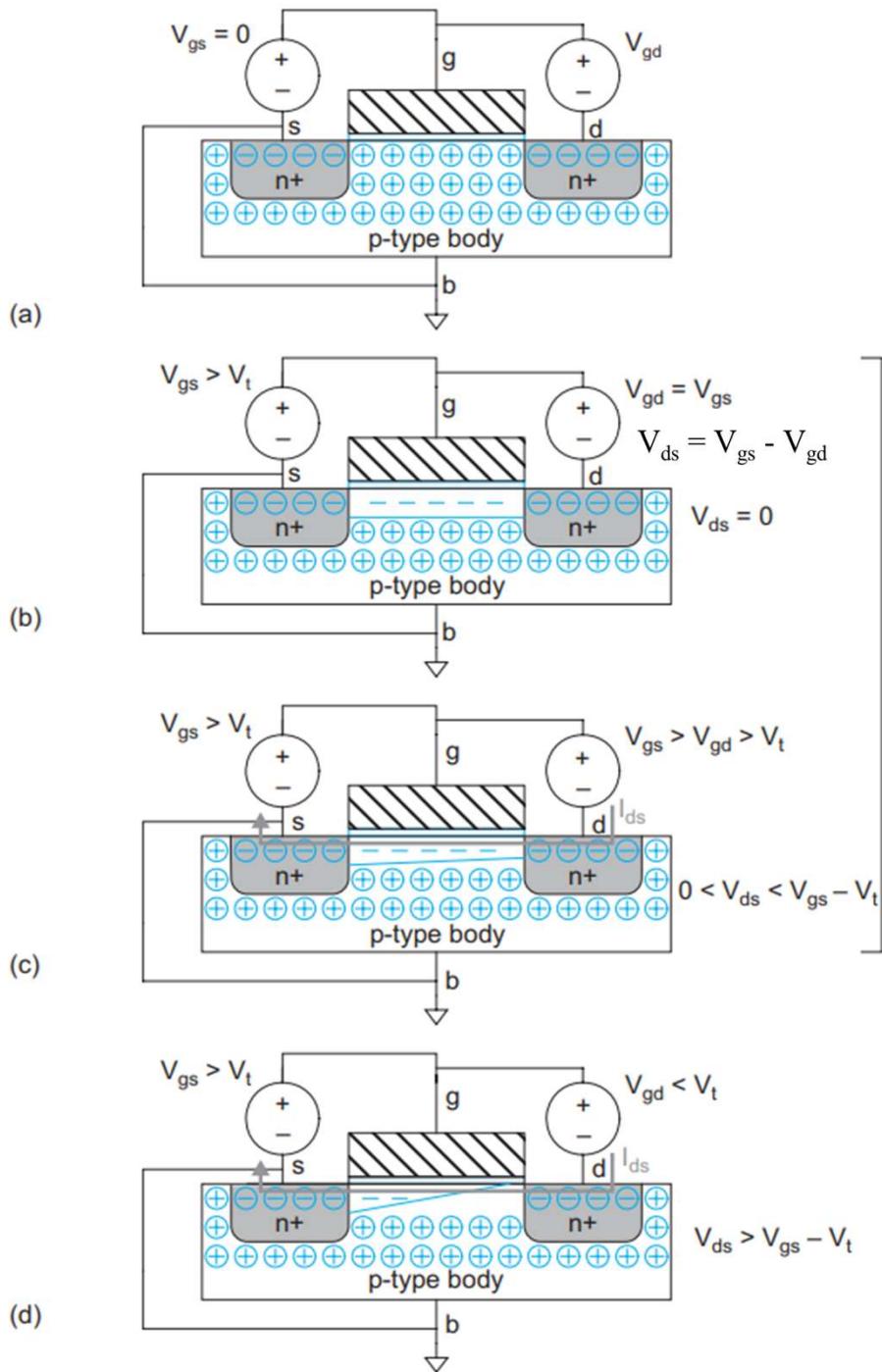


Depletion Type MOS



- In Depletion MOS structure, the source & drain are diffused on P-substrate.
- Positive voltages enhances number of electrons from source to drain.
- Negative voltage applied to gate reduces the drain current
- This is called as ‘ normally ON ’ MOS.

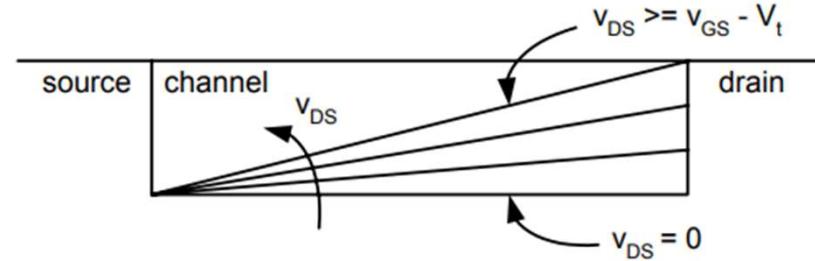
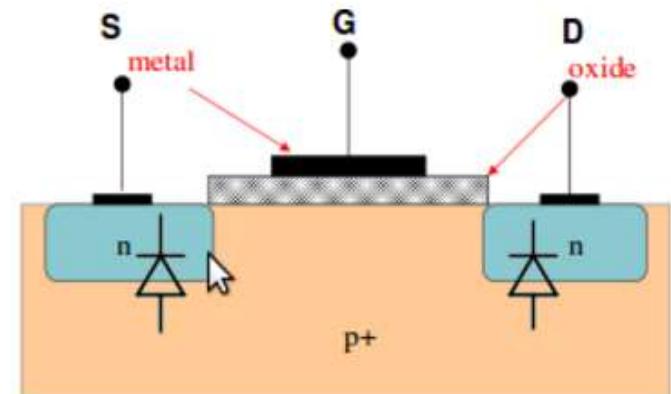
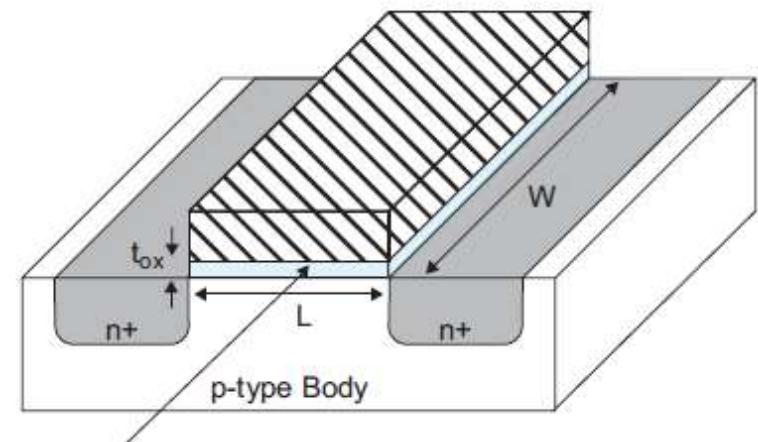
N-MOS Structure



Cutoff:
No Channel
 $I_{ds} = 0$

Linear:
Channel Formed
 I_{ds} Increases with V_{ds}

Saturation:
Channel Pinched Off
 I_{ds} Independent of V_{ds}



Current Equations

$$I_{ds} = \frac{C_{ox}\mu W}{L} \left((V_{GS} - V_T) - \frac{V_{DS}}{2} \right) V_{DS}$$

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

β

$$I_{ds} = \frac{C_{ox}\mu W}{2L} (V_{GS} - V_T)^2$$

Linear Operating region

$$V_{gs} > V_t$$

$$V_{ds} < V_{gs} - V_t$$

Saturation Operating region

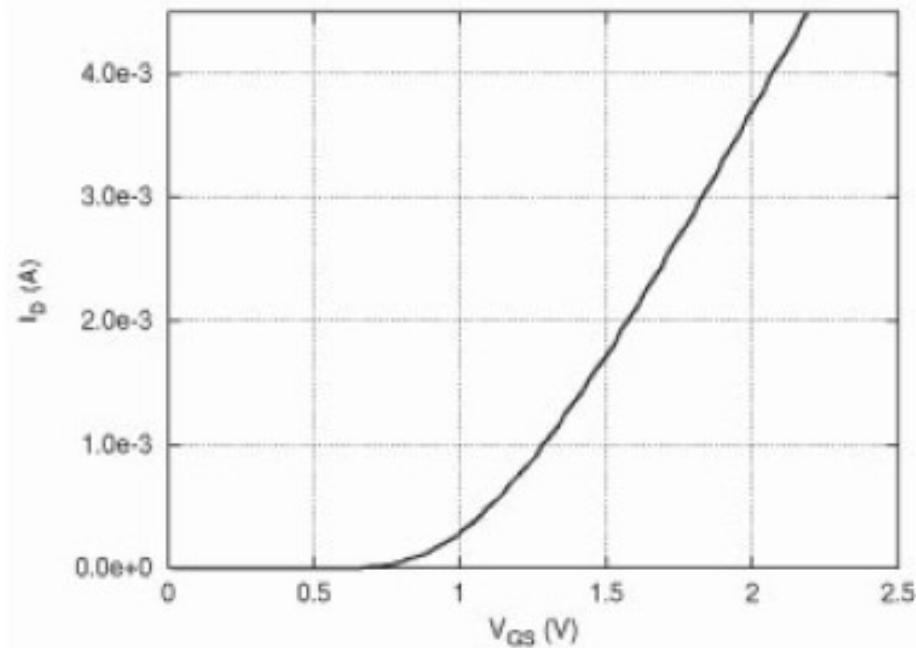
$$V_{gs} > V_t$$

$$V_{ds} \geq V_{gs} - V_t$$

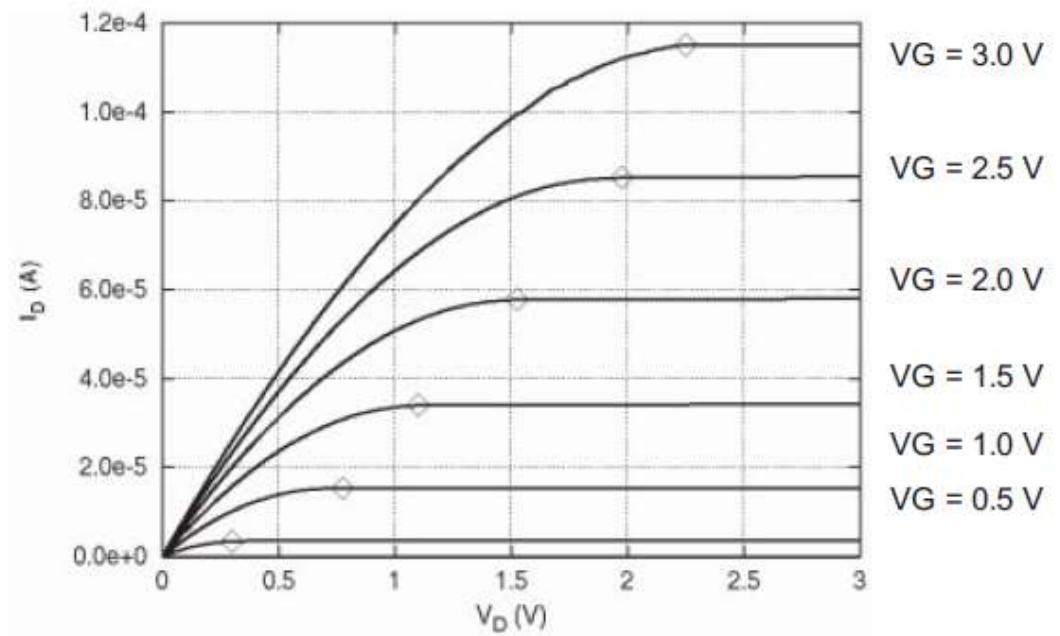
Important Observations

- The bulk or substrate of *n*MOS transistors must always be connected to the lower voltage that is the reference terminal.
- The positive convention current in an *n*MOS device is from the drain to the source, and is referred to as I_{DS} or just I_D , since drain and source current are equal.
- When a positive voltage is applied to the drain terminal, the drain current depends on the voltage applied to the gate control terminal.

I/O Characteristics

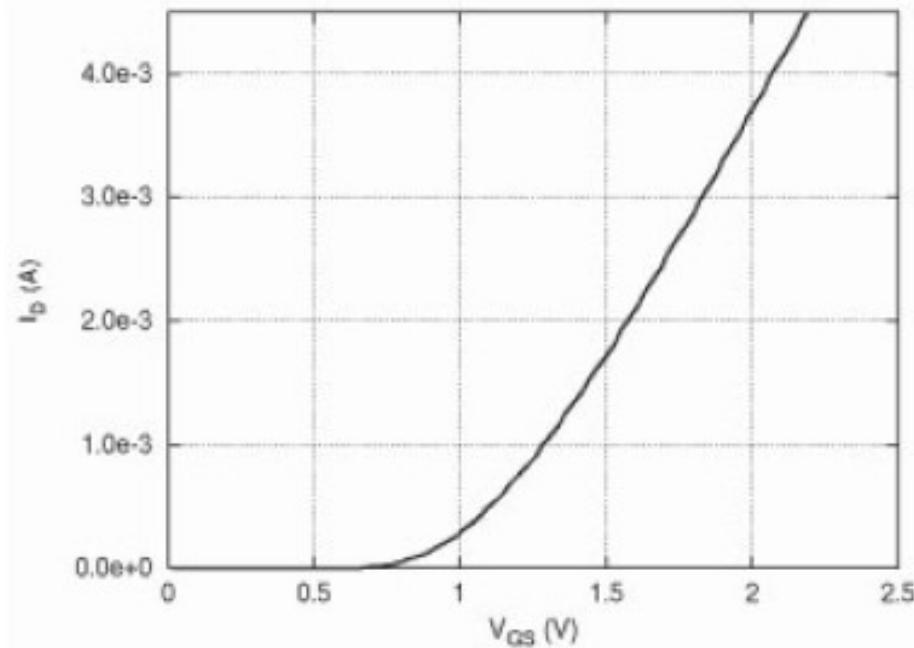


input characteristics (I_D vs. V_{GS})
for an *n*MOS,

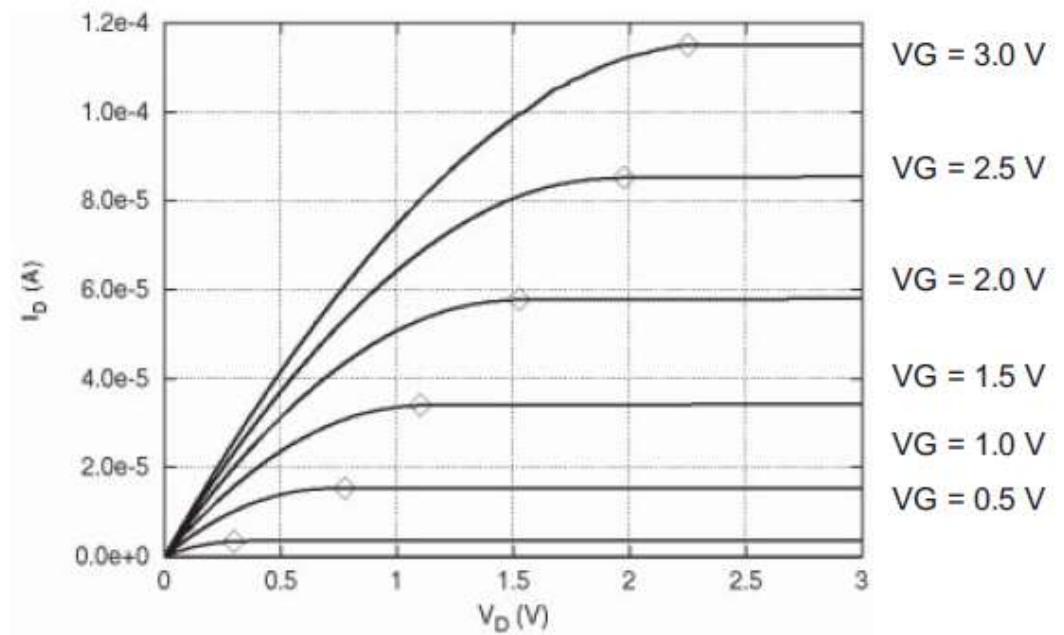


*n*MOS transistor output
characteristics

I/O Characteristics - NMOS



input characteristics (I_D vs. V_{GS})
for an *n*MOS,



*n*MOS transistor output
characteristics

NMOS Threshold Voltage

$$V_t = V_{t0} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

V_{t0} is the threshold voltage when the source is at the body potential.

ϕ_s is the *surface potential* at threshold

γ is the *body effect coefficient*

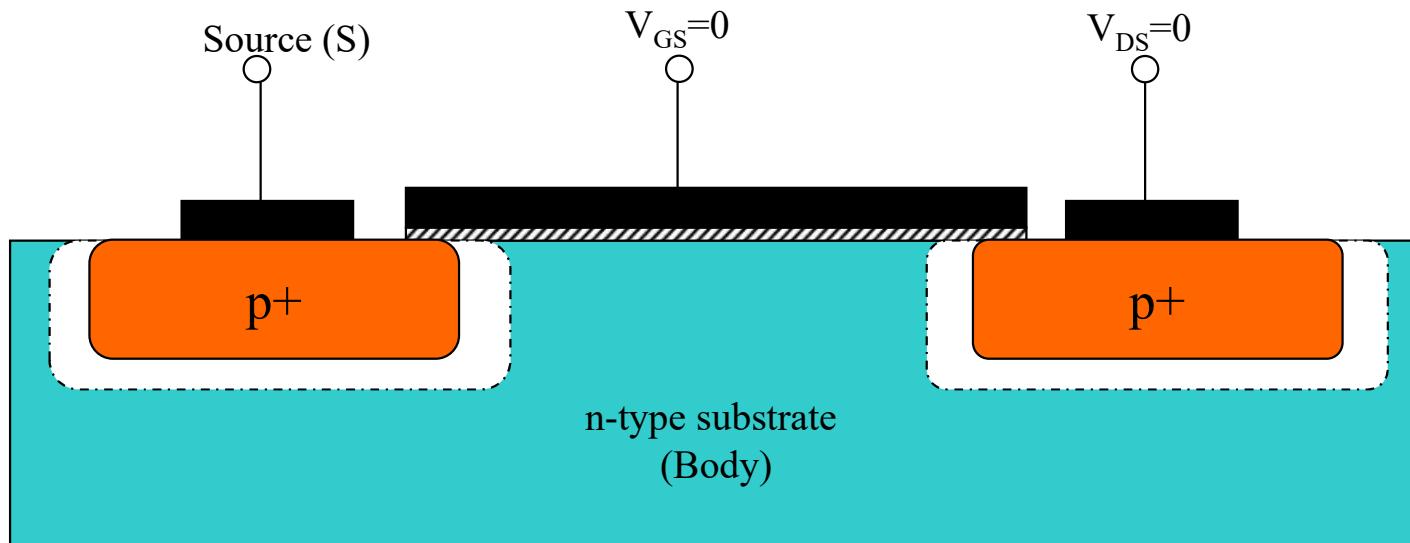
$$\gamma = \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \sqrt{2q\epsilon_{\text{si}}N_A} = \frac{\sqrt{2q\epsilon_{\text{si}}N_A}}{C_{\text{ox}}} \quad \text{and}$$

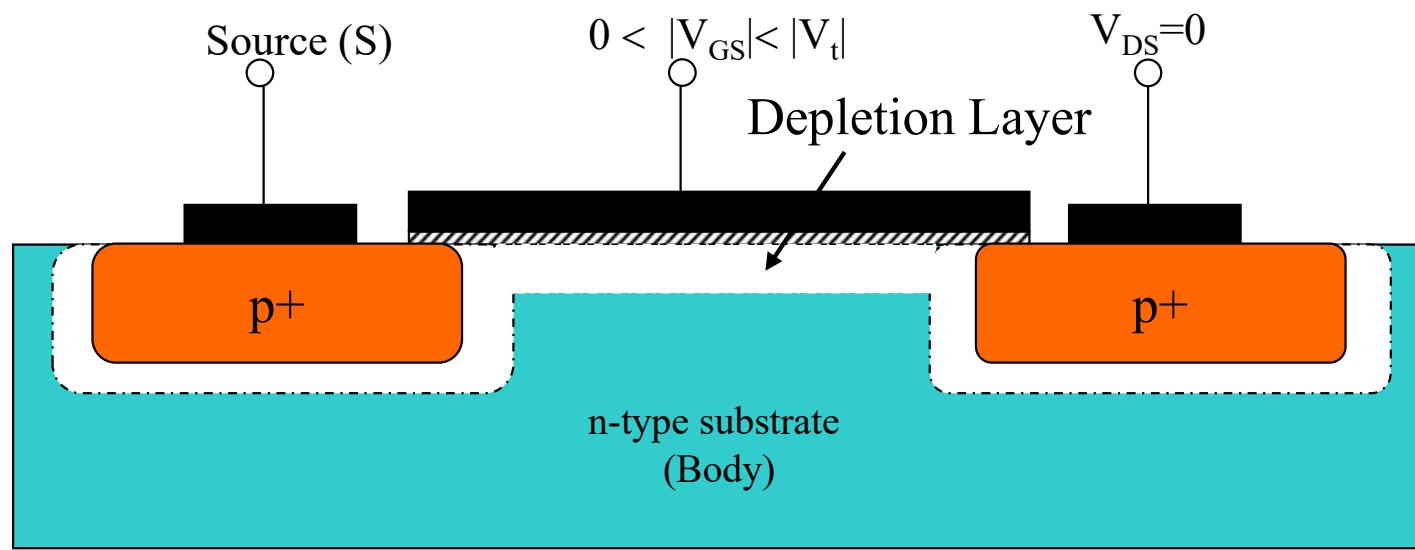
$$\phi_s = 2v_T \ln \frac{N_A}{n_i}$$

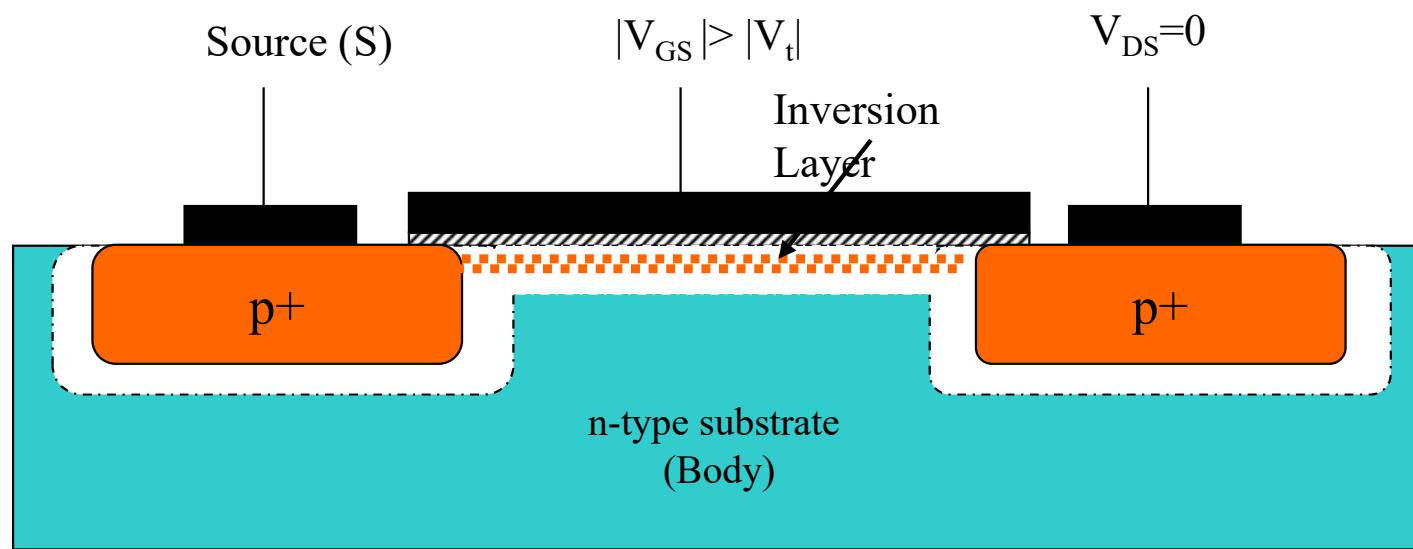
v_T is thermal voltage, which is around 26mV at room temperature.

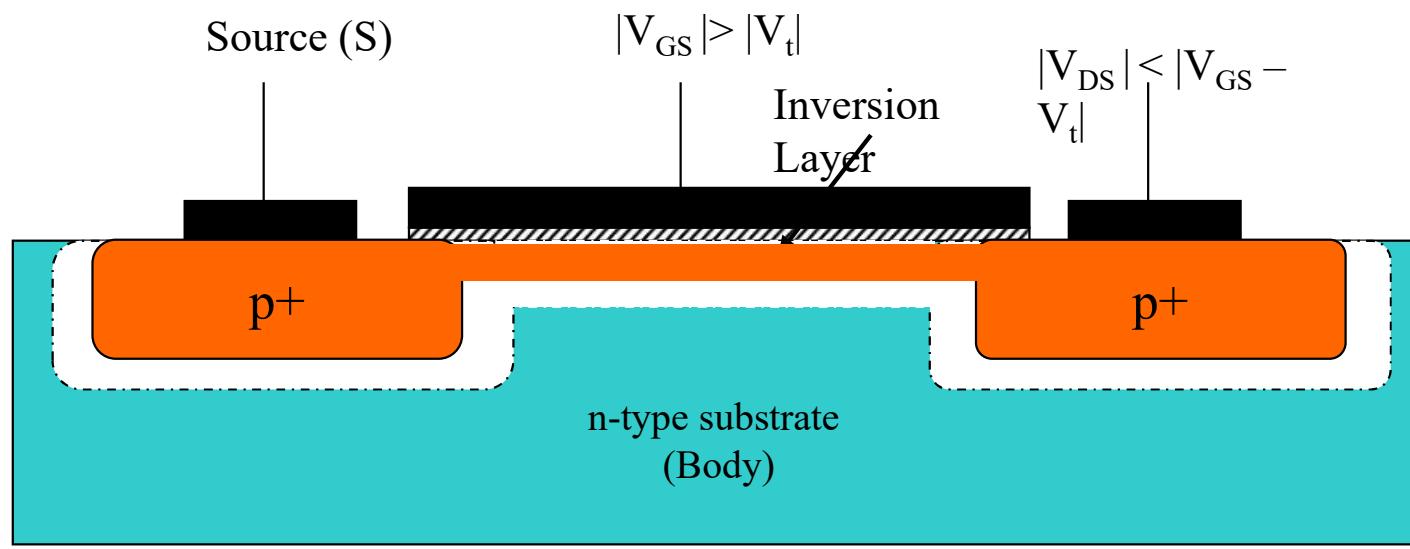
Enhancement PMOS Transistor

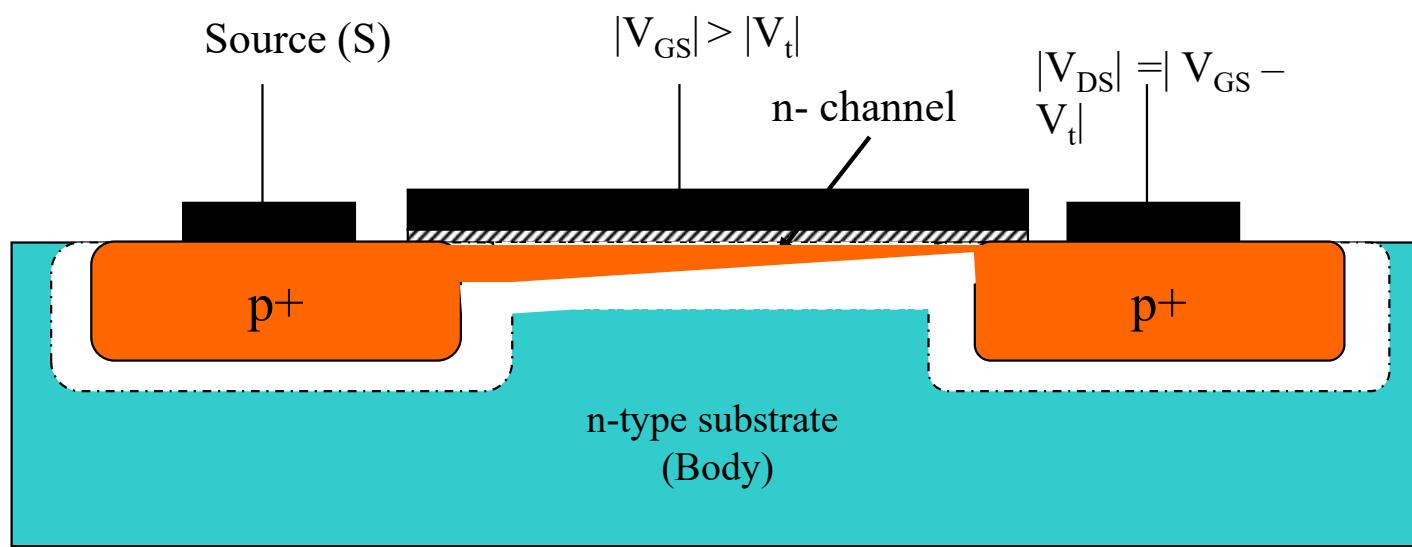
Cut-off Region



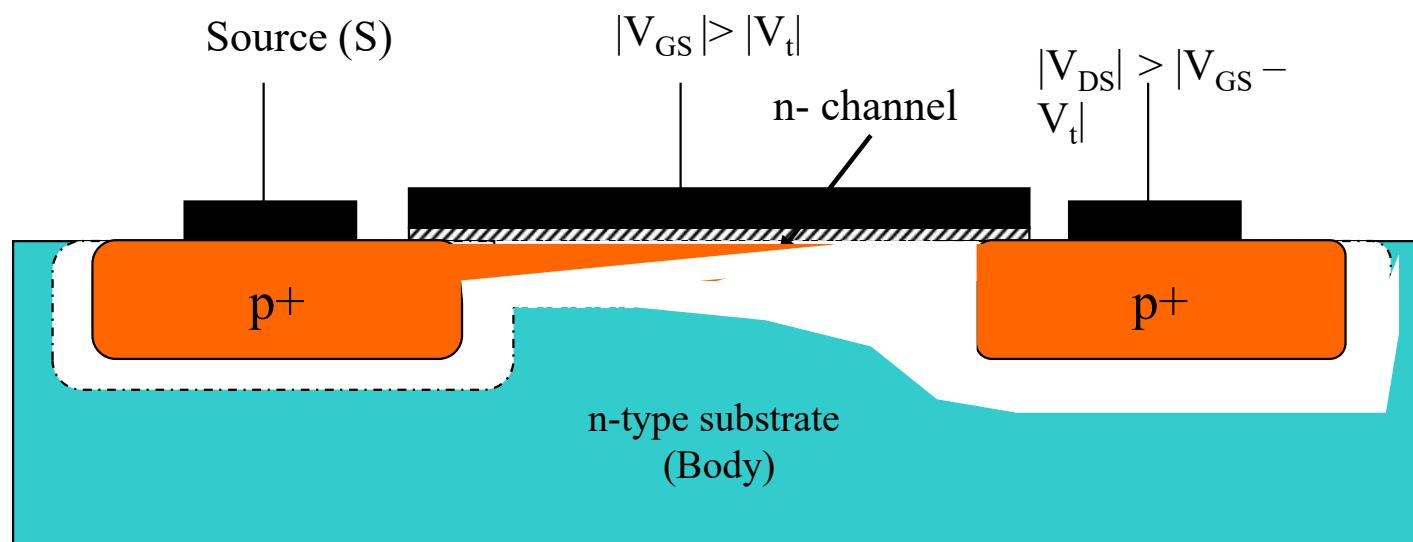




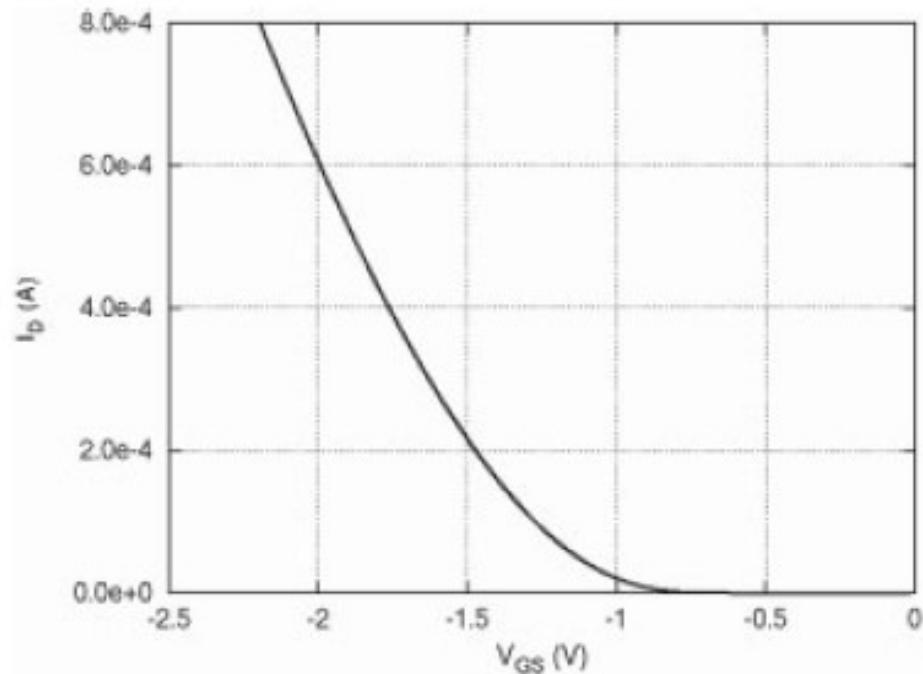




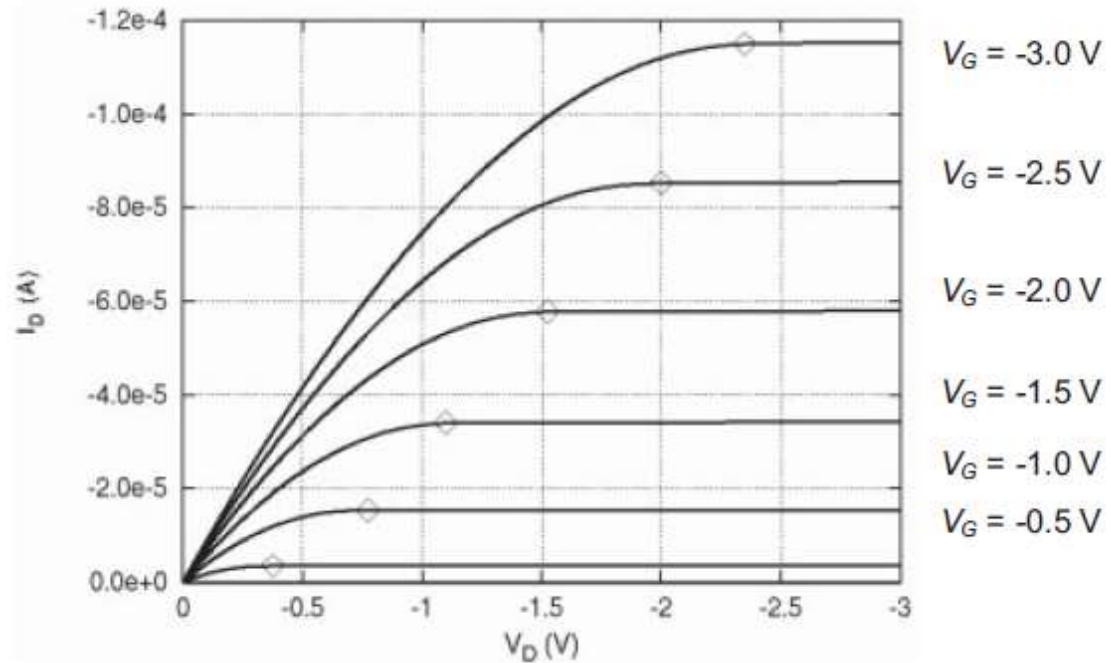
Saturation Region



I/O Characteristics



Input characteristics (I_D vs. V_{GS})
for an *p*MOS,



*p*MOS transistor output
characteristics

Examples:

1. Consider an n-MOSFET that has a gate oxide thickness $t_{ox}=12$ nm and an electron mobility of $\mu_n=540 \text{ cm}^2/\text{V}\cdot\text{sec}$. Find the process transconductance.
2. An n-MOSFET with $W=20 \mu\text{m}$ and $L=0.5 \mu\text{m}$ is built in a process where $K'_n=120 \mu\text{A}/\text{V}^2$ and $V_{Tn}=0.65 \text{ V}$. The voltages are set to a value of $V_{GS} = V_{DS} = 5 \text{ V}$.
 - (a) Is the transistor saturated or non-saturated?
3. Consider an n-MOSFET with the following characteristics:
 $t_{ox}=10 \text{ nm}$, $\mu_n=520 \text{ cm}^2/\text{V}\cdot\text{sec}$, $W/L=8$, $V_{Tn}=0.7 \text{ V}$
 - (a) Calculate the drain current for $V_{GS}=2 \text{ V}$, $V_{DS}= 2 \text{ V}$.
 - (b) If the voltage values are $V_{DS}=1.2 \text{ V}$ and $V_{GS}=2 \text{ V}$, find the operating region and current
4. Consider an n-MOSFET where $V_{Ton}=0.7 \text{ V}$, $\gamma=0.08 \text{ V}^{1/2}$ and $2|\Phi_F|=0.58 \text{ V}$. Calculate the threshold voltage for the given body-bias voltage $V_{SB} = 1 \text{ V}, 2 \text{ V}$ and 3 V .
5. An n-MOSFET has a gate oxide with a thickness of $t_{ox}=120 \text{ \AA}$. The p-type bulk region is Doped with boron at a density of $N_a=8\times10^{14} / \text{cm}^3$. It is given that $V_{Ton}=0.55 \text{ V}$. Calculate the body-bias coefficient γ .

Examples:

SOLUTION 1 \Rightarrow

$$t_{ox} = 12 \text{ nm}$$

$$= 12 \times 10^{-7} \text{ cm}$$

$$m_n = 540 \text{ cm}^2/\text{V-sec}$$

$$\epsilon_{Si} = 11.7 \epsilon_0$$

$$k_n = m_n C_{ox} \Rightarrow k_n = 540 \times \frac{\epsilon_{SiO_2}}{t_{ox}}$$

$$\epsilon_{SiO_2} = 3.97 \epsilon_0$$

$$\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$$

$$\Rightarrow k_n = 540 \text{ cm}^2/\text{V-sec} \left(\frac{3.97 \times 8.85 \times 10^{-14} \text{ F/cm}}{12 \times 10^{-7} \text{ cm}} \right)$$

$$\Rightarrow k_n = \left(\frac{540 \times 3.97 \times 8.85}{12} \right) \times 10^{-7} \text{ A/V}^2$$

$$\Rightarrow k_n = 158.1 \text{ mA/V}^2$$

SOLUTION 2 \Rightarrow Since $V_{GS} = V_{DS}$ so it is in Saturation.

Examples:

SOLUTION $\div 3 \Rightarrow$

$$K_n = \mu_n C_{ox}$$

$$= \left(\frac{520 \times 3.97 \times 8.85 \times 10^{-14}}{10 \times 10^{-7}} \right)$$

$$= 182.7 \text{ } \mu\text{A/V}^2$$

$$\mu_n = 520 \text{ cm}^2/\text{V}\cdot\text{sec}$$

$$C_{ox} = 10 \text{ nF} \\ = 10 \times 10^{-9} \text{ F}$$

$$W/L = 8$$

$$V_{Tn} = 0.7 \text{ V}$$

④ $V_{GS} = 2 \text{ V}$; $V_{DS} = 2 \text{ V}$

Since MOS is in Saturation hence

$$\begin{aligned} I_{DS} &= \frac{K_n (W/L)}{2} [V_{GS} - V_T]^2 \\ &= 182.7 \times 10^{-6} \text{ A/V}^2 \left(\frac{8}{2}\right) [2 - 0.7]^2 \\ &= (730.8)(1.3)^2 \times 10^{-6} \\ &= 1235.05 \times 10^{-6} \text{ A} \\ &= 1.235 \text{ mA} \end{aligned}$$

Examples:

⑥ $V_{DS} = 1.2V$ $V_{GS} = 2V$ \Rightarrow MOS is in linear region

So,

$$I_{DS} = K_n (W/L) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= 182 \cdot 7 \times 10^{-6} \cdot 4 \left[(2 - 0.7) \cdot 1.2 - \frac{(1.2)^2}{2} \right]$$

$$= 730.8 \times 10^{-6} \left[1.56 - 0.72 \right]$$

$$= 730.8 \times 0.84 \times 10^{-6}$$

$$= 613.872 \times 10^{-6} A$$

$$= 0.614 mA$$

Examples:

SOLUTION ÷ 4 ÷

$$V_{T0,n} = 0.7 \text{ V}$$

$$\gamma = 0.08 \text{ V}^{1/2}$$

$$2|\phi_f| = 0.58 \text{ V}$$

$$V_T = V_{T0,n} + \gamma \left[\sqrt{0.58 + V_{SB}} - \sqrt{0.58} \right]$$

for different value of V_{SB}

$$\begin{aligned} V_T (V_{SB}=1\text{V}) &= 0.7 + 0.08 \left[\sqrt{0.58+1} - \sqrt{0.58} \right] \\ &= 0.7 + 0.08 \left[\sqrt{1.58} - \sqrt{0.58} \right] \\ &= 0.7396 \end{aligned}$$

$$\begin{aligned} V_T (V_{SB}=2\text{V}) &= 0.7 + 0.08 \left[\sqrt{0.58+2} - \sqrt{0.58} \right] \\ &= 0.7676 \end{aligned}$$

$$\begin{aligned} V_T (V_{SB}=3\text{V}) &= 0.7 + 0.08 \left[\sqrt{0.58+3} - \sqrt{0.58} \right] \\ &= 0.7904 \end{aligned}$$

Examples:

(2)

SOLUTION 5 :-

$$t_{ox} = 120 \text{ \AA}$$

$$N_A = 8 \times 10^{14} / \text{cm}^3$$

$$V_{T0,n} = 0.55 \text{ V}$$

Since

$$\gamma = \frac{\sqrt{2q N_A \epsilon_s}}{C_{ox}}$$

$$C_{ox} = \frac{0.377 \times 8.85 \times 10^{-14}}{120 \times 10^{-8}}$$

$$= 0.293 \times 10^{-6} \text{ F/cm}^2$$

$$= \frac{\sqrt{2 \times 1.6 \times 10^{-19} \times 8 \times 10^{14} \times 11.7 \times 8.85 \times 10^{-14}}}{0.293 \times 10^{-6}}$$

$$= \frac{\sqrt{2 \times 1.6 \times 8 \times 11.7 \times 10^{-19} \times 8.85}}{0.293 \times 10^{-6}} = 0.055$$

Current Summary

Current-voltage equations of the n-channel MOSFET :

$$I_D = 0, \quad \text{for } V_{GS} < V_T \quad (3.54)$$

$$I_D(\text{lin}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for } V_{GS} \geq V_T \\ \text{and } V_{DS} < V_{GS} - V_T \quad (3.55)$$

$$I_D(\text{sat}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \geq V_T \\ \text{and } V_{DS} \geq V_{GS} - V_T \quad (3.56)$$

Current-voltage equations of the p-channel MOSFET :

$$I_D = 0, \quad \text{for } V_{GS} > V_T \quad (3.57)$$

$$I_D(\text{lin}) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for } V_{GS} \leq V_T \\ \text{and } V_{DS} > V_{GS} - V_T \quad (3.58)$$

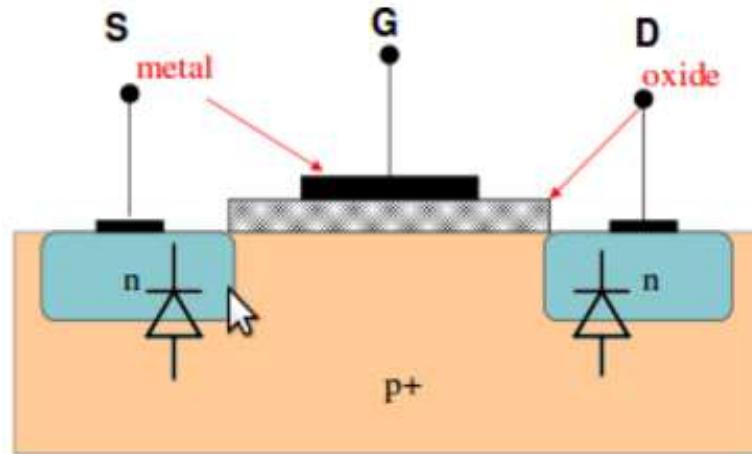
$$I_D(\text{sat}) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \leq V_T \\ \text{and } V_{DS} \leq V_{GS} - V_T \quad (3.59)$$

Second-order Effects

- Body Effect.
- Mobility variation or Velocity Saturation
- Channel length modulation
- Sub threshold conduction
- Mobility variation or Velocity Saturation
- Fowler-Nordheim tunneling
- Drain punchthrough
- Impact Ionization-Hot electrons.

Body Effect

What happens if the bulk voltage of an N-MOSFET drops below the source voltage ?



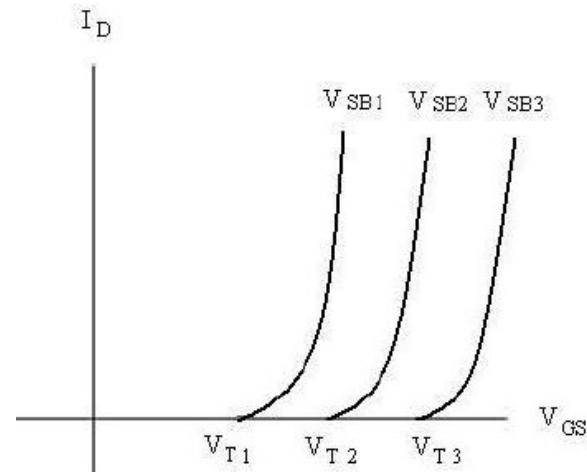
$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right)$$

$$\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$

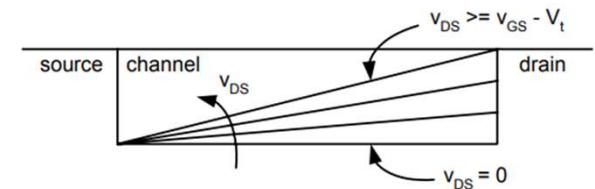
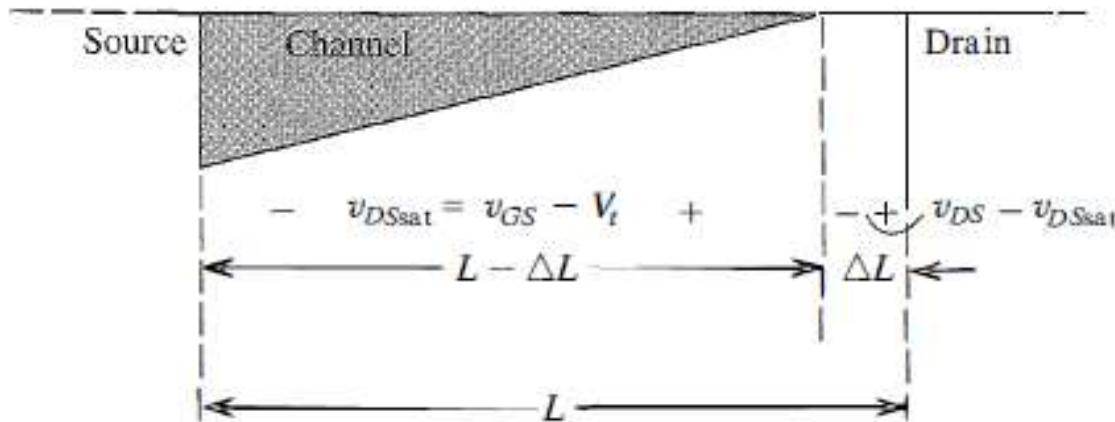
$$V_{TH0} = \varphi_{MS} + 2\varphi_F + \frac{Q_{Dep}}{C_{ox}}$$

where φ_{MS} is the difference between the work functions of the polysilicon gate and the silicon substrate

φ_F = Fermi potential



Channel length modulation



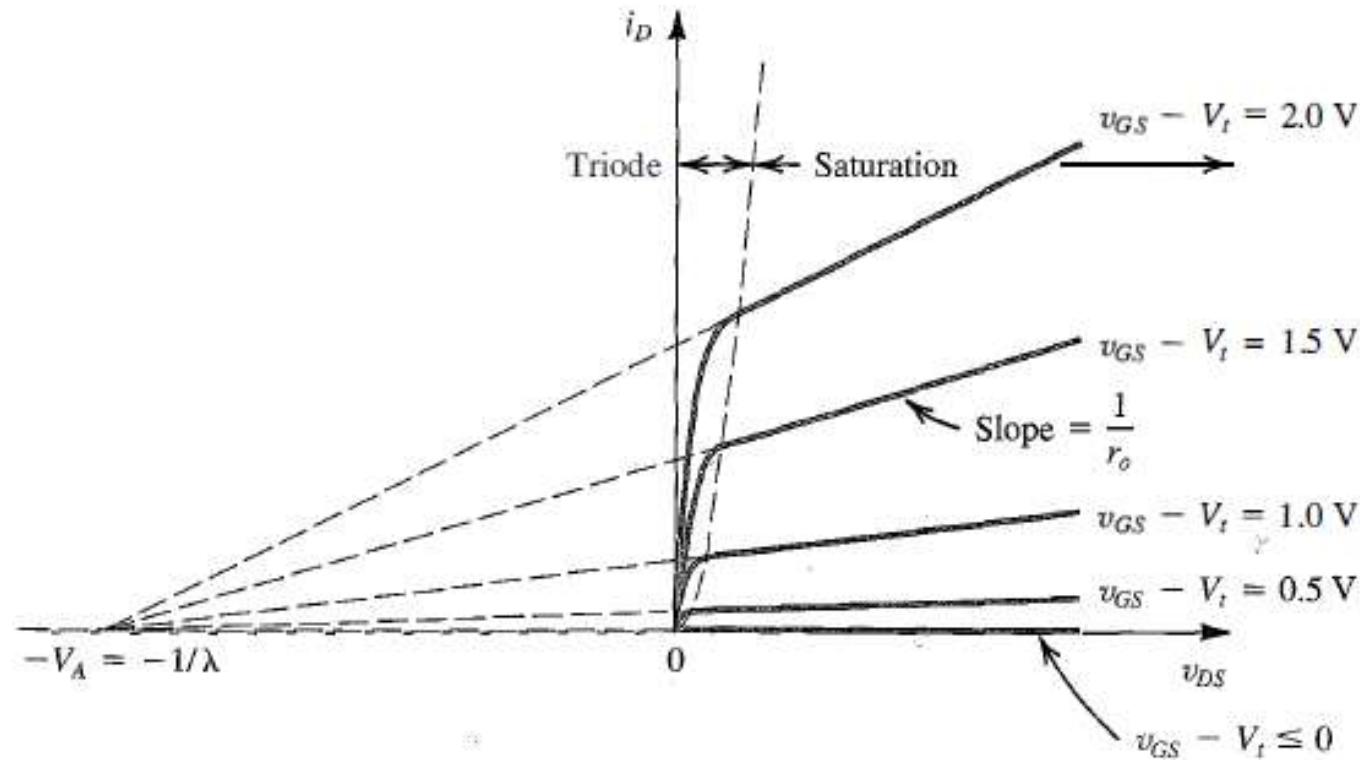
$$\begin{aligned}
 i_D &= \frac{1}{2} k'_n \frac{W}{L - \Delta L} (v_{GS} - V_t)^2 \\
 &= \frac{1}{2} k'_n \frac{W}{L} \frac{1}{1 - (\Delta L/L)} (v_{GS} - V_t)^2 \\
 &\equiv \frac{1}{2} k'_n \frac{W}{L} \left(1 + \frac{\Delta L}{L}\right) (v_{GS} - V_t)^2 \\
 \Delta L &= \lambda' v_{DS}
 \end{aligned}$$

$$\begin{aligned}
 i_D &= \frac{1}{2} k'_n \frac{W}{L} \left(1 + \frac{\lambda'}{L} v_{DS}\right) (v_{GS} - V_t)^2 \\
 \lambda &= \frac{\lambda'}{L}
 \end{aligned}$$

λ is a process-technology parameter with the dimensions of V^{-1}

$$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

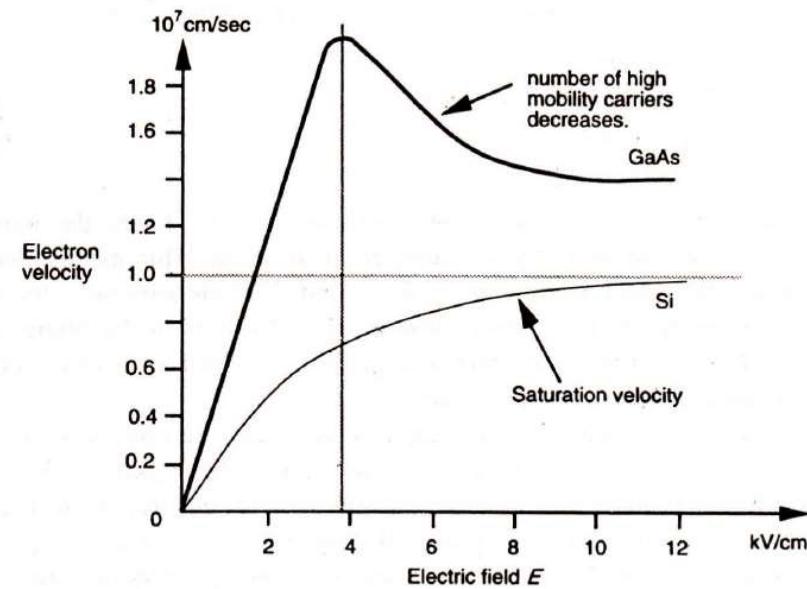
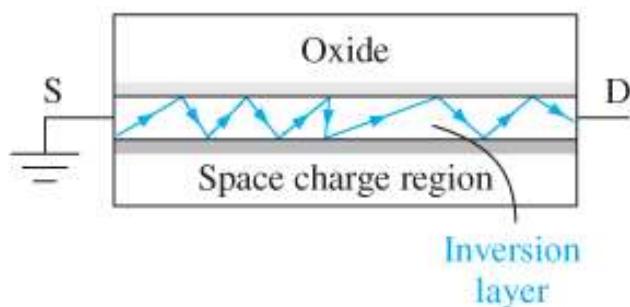
Channel length modulation



V_A is a process-technology parameter with the dimensions of V.

Mobility variation

Mobility is defined as the ease with which the charge carriers drift in the substrate material. Mobility decreases with increase in doping concentration and increase in temperature. Mobility is the ratio of average carrier drift velocity and electric field. Mobility is represented by the symbol μ .



Sub threshold conduction

For $V_{GS} \approx V_{TH}$, a "weak" inversion layer still exists and some current flows from D to S. Even for $V_{GS} < V_{TH}$, I_D is finite, but it exhibits an *exponential* dependence on V_{GS} . Called "subthreshold conduction". this effect can be formulated for V_{DS} greater than roughly 200 m V as

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_T},$$

$\zeta > 1$ is a nonideality factor

Fowler Nordhiem tunneling:

When the gate oxide is very thin there can be a current between gate and source or drain by electron tunneling through the gate oxide. This current is proportional to the area of the gate of the transistor.

Drain punchthrough

When the drain is a high voltage, the depletion region around the drain may extend to the source, causing the current to flow even if gate voltage is zero. This is known as Punchthrough condition.

Impact Ionization-Hot electrons

When the length of the transistor is reduced, the electric field at the drain increases. The field can become so high that electrons are imparted with enough energy we can term them as hot. These hot electrons impact the drain, dislodging holes that are then swept toward the negatively charged substrate and appear as a substrate current. This effect is known as Impact Ionization.

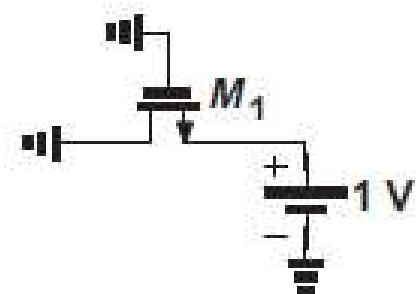
Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of $8 \times 10^{17} \text{ cm}^{-3}$. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?

$$\phi_s = 2(0.026 \text{ V}) \ln \frac{8 \times 10^{17} \text{ cm}^{-3}}{1.45 \times 10^{10} \text{ cm}^{-3}} = 0.93 \text{ V}$$

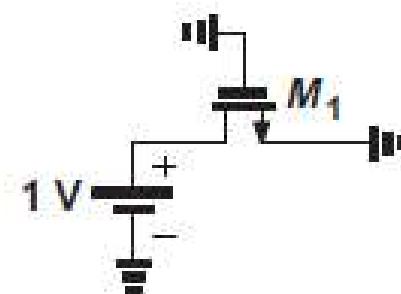
$$\gamma = \frac{10.5 \times 10^{-8} \text{ cm}}{3.9 \times 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}}} \sqrt{2(1.6 \times 10^{-19} \text{ C})(11.7 \times 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}})(8 \times 10^{17} \text{ cm}^{-3})} = 0.16$$

$$V_t = 0.3 + \gamma \left(\sqrt{\phi_s + 0.6 \text{ V}} - \sqrt{\phi_s} \right) = 0.34 \text{ V}$$

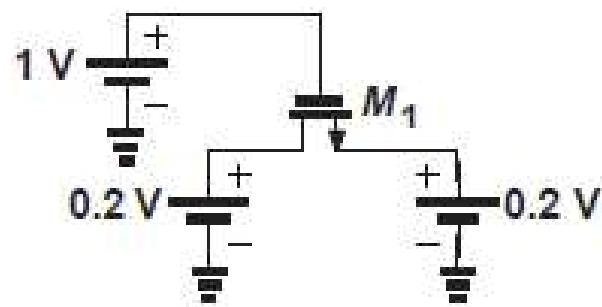
Determine the region of operation of M_1 in each of the circuits shown in Fig.



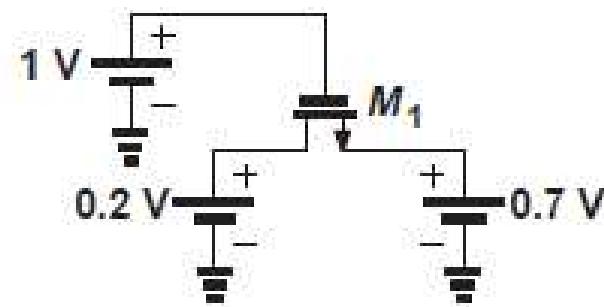
(a)



(b)

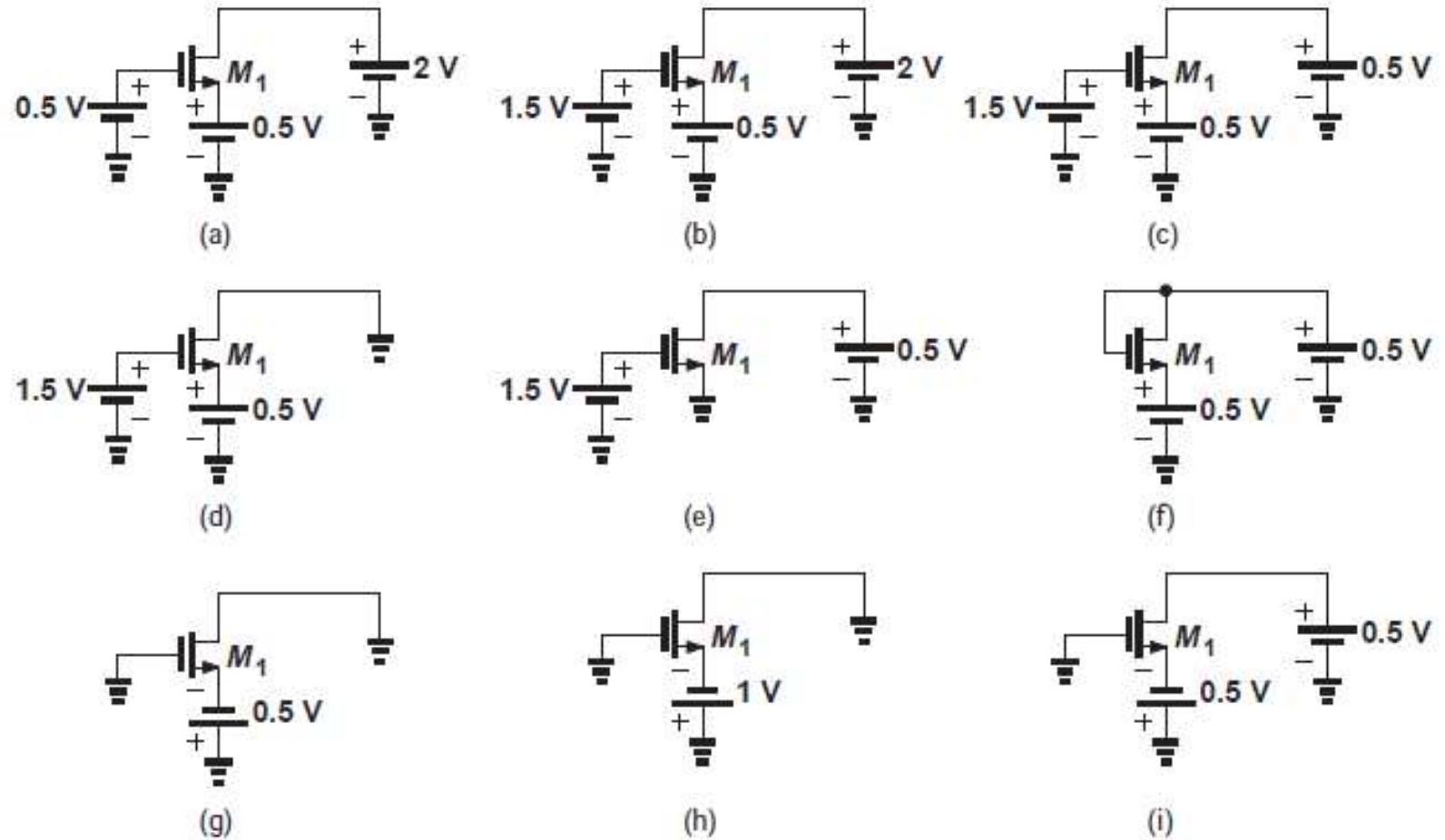


(c)



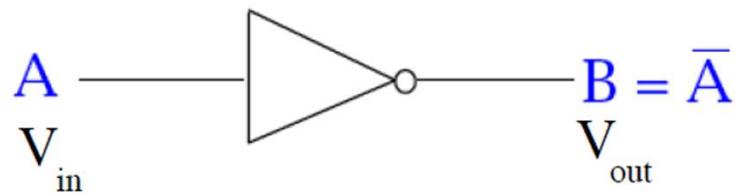
(d)

$V_{th} = 0.4 \text{ V}$ for NMOS devices and -0.4 V for PMOS devices.

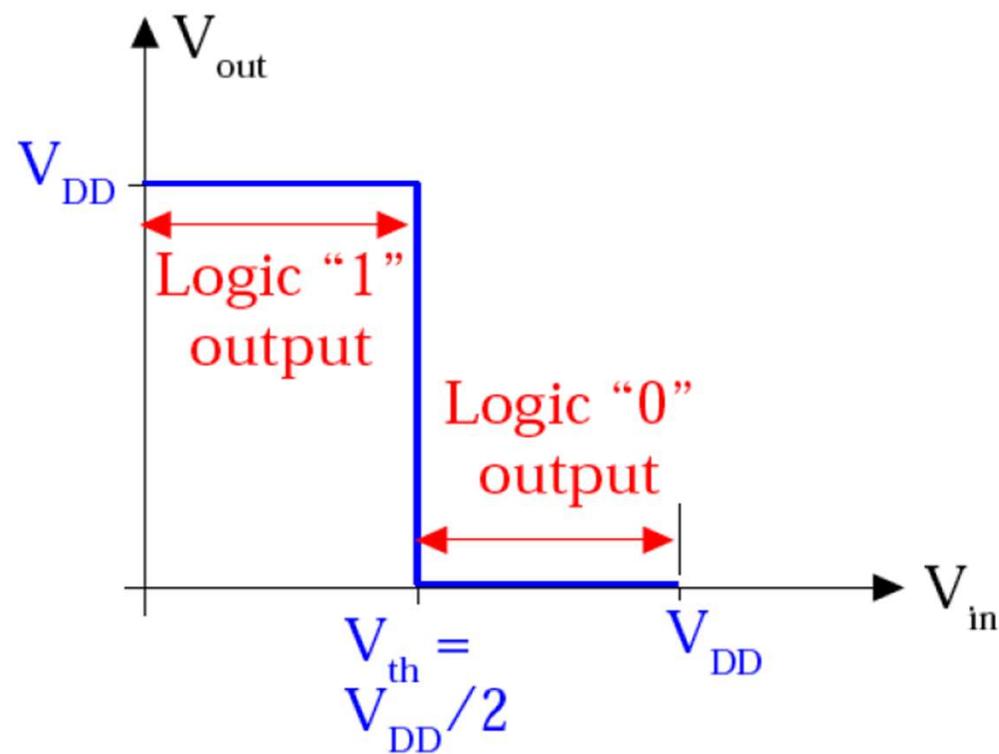


$V_{th} = 0.4 \text{ V}$ for NMOS devices and -0.4 V for PMOS devices.

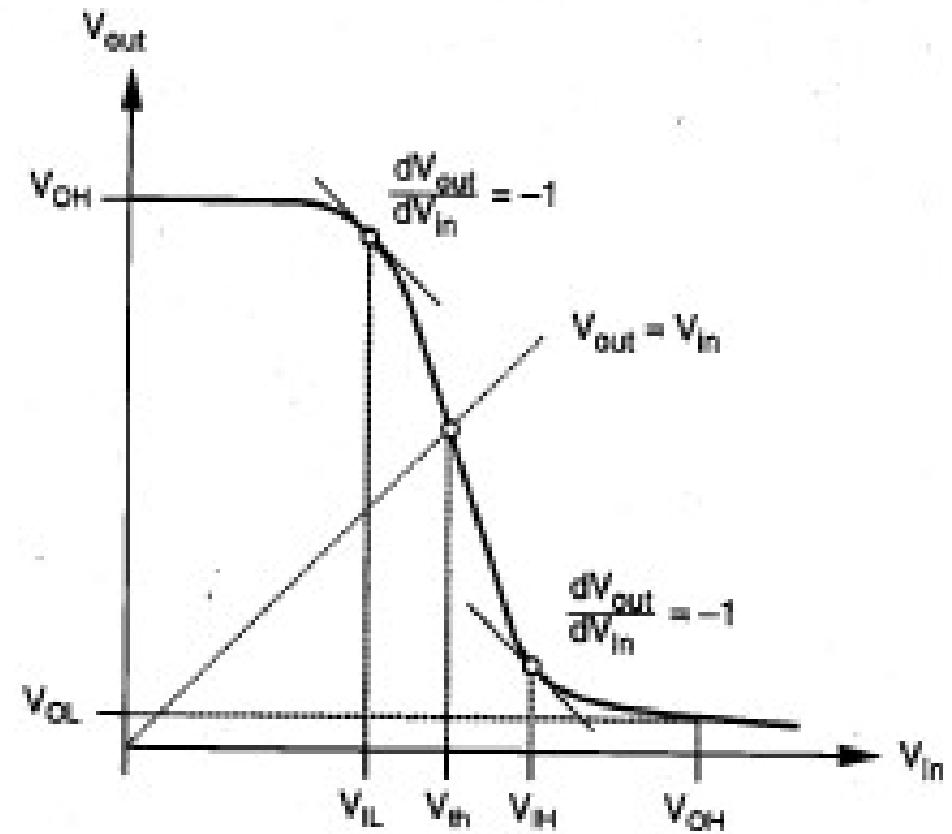
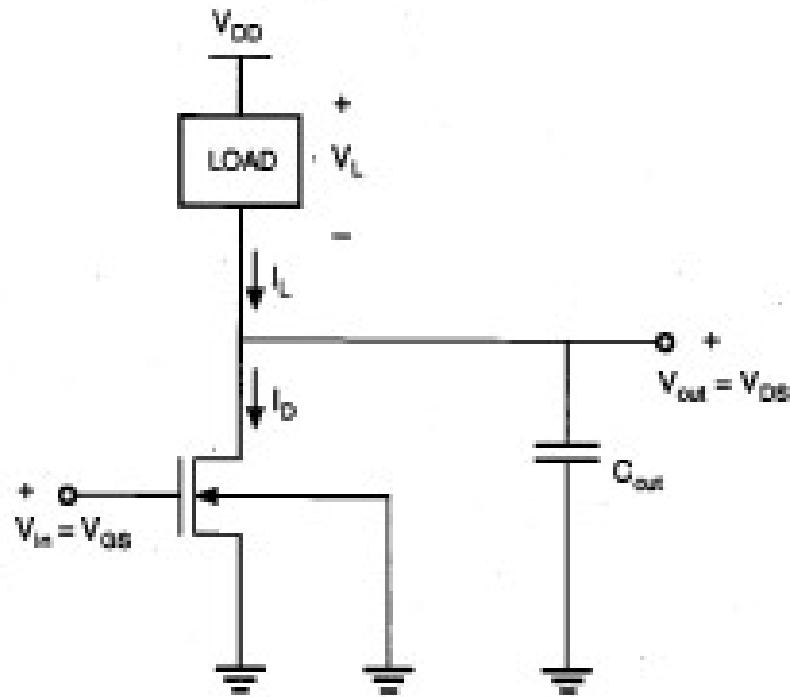
Inverters



A	B
0	1
1	0



Inverters



V_{OH} : Maximum output voltage when the output level is logic "1"

V_{OL} : Minimum output voltage when the output level is logic "0"

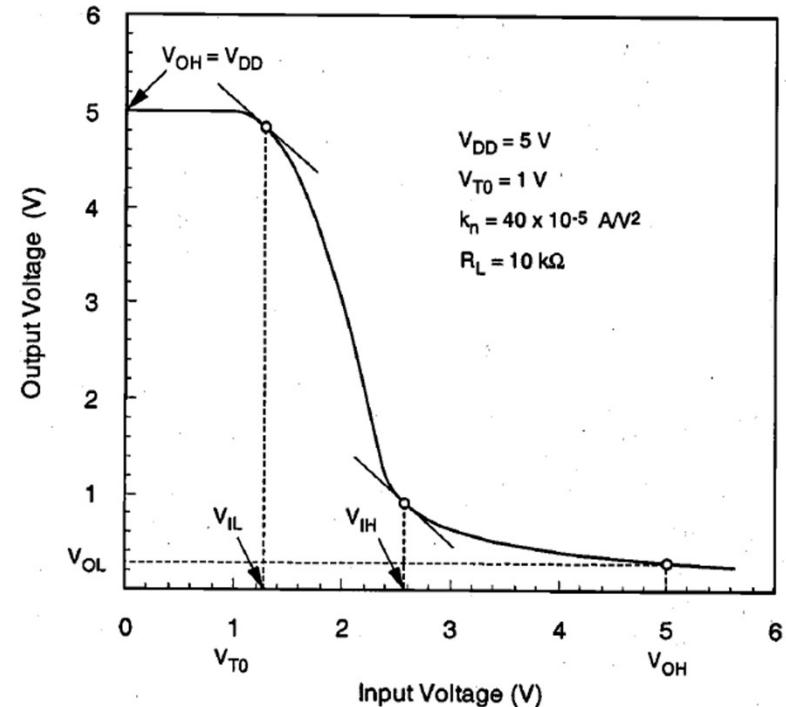
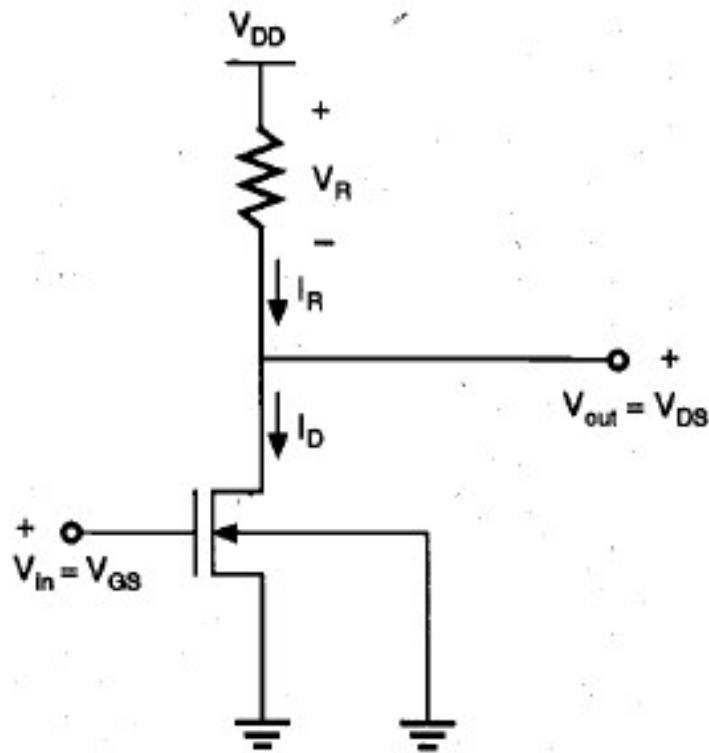
V_{IL} : Maximum input voltage which can be *interpreted* as logic "0"

V_{IH} : Minimum input voltage which can be *interpreted* as logic "1"

Inverters

- ❖ Resistive Load Inverter
- ❖ Enhancement-load Inverter
- ❖ Depletion-load Inverter
- ❖ CMOS Inverter

Resistive-load Inverters



Saturation Current:

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

Linear Current:

$$I_R = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2]$$

Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	cut-off
$V_{T0} \leq V_{in} < V_{out} + V_{T0}$	saturation
$V_{in} \geq V_{out} + V_{T0}$	linear

Resistive-load Inverters

V_{OH}

$$V_{out} = V_{DD} - R_L \cdot I_R$$

$$V_{OH} = V_{DD}$$

V_{OL}

$$I_R = \frac{V_{DD} - V_{out}}{R_L}$$

Using KCL for the output node, i.e., $I_R = I_D$, we can write the following equation:

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{DD} - V_{T0}) \cdot V_{OL} - V_{OL}^2]$$

$$V_{OL}^2 - 2 \cdot \left(V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right) \cdot V_{OL} + \frac{2}{k_n R_L} \cdot V_{DD} = 0$$

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$

Resistive-load Inverters

V_{IL}

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

Differentiate w.r.t. V =

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = k_n \cdot (V_{in} - V_{T0})$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

$$\begin{aligned} V_{out}(V_{in} = V_{IL}) &= V_{DD} - \frac{k_n R_L}{2} \cdot \left(V_{T0} + \frac{1}{k_n R_L} - V_{T0} \right)^2 \\ &= V_{DD} - \frac{1}{2 k_n R_L} \end{aligned}$$

V_{IH}

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2]$$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot \frac{dV_{out}}{dV_{in}} + 2 V_{out} - 2 V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$V_{IH} = V_{T0} + 2 V_{out} - \frac{1}{k_n R_L}$$

Resistive-load Inverters

V_{IH}

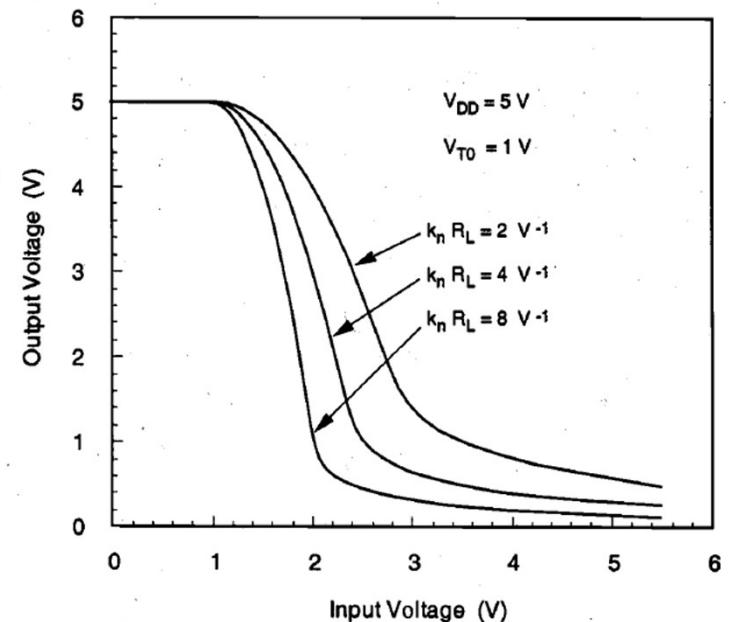
$$V_{IH} = V_{T0} + 2V_{out} - \frac{1}{k_n R_L}$$

Utilize $\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2]$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot \left(V_{T0} + 2V_{out} - \frac{1}{k_n R_L} - V_{T0} \right) \cdot V_{out} - V_{out}^2 \right]$$

$$V_{out} (V_{in} = V_{IH}) = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}}$$



Consider a resistive-load inverter circuit with $V_{DD} = 5$ V, $k_n' = 20 \mu\text{A}/\text{V}^2$, $V_{T0} = 0.8$ V, $R_L = 200 \text{k}\Omega$, and $W/L = 2$. Calculate the critical voltages (V_{OL} , V_{OH} , V_{IL} , V_{IH}) on the VTC and find the noise margins of the circuit.

Solution:

$$V_{OH} = V_{DD} = 5 \text{ V}$$

Note that in this resistive-load inverter example, the transconductance of the driver transistor is $k_n = k_n' (W/L) = 40 \mu\text{A}/\text{V}^2$ and, hence, $(k_n R_L) = 8 \text{ V}^{-1}$.

$$\begin{aligned} V_{OL} &= V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2 V_{DD}}{k_n R_L}} \\ &= 5 - 0.8 + \frac{1}{8} - \sqrt{\left(5 - 0.8 + \frac{1}{8}\right)^2 - \frac{2 \cdot 5}{8}} \\ &= 0.147 \text{ V} \end{aligned}$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L} = 0.8 + \frac{1}{8} = 0.925 \text{ V}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} = 0.8 + \sqrt{\frac{8}{3} \cdot \frac{5}{8}} - \frac{1}{8} = 1.97 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.93 - 0.15 = 0.78 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.97 = 3.03 \text{ V}$$

For better noise immunity, the NM_L should be at least about 25% of the power supply voltage V_{DD} , i.e., about 1.25 V.