DEPARTMENT OF Electronics and Communication Engineering

IV Semester B.Tech. EE(VLSI Design and Technology)

Assessment-4 (FISAC-2)

Course: FPGA based System Design using Verilog **Course Code: ECE 2229**

Max. Marks: 5

Q. No.	Questions
1.	**Design a Traffic Light Controller for an intersection of four roads (A-B-C-D). Consider:** • Road 'A' has the highest priority, and road 'D' has the lowest priority. • At a time, vehicles are moving in one direction only. Draw the state diagram and provide Verilog code for the same.
2	Design a 32-bit RISC processor with four ALU operations (Add, Sub, Mul, Divide) and a 2-memory operation (memory read and memory right). You can consider a 5-bit opcode, one program memory of 512KB, and one data memory of 512KB (total 1024KB of BRAM). Make the possible circuit and write the Verilog code for the same.
3.	Explain in detail about the top-down design flow of FPGA.
4.	What are the different types of FPGA families there? Provide detailed architecture for the Xilinx FPGA Board, including CLB architecture and I/O circuitry.
5.	**Explain:** Fine vs Coarse Grain Architecture Logic Mapping in FPGA Partitioning for Multi-FPGA system