Question Paper

Exam Date & Time: 11-May-2024 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) DEGREE EXAMINATIONS - APRIL / MAY 2024
SUBJECT: ECE 2221/ECE_2221 - VLSI DESIGN

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A) A 0.18-µm fabrication process is specified to have tox= 4nm, μ_n=450cm^2/Vs and VT=0.5V. Find the value of Cox and µnC_{ox}. For a MOSFET with minimum length L=0.18-µm fabricated in this process, find the required value of W so that the device exhibits a channel resistance of 1K ohm at V_{GS}=1V. Given ε_{ox}=3.45e-11 F/m. Calculate the values of Overdrive voltage V_{OV}, Gate Source Voltage V_{GS} and minimum Drain Source Voltage V_{DSmin} , needed to operate the transistor in saturation region with a dc current of I_D=60µA. (4)

1B) With neat circuit diagram and VI characteristics explain the working of NMOS FET in different regions. (3)

1C) An NMOS transistor with W/L =8/1 has V_{TN} =1V , $2\varphi_F$ = 0.6V and γ = 0.7 $V^{1/2}$. The transistor operating with V_{SB}=3V, V_{GS}=2.5V and V_{DS}=5V. What is the drain current in the transistor? Repeat for V_{DS} =0.5V. (3)

2A) Derive the pull-up to pull-down ratio for an NMOS inverter driven through one or more pass transistors as shown in Figure 2A . (4)

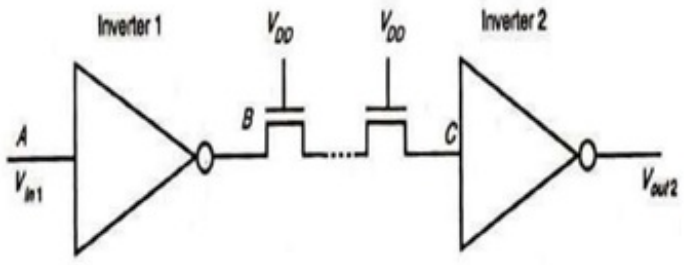


Figure 2A.

2B) Design F=[(A+BC)D +E] logic using static CMOS design style and draw its stick diagram. (3)

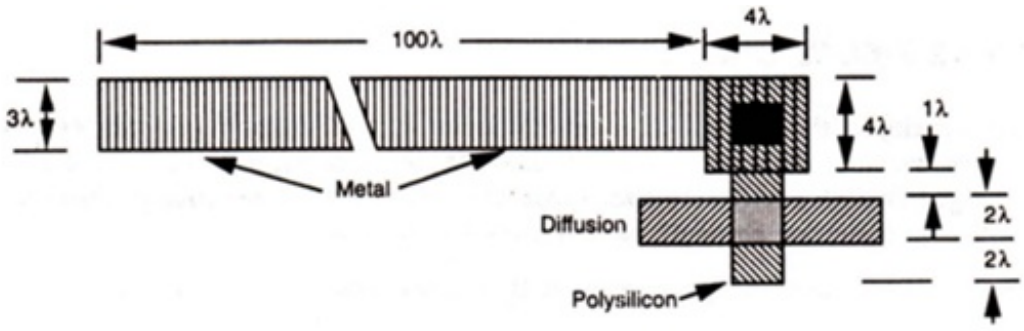
2C) Derive scaling factors for (3)
1) Gate area (Ag)
2) Gate capacitance per unit area (Cox)
3) Gate capacitance (Cg).

3A) Explain the steps involved in the fabrication of a depletion PMOS transistor. (4)

3B) Draw the layout and stick diagram of NMOS inverter (3)

3C) Determine the overall capacitance for the layout depicted in Fig. Q3C, expressed in terms of unit area gate (3)

capacitance(□ Cg). Consider the technology parameters for a 2 µm process.



Typical area capacitance values for MOS circuits

Capacitance	*Value in pF × 10^{-4}/µm² (Relative values in brackets)*
	2 µm
Gate to channel	8 (1.0)
Diffusion (active)	1.75 (0.22)
Polysilicon* to substrate	0.6 (0.075)
Metal 1 to substrate	0.33 (0.04)
Metal 2 to substrate	0.17 (0.02)
Metal 2 to metal 1	0.5 (0.06)
Metal 2 to polysilicon	0.3 (0.038)

Notes: Relative value = specified value/gate to channel value for that technology.

4A) Implement a Full adder using CMOS PLA (4)

4B) Two inverters are cascaded to drive a capacitive load C_L = 15 □ Cg as shown in Fig. Q 4B. (3)

Inverters 1 and 2 are pseudo NMOS and CMOS inverter, respectively. Calculate the pair delay in terms of τ by taking the minimum required dimension of each transistor.

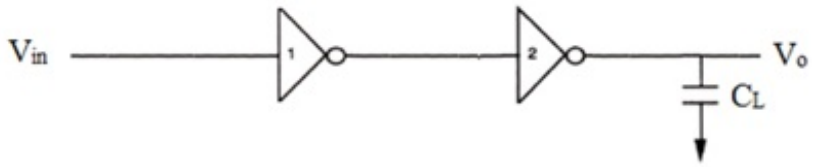


Fig. Q 4B

4C) Implement a SR latch using 2 input CMOS NAND gate. (3)

5A) Implement 3 input minority function using 3 stage DOMINO logic. (4)

5B) Explain the working of 6-T DRAM (3)

5C) Explain the operation of a 4 × 4 barrel shifter and demonstrate how it facilitates the "divided by 2" operation. (3)

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Question Paper

Exam Date & Time: 31-May-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) DEGREE EXAMINATIONS - MAY/JUNE 2023
SUBJECT: ECE 2254/ECE_2254 - VLSI DESIGN

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Missing data may be suitably assumed.

1A) Discuss the operation of any two different forms of pull-up for an NMOS inverter circuit. Draw transfer characteristics for these different forms of pull-up. Compare the relative merits of these different forms of pull-up. (4)

1B) With neat diagrams, explain the working of the MOS capacitor. Briefly illustrate the fabrication steps of a MOS Capacitor. (3)

1C) Refer the pass-transistor based logic network given in **FIG 1C**. (3)
(a) Determine the truth table for the circuit and indicate the logic function performed by the topology?
(b) Specify the role of PMOS transistor in this circuit?

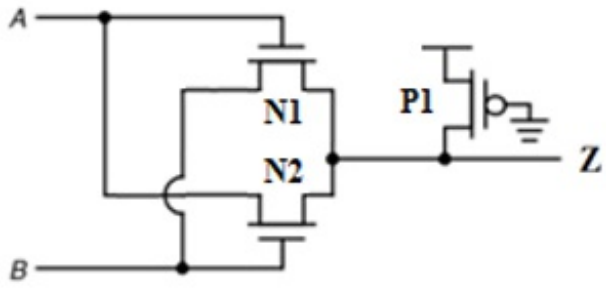


Fig. 1C

2A) Implement Static CMOS circuit of half Adder with truth table. (4)

2B) Implement and explain the working of 2 input NOR using clocked CMOS(C²MOS) and draw the stick diagram. (3)

2C) Explain with diagram, the working of 4X4 OR ROM for the table given and draw Stick diagram. (3)

word	BL[1]	BL[2]	BL[3]	BL[4]
W[1]	1	0	0	1
W[2]	0	1	1	0
W[3]	1	0	1	1
W[4]	1	1	0	1

3A) Sketch the layout of a CMOS 3-input NAND gate using λ-based design rules. Use either colour code/ shades as per the standard conventions to distinguish different regions/layers. (4)

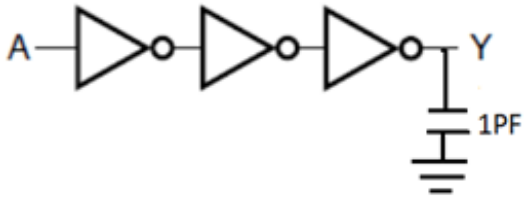
3B) A semi-conductor industry wants to fabricate a MOS with its substrate as pentavalent impurities and (3)

trivalent impurities as source and drain. Explain the steps involved in the fabrication of the mentioned MOS.

3C) List the steps involved Fin-FET fabrication process with neat diagrams. (3)

4A) Implement an static CMOS circuit of Y=(A+B+C)| and Draw the layout. (4)

4B) Calculate the total delay in geometrically cascaded CMOS inverters shown in the figure below. Assume f=e=2. 7==3. (3)



4C) Derive the scaling factors with respect to MOSFET. (3)
i) Gate Area
ii) Gate capacitance per unit Area
iii) Gate capacitance

5A) Construct a CMOS PLA to implement the following functions (4)
X = AB′D + A′C′ + BC + C′D′
Y = A′C′ + AC + C′D′
Z = CD + A′C′ + AB′D

5B) Demonstrate how the basic building block of an Arithmetic Logic Unit (ALU) can be employed to implement a 2-input logic OR function. (3)

5C) Illustrate a 1-bit right shift operation on the input word '0010' using Barrel shifter and provide its circuit diagram. (3)

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FOURTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

JUNE 2022

SUBJECT: VLSI DESIGN (ECE - 2254)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Graph sheet will be provided

Q. No.	Questions	M*	C*	A*	B*
1A.	Describe the steps involved in the fabrication of CMOS inverter using SOI (Silicon on Insulator) process with neat diagram.	4	3	1	2
1B.	Implement the given words using NOR ROM and draw its stick diagram. $\begin{bmatrix} w0 \\ w1 \\ w2 \\ w3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	3	2	1	3
1C.	Implement the given expression using pseudo NMOS logic and indicate L: W ratio of each transistor $Z = \overline{A.B + C.(D + E)}$	3	2	1	3
2A.	Describe latch-up problem in CMOS and suggest solutions.	4	3	1	2
2B.	Implement a full adder using NMOS pass transistors. Assume input and its complements are available.	3	2	1,1 2	3
2C.	Implement 3-input NOR gate using BiCMOS logic.	3	2	1	3
3A.	Describe the fabrication of N-channel Enhancement MOSFET with the help of neat diagram.	4	3	1	2
3B.	Implement full subtractor using NMOS PLA	3	5	1	3
3C.	Describe the fabrication of Depletion MESFET with the help of neat diagram.	3	5	1	2
4A.	Draw the layout of Pseudo NMOS inverter using λ based design rule.	4	4	1,1 2	3
4B.	Perform following function using ALU unit i. 1000 SUB 1001 ii. 1010 XOR 0011 iii. 0101 AND 1100	3	5	1	2
4C.	Describe the working of 4×4 barrel shifter with the help of a suitable circuit / diagram.	3	5	1	2

5A.	Find the optimal number of NMOS inverters to be cascaded so as to drive load capacitance of 0.54 pF off-chip capacitive load such that the total delay is minimized. Given that 1□Cg = 0.01pF. Give the cascaded structure with L:W ratios indicated. Find the overall delay.	4	4	1,2	2
5B.	Describe the working of bus arbitration logic using structured approach.	3	5	1	2
5C.	Describe the working of 3-T DRAM with the help of circuit and timing diagram.	3	2	1	2

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level

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FOURTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

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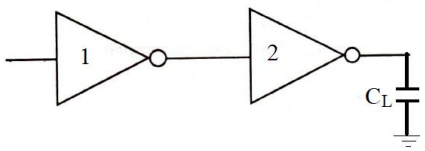
Q. No.	Questions	M*	C*	A*	B*
1A.	Two Pseudo NMOS inverters are cascaded to drive a capacitive load of $C_L = 16 \square C_g$ as shown in the **Fig. Q 1A.** Calculate the pair delay in terms of τ for the inverter geometry indicated in the figure.  Inverter-1: $L_{PU}=6\lambda$, $W_{PU}=2\lambda$, $L_{PD}=2\lambda$, $W_{PD}=2\lambda$ Inverter-2: $L_{PU}=12\lambda$, $W_{PU}=4\lambda$, $L_{PD}=4\lambda$, $W_{PD}=4\lambda$ **Fig. Q1A**	4	4	1,2	3
1B.	Implement 3-input NAND gate using BiCMOS logic.	3	2	1	3
1C.	Describe the working of 4×4 cross bar switch with the help of neat diagram and list its disadvantages.	3	5	1	2
2A.	Draw the layout of depletion load NMOS inverter using λ based design rule.	4	4	1,12	2
2B.	Show that a full adder block can be used as subsystem to implement the following functions i. 2 input XNOR ii. 2 input OR iii. 2 input AND	3	5	1,12	2
2C.	Describe the working of n-bit parity generator using structured approach.	3	5	1	1
3A.	Describe the fabrication of P-channel Enhancement MOSFET with the help of neat diagram.	4	3	1	1

3B.	Explain the working on non-inverting super buffer.	3	2	1	1
3C.	Implement $Z = \overline{(A.B + C).D}$ using CMOS logic.	3	2	1	3
4A.	Describe the problem associated with N-Well CMOS process and its solution.	4	3	1	1
4B.	Describe the fabrication of Enhancement MESFET with the help of neat diagram.	3	5	1	1
4C.	Describe the working (Read and Write operation) of 6-T SRAM.	3	2	1	1
5A.	Give the circuit implementation of following multiple output function using Pseudo-NMOS PLA. F=AB+A'B'C G= A XOR B H=AB+BC+AC	4	5	1	3
5B.	Implement the given words using NAND ROM and draw its stick diagram. $\begin{bmatrix} w0 \\ w1 \\ w2 \\ w3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	3	2	1	3
5C.	Implement N-Input NOR gate using dynamic CMOS logic.	3	2	1	3

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level