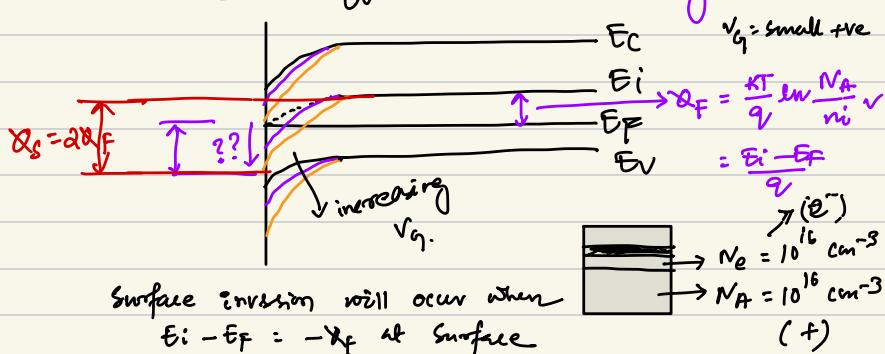
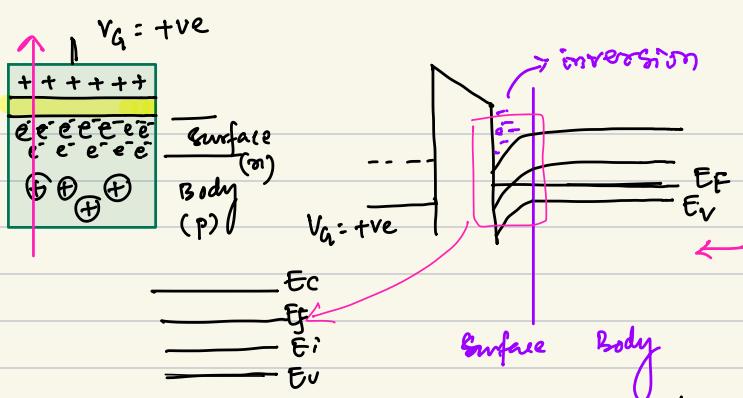


# VLSI DESIGN

Class note, Sec-D, Jan - 2025

Dr. Pramod Martha  
Assistant Professor,  
ECE, MIT Manipal, MAHE

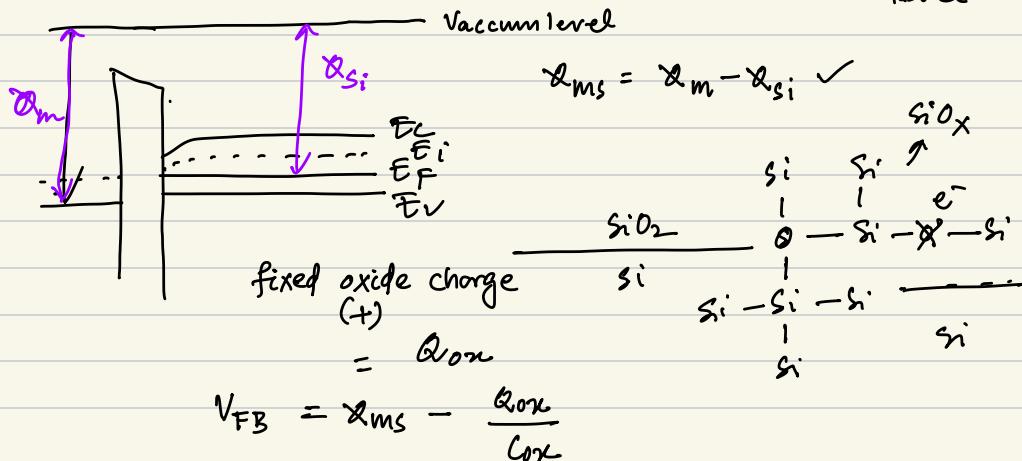


$$\alpha_s = \text{Surface potential} = \frac{E_i(\text{bulk}) - E_i(\text{surface})}{q}$$

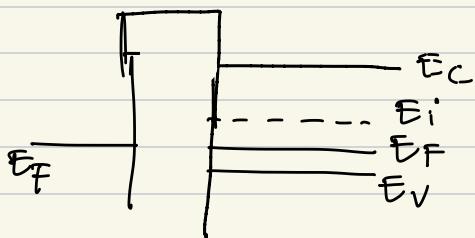
$$\text{cond}^n \text{ for surface inversion} = \alpha_s = 2\alpha_F$$

Threshold voltage :- 4 components.

① Work func<sup>n</sup> :- energy reqd. to move an  $e^-$  fr<sup>n</sup> vacuum level.



$V_{FB}$  = to make the bands flat  
flat band voltage

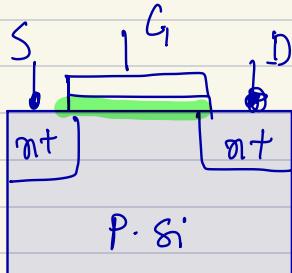


$$\textcircled{2} \quad 2\alpha_F = \alpha_s$$

$$\textcircled{3} \quad Q_D = - \sqrt{2.9 \cdot \epsilon_{Si} \cdot 2\alpha_F \cdot N_A}$$

$$V_{TO} = \alpha_{ms} + 2\alpha_F - \frac{Q_{on}}{C_{ox}} - \frac{Q_D}{C_{ox}}$$

**MOSFET** :- Metal oxide Semiconductor field effect transistor.



$n+$  → to make S/D more conductive to form ohmic contact

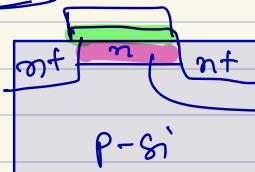
→ two type of MOSFET

$\xrightarrow{\quad}$

E-MOSFET      Depletion MOSFET

→ to create channel we need some voltage :  $V_{th}$  (Threshold voltage)

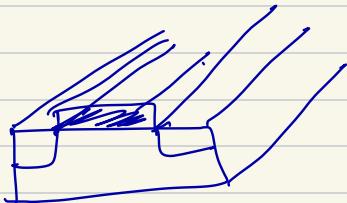
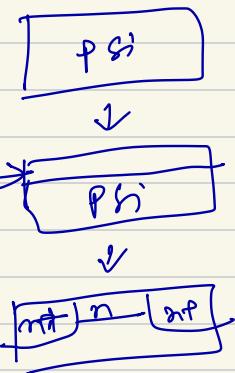
→ D MOSFET



$\rightarrow$  n-channel

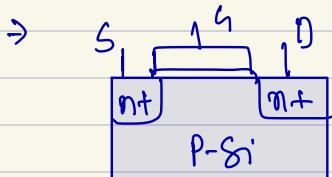
$G$  always 'on' transistor  
at  $V_g = 0$ , channel is present.

n-Si  
mg doping

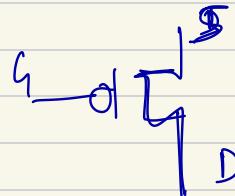
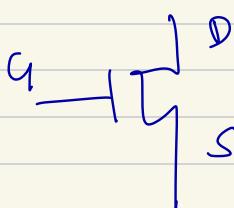
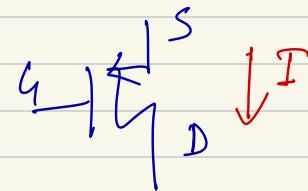
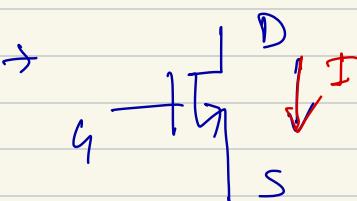
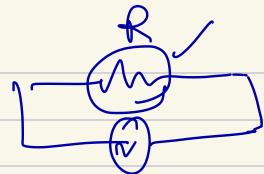
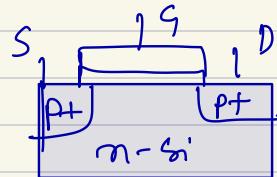


## Enhancement MOSFET:

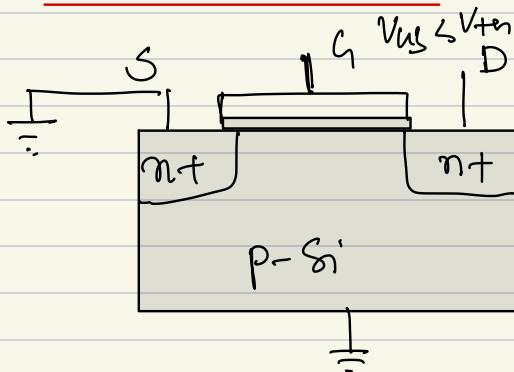
nMOSFET



pMOSFET



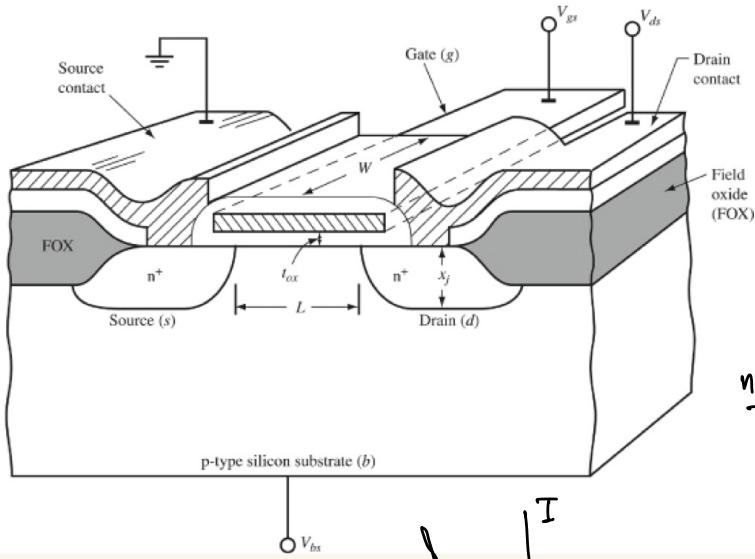
## MOSFET operation :-



→ when  $V_G = 0$ ,  $V_{DS}$  may  
 $V_{DS} = 0 \Rightarrow V_{GS} < V_{th}$  value  
 $V_{DS} \neq 0$ .

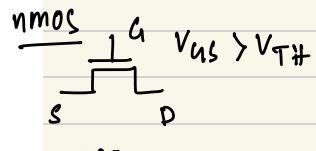
no surface inversion  
 no current flow b/w  
 source & drain

→ **Cutoff**

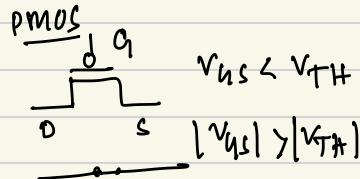
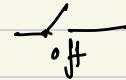


$$nMOS : V_{TH} = +ve$$

$$pMOS : V_{TH} = -ve$$

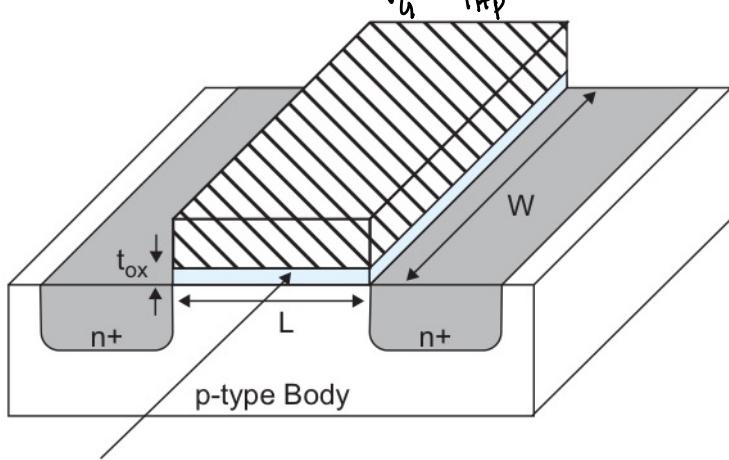
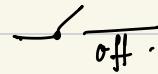


$$\text{if } V_{GS} < V_{TH}$$



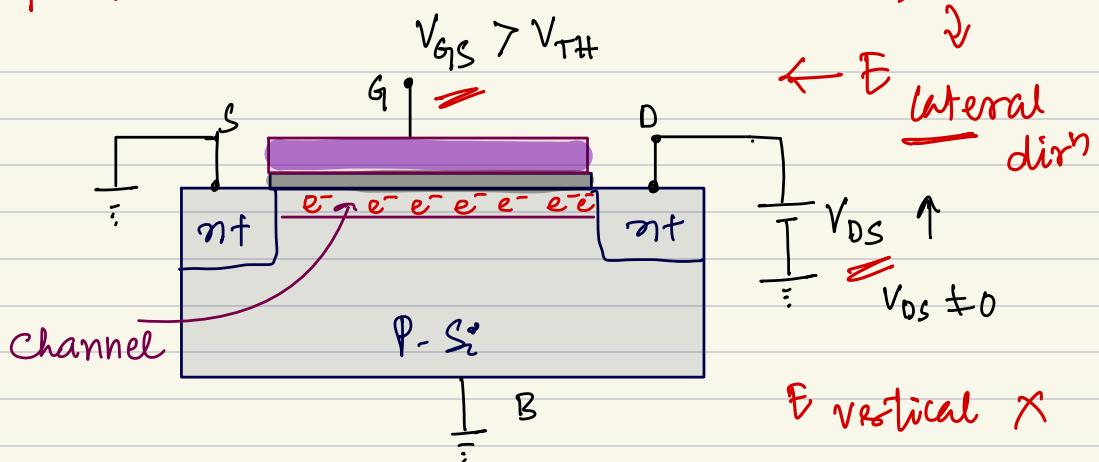
$$\text{if } V_{GS} > V_{TH}$$

$$|V_{GS}| > |V_{TH}|$$

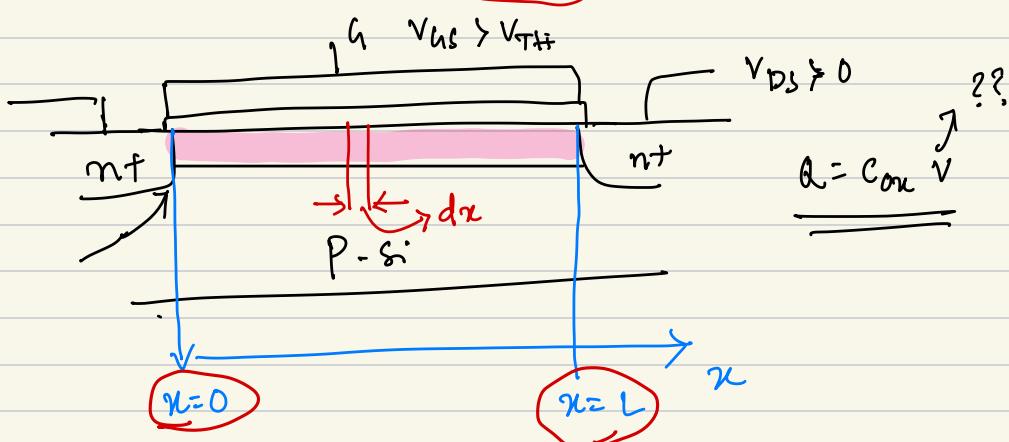


$\text{SiO}_2$  Gate Oxide  
(insulator,  $\epsilon_{ox} = 3.9\epsilon_0$ )

# Gradual channel Approximation (GCA)

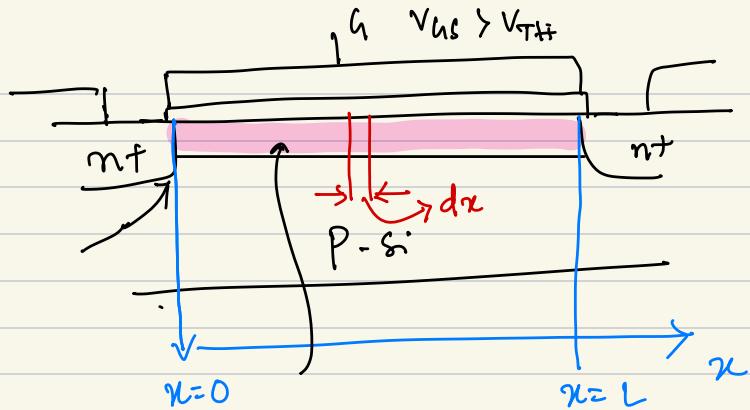


$L$ : channel length  
 $w$ : width



in small  $dx \Rightarrow d\varphi$

at source :  $V_S = 0$ , out of  $V_{GS}$ ,  $V_T$  utilized for channel  
So at Source =  $V_G - V_T$  is the potential



at drain side

$$V_{GS} - V_T - V_{DS}$$

$\downarrow$  ve free charge at any point; let's  $x$ : the potential

$$dQ = -Cox [V_{GS} - V_T - V(x)] / \text{per unit area.}$$

$= [V_{GS} - V_T - V(x)]$

where  $0 \leq V(x) \leq V_{DS}$ .

$$dQ = -Cox W \cdot dx [V_{GS} - V_T - V(x)] \quad \text{area} = W \cdot dx.$$

$$\text{for current } I_{DS} = \frac{dQ}{dt}$$

$$\Rightarrow \frac{dQ}{dt} = -Cox W [V_{GS} - V_T - V(x)] \frac{dx}{dt}$$

$$= -Cox W [V_{GS} - V_T - V(x)] \underline{\underline{v_d}}$$

ang. velocity of  $e^-$   $\leftarrow$  drift velocity  
in the channel.

$$v_d = \mu_n E \xrightarrow{\text{mobility of } e^-} \text{electric field.}$$

$E = \frac{-dV}{dx}$  potential.

$$\Rightarrow I = -\mu_n Cox W [V_{GS} - V_T - V(x)] \left[ -\frac{dV}{dx} \right]$$

$$\Rightarrow I dx = \mu_n C_o w [V_{GS} - V_T - v(x)] dx$$

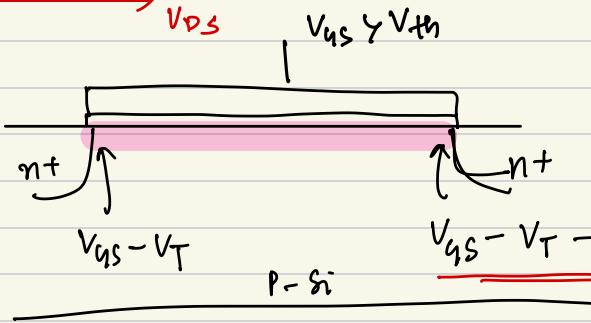
$$\Rightarrow \int_{x=0}^L I dx = \int_{V=0}^{V_{DS}} \mu_n C_o w [V_{GS} - V_T - v(x)] dV$$

$$\Rightarrow I_L = \mu_n C_o w [(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}]$$

$$\Rightarrow I = I_{DS} = \mu_n C_o w [(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}]$$

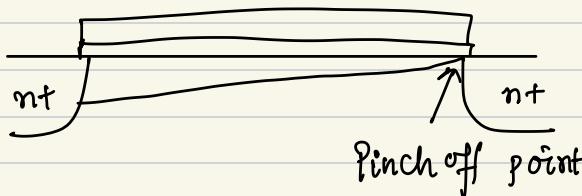


Linear region



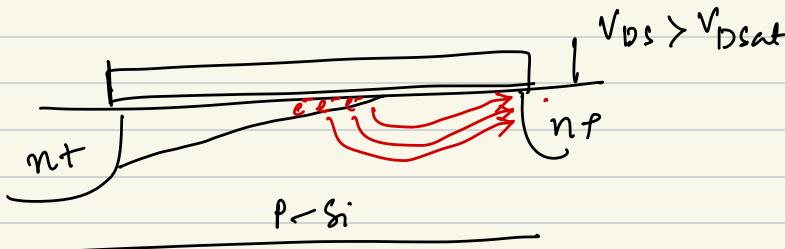
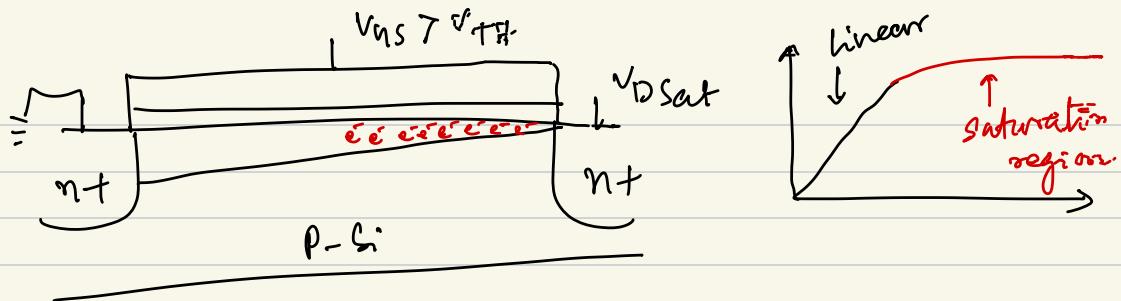
if  $V_{DS} = V_{GS} - V_T$   
 ↓  
 patch off pt  
 the  
 $V_{DS} = V_{GS} - V_T$   
 $= V_{Dsat}$

$$V_{GS} - V_T - V_{DS} = 0$$



Saturation drain voltage

So at  $V_{DS} = V_{GS} - V_T = V_{Dsat} \rightarrow$  channel is pinched off at drain end



$$I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

at  $V_{DS} = V_{GS} - V_T$

$$I_{D\text{sat}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_{T+}]^2$$

saturation region

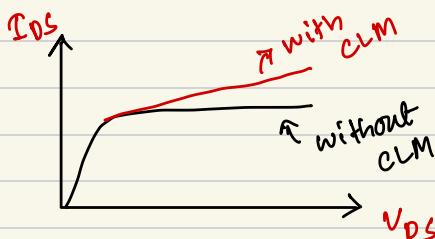
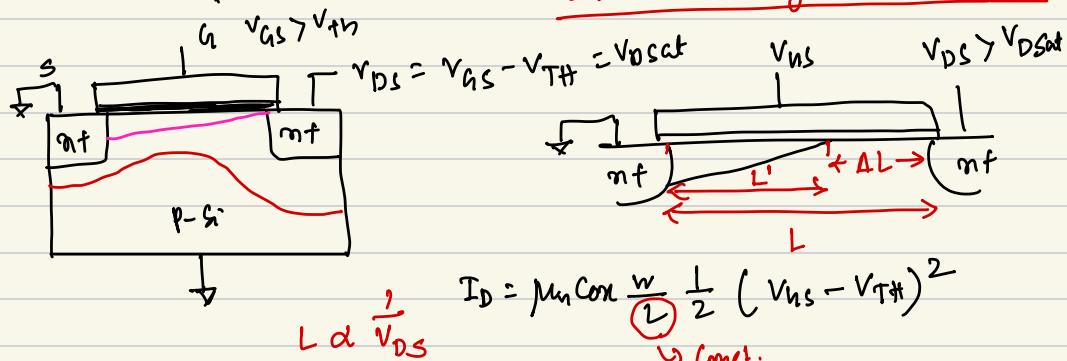
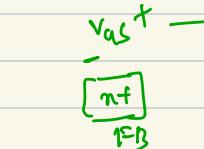
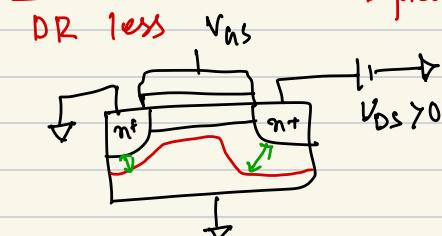
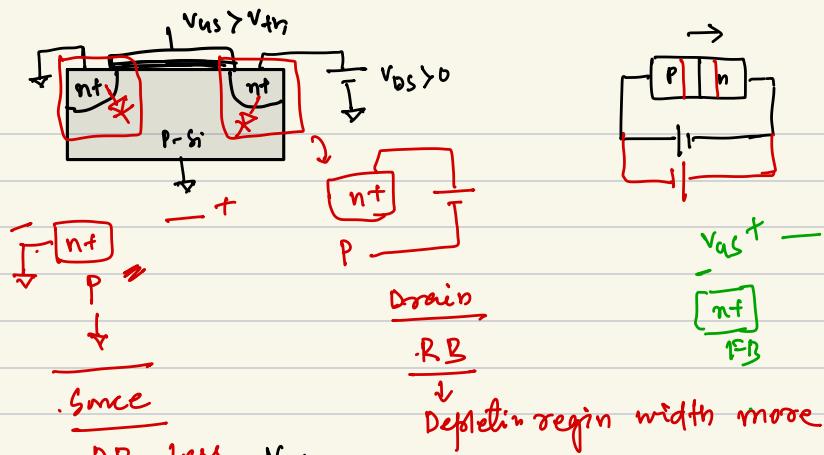
$$I_D = 0 \quad \text{cutoff}$$

$$= \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{T+}) V_{DS} - \frac{V_{DS}^2}{2} \right] - \text{linear}$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_{T+}]^2 - \text{saturated}$$

$$\mu_n C_{ox} = K'_n \rightarrow \text{process transconductance}$$

$$K'_n (W/L) = \text{gain factor.}$$



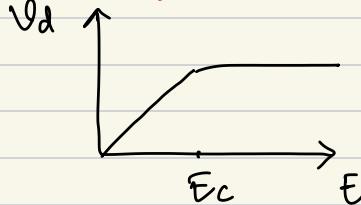
$$\begin{aligned}
 I_{DS} &= \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \\
 &= \frac{1}{2} \mu n C_{ox} \frac{W}{L - \Delta L} (V_{GS} - V_{TH})^2 \\
 &= \frac{1}{2} \mu n C_{ox} \frac{W}{L} \left(1 - \frac{\Delta L}{L}\right) (V_{GS} - V_{TH})^2
 \end{aligned}$$

$$\frac{\Delta L}{L} = \gamma V_{DS}$$

↑ channel length modulation (CLM) parameter

$$I_{DS} = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \gamma V_{DS}\right)$$

## velocity saturation



$$= 1.5 \times 10^6 \text{ V/m}$$

$$= 1.5 \text{ V/}\mu\text{m}$$

$$L = 1 \mu\text{m}.$$

## mobility degradation

$$V_d = \mu E \rightarrow \mu = \text{const}$$

$$\mu_e = ?$$

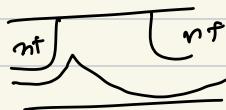
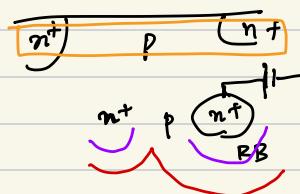
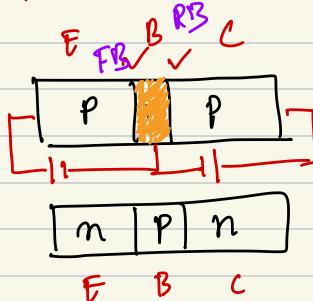
$$\mu_h = ?$$



$\rightarrow e^-$  face-on E field due to  $V_{DS}$ , and also due to  $V_{AS}$

Hence,  $\mu_{\text{surface}} < \mu_{\text{bulk}}$ .  $\rightarrow$  at Si-SiO<sub>2</sub> interface  $\rightarrow$  traps + fixed oxide charge makes the  $e^-$  movement slow.

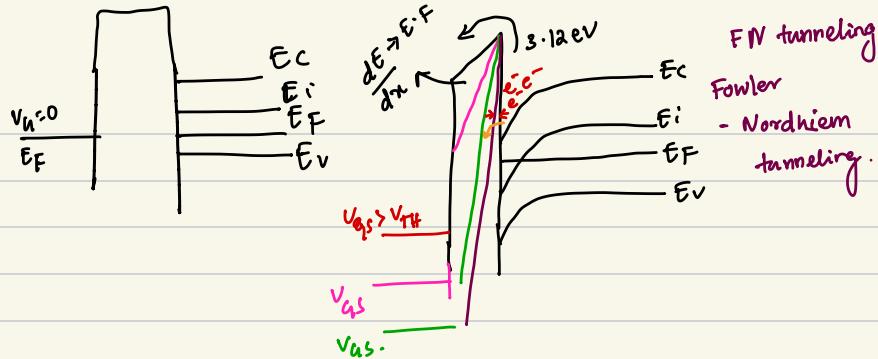
### DRain Punchthrough



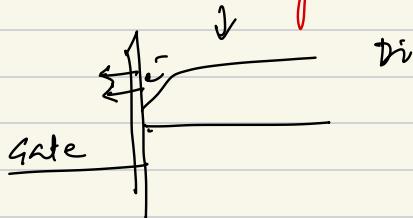
$$V_d = \mu E ; E \uparrow V_d \uparrow$$

if reaches a critical E field, the velocity of  $e^-$  saturates & become const  $\rightarrow$  velocity saturation

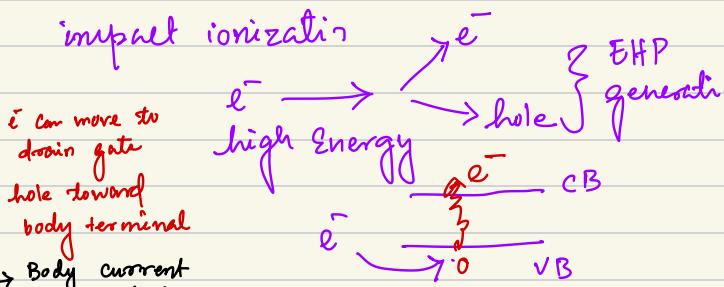
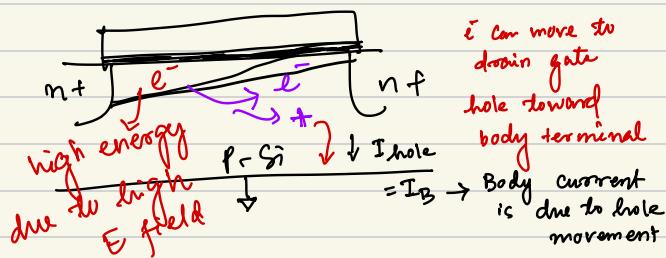
$$V_{\text{sat}} = 10^5 \text{ m/s.}$$



Direct tunneling  $\doteq$  from very small  $\approx 50 \text{ \AA}$  5 nm

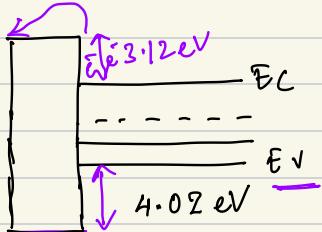


Hot carrier effect:



as it is having high energy this is called hot carrier

hot electron

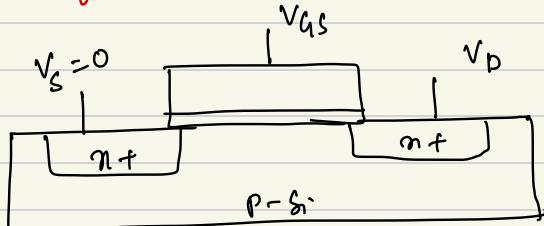


hot eis not hot holes

$$\text{as. } E_{C_{Si}} - E_{C_{SiO_2}} = 3.12 \text{ eV}$$

$$\text{but } E_{V_{Si}} - E_{V_{SiO_2}} = 4.02 \text{ eV}$$

## Body effect :-



$$V_{TH} = \frac{\chi_m}{\text{const.}} + \frac{2\chi_f}{\text{const.}} - \frac{Q_D}{C_{ox}} - \frac{Q_{ox}}{C_{ox} \text{ const.}}$$

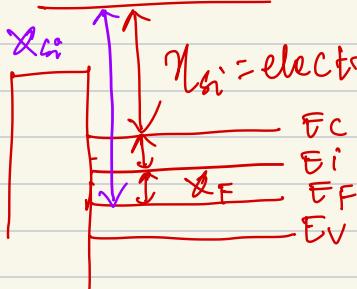
Metal to SC  
WF diff<sup>n</sup> { const. -

$$\frac{\chi_m - \chi_{Si}}{q} \quad \chi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_C - E_i}{q}$$

$$\text{const.} \rightarrow \text{material property} + \frac{E_i - E_F}{q}$$

$$AL: 4.2 \text{ eV}, An: 4.67 \text{ eV}$$

vacuum level



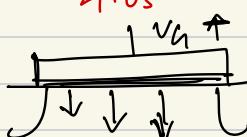
work func<sup>n</sup> = energy reqd  
for an e<sup>-</sup> to move from  
E\_F to vacuum

$$\chi_{Si} = \chi_{Si} + \frac{E_C - E_i}{q} + \frac{KT}{q} \ln \frac{N_A}{n_i}$$

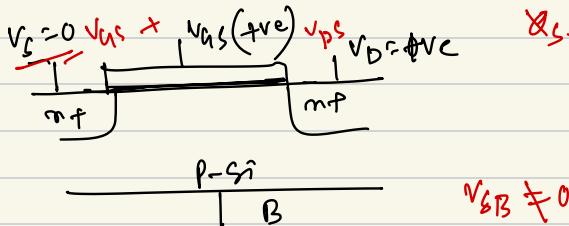
$$4.05 \quad 0.55$$

$$\text{const.}$$

$$V_{TH} = \text{const.} - \frac{Q_D}{C_{ox}}$$



$$Q_D = - \frac{2q\chi_{Si}N_A \cdot 2\chi_f}{\text{const.}} \rightarrow \text{in inversion}$$

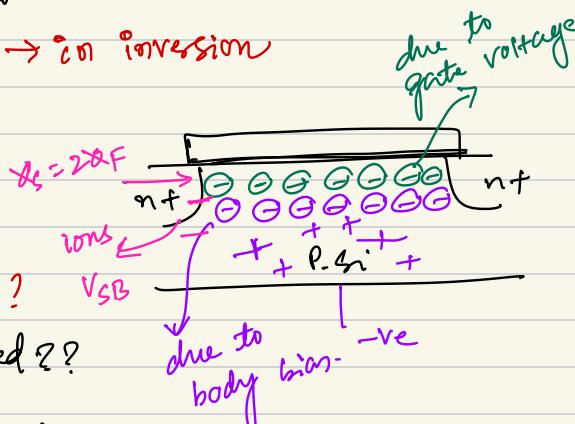


What if Body is not grounded ??

$$V_T' = \text{const.} - \frac{Q_D}{C_{ox}} \rightarrow \text{depletion region}$$

charge due to body bias.

$$\Delta V_T = V_T' - V_T = - \frac{Q_D}{C_{ox}} - \left( - \frac{Q_D}{C_{ox}} \right)$$



$$Q_0 = -\sqrt{2qN_A\epsilon_{Si}} \frac{\Delta S}{\downarrow}$$

$$\Delta S_F + V_{SB}$$

$$\Delta V_T = -\left[ \frac{-\sqrt{2qN_A\epsilon_{Si}(\Delta S_F + V_{SB})}}{\text{con}} \right] + \left[ \frac{-\sqrt{2qN_A\epsilon_{Si}\Delta S_F}}{\text{con}} \right]$$

$$\Rightarrow \frac{2qN_A\epsilon_{Si}}{\text{con}} \left[ \sqrt{\Delta S_F + V_{SB}} - \sqrt{\Delta S_F} \right]$$

$$\Delta V_T = \gamma \left[ \sqrt{\Delta S_F + V_{SB}} - \sqrt{\Delta S_F} \right]$$

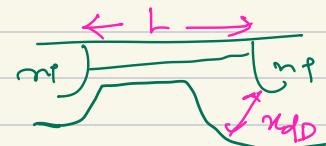
Change in  $V_{TH}$  due to body effect.

$\gamma$  = Body effect coefficient.

$L \approx x_D$  at drain side

↳ depletion region

short channel effect.



$$L = 10 \mu m \rightarrow \Delta L = 100 nm$$

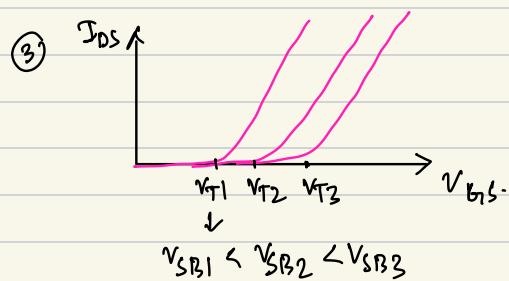
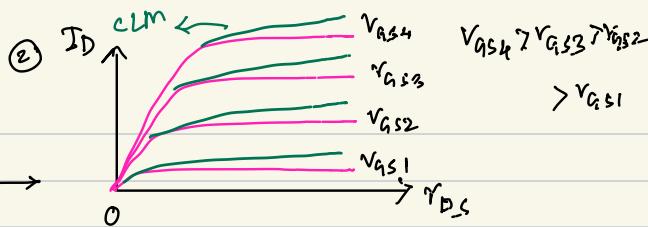
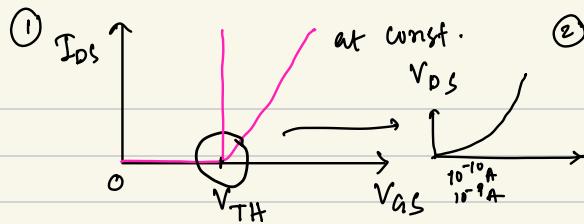
$$L = 500 nm \rightarrow \Delta L = 100 nm$$

$$\lambda V_{DS} = \frac{\Delta L}{L}$$

$$\textcircled{1} \quad \frac{100 n}{10 \mu m} = 10 \times 10^{-3}$$

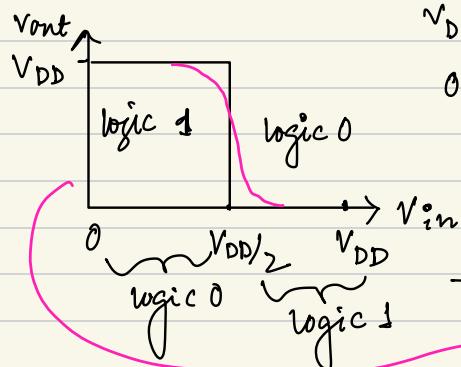
$$\textcircled{2} \quad \frac{100 n}{500 nm} = \frac{1}{5}$$





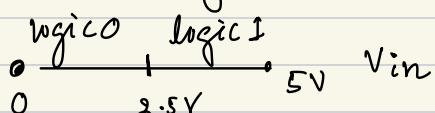
Inverter:  $A \rightarrow B$

most basic ckt.



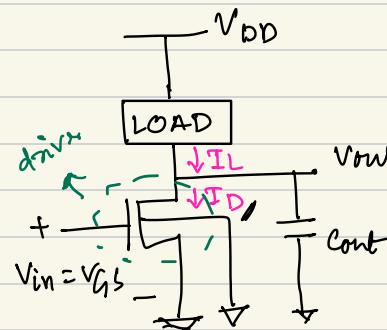
$V_{DD}$  = max<sup>m</sup> power supply

0 = min<sup>m</sup> power supply



$V_{in}$

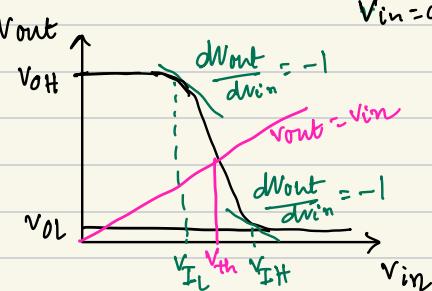
→ voltage Transfer Curve (VTC)  
(ideal VTC)

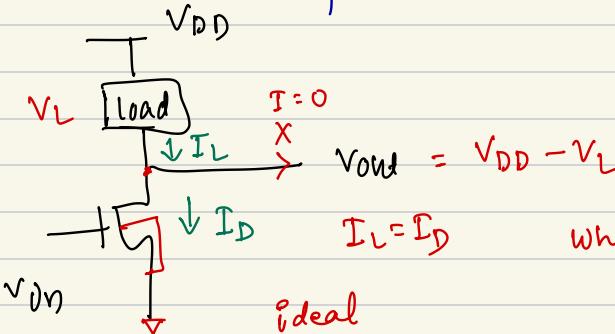
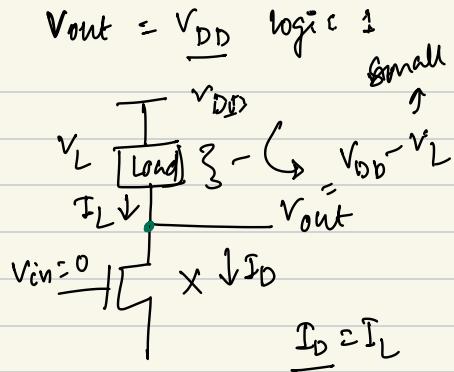
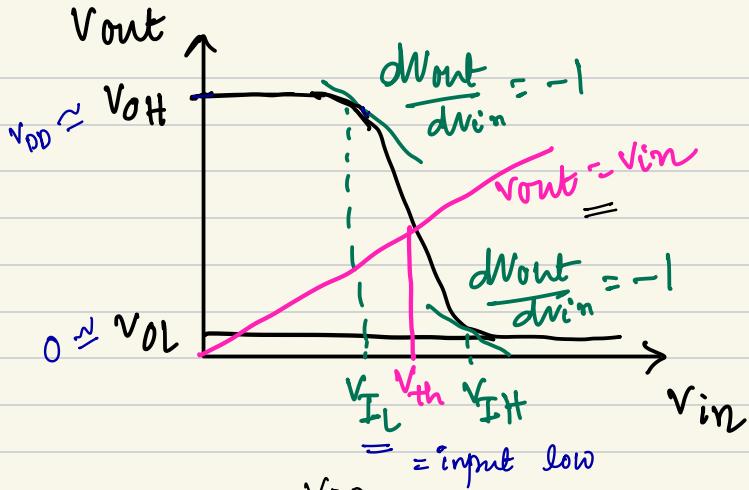


$I_L$  = load current ;  $I_D$  = drain current .

$V_{in} = 0$ ; nMOS off

$V_{out} = \text{high o/p voltage}$   
 $V_{OL} = \text{low o/p voltage}$





Practical

$$I_D \approx 10^{-9} A = I_L \rightarrow V_L \neq 0 \rightarrow \text{very small}$$

$$V_{out} \neq V_{DD} \text{ but } V_{out} = V_{OH} \approx V_{DD}$$

$$V_{out} = 5 \text{ logic 1} \text{ but } V_{out} = 4.9 \text{ logic 1}$$

$$\text{for low} \therefore V_{out} = 0 ; V_{DD} - V_L = 0 \Rightarrow V_{DD} = V_L$$

$$\text{ideal } V_{out} = 0 \text{ for logic 0}$$

$$\text{Practical } V_{out} = V_{OL} \approx 0 \text{ logic 0.}$$

Subthreshold Current

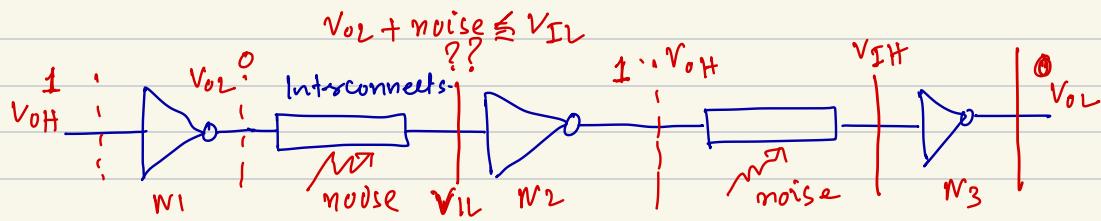
$V_{OH} = \text{max}^m$  output voltage for logic 1

$V_{OL} = \text{min}^m$  " " " for logic 0

$V_{IL} = \text{max}^m$  input voltage for which output is logic 0  
(low i/p voltage)

$V_{IH} = \text{min}^m$  input voltage for which output is logic 1  
(high i/p voltage)

$V_{TH}$  = at which  $V_{out} = V_{in}$

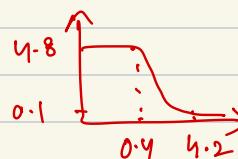
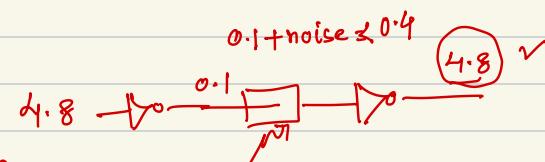


$$V_{OH} = 4.8$$

$$V_{OL} = 0.1$$

$$V_{IL} = 0.4$$

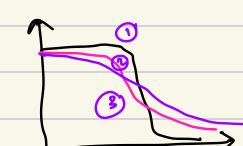
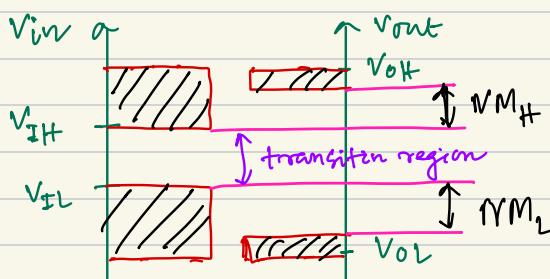
$$V_{PH} = 4.2$$



Noise Margin :-

$$NM_H = V_{OH} - V_{IH}$$

Noise margin  
for high signal level

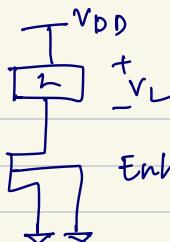


$$NM_L = V_{IL} - V_{OL}$$

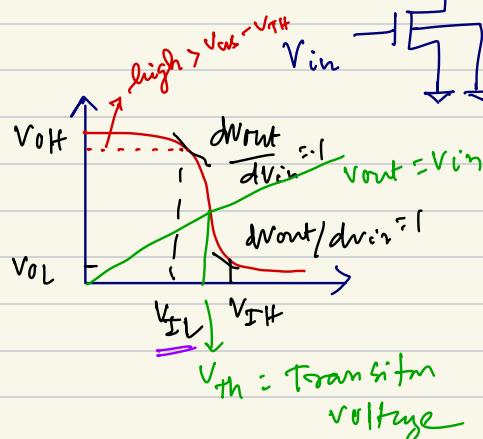
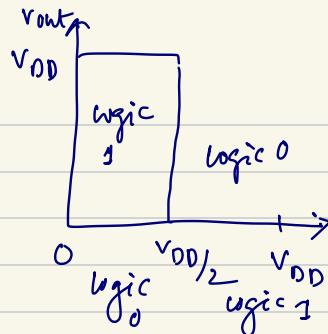
Noise margin for  
low signal level

$$\text{Transition region} = V_{IH} - V_{IL}$$

$$A \rightarrow D_0 \rightarrow B \quad B = \bar{A}$$



Enhancement  
in MOSFET



$$NM_L = V_{IL} - V_{OL}$$

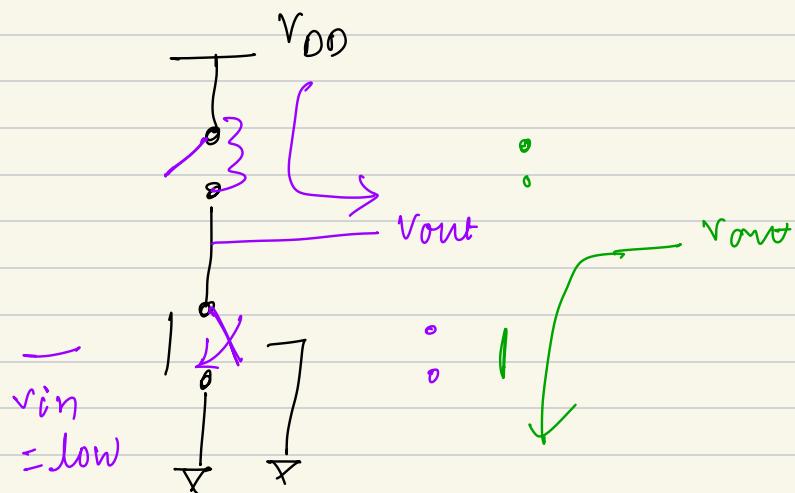
$$NM_H = V_{OH} - V_{IH}$$

$$\begin{aligned} V_{OH} &= \max^m \\ &\text{Vout} = \text{logic 1} \end{aligned}$$

$$V_{OL} = \min \text{ logic 0}$$

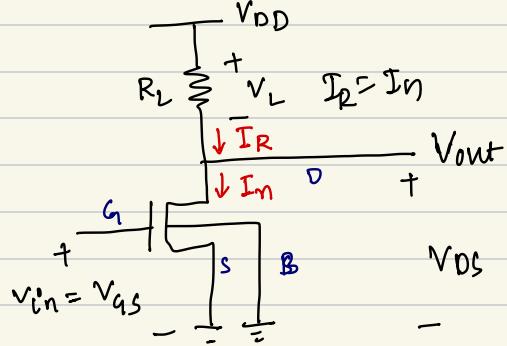
$$\begin{aligned} V_{IH} &= \min \quad i/p \text{ at } o/p = 0 \\ \min i/p v_{OH} &= \text{logic 2} \end{aligned}$$

$$\begin{aligned} V_{IL} &= \max^m \quad i/p \text{ at which } o/p = \text{logic 1} \\ \max i/p v_{OH} &= \text{logic 0} \end{aligned}$$



$$V_{in} = \text{high}$$

Resistive Load Inverter : No channel length modulation  $\lambda = 0$   
 No body effect :  $V_{SB} = 0$



$$(i) \underline{V_{in} = 0; I_D = 0} \Rightarrow V_{out} = V_{DD}$$

$$V_{out} = V_{DD} - I_R R_L$$

$$V_{out} = V_{DD}.$$

$$(ii) \underline{V_{in} = low > V_{TO}} \Rightarrow V_{ds} > V_{TO}$$

$$I_n \text{ small} = I_R$$

$\Rightarrow V_{out}$  is still high.  $= V_{DS}$

$$V_{GS} - V_T = \text{small}$$

for nmos ;  $V_{DS} > V_{GS} - V_T$  Saturated.

$$I_n = \frac{1}{2} \mu_n C_o x \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_n = \frac{1}{2} K_n^1 (V_{in} - V_T)^2 \quad K_n^1 = \mu_n C_o \frac{W}{L}$$

(iii)  $V_{in}$  high :  $V_{GS}$  high.

$I_R \uparrow$  as  $I_n \uparrow \Rightarrow V_{out} = V_{DS} \downarrow \downarrow < V_{GS} - V_T$

$$I_n = \frac{1}{2} K_n \frac{W}{L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad \text{linear mode}$$

$$I_n = I_R = \frac{1}{2} K_n \frac{W}{L} [2(V_{in} - V_T)V_{out} - V_{out}^2]$$

$$V_{OH} = ??$$

$$V_{out} = V_{DD} - I_R R_L; \text{ when } V_{in} < V_{TO}$$

↓  
 logic high (1)  
 0) P at low  $V_{in}$   
 (0)

$$\Rightarrow V_{out} = V_{OH} = V_{DD}.$$

nMOS is off

$$I_n = 0 = I_R$$

$$\Rightarrow I_R R_L = 0$$

$V_{OL} = ?$  logic low (0) when  $V_{in}$  is high.

$$V_{in} = V_{OH} = V_{DD}$$

$$K_n = \mu_n C_o \frac{W}{L}$$

$\Rightarrow$  nmos is in linear mode

$$I_n = I_R = \frac{1}{2} K_n [2(V_{GS} - V_T) V_{DS} - V_{DS}^2]$$

$$= \frac{1}{2} K_n [2(V_{in} - V_T) V_{out} - V_{out}^2]$$

$$V_{out} = V_{DD} - I_R R_L$$

$$\Rightarrow I_R = \frac{V_{DD} - V_{out}}{R_L} = \frac{1}{2} K_n [2(V_{in} - V_T) V_{out} - V_{out}^2]$$

$$\Rightarrow V_{out}^2 - 2(V_{DD} - V_T + \frac{1}{K_n R_L}) \cdot V_{out} + \frac{2}{K_n R_L} V_{DD} = 0$$

$$\Rightarrow V_{OL}^2 - 2(V_{DD} - V_T + \frac{1}{K_n R_L}) V_{OL} + \frac{2}{K_n R_L} \cdot V_{DD} = 0$$

$$\left[ \begin{array}{l} a = 1 \\ b = 2(V_{DD} - V_T + \frac{1}{K_n R_L}) \\ c = \frac{2}{K_n R_L} \cdot V_{DD} \end{array} \right] \quad \left[ \begin{array}{l} a \cdot n^2 + b \cdot n + c = 0 \\ \Rightarrow n = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \end{array} \right]$$

$$\Rightarrow \boxed{\frac{V_{OL}}{1} = V_{DD} - V_T + \frac{1}{K_n R_L} - \left[ \left( V_{DD} - V_T + \frac{1}{K_n R_L} \right)^2 - \frac{2V_{DD}}{K_n R_L} \right]}$$

$$\downarrow \quad \uparrow$$

$\frac{1}{K_n R_L} \uparrow$

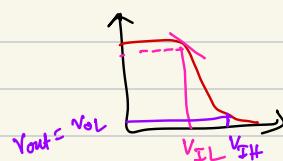
✓

$V_{IL} = ??$  smaller  $V_{in}$  at which  $\frac{dV_{out}}{dV_{in}} = -1$  ✓

↳  $V_{out}$  is still high  $\rightarrow V_{out} > V_{in} - V_T \rightarrow$  Saturat<sup>ion</sup>

$$I_n = I_R = \frac{1}{2} k_n [V_{in} - V_T]^2$$

$$\Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{1}{2} k_n [V_{in} - V_T]^2$$



Differentiate w.r.t  $V_{in}$

$$\Rightarrow -\frac{1}{R_L} \frac{dV_{out}}{dV_{in}} = k_n (V_{in} - V_T) \xrightarrow{-1}$$

$$\Rightarrow \frac{1}{R_L} = k_n (V_{IL} - V_T) \Rightarrow V_{IL} = V_T + \frac{1}{k_n R_L}$$

✓

When  $V_{in} = V_{IL} \Rightarrow V_{out} = ??$

$$\begin{aligned} V_{out} &= V_{DD} - I_R R_L = V_{DD} - \frac{k_n}{2} (V_{IL} - V_T)^2 \cdot R_L \\ &= V_{DD} - \frac{k_n}{2} \left( V_T + \frac{1}{k_n R_L} - V_T \right)^2 \end{aligned}$$

$$V_{out} (V_{in} = V_{IL}) = V_{DD} - \frac{1}{2 k_n R_L}$$

✓

$V_{IH} = ??$  higher i/p voltage at which  $\frac{dV_{out}}{dV_{in}} = -1$

at this p.t  $V_{out}$  is low  $\Rightarrow V_{out} < V_{in} - V_T$

$$I_n = I_R = \frac{k_n}{2} \left[ 2(V_{in} - V_T) V_{out} - V_{out}^2 \right] \quad \text{Linear region}$$

$$\Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \left[ 2(V_{in} - V_T) V_{out} - V_{out}^2 \right]$$

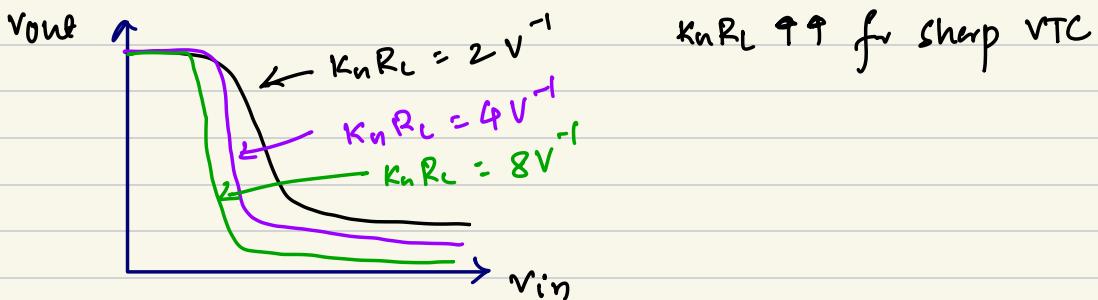
Differentiate w.r.t  $V_{in}$

$$\Rightarrow -\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \cdot 2(V_{in} - V_T) \frac{dV_{out}}{dV_{in}} + \frac{k_n}{2} \cdot 2V_{out} - 2V_{out} \frac{dV_{out}}{dV_{in}} \cdot \frac{k_n}{2}$$

$$V_{TH} = V_{TH} + \sqrt{\frac{8}{3} \frac{V_{DD}}{K_n R_L}} - \frac{1}{K_n R_L}$$

$$V_{out} (V_{in} = V_{TH}) = \sqrt{\frac{2}{3} \frac{V_{DD}}{K_n R_L}}$$

$K_n R_L \rightarrow$  as large as possible  $\rightarrow \frac{1}{K_n R_L}$  small.



$$\rightarrow \text{Power} = V \cdot I ; \quad \underbrace{V_{in} = \text{low} = V_{OL}}_{\downarrow \text{nmOS off}} \Rightarrow V_{out} = V_{OH}$$

$$V_{in} = \text{high} = V_{OH} \quad V_{out} = V_{OL} \quad \text{Power} = 0$$

$$I_n = I_p \neq 0 \quad \text{assume} \rightarrow 50\% \text{ of time } V_{in} = V_{OL}$$

$$\text{test} \rightarrow V_{in} = V_{OH}$$

$$\Rightarrow I_R = \frac{V_{DD} - V_{out}}{R_L}$$

$$P_{avg} = \frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L}$$

Q.  $V_{DD} = 5V$ ;  $K_n^1 = 30 \mu A/V^2$ ;  $V_{TO} = 1V$   $K_n = K_n^1 w/L$   
 Design the inverter with  $V_{OL} = 0.2V$ ?  $\hookrightarrow m_n C_{ox}$   
 find  $(w/L)$  &  $R_L$  to achieve required  $V_{OL}$  ??

A.  $V_{OL} = 0.2V \rightarrow V_{in} = V_{OH} = V_{DD} = 5V \rightarrow$  nmos is in linear.

$$\frac{V_{DD} - V_{out}}{R_L} \xrightarrow{\rightarrow V_{OL}} = \frac{K_n^1}{2} \left( \frac{W}{L} \right) \left[ 2(V_{GS} - V_T) \xrightarrow{V_{in} = V_{DD} = 5V} V_{DS} - V_{DS}^2 \right]$$

$$\Rightarrow \frac{5 - 0.2}{R_L} = \frac{30 \times 10^{-6}}{2} \left( \frac{W}{L} \right) [2 \cdot (5 - 1) 0.2 - 0.2^2]$$

$$\Rightarrow \boxed{\left( \frac{W}{L} \right) \cdot R_L = 2.05 \times 10^5 \Omega} \quad * P_{avg} = \frac{V_{DD}}{2} \frac{V_{DD} - V_{OL}}{R_L}$$

$$= \frac{5}{2} \frac{5 - 0.2}{R_L} = 12 \frac{1}{R_L}$$

$\frac{W}{L}$	$R_L (k\Omega)$	$P_{avg} (\mu W)$
1	20.5	5.8
2	10.25 ↑	11.7 ↑
3	6.84	17.54
4	5.13	23.39
5	4.10	29.27

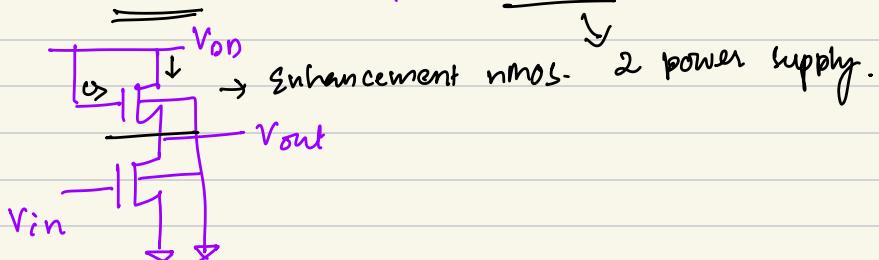
\*  $R = \frac{L}{A} \rightarrow$  <sup>cross</sup><sub>scat</sub> area  
 as  $R \propto$ ; the silicon area increases.

\* in resistive load inv. if power dissipation reduce area increases & vice versa.

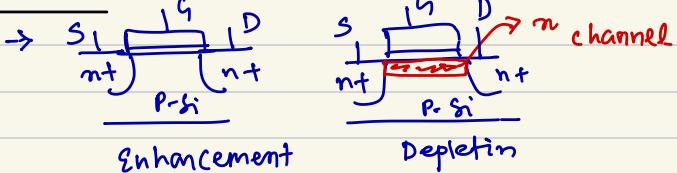
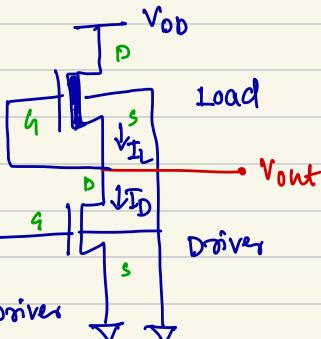
by Area-Power trade off.



Enhancement load inverter



Depletion MOSFET load inverter:- → Area is less due to DMOSFET



1 extra process step to create n channel in D MOSFET

→ Gate & Source of DMOSFET connected

$$V_{GS} = 0 \quad \checkmark$$

$$\rightarrow V_{TH} \text{ of DMOSFET} = -V_0$$

DMOSFET always on.

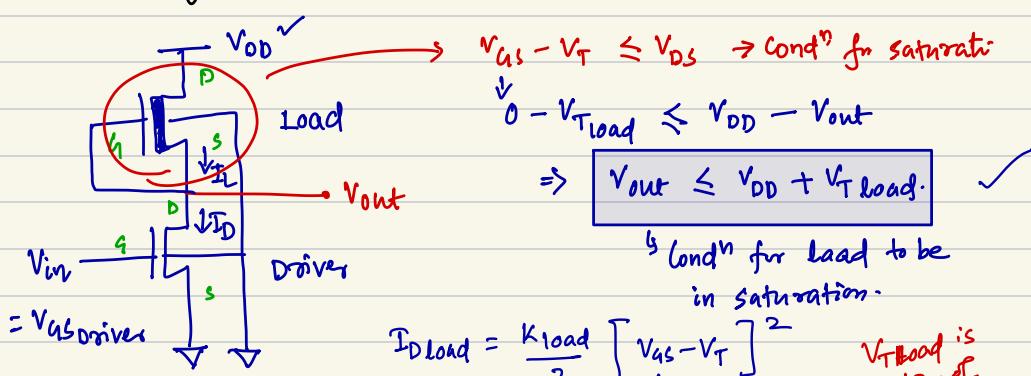
→ Current eqn for DMOSFET is same as enhancement type  
only difference is  $V_{TH} = -V_0$ .

→ Body effect = ? is present as source connected to Vout & body to ground.

$$V_{TH\text{load}} = V_{T\text{load}} + \frac{1}{2} \left[ \sqrt{2\alpha_F} + V_{out} - \sqrt{2\alpha_F} \right]$$

Threshold volt- without  $V_{SB\text{load}}$ .  
of load DMOSFET body effect.

→ Operating Region:- When  $V_{out} = \text{low}$



$$V_{GS} - V_T \leq V_{DS} \rightarrow \text{Cond'n for saturation:}$$

$$0 - V_{T\text{load}} \leq V_{DD} - V_{out}$$

$$\Rightarrow V_{out} \leq V_{DD} + V_{T\text{load}}. \quad \checkmark$$

<sup>b</sup> Cond'n for load to be in saturation.

$$I_{D\text{load}} = \frac{k_{load}}{2} \left[ \frac{V_{GS} - V_T}{V_0} \right]^2$$

$$I_{D\text{load}} = \frac{k_{load}}{2} \left[ -V_{T\text{load}} (V_{out}) \right]^2$$

$V_{T\text{load}} (V_{out}) \rightarrow$  function of  $V_{out}$

$\rightarrow V_{out} = \text{large}$  : Depletion MOSFET load  $\rightarrow$  linear region

$$I_{load} = \frac{K_{load}}{2} \left[ 2 [V_{GS} - V_{Tload}] V_{DS} - V_{DS}^2 \right]$$

$$I_{load} = \frac{K_{load}}{2} \left[ 2 |V_{Tload}(V_{out})| (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

V <sub>in</sub>	V <sub>out</sub>	Driver operating region	Load operating region
$\checkmark \underline{V_{OL}}$	$V_{OH}$ ✓	Cutoff ✓	Linear ✓
$\checkmark \underline{V_{IL}}$	$\approx V_{off}$ ✓	Saturation ✓	Linear ✓
$\checkmark \underline{V_{IH}}$	$\approx V_{OL}$	linear	Saturation
$\checkmark \underline{V_{OH}}$	$V_{OL}$	linear	Saturation

$V_{off} = ??$   $V_{OH}$  output voltage ( $V_{out}$ ) when  $V_{in} = V_{OL}$  or 0.

Driver nmos = Cutoff ; Load DMOS = linear.

$$I_{Driver} = 0 = I_{load} = \frac{K_{load}}{2} \left[ 2 |V_{Tload}(V_{OH})| (V_{DD} - V_{OH}) - (V_{DD} - V_{OH})^2 \right]$$

Solution :  $V_{OH} = V_{DD}$

$V_{OL} = ??$   $V_{out} = V_{OL}$  when  $V_{in} = V_{OH}$

Driver nmos = linear ; Load DMOS = Saturation.

$$\Rightarrow \frac{K_{Driver}}{2} \left[ 2(V_{OH} - V_{TO}) V_{OL} - V_{OL}^2 \right] = \frac{K_{load}}{2} \left[ -V_{Tload}(V_{OL}) \right]^2$$

$\underbrace{I_{Driver}}_{\text{Idriver}}$        $\underbrace{I_{load}}_{I_{load}}$

bring  $\rightarrow ax^2 + bx + c = 0$

$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \left[ \frac{K_{load}}{K_{Driver}} \right] |V_{Tload}(V_{OL})|^2}$$

let's  $V_{T\text{load}} = V_T$  (given)

(i) use it to find  $V_{IL}$

(ii) now use obtained  $V_{IL}$  to find  $V_{I\text{load}}$ .

(iii) Again use new  $V_{I\text{load}}$  to find  $V_{OL}$ .

$V_{IL} = ??$   $\rightarrow$  max<sup>m</sup> voltage for which D/P is  $\approx V_{OH}$

$V_{in} = V_{IL} \rightarrow$  driver nMOS = saturation load = linear

$$\Rightarrow \frac{k_{\text{driver}}}{2} \left[ V_{IL} - V_{TO} \right]^2 = \frac{k_{\text{load}}}{2} \left[ 2 |V_{I\text{load}}(V_{out})| (V_{DD} - V_{out}) - (V_{DD} - V_{DTH})^2 \right] \quad \text{--- (1)}$$

$I_{\text{drive}}$      $I_{\text{load}}$

at  $V_{IL}$ ;  $dV_{out}/dV_{in} = -1$

differentiate both side w.r.t  $V_{in}$  & apply  $\frac{dV_{out}}{dV_{in}} = -1$

$$\Rightarrow V_{IL} = V_{TO} + \left( \frac{k_{\text{load}}}{k_{\text{driver}}} \right) [V_{out} - V_{DD} + |V_{I\text{load}}(V_{out})|]$$

(i) assume  $V_{out} = V_{OH}$  &  $V_{in} = V_{IL} \rightarrow$  find  $V_{TO}$

$$V_T \leq 1V$$

(ii) find  $V_{IL}$  with obtained  $V_{T\text{load}}$   $\rightarrow V_{IL} = f(V_{out})$

$$V_{IL} = 0.5V$$

(iii) use eqn (1) to find  $V_{IL}$

$V_{IH} = ??$  : When  $V_{in} = V_{IH}$ ; nMOS = linear : load pMOS = saturation

$$\Rightarrow \frac{k_{\text{driver}}}{2} \left[ 2 (V_{in} - V_{TO}) V_{out} - V_{out}^2 \right] = \frac{k_{\text{load}}}{2} \left[ -V_{I\text{load}}(V_{out}) \right]^2$$

differentiate at pt  $\frac{dV_{out}}{dV_{in}} = -1$

$$\Rightarrow V_{IH} = V_{TO} + 2V_{out} + \frac{k_{\text{load}}}{k_{\text{driver}}} \left[ -V_{I\text{load}}(V_{out}) \right] \left[ \frac{dV_{I\text{load}}}{dV_{out}} \right]$$

$$\frac{dV_{I\text{load}}}{dV_{out}} = \frac{\sqrt{2}}{2\sqrt{2V_F} + V_{out}}$$

(iv)  $V_{IH} = f(V_{out})$

(v)  $V_{out} \approx V_{IH}$

(i) assume:  $V_{out} = V_{OL}$  : (ii)  $V_{I\text{load}}(V_{out} = V_{OL}) = ??$  (iii)  $\frac{dV_{I\text{load}}}{dV_{out}} = ??$

$$V_{OL} = V_{DD} - V_{TO} - \sqrt{(V_{DH} - V_{TD})^2 + \frac{K_{load}}{K_{driver}} |V_{T,load}(V_{OL})|^2}$$

~~$\frac{V_{DD}}{V_{DD}}$~~

ideal  $\Rightarrow V_{DH} = V_{DD}$

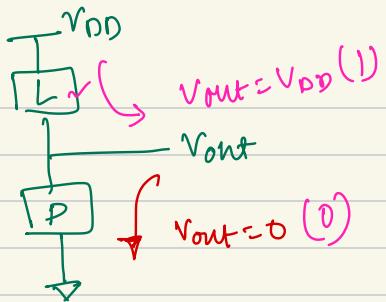
$V_{OL} = 0 \rightarrow V_{OC}$  as small as possible

$$\frac{K_{load}}{K_{driver}}$$

$$(V_{DH} - V_{TO})^2 - \frac{K_{load}}{K_{driver}} |V_{T,load}|^2$$

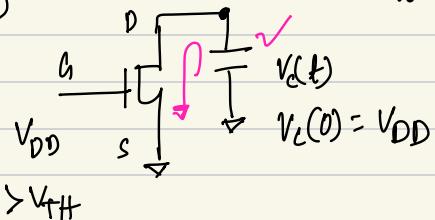
$$\text{load to drivers ratio } (K_D) = \frac{K_{load}}{K_{driver}} = \frac{\mu_n C_{ox} (w/l)_{load}}{\mu_n C_{ox} (w/l)_{driver}} = (w/l)_{ratio} = \frac{(w/l)_{load}}{(w/l)_{driver}}$$

$V_{out} = V_{DD}$



nmos → Which one is load  
pmos → & which one drives.

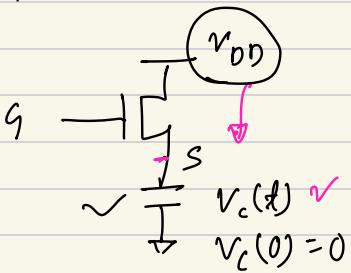
(i)



When  $V_{in} = V_{GS} = \underline{V_{DD}}$  Capacitor is discharging

$$\frac{V_c(t)}{\text{Strong logic } 0} = 0$$

(ii)



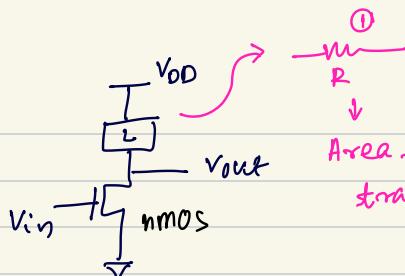
$$V_c(0) = 0 ; V_{in} = V_{DD}$$

$$\begin{aligned} V_{DD} &= 5V \\ V_{TH} &= 1V \end{aligned}$$

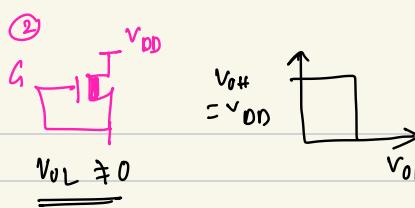
$$V_{DD} - V_c(t) > V_{TH} \quad \text{at} \quad \begin{array}{c} \downarrow \\ V_G \\ \downarrow \\ V_S \end{array} \Rightarrow \underline{V_c(t)} \leq V_{DD} - V_{TH}$$

$$V_c(t)_{(\max)} = V_{DD} - V_{TH}$$

Weak logic 1

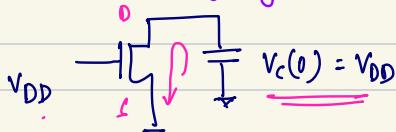


Area-power  
trade off.



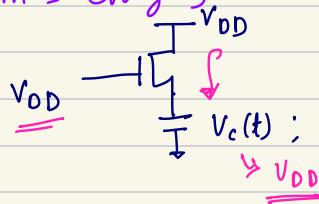
we need.

## nmos discharging



as long as  $V_C(t) = 0 \rightarrow$  strong 0

## nMOS Charging

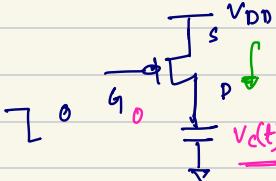


$$V_r(0) = 0 \quad ; \quad V_{GS} = V_{DD} - V_c(t) > V_{TH,n}$$

$$V_{DD} - V_C(t) < V_{TH,N} \rightarrow \text{NMOS off}$$

$V_{DD}$   $\int$  maximum value to which capacitor  
weak logic 1 can be charged.

## PMOS - charging

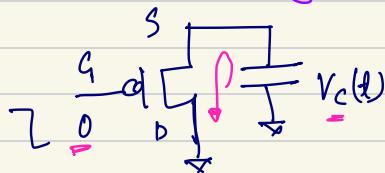


$$V_{GS} = -V_{DD} \approx V_{TH,P} ; V_C(t) \text{ going to charge}$$

to  $V_{DD} \rightarrow \text{logic 1}$

→ Strong logic 1

pmos discharging



$$V_c(0) = V_{DD} \quad ; \quad V_{CISP} = -V_c(t)$$

$$\Rightarrow -v_c(t) < v_{TP} \Rightarrow v_c(t) > -v_{TP}$$

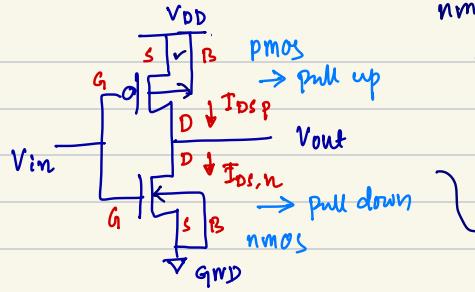
$V_C(t)$  can only be discharged up to  $V_{TP}$   
not to 0 → weak logic 0

\* nmos pulled-down the output node voltage to 0

\* pmos pulled- up the output node voltage to  $V_{DD}$

→ Hence; PMOS is used as pull up device / network (PVN)  
NMOS is used as pull down device / network (PDN)

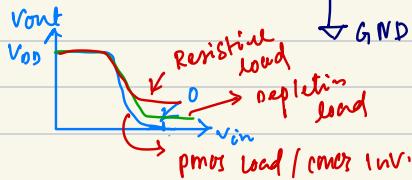
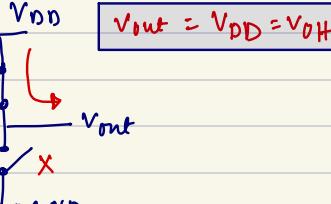
## c mos Inverter:-



$$V_{in} = 0 \therefore V_{qsn} = 0 < V_{Tn} \\ \text{NMOS off}$$

$$V_{qsp} = -V_{DD} < V_{Tp}.$$

PMOS on



$\rightarrow$  steady state power dissipation  $\approx 0$

In other circuits; power dissipation is high as every time driver NMOS is on : steady state current drawn from power source.

But in CMOS  $\rightarrow$  no connection betw VDD to GND.

$$V_{qsn} = V_{in} ; \quad V_{qsp} = V_{in} - V_{DD}$$

$$V_{DSn} = V_{out} ; \quad V_{Dsp} = V_{out} - V_{DD}$$

$$V_{qsn} - V_{Tn} \leq V_{DS}$$

$$V_{qsp} - V_{Tp} \geq V_{Dsp}$$

## Complementary MOS Inverter.

NMOS + PMOS both are complementary

When  $V_{in} = \text{high} (V_{DD}) \rightarrow \text{NMOS on}$   
 $\text{PMOS off}$

$$V_{qsn} = V_{in}$$

$$V_{qsp} = V_{in} - V_{DD}$$

$$V_{DD}$$

$$\times$$

$$I_{DP}$$

$$I_{Dn}$$

$$GND$$

$$V_{in} = V_{DD}$$

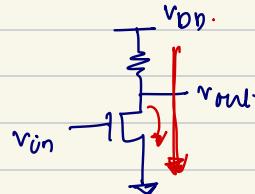
$$\rightarrow V_{qsp} = 0 > V_{Tp}$$

$$V_{out} = 0 = V_{OL}$$

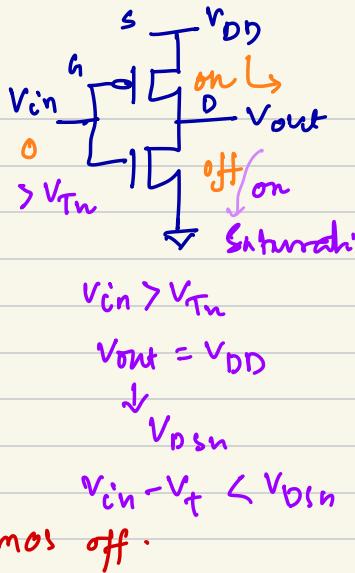
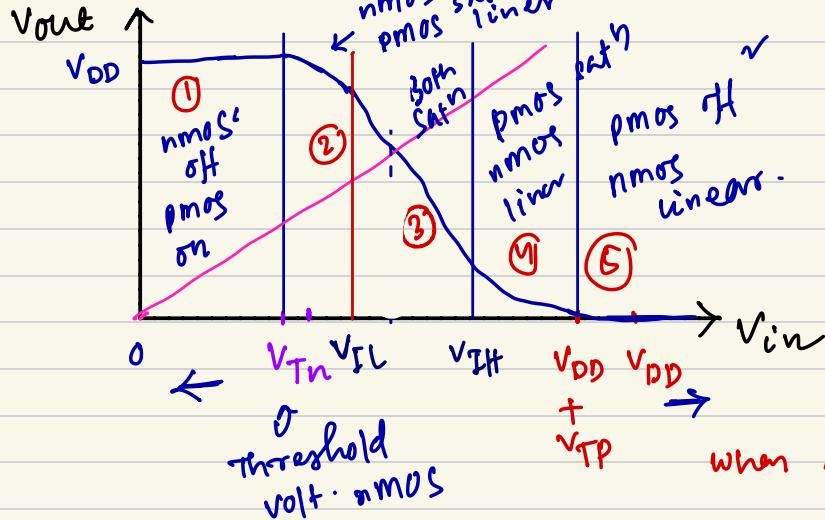
$$I_{Dp} = 0 = I_{Dn}$$

In CMOS inverter;

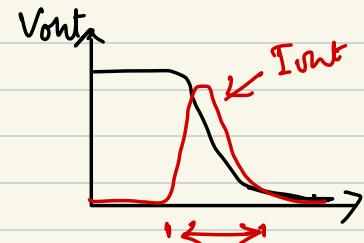
The output voltage ( $V_{out}$ )  
 Swings from 0 to  $V_{DD}$   
 i.e. full power supply



## Voltage Transfer Curve (VTC) :-



Region	$V_{in}$	$V_{out}$	nmos	pmos	$V_{ASp} \geq V_{Tp}$
1	$< V_{Th}$	$V_{off} = V_{DD}$	Cutoff	Linear	$\Rightarrow V_{in} - V_{DD} > V_{Tp}$
2	$V_{IL}$	$\approx V_{off}$	Sat <sup>h</sup>	Linear	$\Rightarrow V_{in} > V_{DD} + V_{Tp}$
3	$V_{th}$	$V_{th}$	Sat <sup>h</sup>	Sat <sup>h</sup>	
4	$V_{IH}$	$\approx V_{D}$	Linear	Sat <sup>h</sup>	
5	$> V_{DD} + V_{Tp}$	$V_{D}$	Linear	Cutoff	



$V_{IL} = ?$  when  $V_{in} = V_{IL}$

$\Rightarrow$  PMOS = Linear, NMOS Saturation

$$I_{DP}$$

$$I_{Dn}$$

$$\Rightarrow \frac{k_n}{2} (V_{AS} - V_{Th})^2 = \frac{k_p}{2} [2(V_{AS} - V_{Tp})] V_{Dsp} - V_{Dsp}^2$$

$$\Rightarrow \frac{k_n}{2} (V_{in} - V_{Th})^2 = \frac{k_p}{2} [2(V_{in} - V_{DD} - V_{Tp})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

differentiating w.r.t  $V_{in}$  & applying  $\frac{dV_{out}}{dV_{in}} = -1$

$$\Rightarrow K_n (V_{in} - V_{Tn}) = K_p \left[ (V_{in} - V_{DD} - V_{Tp}) \frac{dV_{out}}{dV_{in}} + (V_{out} - V_{DD}) \right. \\ \left. - (V_{out} - V_{DD}) \frac{dV_{out}}{dV_{in}} \right]$$

put  $V_{in} = V_{IL}$

$$\Rightarrow V_{IL} = \frac{2V_{out} + V_{Tp} - V_{DD} + K_p V_{Tn}}{1 + K_p}$$

$$\text{where } K_R = \frac{K_n}{K_p}$$

$V_{IH} = ??$  when  $V_{in} = V_{IH}$ ; nmos linear  
pmos saturation

$$\frac{K_n}{2} \left[ 2(V_{S_n} - V_{Tn}) V_{out} - V_{DD}^2 \right] = \frac{K_p}{2} (V_{out} - V_{Tp})^2 \\ = \frac{K_n}{2} \left[ 2(V_{in} - V_{Tn}) V_{out} - V_{DD}^2 \right] = \frac{K_p}{2} (V_{in} - V_{DD} - V_{Tp})^2$$

differentiate w.r.t  $V_{in}$  & apply  $\frac{dV_{out}}{dV_{in}} = -1$   
&  $V_{in} = V_{IH}$

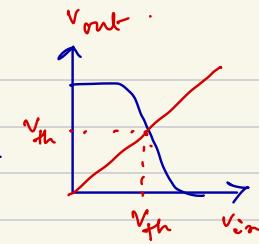
$$V_{IH} = \frac{V_{DD} + V_{Tp} + K_p (2V_{out} + V_{Tn})}{1 + K_p}$$

$V_{th} = ??$  Both nmos & pmos in saturation

$$\frac{k_n}{2} (V_{in} - V_{Tn})^2 = \frac{k_p}{2} (V_{out} - V_{TP})^2$$

$$\Rightarrow \frac{k_n}{2} (V_{in} - V_{th})^2 = \frac{k_p}{2} (V_{in} - V_{DD} - V_{TP})^2$$

at  $V_{th} = V_{in} = V_{out} = V_{th}$



$$\Rightarrow \frac{k_n}{2} (V_{th} - V_{Tn})^2 = \frac{k_p}{2} (V_{th} - V_{DD} - V_{TP})^2$$

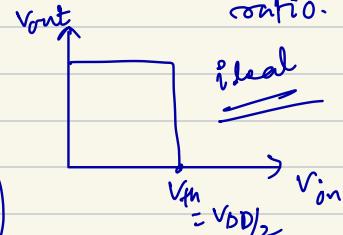
$$\Rightarrow V_{th} = V_{Tn} + \frac{1/k_p (V_{DD} + V_{TP})}{(1 + 1/k_p)}$$

$$k_p = \frac{k_n}{k_p}$$

= Transconductance ratio.

for ideal inverter?  $V_{th} = V_{DD}/2$

$$\sqrt{1/k_p} = \frac{V_{th} - V_{Tn}}{V_{DD} + V_{TP} - V_{th}}$$



$$\Rightarrow k_p = \left[ \frac{V_{DD} + V_{TP} - V_{th}}{V_{th} - V_{Tn}} \right]^2$$

$$= \left[ \frac{V_{DD} + V_{TP} - 0.5 V_{DD}}{0.5 V_{DD} - V_{Tn}} \right]^2 = \left[ \frac{0.5 V_{DD} + V_{TP}}{0.5 V_{DD} - V_{Tn}} \right]^2$$

pmos & nmos symmetry to each other:  $V_{Tn} = |V_{TP}|$

$$k_p = 1 \text{ ideal inverter.}$$

$$k_p = \frac{k_n}{k_p} = \frac{(W/L)_n}{(W/L)_p} \cdot \frac{\mu_n}{\mu_p}$$

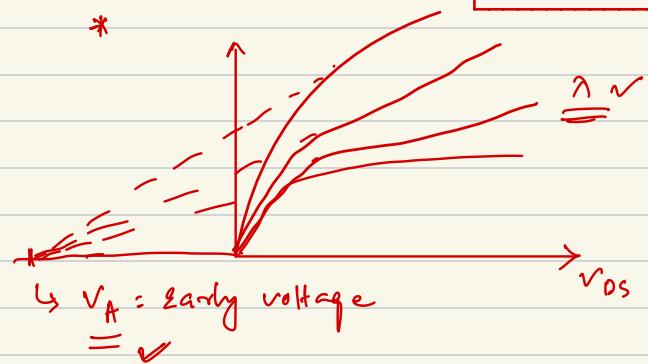
$$\frac{0.5 V_{DD} - V_{Tn}}{0.5 V_{DD} + V_{TP}} = 1$$

$$\frac{V_{Tn} = -V_{TP}}{0.7 - (-0.7)} = 0.7$$

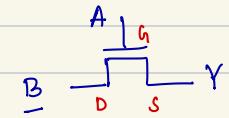
$$k_p^2 \frac{\mu_n}{\mu_p} \frac{(w/l)_p}{(w/l)_n} = 1 \Rightarrow \frac{(w/l)_n}{(w/l)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230 \text{ cm}^2/\text{V.s}}{580 \text{ cm}^2/\text{V.s}}$$

$\approx \frac{1}{2.5}$

$$\Rightarrow (w/l)_p = 2.5 (w/l)_n.$$



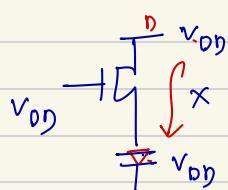
Pass Transistor logic :- Transistor that parses the logic I/O.



$$A = 1 \quad (\approx V_{DD}) \rightarrow \text{PMOS on}$$

$$B = 1 \quad (\approx V_{DD}) \rightarrow Y = 1$$

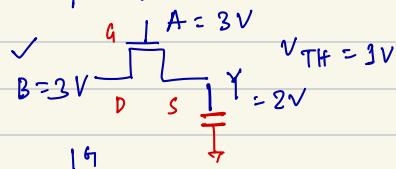
$$Y = AB$$



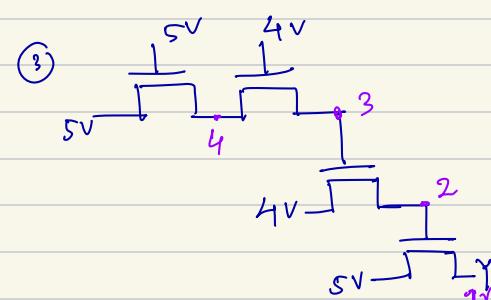
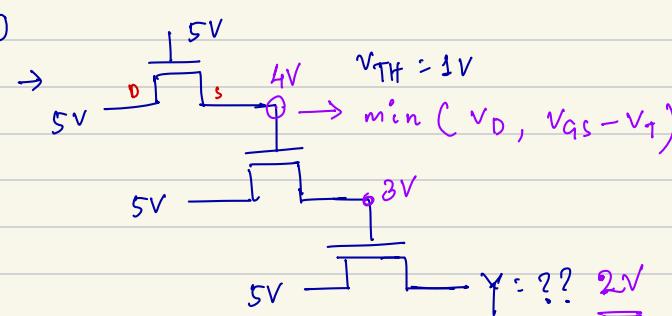
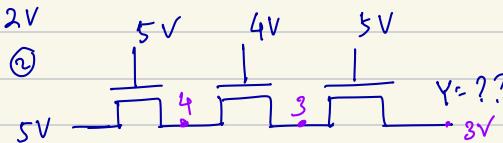
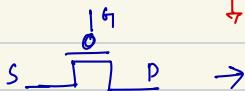
$$\text{if } A = 0 \text{ or } B = 0 \text{ then } Y = 0$$

A	B	Y (AND)
0	0	0
0	1	0
1	0	0
1	1	1

$\frac{1}{V_{DD}} \neq V_{DD}$   
 $(\approx V_{DD})$   
 $\downarrow$   
weak logic 1



$$\begin{aligned} V_{GS} &> V_{TH} \\ \Rightarrow A - Y &> 3V \\ \Rightarrow 3 - Y &> 1V \\ \Rightarrow Y &< 2V \end{aligned}$$



(i)  $V_{GS} - V_T$  at output

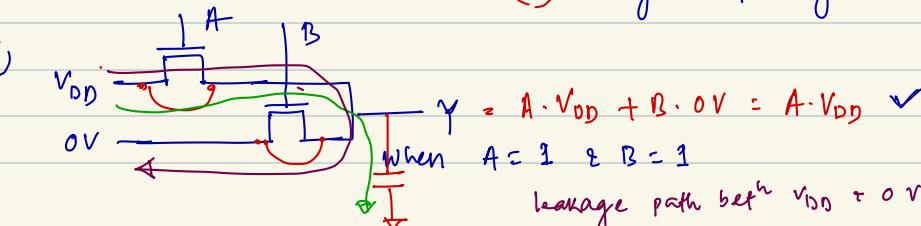


Let's nmos on  $\rightarrow$

resistance of channel  $= R_{DS}$

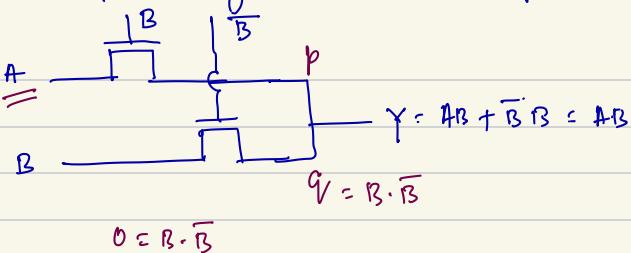
delay  $\rightarrow$  RC delay

(ii) delay in passing the signal.



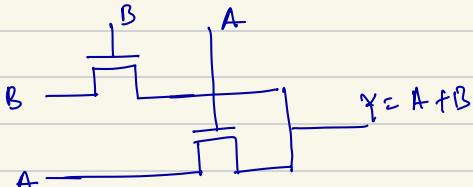
(i) AND gate using CPL :-  $\rightarrow$  complementary pass transistor logic.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

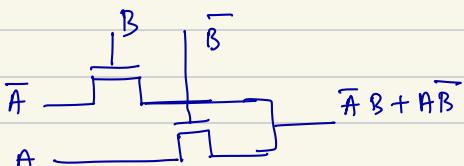


(ii) OR

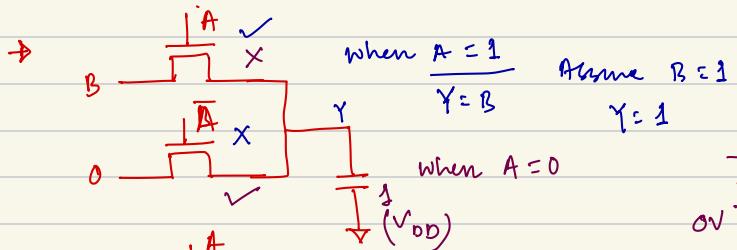
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



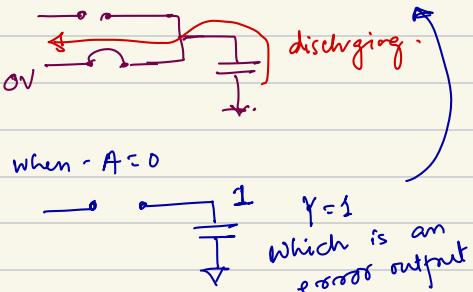
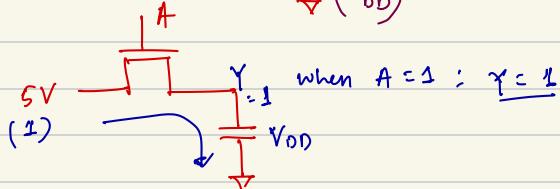
(iii) XOR =  $Y = \overline{AB} + A\overline{B}$



(iv) XNOR :-  $Y = AB + \overline{A}\overline{B}$



\* There should be a ✓ changing & discharging path.

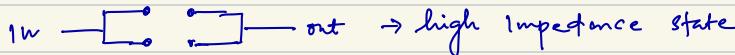
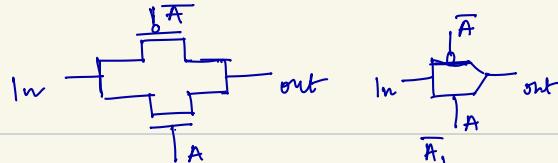


which is an error output

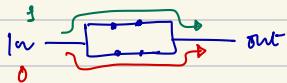
## Transmission Gate (TG) :-

Both pmos & nmos connected in parallel

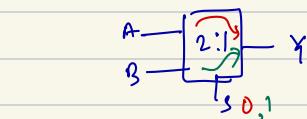
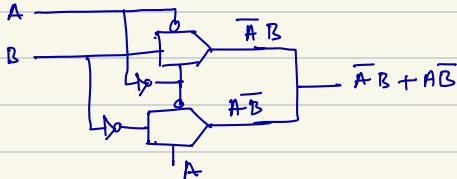
when  $A = 0$  : Both off



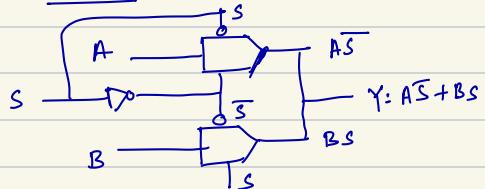
when  $A = 1$  : Both on



XOR :-



2:1 MUX       $Y = A\bar{S} + B\bar{S}$



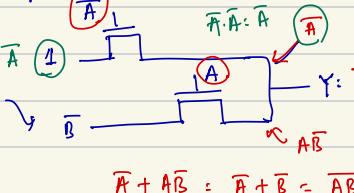
NAND gate using Pass transistor :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

When  $A=0$ :  
 $A=\bar{1}$ ;  $Y=1$   
 $A=\bar{1}$ ;  $Y=\bar{B}$   
 Gate      input

we need one control signal - Gate

i/p      "      drain



$$\bar{A} + \bar{A}\bar{B} = \bar{A} + \bar{B} = \bar{AB}$$

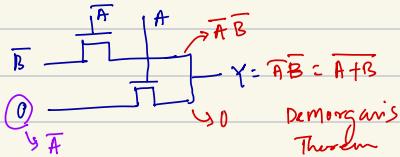
NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$A=0 \rightarrow Y=B$$

$$A=1 \rightarrow Y=0$$

↓      ↓  
 (control)      D(i/p)



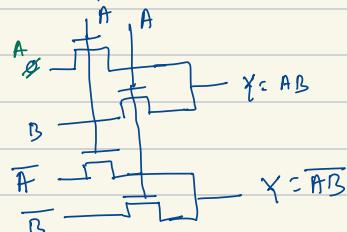
Demorgan's  
Theorem

Both AND & NAND :-

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$$A=0 \rightarrow Y=0$$

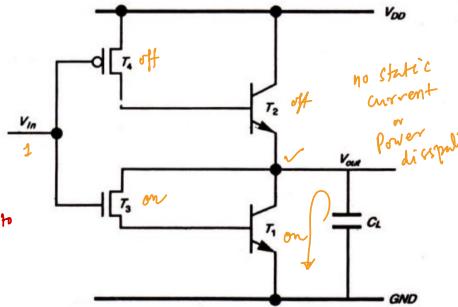
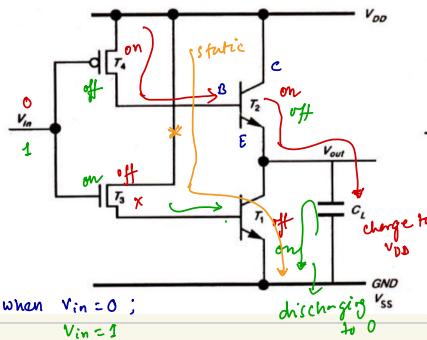
$$A=1 \rightarrow Y=1$$



complementary  
pass transistors  
logic (CPL)

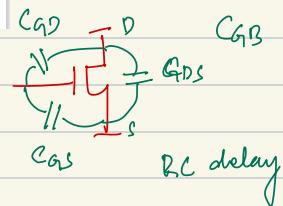
OR-NOR : XOR-XNOR ?? 4:1 mux in CPL ??

# BiCMOS Inverter



→ Speed is higher than CMOS.

(i) the capacitance in MOSFET  
    > BJT



Combine both

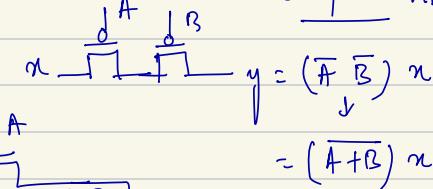
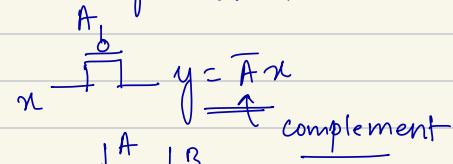
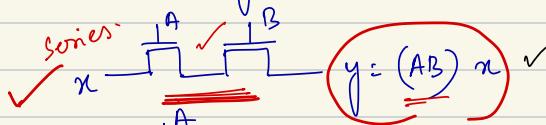
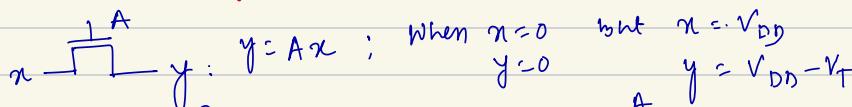
CMOS + BJT → BiCMOS

↙     ↘  
Speed ↑ Power ↓

→ CMOS have 0 static power < BJT

→ Scalability of MOSFET > BJT

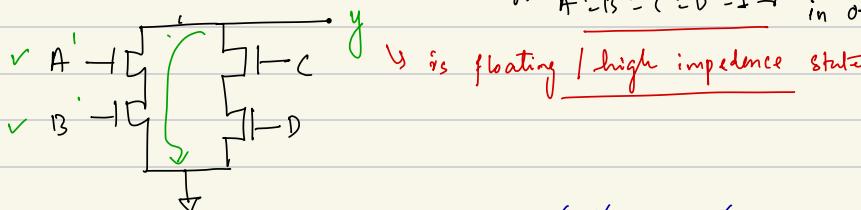
## Combinational logic implementation using CMOS:-



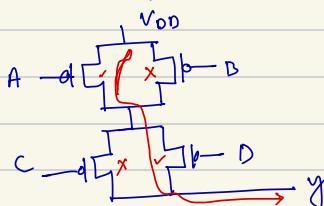
\* NMOS + PMOS circuit  
complement to each other  
\* NMOS circuit + PMOS circuit  
duality in nature.

$$\rightarrow y = \overline{AB+CD}$$

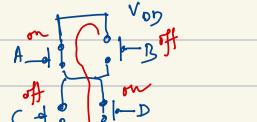
(i) NMOS :  $\bar{y} = AB+CD$  : when  $A=B=1$   
 $C=D=1$  or  $A=B=C=D=1$  in other cases  $\bar{y}=0$   $\Rightarrow y=1$   $\Rightarrow y=0$



$$(ii) \text{ PMOS} = y = \overline{AB+CD} = \overline{AB} \cdot \overline{CD} = (\bar{A} + \bar{B})(\bar{C} + \bar{D})$$



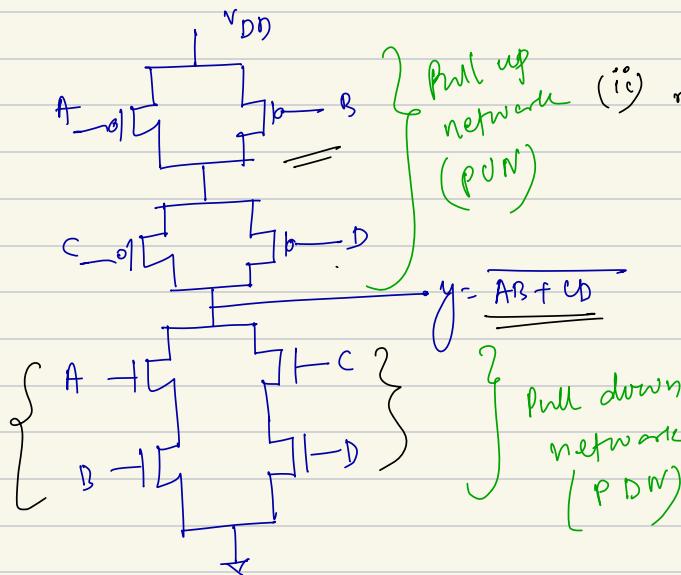
$$\rightarrow \underline{A=0}; \underline{B=1}; \underline{C=1}, \underline{D=0}$$



When  $A=1 B=1 C=0 D=0 \rightarrow y = \text{high impedance state}$

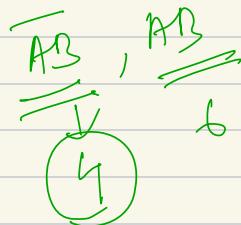
$$y = \overline{AB + CD}$$

(i) CMOS circuit implements the complement func.

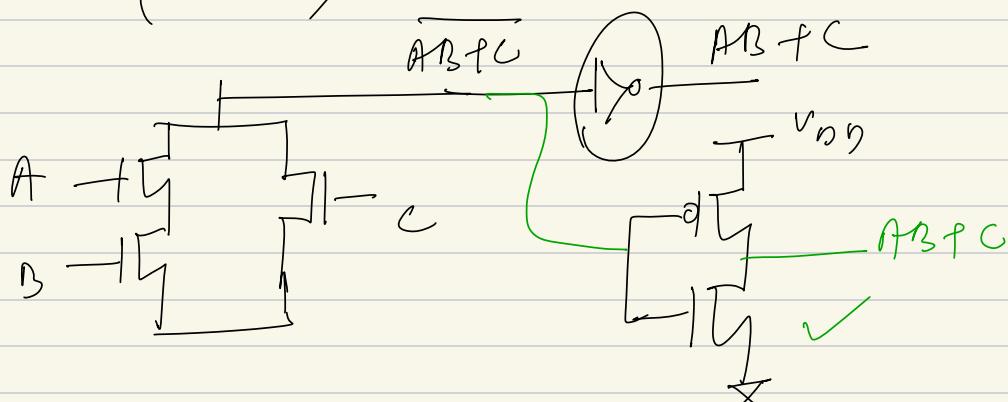


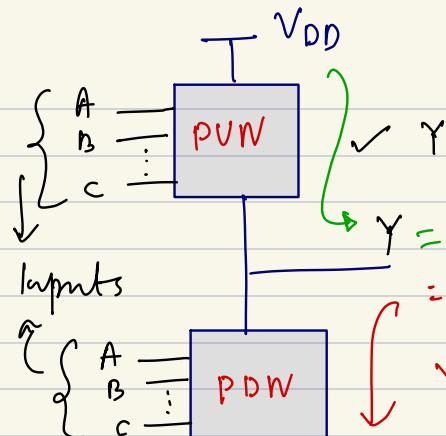
$$y = \overline{AB + C} ; \quad y = \overline{AB + C(D+E)}$$

$$\boxed{y = AB + C}$$



(PUVN)





$$Y = f(A, B, \dots, C)$$

$$Y = \overline{AB}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$Y = 1 = f(A, B, \dots, C)$$

$$Y = 0$$

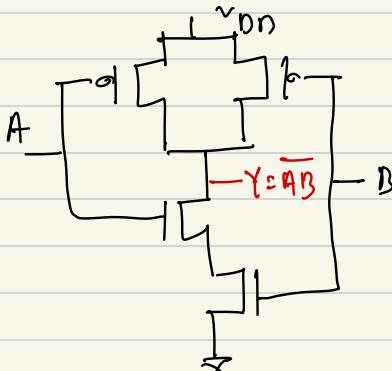
$$Y = 0 = f(A, B, \dots, C)$$

PUV  $\rightarrow$  pMOS n/w

PDW  $\rightarrow$  nMOS n/w

if **'n'** inputs :- no. of transistors =  $2N$  ✓

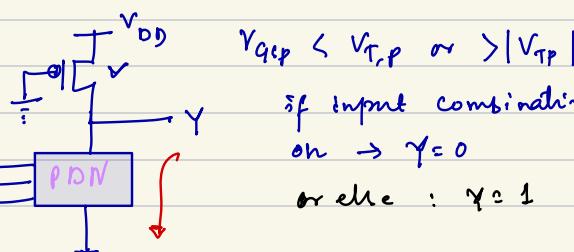
$Y = \overline{AB}$  : 2 inputs : no. of transistors  $\leq 4$   
 (2 nMOS, 2 pMOS)



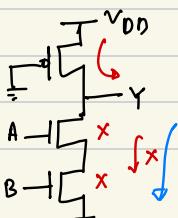
pseudo nMOS :-

Adv  
for N ill  
= N+1 transistors  
read:

input {



eg.  
When there  
is need of  
reducing  
area  
while sacrificing  
a small power  
dissipation



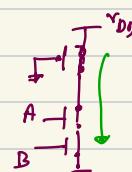
$$A = 0, B = 0 \rightarrow Y = 1$$

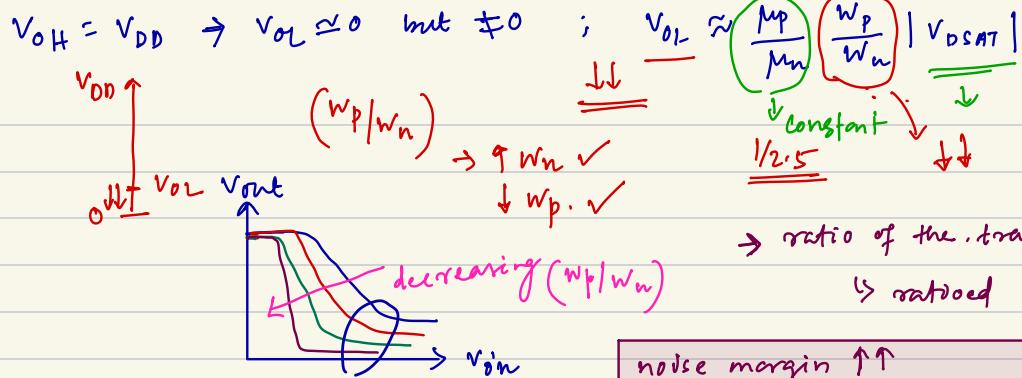
$$A = 0, B = 1 \rightarrow Y = 1$$

$$A = 1, B = 0 \rightarrow Y = 1$$

$$\boxed{A = 1, B = 1 \rightarrow Y = 0}$$

Static power dissipation  
 $>$  CMOS





$$NM_H = V_{OH} - V_{FH}$$

$$NM_L = V_{OL} - V_{IL} \uparrow \downarrow$$

power  $\uparrow \downarrow$

Area  $\downarrow \downarrow$

noise margin  $\uparrow \uparrow$

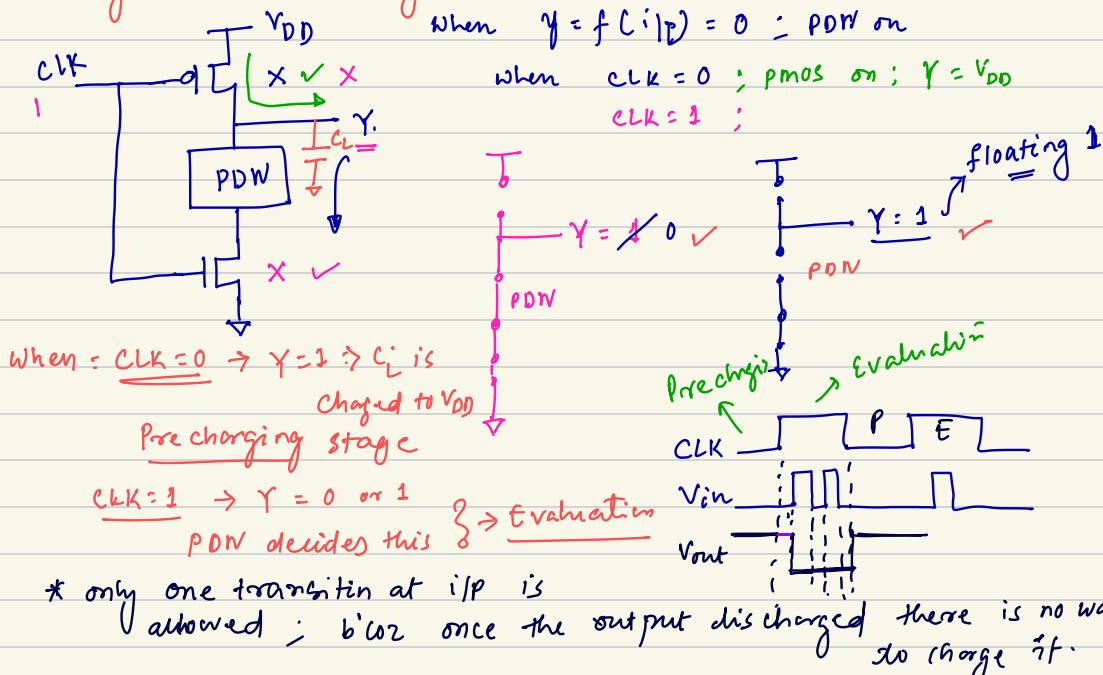
delay  $\downarrow \downarrow$  speed  $\uparrow \uparrow$

area  $\downarrow \downarrow$

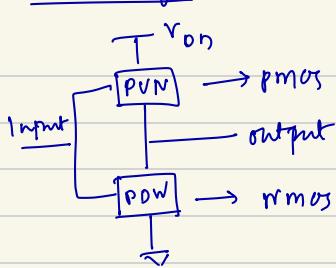
power  $\downarrow \downarrow$

## CLOCKED CMOS LOGIC : (C<sup>2</sup> logic)

Dynamic CMOS logic.



## CMOS logic :-



$\rightarrow N$  inputs =  $2N$  transistors

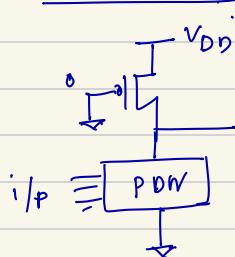
+ static power dissipation  $\approx 0$   
( $N$  nmos,  $N$  pmos)

$\rightarrow$   $P_{DN} \approx P_{DP}$  in dual n/w series - II<sup>d</sup>.

$$\rightarrow P_{DN} - f(i/p) = 1 \quad P_{DP} = f(i/p) = 0$$

$$\rightarrow V_{OH} = V_{DD}; \quad V_{OL} = 0 \quad \rightarrow NM \uparrow$$

## Pseudo nMOS :-



$\rightarrow$  PMOS is always on

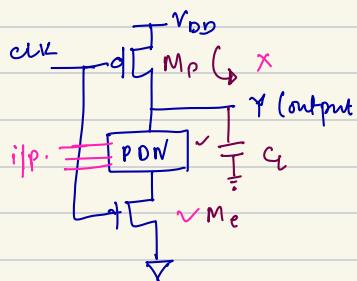
$\rightarrow$  less transistors:  $N+1 < CMOS (2N)$

$\rightarrow$  static power dissipation  $>>$  CMOS

$$V_{OH} = V_{DD}; \quad V_{OL} \neq 0$$

$$\rightarrow NM (P-nMOS) < NM (CMOS)$$

## Clocked CMOS :- Dynamic CMOS :-



$\rightarrow CLK=0 : M_p \text{ on} : Y=1 (C_L \text{ charged to } V_{DD})$

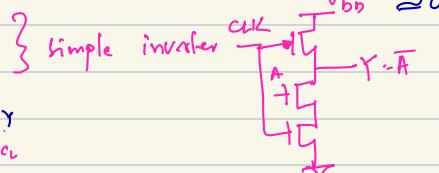
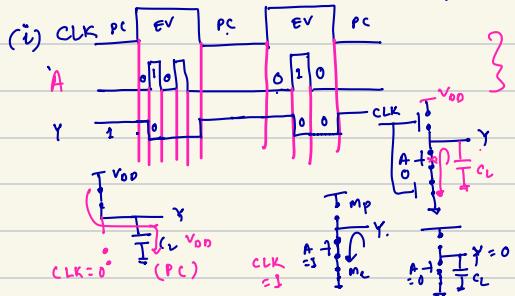
$M_e = \text{off} :$

pre charging stage ✓

$\rightarrow CLK=1 : M_p \text{ off}$

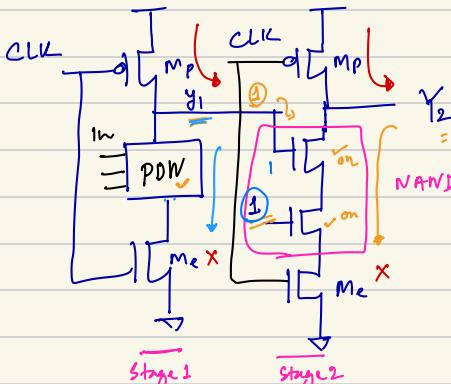
$M_e \text{ on} ; Y \text{ depends on the } P_{DN} \text{ n/w}$   
depending on the evaluation of  $P_{DN}$  n/w  
 $Y=1 \text{ or } 0.$

$\rightarrow$  This solved the static power consumption issue



$\rightarrow$  inputs can make only one transition per evaluation phase

# (ii) cascading of dynamic CMOS

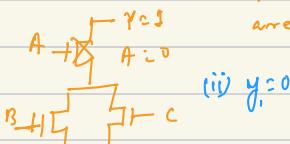


$\rightarrow CLK = 0 ; y_1 = 1 ; y_2 = 1$   
Precharge

$\rightarrow CLK = 1$ ; depending on the PON of 1st stage  
 $y_1$  is evaluated.

2nd stage - NAND gate

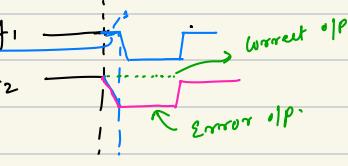
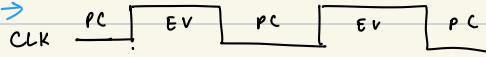
- (i) let's due to pon:  $y_1 = 1$  ✓
- 2nd stage NAND gate i/p: are 1, 1 =  $y_2 = 0$



$t = 0.5$ :  $y_1 = 1 \rightarrow$  Stage 2  
 $t = 0.15$ :  $y_1 = 0 \rightarrow$

$$\begin{array}{l} y_1 = 0 \\ \hline y_2 = 1 \end{array}$$

Time my taken by  
stage 1 to  
discharge the  
capacitor

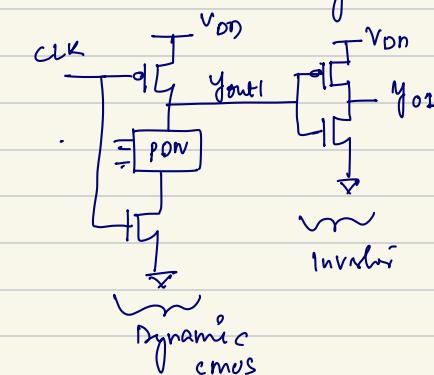


Transition at  
stages o/p takes  
some time due to  
discharging of capacitor  
which leads to  
error at the stage 2  
output.

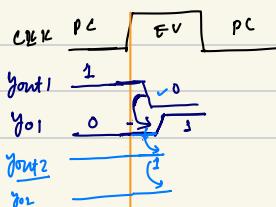
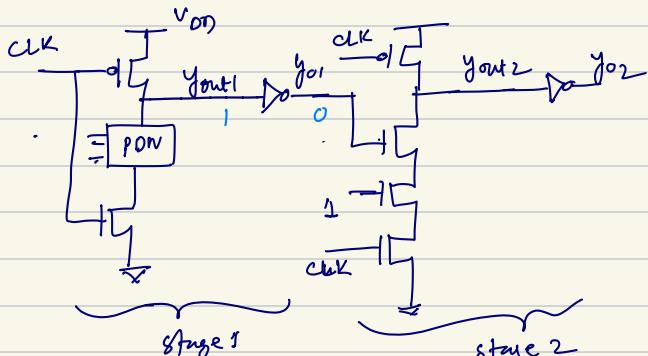
$\rightarrow$  Cascading dynamic CMOS circuit leads to  
reliability issues in the circuit

## Domino CMOS :-

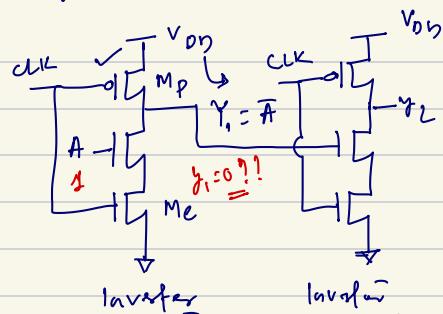
Dynamic CMOS + static inverter



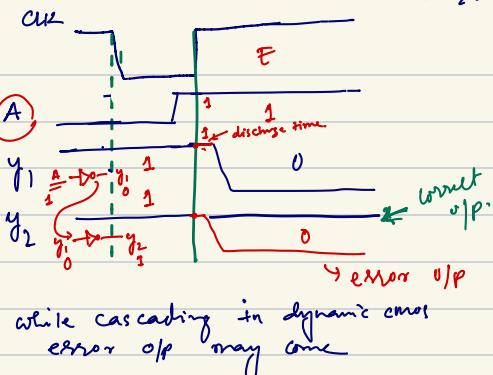
$\rightarrow CLK = 0$ ; Precharge :  $y_{out1} = 1, y_{out2} = 0$



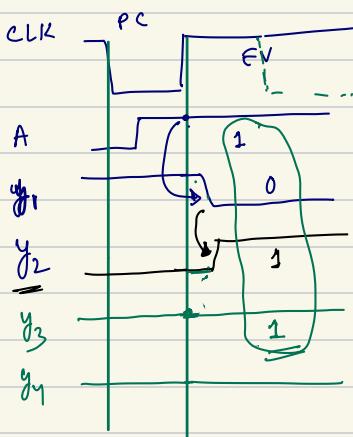
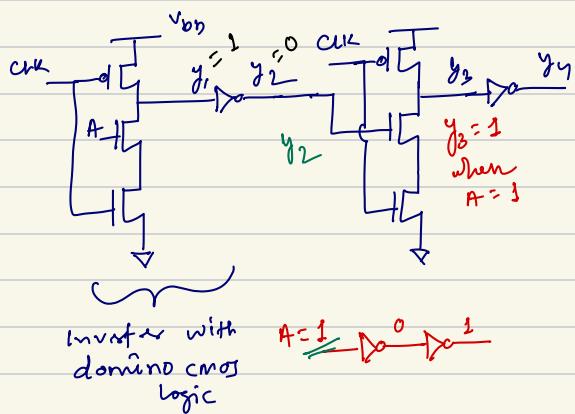
## Dynamic CMOS :-



CK = 0 → Prechage → Y = 1  
 $\rightarrow 1 \rightarrow$  Evaluation → Y = 0  
 $\infty 1$

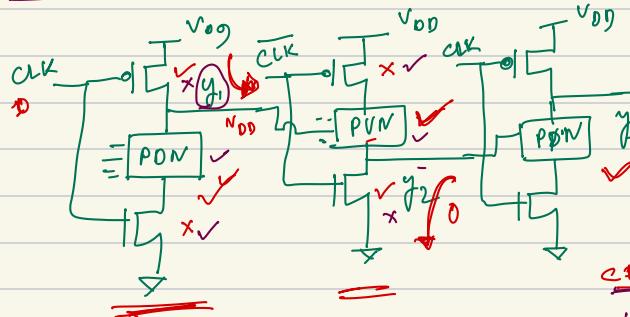


## Domino CMOS



→ only one transistor is allowed.

n-p logic (NORA logic) :-



CLK=0 ÷ The PDN stage

output = high

## The pVN stage

output = low

NMOS stage  
Predicing

PMOS stage Predicibus

C2K=3 : PUN stage are going to decide the output i.e evaluation.

## 2.7 DETERMINATION OF PULL-UP TO PULL-DOWN RATIO ( $Z_{p.u.}/Z_{p.d.}$ ) FOR AN nMOS INVERTER DRIVEN BY ANOTHER nMOS INVERTER

Consider the arrangement in Figure 2.8 in which an inverter is driven from the output of another similar inverter. Consider the depletion mode transistor for which  $V_{gs} = 0$  under all conditions, and further assume that in order to cascade inverters without degradation of levels we are aiming to meet the requirement

$$V_{in} = V_{out} = V_{inv}$$

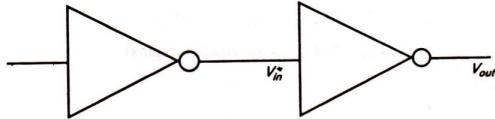


FIGURE 2.8 nMOS inverter driven directly by another inverter.

For equal margins around the inverter threshold, we set  $V_{inv} = 0.5V_{DD}$ . At this point both transistors are in saturation and

$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

In the depletion mode

$$I_{ds} = K \frac{W_{p.u.}}{L_{p.u.}} \frac{(-V_{td})^2}{2} \text{ since } V_{gs} = 0 \quad V_{ds} < V_{DD}/2$$

and in the enhancement mode

$$I_{ds} = K \frac{W_{p.d.}}{L_{p.d.}} \frac{(V_{inv} - V_t)^2}{2} \text{ since } V_{gs} = V_{inv}$$

Equating (since currents are the same) we have

$$\frac{W_{p.d.}}{L_{p.d.}} (V_{inv} - V_t)^2 = \frac{W_{p.u.}}{L_{p.u.}} (-V_{td})^2$$

where  $W_{p.d.}$ ,  $L_{p.d.}$ ,  $W_{p.u.}$ , and  $L_{p.u.}$  are the widths and lengths of the pull-down and pull-up transistors respectively.

Now write

$$Z_{p.d.} = \frac{L_{p.d.}}{W_{p.d.}}; Z_{p.u.} = \frac{L_{p.u.}}{W_{p.u.}}$$

we have

$$\frac{1}{Z_{p.d.}} (V_{inv} - V_t)^2 = \frac{1}{Z_{p.u.}} (-V_{td})^2 \quad \left[ \begin{array}{c} Z_{p.u.} \\ \hline Z_{p.d.} \end{array} \right]$$

whence

$$V_{inv} = V_t - \frac{V_{td}}{\sqrt{Z_{p.u.}/Z_{p.d.}}} \quad (2.9)$$

Now we can substitute typical values as follows:

$$V_t = 0.2V_{DD}; V_{td} = -0.6V_{DD}$$

$$V_{inv} = 0.5V_{DD} \text{ (for equal margins)}$$

thus, from equation (2.9)

$$0.5 = 0.2 + \frac{0.6}{\sqrt{Z_{p.u.}/Z_{p.d.}}}$$

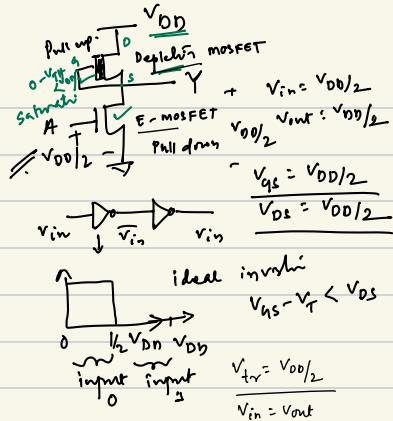
whence

$$\sqrt{Z_{p.u.}/Z_{p.d.}} = 2$$

and thus

$$Z_{p.u.}/Z_{p.d.} = 4/1$$

for an inverter directly driven by an inverter.



$$V_{GS} \approx V_{TH} \rightarrow \text{Cut off}$$

$$I_D = 0$$

$$V_{GS} - V_{TH} = V_{DSAT}$$

$$V_{DS} < V_{GS} - V_{TH} = \text{Linear}$$

$$V_{DS} > V_{GS} - V_{TH} = \text{Saturation}$$

$$V_{in} = V_{out}$$

## 2.8 PULL-UP TO PULL-DOWN RATIO FOR AN nMOS INVERTER DRIVEN THROUGH ONE OR MORE PASS TRANSISTORS

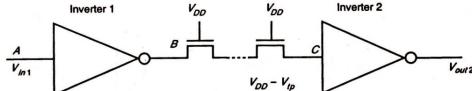


FIGURE 2.9 Pull-up to pull-down ratios for inverting logic coupled by pass transistors.

$V_{tp}$ , however many are connected in series, since no static current flows through them and there can be no voltage drop in the channels. Therefore, the input voltage to inverter 2 is

$$V_{in2} = V_{DD} - V_{tp}$$

where

$V_{tp}$  = threshold voltage for a pass transistor.

We must now ensure that for this input voltage we get out the same voltage as would be the case for inverter 1 driven with input =  $V_{DD}$ .

Consider inverter 1 (Figure 2.10(a)) with input =  $V_{DD}$ . If the input is at  $V_{DD}$ , then the p.d. transistor  $T_2$  is conducting but with a low voltage across it; therefore, it is in its resistive region represented by  $R_1$  in Figure 2.10. Meanwhile, the p.u. transistor  $T_1$  is in saturation and is represented as a current source.

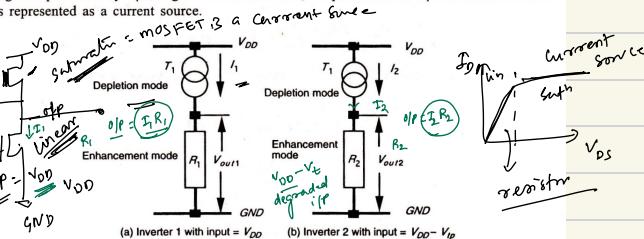


FIGURE 2.10 Equivalent circuits of inverters 1 and 2.

For the p.d. transistor

$$I_{ds} = K \frac{W_{p.d.1}}{L_{p.d.1}} \left( (V_{DD} - V_t) V_{ds1} - \frac{V_{ds1}^2}{2} \right) \checkmark \Rightarrow \frac{\sqrt{I_{ds}}}{\sqrt{Z_{p.d.1}}} \quad (\text{from 2.4})$$

Therefore

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{1}{K} \frac{L_{p.d.1}}{W_{p.d.1}} \left( \frac{1}{V_{DD} - V_t - \frac{V_{ds1}}{2}} \right) \checkmark$$

Note that  $V_{ds1}$  is small and  $V_{ds1}/2$  may be ignored.

Thus

$$R_1 \approx \frac{1}{K} Z_{p.d.1} \left( \frac{1}{V_{DD} - V_t} \right) \checkmark$$

Now, for depletion mode p.u. in saturation with  $V_{gs} = 0$

$$I_1 = I_{ds} = K \frac{W_{p.u.1}}{L_{p.u.1}} \frac{(-V_{td})^2}{2} \checkmark \quad (\text{from 2.5})$$

The product

$$I_1 R_1 = V_{out1}$$

Thus

$$V_{out1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}} \left( \frac{1}{V_{DD} - V_t} \right) \frac{(V_{td})^2}{2}$$

Consider inverter 2 (Figure 2.10(b)) when input =  $V_{DD} - V_{tp}$ . As for inverter 1

$$R_2 \approx \frac{1}{K} Z_{p.d.2} \frac{1}{((V_{DD} - V_{tp}) - V_t)} \checkmark$$

$$I_2 = K \frac{1}{Z_{p.d.2}} \frac{(-V_{td})^2}{2}$$

whence

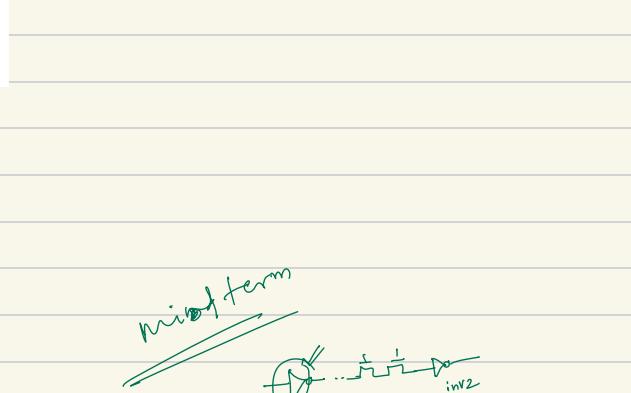
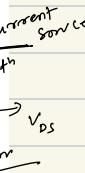
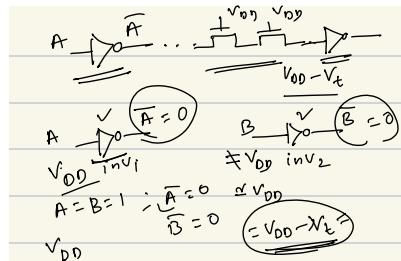
$$V_{out2} = I_2 R_2 = \frac{Z_{p.d.2}}{Z_{p.u.2}} \left( \frac{1}{V_{DD} - V_{tp} - V_t} \right) \frac{(-V_{td})^2}{2}$$

If inverter 2 is to have the same output voltage under these conditions then  $V_{out1} = V_{out2}$ . That is

$$I_1 R_1 = I_2 R_2$$

Therefore

$$\boxed{\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)}} \checkmark$$



Taking typical values

$$V_t = 0.2V_{DD} \checkmark$$

$$V_{tp} = 0.3V_{DD} \checkmark$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{0.8}{0.5} = \frac{4}{1} \cdot \frac{0.8}{0.5} = \frac{4}{1} \cdot \frac{1.6}{1} = \frac{6.4}{1}$$

Therefore

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} \approx 2 \frac{Z_{p.u.1}}{Z_{p.d.1}} = \frac{8}{1}$$

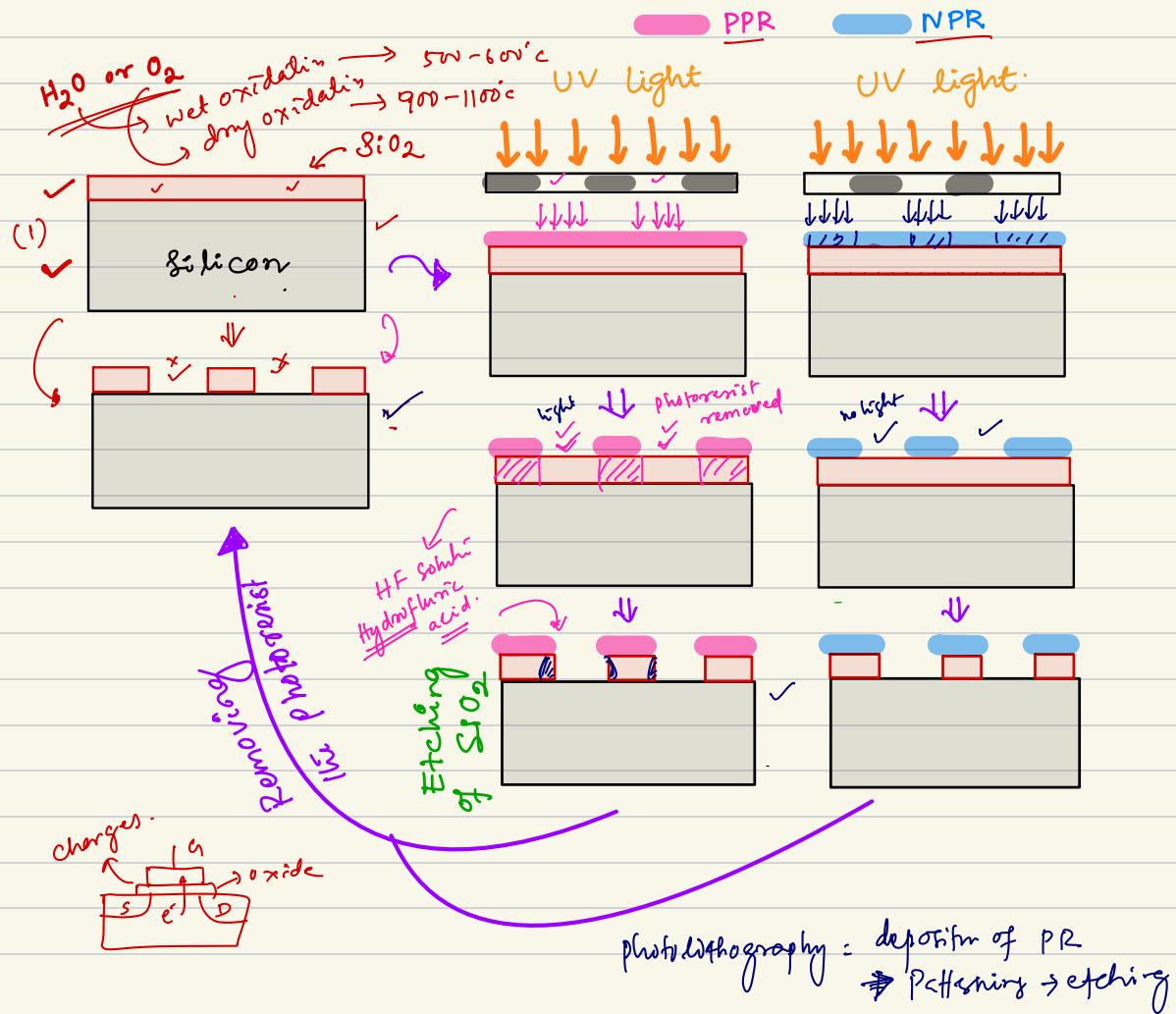
Summarizing for an nMOS inverter:

- An inverter driven directly from the output of another should have a  $Z_{p.u.}/Z_{p.d.}$  ratio of  $\geq 4/1$ .
- An inverter driven through one or more pass transistors should have a  $Z_{p.u.}/Z_{p.d.}$  ratio of  $\geq 8/1$ .

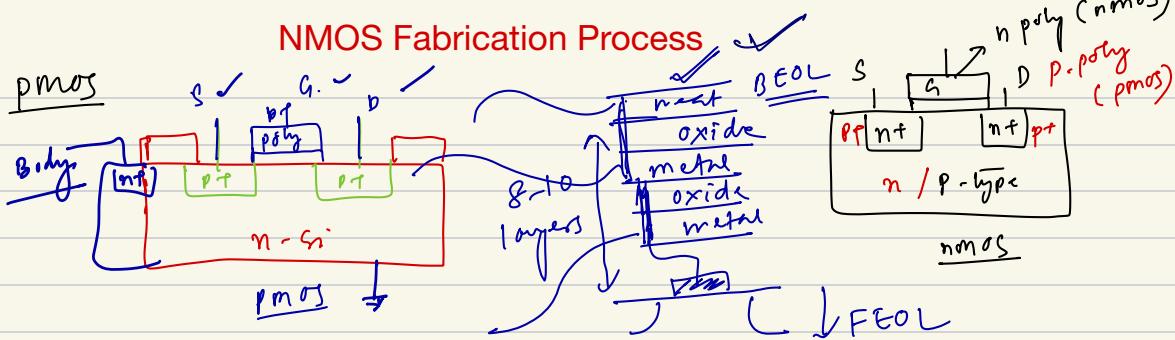
Note: It is the driven, not the driver, whose ratio is affected.

# Photolithography

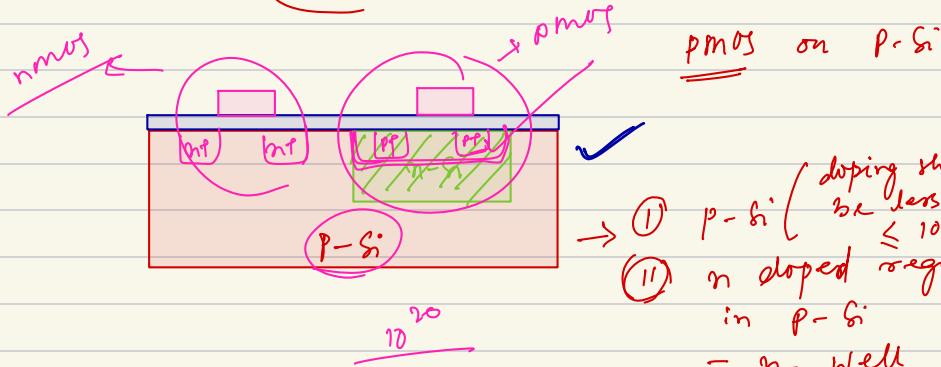
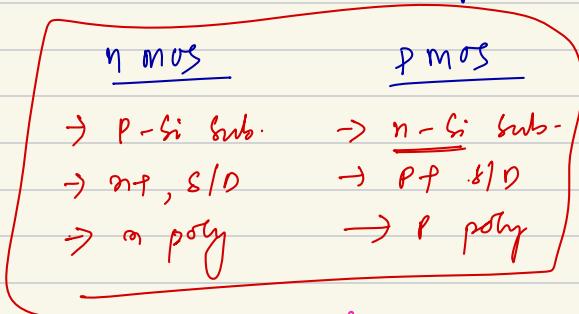
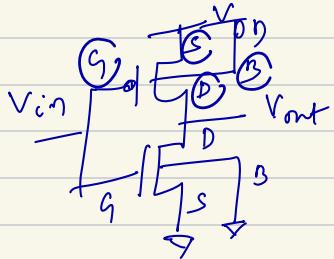
- The Process of using an optical image and a photosensitive film to produce a pattern on a substrate is **photolithography**
- Photolithography depends on a photosensitive film called a **photo-resist**.
- Types of resist
  - Positive resist, a resist that become soluble when exposed and forms a positive image of the plate.
  - Negative resist, a resist that lose solubility when illuminated forms a negative image of the plate.



## NMOS Fabrication Process



MIM capacitor

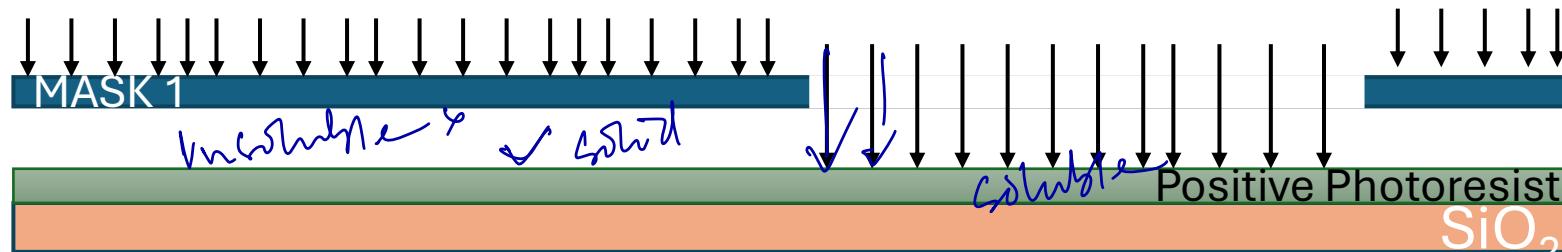


- ① p-Si (doping should be less  $\leq 10^{15} \text{ cm}^{-3}$ )
- ② n doped regions in p-Si
  - n- well

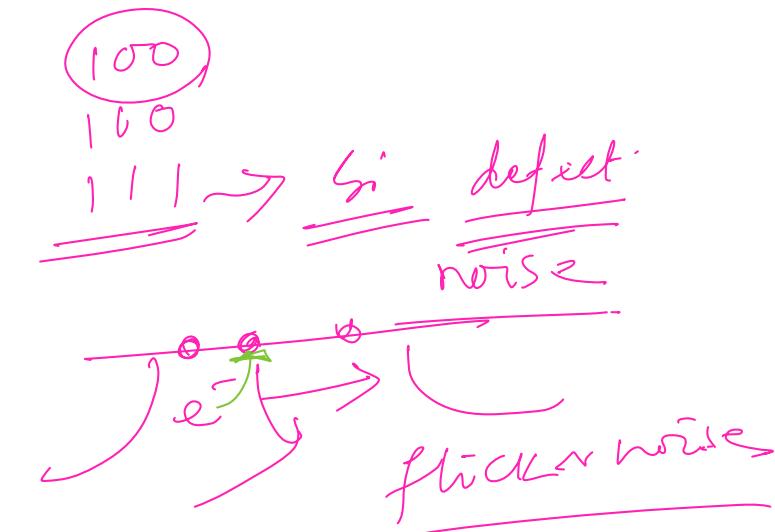
Si (100)  
P -type

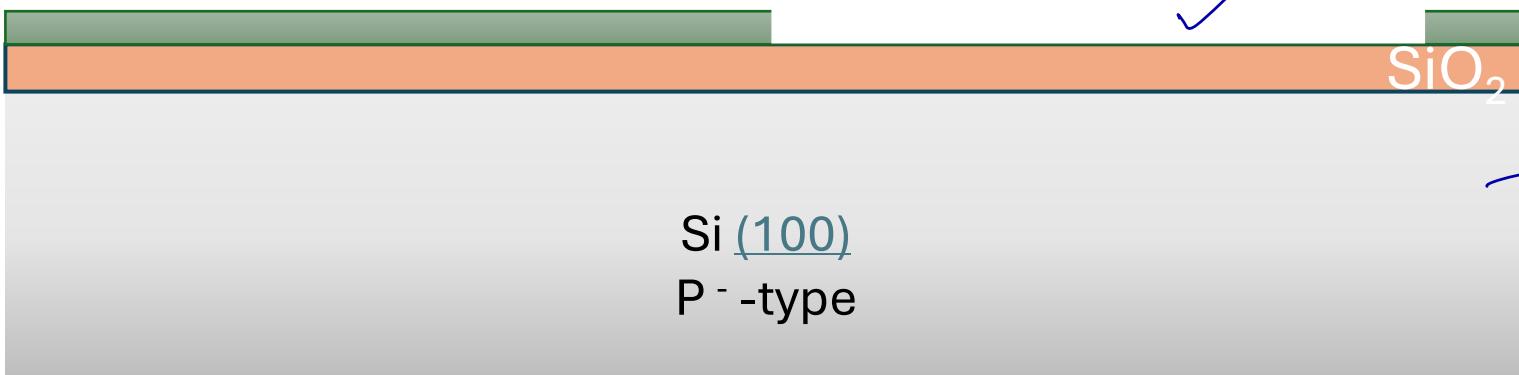


Si (100)  
P -type

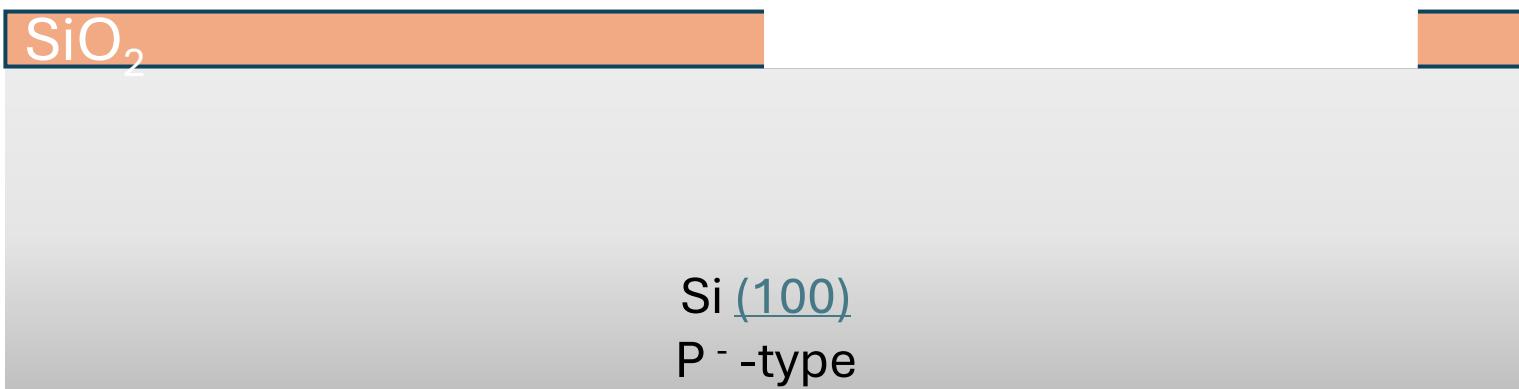
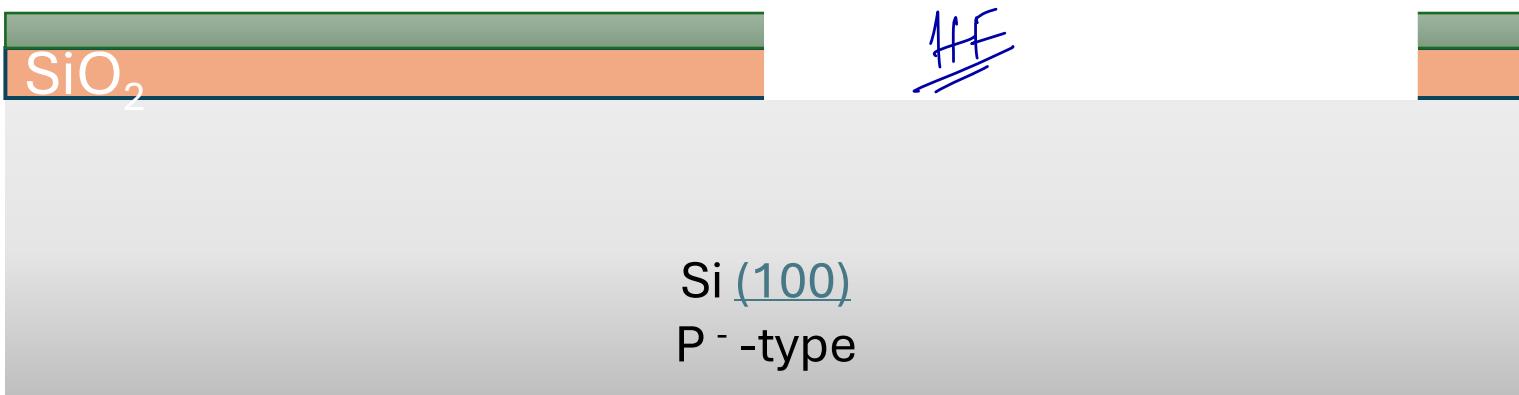


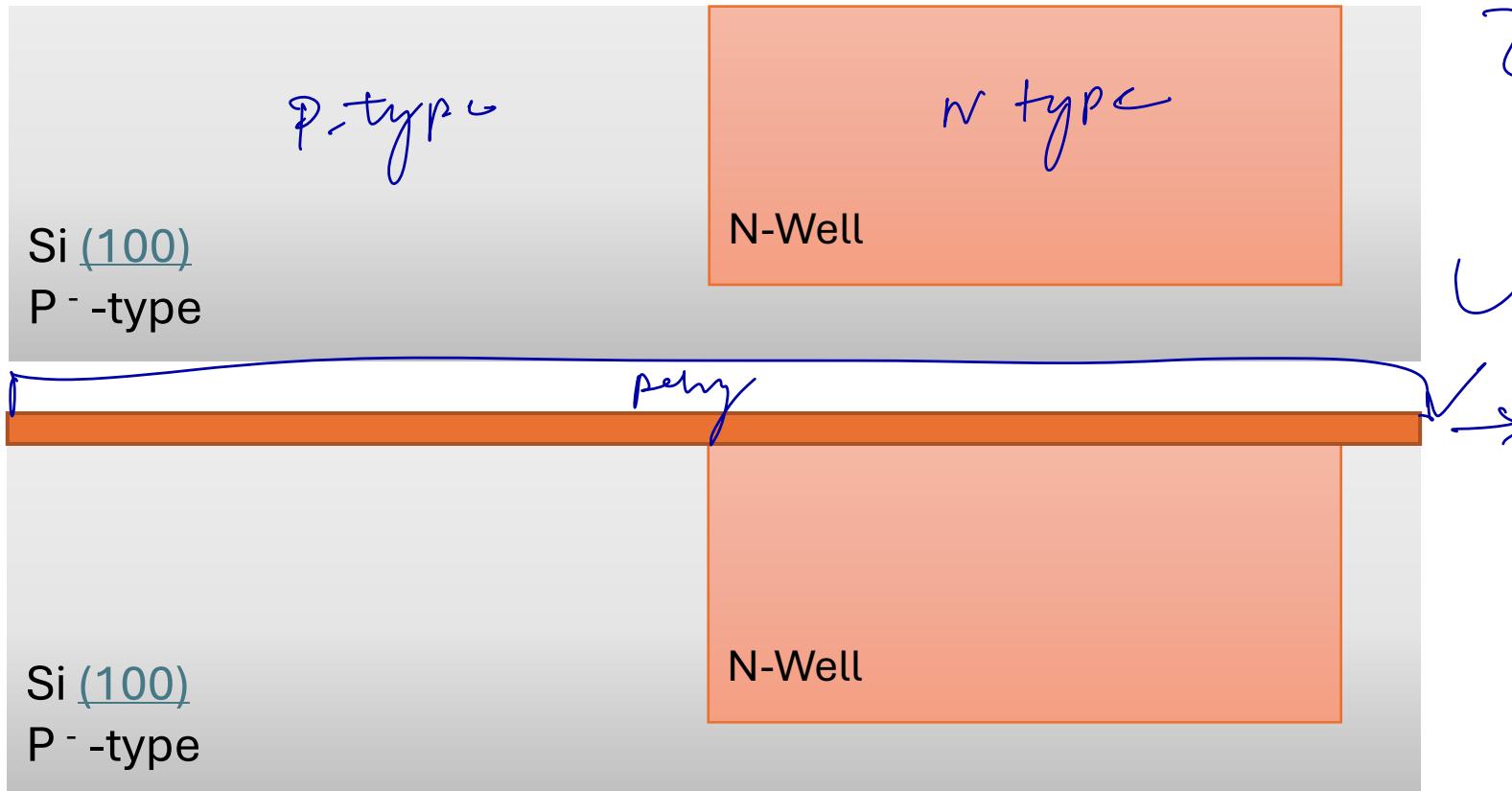
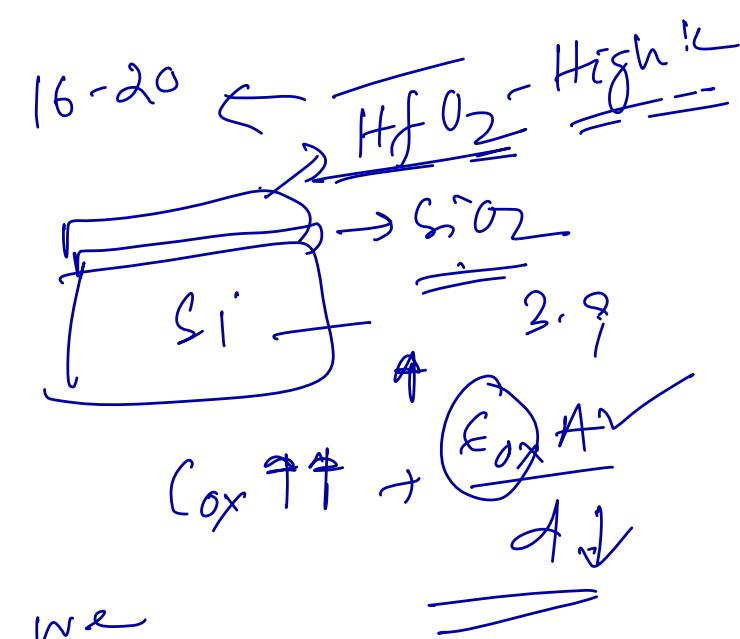
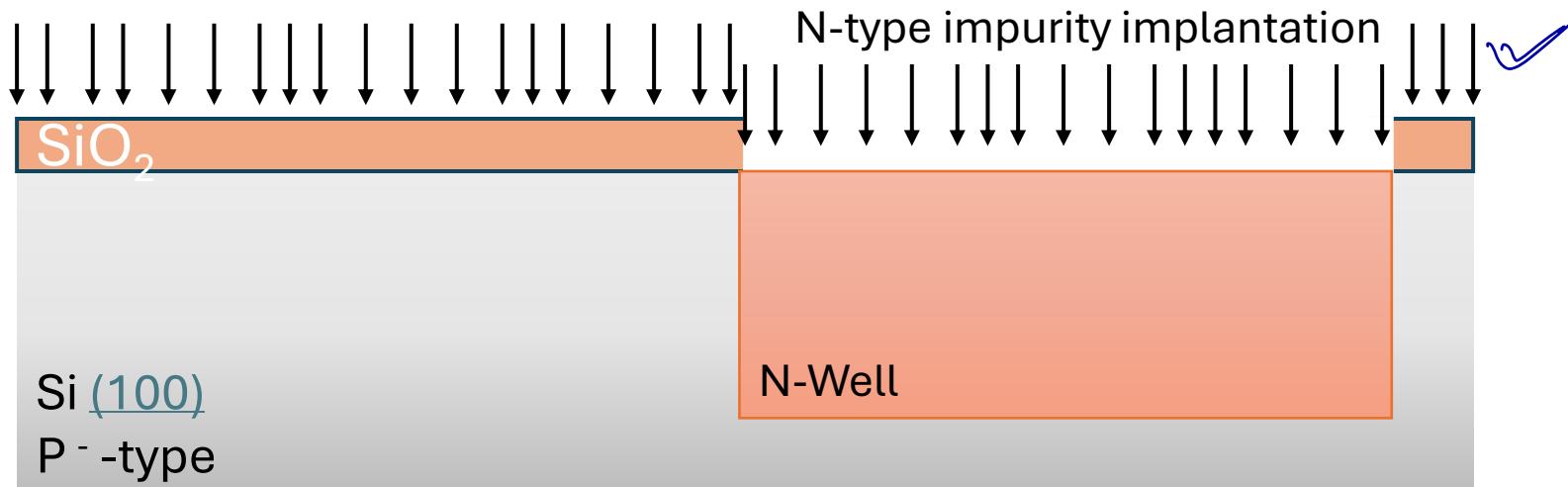
Si (100)  
P -type

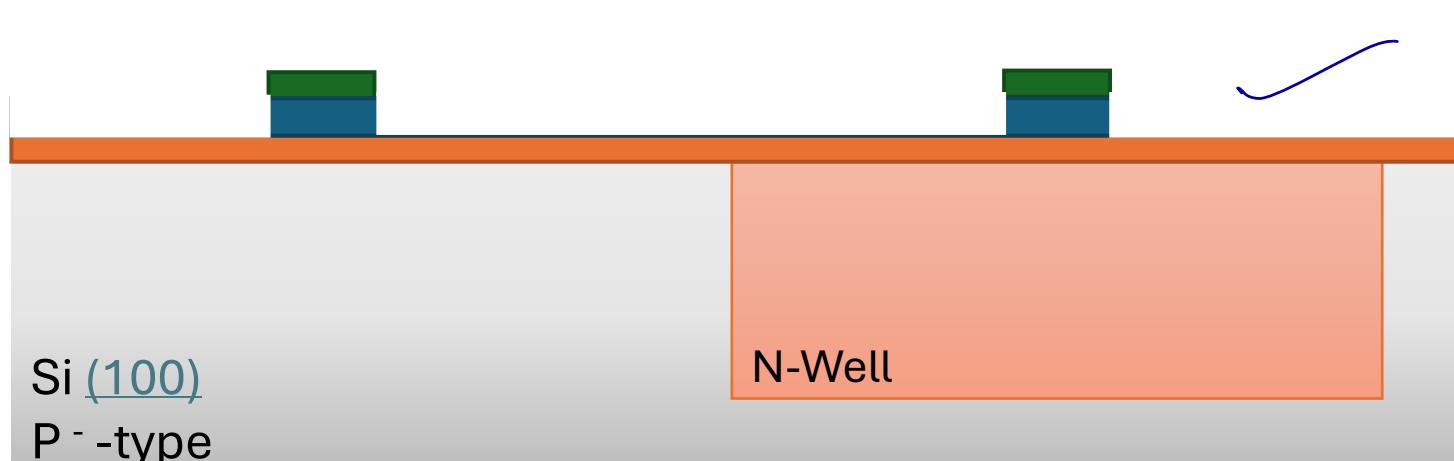
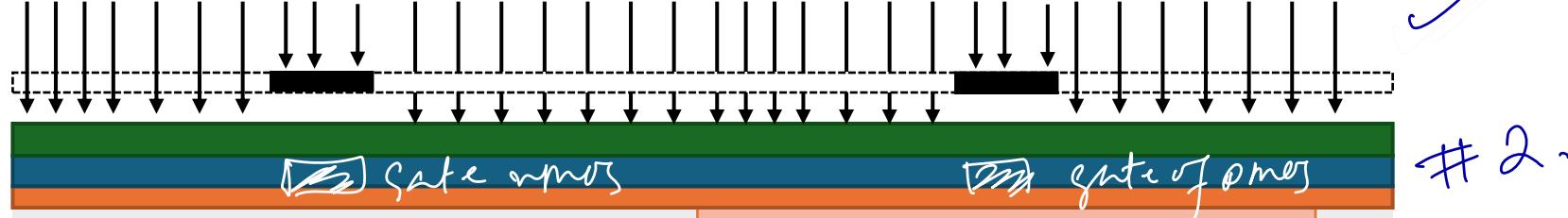




→ HF (Hydrofluoric Acid)  
BOE (Buffered oxide etchant)

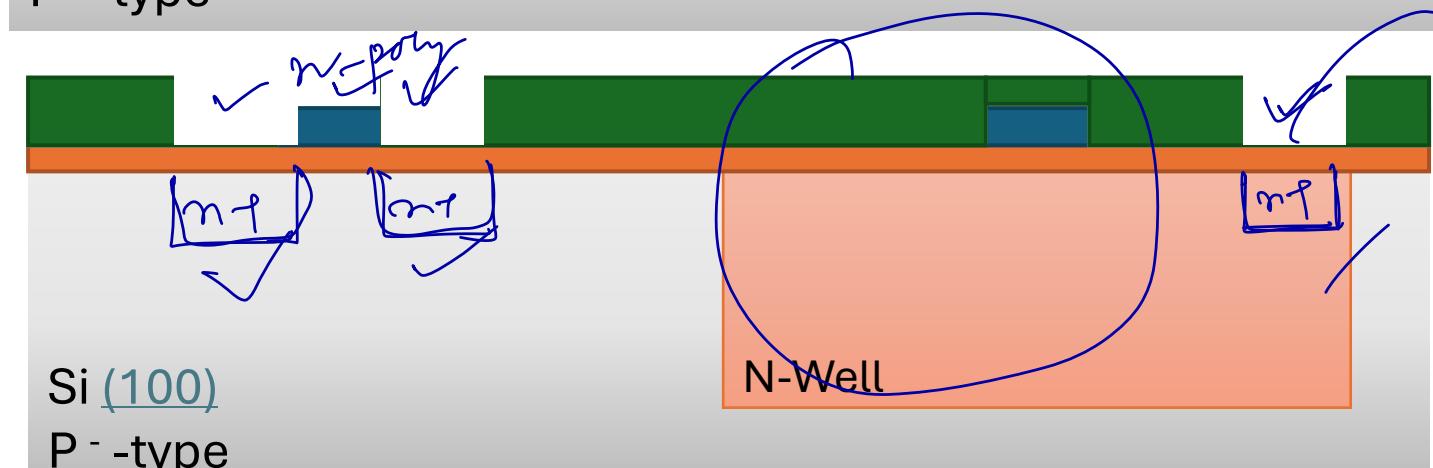
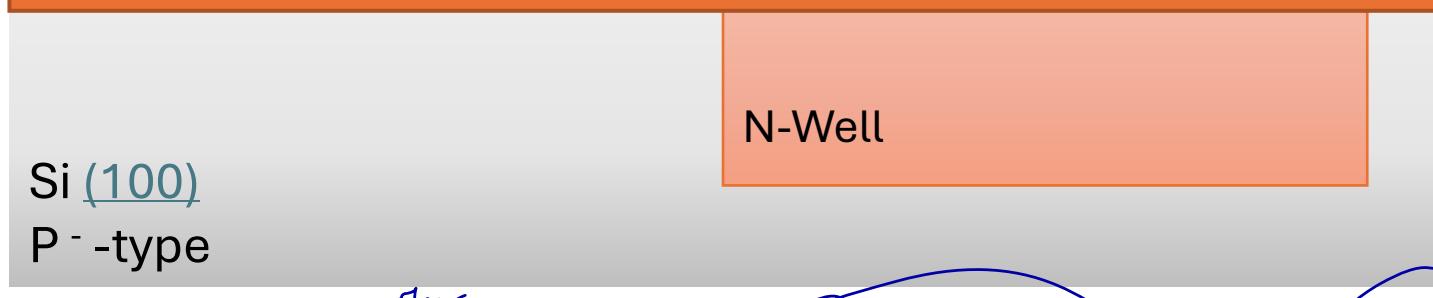
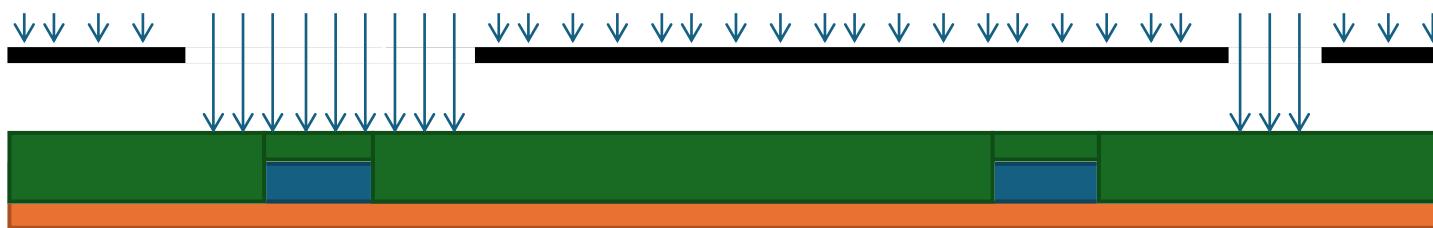


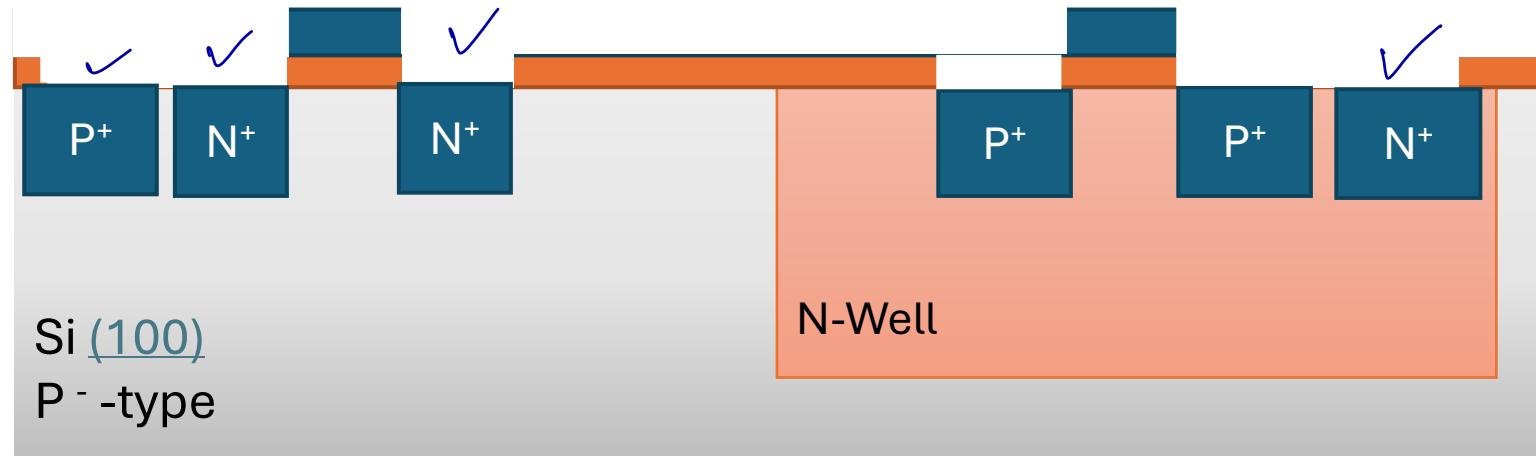
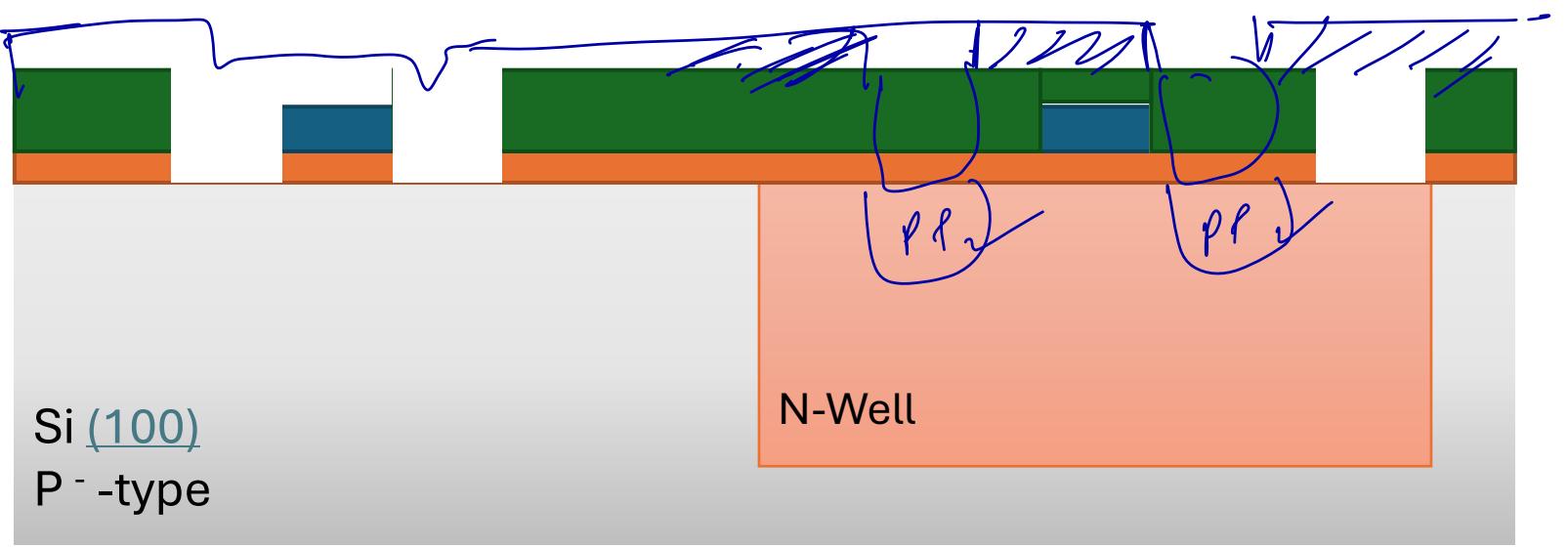


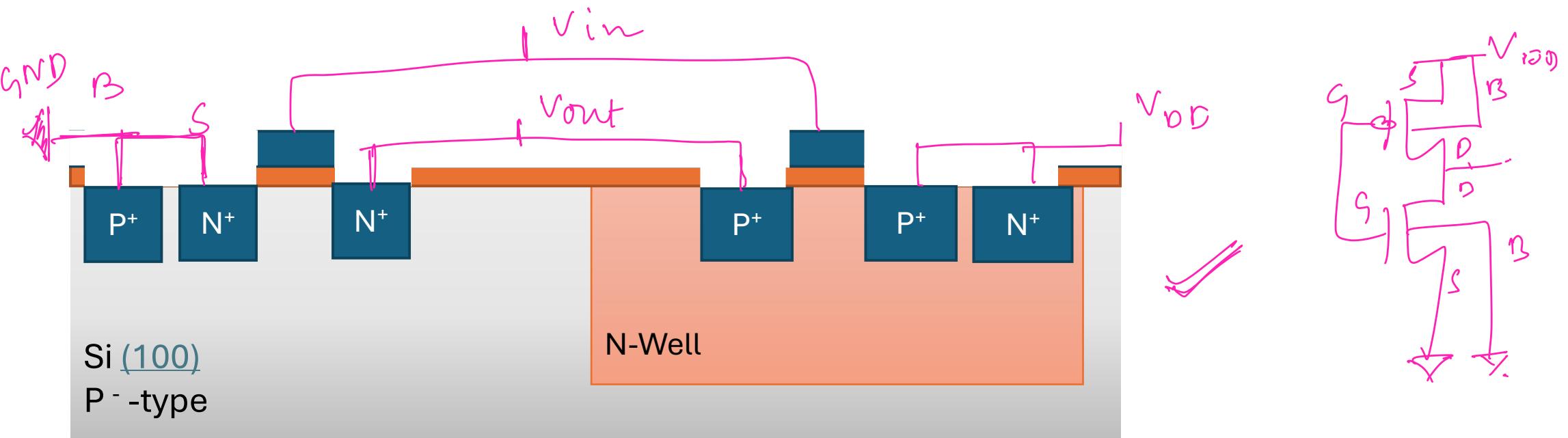




✓  
at in pmos  
·pf in nmos



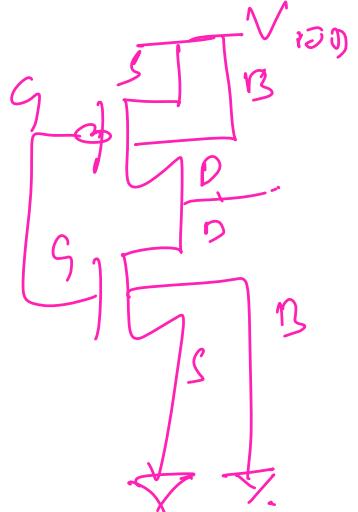


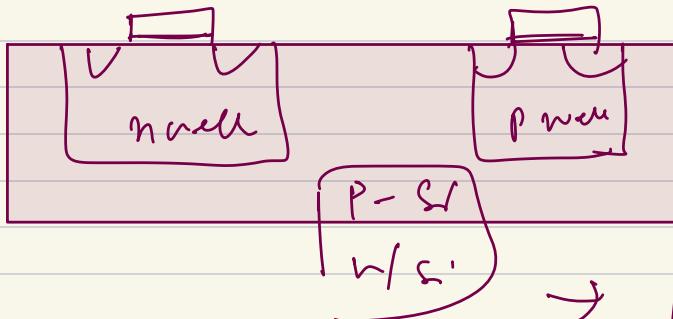
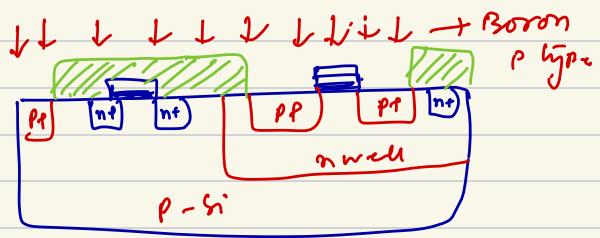
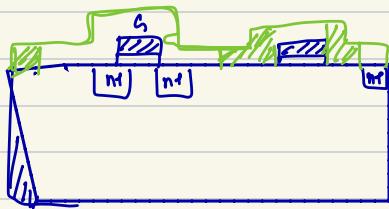


Twin TUB process → 2 wells · n well p well

TCAD

single well CMOS process





$\rightarrow$  1st doping.

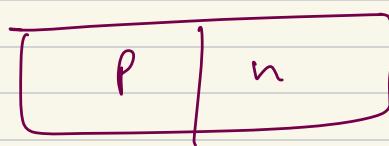
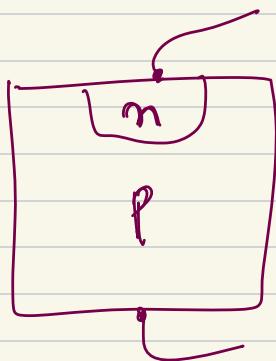
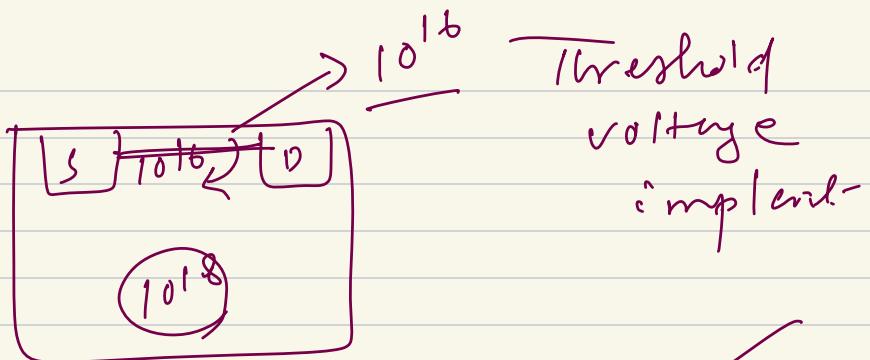
$$10^{17} \text{ cm}^{-3}$$

~~$10^{18} \text{ cm}^{-3}$~~

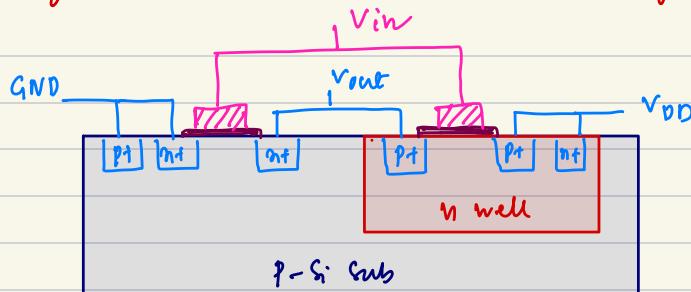
$\frac{10^{20}}{2\pi F} \text{ cm}^{-3}$

$\checkmark$

$$\checkmark F = \frac{kT}{q} \ln \frac{N_A}{N_i}$$



# Single well CMOS device - challenges.

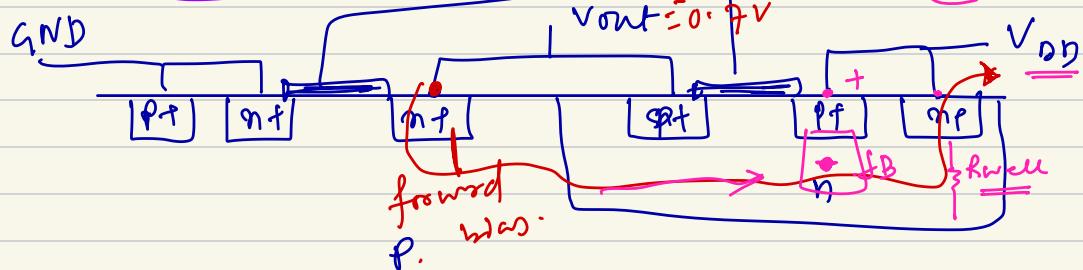
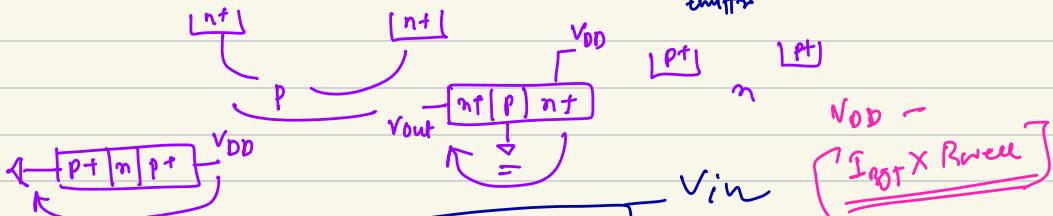
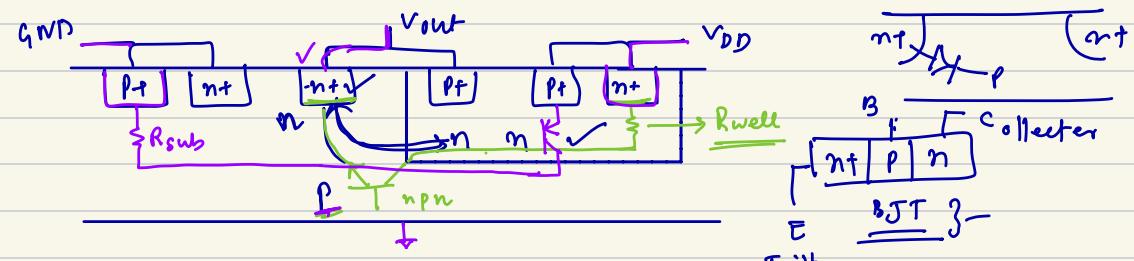


$V_{TH}$  depends on  $N_A$

$\uparrow N_A \rightarrow \uparrow V_{TH}$

$p_{Si}$  / n well  
all substrates are of low doping

Substrate doping

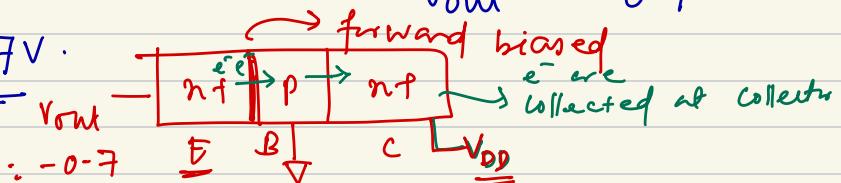


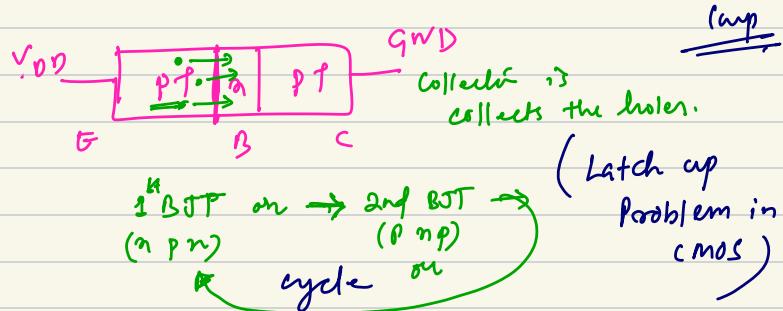
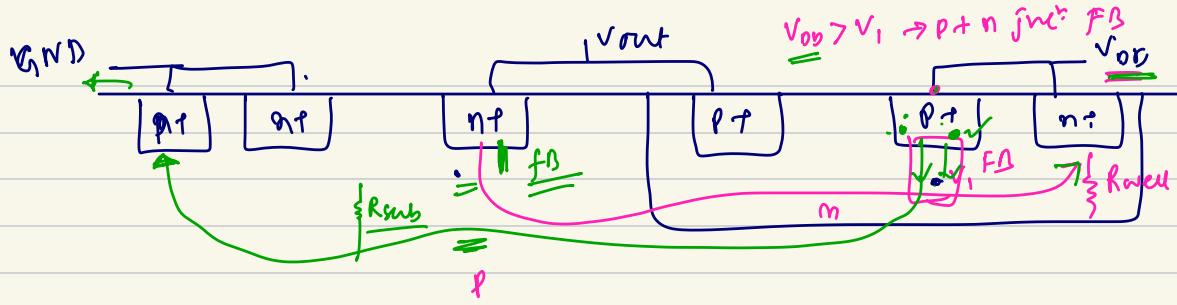
$$\underline{V_{in}} = \underline{V_{DD}} \Rightarrow \underline{V_{out}} = 0$$

Let's assume due to noise or any other external factor

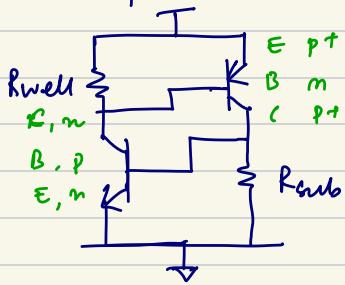
$$\underline{V_{out}} = -0.7V$$

$$\underline{V_{out}} = -0.7V$$





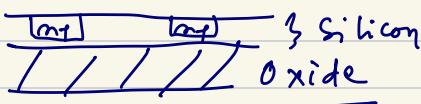
To do latch up issue there is a connection established between  $V_{DD}$  & GND ; making non zero static power dissipation-



→ Due to current flow in n-well voltage drop occurs across it due to Rwell  
→ same happens with Rsub

①  $\underline{R = 0}$  → let's make voltage drop = 0  
by marking  $R = 0$   
→ Substrate doping.

② → CMOS Twin Tub process.  
→ SOI ( Silicon on Insulator )



$N_A$  should low  
 $\uparrow$   $V_{DD}$   
 $\downarrow$   $N_A$  should high.