Question Paper

Exam Date & Time: 11-May-2024 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) DEGREE EXAMINATIONS - APRIL / MAY 2024
SUBJECT: ECE 2221/ECE_2221 - VLSI DESIGN

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A) A 0.18-µm fabrication process is specified to have tox= 4nm, μ_n=450cm^2/Vs and VT=0.5V. Find the value of Cox and µnC_{ox}. For a MOSFET with minimum length L=0.18-µm fabricated in this process, find the required value of W so that the device exhibits a channel resistance of 1K ohm at V_{GS}=1V. Given ε_{ox}=3.45e-11 F/m. Calculate the values of Overdrive voltage V_{OV}, Gate Source Voltage V_{GS} and minimum Drain Source Voltage V_{DSmin} , needed to operate the transistor in saturation region with a dc current of I_D=60µA. (4)

1B) With neat circuit diagram and VI characteristics explain the working of NMOS FET in different regions. (3)

1C) An NMOS transistor with W/L =8/1 has V_{TN} =1V , $2\varphi_F$ = 0.6V and γ = 0.7 $V^{1/2}$. The transistor operating with V_{SB}=3V, V_{GS}=2.5V and V_{DS}=5V. What is the drain current in the transistor? Repeat for V_{DS} =0.5V. (3)

2A) Derive the pull-up to pull-down ratio for an NMOS inverter driven through one or more pass transistors as shown in Figure 2A . (4)

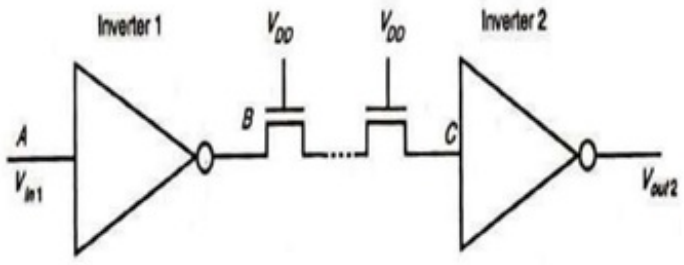


Figure 2A.

2B) Design F=[(A+BC)D +E] logic using static CMOS design style and draw its stick diagram. (3)

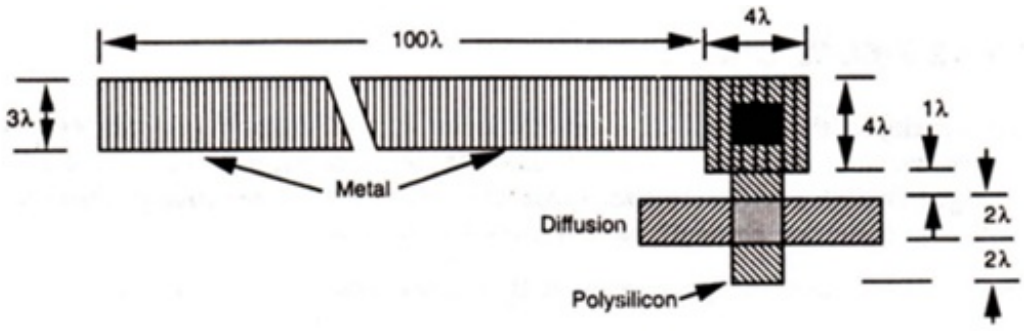
2C) Derive scaling factors for (3)
1) Gate area (Ag)
2) Gate capacitance per unit area (Cox)
3) Gate capacitance (Cg).

3A) Explain the steps involved in the fabrication of a depletion PMOS transistor. (4)

3B) Draw the layout and stick diagram of NMOS inverter (3)

3C) Determine the overall capacitance for the layout depicted in Fig. Q3C, expressed in terms of unit area gate (3)

capacitance(□ Cg). Consider the technology parameters for a 2 µm process.



Typical area capacitance values for MOS circuits

Capacitance	*Value in pF × 10^{-4}/µm² (Relative values in brackets)*
	2 µm
Gate to channel	8 (1.0)
Diffusion (active)	1.75 (0.22)
Polysilicon* to substrate	0.6 (0.075)
Metal 1 to substrate	0.33 (0.04)
Metal 2 to substrate	0.17 (0.02)
Metal 2 to metal 1	0.5 (0.06)
Metal 2 to polysilicon	0.3 (0.038)

Notes: Relative value = specified value/gate to channel value for that technology.

4A) Implement a Full adder using CMOS PLA (4)

4B) Two inverters are cascaded to drive a capacitive load C_L = 15 □ Cg as shown in Fig. Q 4B. (3)

Inverters 1 and 2 are pseudo NMOS and CMOS inverter, respectively. Calculate the pair delay in terms of τ by taking the minimum required dimension of each transistor.

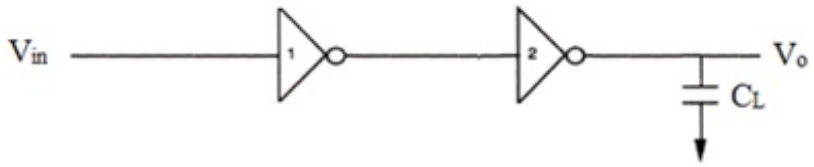


Fig. Q 4B

4C) Implement a SR latch using 2 input CMOS NAND gate. (3)

5A) Implement 3 input minority function using 3 stage DOMINO logic. (4)

5B) Explain the working of 6-T DRAM (3)

5C) Explain the operation of a 4 × 4 barrel shifter and demonstrate how it facilitates the "divided by 2" operation. (3)

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