COURSE PLAN

Department	:	Electronics and Communication Engineering
Course Name & code	:	Computer Organization and Architecture & ECE-2152
Semester & branch	:	Third Semester & E& C
Name of the faculty	:	Dr. Sampath Kumar, Dr.Kanthi.M, Ms. Navya KT
No of contact hours/week:		

L	T	P	C
3	0	0	3

ASSESSMENT PLAN

Course Outcomes (COs)

	At the end of this course, the student should be able to:	**No. of Contact Hours**	**Marks**
CO1:	*Describe general and specific computer architectures and to analyse instruction formats*	12	30
CO2:	*Design processing unit and control unit*	13	40
CO3:	*Discuss memory hierarchy and cache mapping techniques.*	4	10
CO4:	*Describe basic input and output techniques*	4	10
CO5:	*Discuss performance enhancement techniques*	3	10
	Total	36	100

Components	Quizzes	Sessional Tests	End Semester/ Make-up Examination
Duration	20 to 30 minutes	60 minutes	180 minutes
Weightage	20 % (4 X 5 marks)	30 % (2 X 15 Marks)	50 % (1 X 50 Marks)
Typology of Questions	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation	Knowledge/ Recall; Understanding/ Comprehension; Application	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation
Pattern	Answer one randomly selected question from the problem sheet (Students can refer their class notes)	MCQ: 10 questions (0.5 marks) Short Answers: 5 questions (2 marks)	Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks
Schedule	4, 7, 10, and 13th week of academic calendar	Calendared activity	Calendared activity
Topics Covered	Quiz 1 (L 1-L7 & T_{y1-y2}) **(CO1)**	Test 1 (L 1-L13 & T_{b1-b2}) **(CO1- CO2)**	Comprehensive examination covering full syllabus. Students are expected to answer all questions **(CO1-CO5)**
	Quiz 2 (L **8-L15** & T_{y3-y4}) **(CO2)**		
	Quiz 3 (L 16-L26 & T_{y5-y6}) **(CO3, CO4, CO2)**	Test 2 (L 14-L30 & T_{b3-b4}) **(CO2,CO3,CO4,CO5)**	
	Quiz 4 (L 27-L34 & T_{y7-y8}) **(CO2, CO5,CO1)**		

Course Plan

L. No./ T. No.	Topics	Course Outcome Addressed
L0	Introduction, Course plan discussion, Hardware ,software, firmware. Instruction cycle, stored program concept.	1
1	**Processor organization and Instruction sets**	1
2	CPU structures: General Register CPU; Elements of machine instructions and instruction formats:- 3 address , 2 address instruction examples	1
3	Accumulator based machine, 1 address instruction format, example programs, program size	1
4	Stack based machine; concept of stacks; zero address instruction examples	1
5	Instruction types: data transfer, arithmetic, logical and control, shift and rotate , other instructions.	1
6	Addressing modes- general; concept of subroutines & its linking. ; Interrupts	1
7	Encoding of machine instructions: expanding opcode technique, examples.	1
8	Processing unit design: Adder design-carry look ahead adder , delay calculations	2
9	Carry select adder, carry save adder, Wallace tree structure for adding n – numbers.	2
10	Series parallel adder, Delay calculations , ALU design	2

11	Floating point arithmetic; IEEE floating point representation	2
12	Multiplication of un signed integers: array multipliers, sequectial multipliers, Wallace tree structures.	2
13	Multiplication of signed numbers- Booths alogorithm, examples; Modified Booths Algorithm, examples	2
14	Divide overflow concept; Division of unsigned numbers, examples	2
15	Register design , Combinational shifter design.	2
16	Memory organization: Random access and serial access memory; Memory hierarchy; characteristics of memory systems.	3
17	Main memory, cache memory, memory interface.	3
18	Cache memory mapping functions: Associative, set-associative and direct mapping.	3
19	Example mapping functions.	3
20	Input –OUTPUT: Basic concepts of I/O interfacing, accessing I/Os- standard I/O, programmed I/O, Interrupt driven I/O	4
21	Memory mapped I/O, DMA	4
22	Bus strctures: single bus, multiple bus	4
23	Ports; Timers/ counters	4
24	Basic concepts of control unit- microinstructions, hardware implementations	2
25	Control unit deisgn: hardwired control unit	2
26	Hardwired control unit design- continued	2
27	Microprogrammed control unit design	2
28	continued	2
29	Types of architecture: RISC, CISC, dual core, multicore.	5
30	SIMD, MIMD, VLIW, scalar and vector processors.	5
31	Pipelining and parallel processing processing, instruction pipeline, pipeline hazards	5
32	DSP architecture: MAC unit, Floating point unit, special addressing modes	1
33	DSP computational building blocks, Bus architecture and memory, Address generation unit, Modified bus structures and memory access schemes.	1
34	Programmability and program execution	1
35	Fixed point DSP	1
36	Floating point DSP	1

References:

1.	M.Raffiquzzaman & Chandra, "Modern Computer Architecture, Galgotia publications", New Delhi, 1990
2.	David A. Patterson & John L. Hennessy, "Computer Organization and Design. The Hardware/Software Interface", 3rd Edition, Elsevier, 2005
3.	Nicholas Carter, "Computer architecture", Schaum's outlines, McGraw.Hill, New Delhi, 2006.
4.	William Stallings, "Computer Organization and Architecture", Ninth edition, Pearson Education, 2013
5.	Sen M Kuo, Woon Seng Gan, "Digital Signal Processors-Architectures, Implementations and Applications", Pearson Education, 2005.
6.	Venkataramani and Bhaskar, "Digital signal processors- Architecture, programming and Applications", Tata McGraw-Hill Publishing, 2003
7.	Click or tap here to enter text.

Submitted by: Dr. Sampath Kumar

(Signature of the faculty)

Date: 16-08-2022

Approved by: Dr. G. Subrahmanya Nayak

(Signature of HOD)

Date: Click or tap to enter a date.

FACULTY MEMBERS TEACHING THE COURSE (IF MULTIPLE SECTIONS EXIST):

FACULTY	SECTION	FACULTY	SECTION
Dr. Sampath Kumar	A		
Dr. Kanthi Mallya	B		
Ms. Navya K T	C		
Dr. Sampath Kumar	D		
