CHAPTER 4 - SOI CMOS Technology

Complementary MOS (CMOS) is, by far, the technology of choice for the realization of integrated circuits on SOI substrates. This Chapter will compare CMOS processing on bulk silicon and on SOI wafers. Processing of both thin and thicker SOI films will be discussed. We will assume that circuit processing is carried out on commercially available substrates, such as SIMOX wafers. It is worthwhile keeping in mind that, unlike in the case of SOS, SOI wafers contain only silicon and silicon dioxide, and that the appearance of SOI wafers is very similar to that of bulk silicon wafers. As a consequence, SOI circuit processing can be carried out in standard bulk silicon processing lines. Mixed batches (containing both bulk and SOI substrates) can be processed as well.

4.1. Comparison between bulk and SOI processing

Processing techniques for the fabrication of CMOS circuits in bulk silicon and in SOI are very similar. Figure 4.1.1 presents cross-sections of CMOS inverters made in bulk (p-well technology), in "thick-film" SOI (200-500 nm-thick films), and in thin-film SOI.

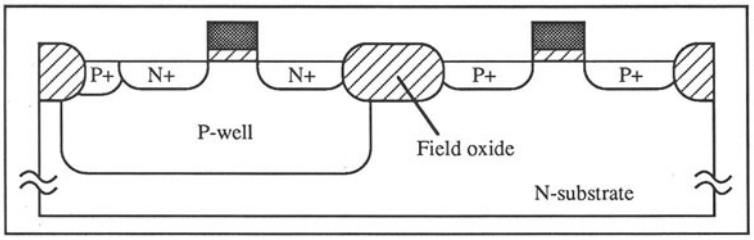

Figure 4.1.1.A: Cross-section of a bulk CMOS inverter.

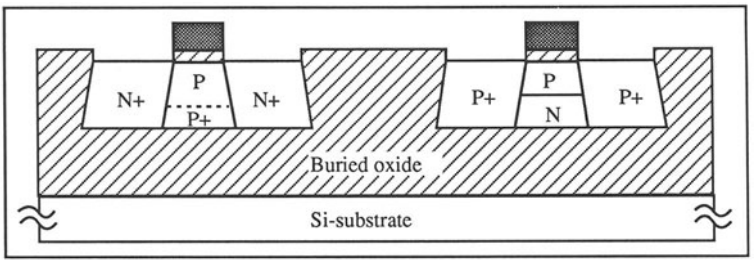

Figure 4.1.1.B: Cross-section of a "thick-film" SOI CMOS inverter.

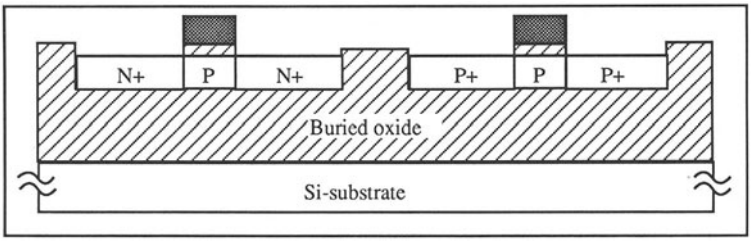

Figure 4.1.1.C: Cross-section of a thin-film SOI CMOS inverter.

The cross sections of Figure 4.1.1 are, of course, quite schematic. For instance, bulk CMOS can be much more complicated than in Figure 4.1.1.A and can make use of an epitaxial substrate, twin wells, or retrograde wells. From the cross sections, it is obvious that SOI processing, and more specifically thin-film SOI processing, is simpler than bulk processing. For instance, there is no need to create diffused wells in SOI. The anti-punchthrough implant used in bulk CMOS is kept unchanged in the case of a p-channel SOI device, and is replaced by a back-channel leakage suppression implant for the n-channel device (Figure 4.1.1.B). In thin-film, fully-depleted SOI devices, these deep implants are unnecessary, and the entire impurity profile in the channel area is determined by a single shallow implant. In the frequent case where N^+ polysilicon is used as gate material, p-type impurities (boron) are used to control the threshold voltage in both the n-channel and the p-channel devices (Figure 4.1.1.C). Table 4.1.1 compares simplified CMOS process flows for bulk, "thick-film", partially-depleted (PD) SOI, and thin-film, fully-depleted (FD) SOI. It can be observed that SOI processing is simpler (less steps), and that at least one mask step is