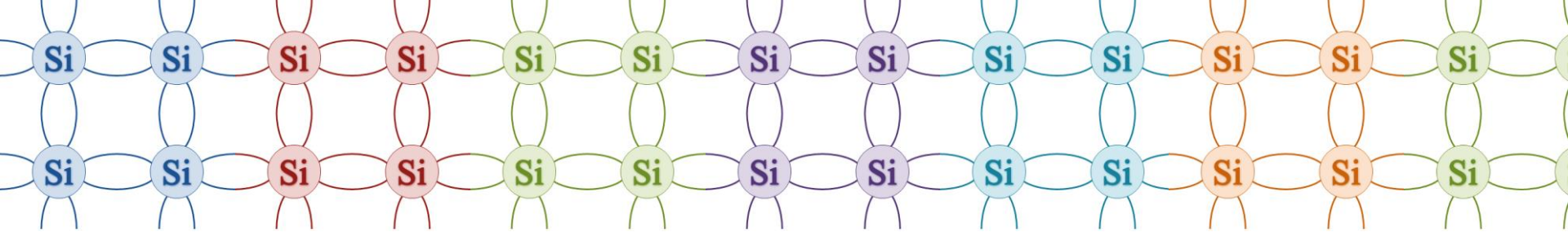
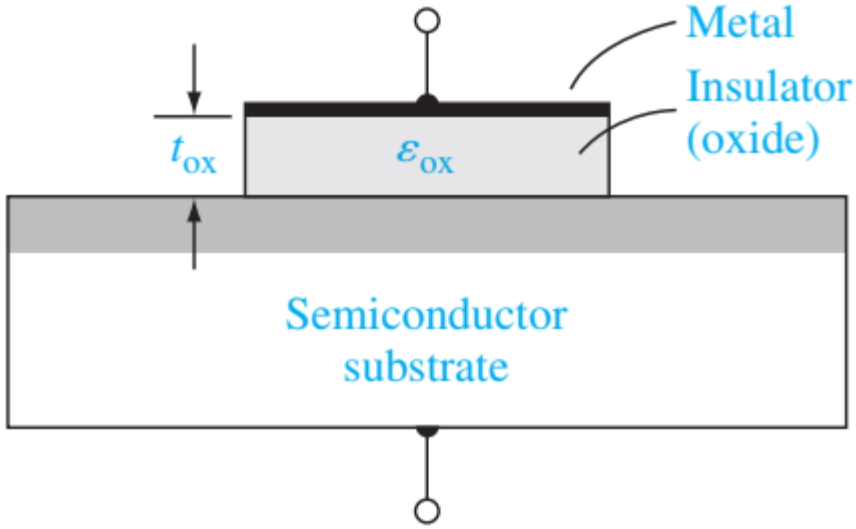


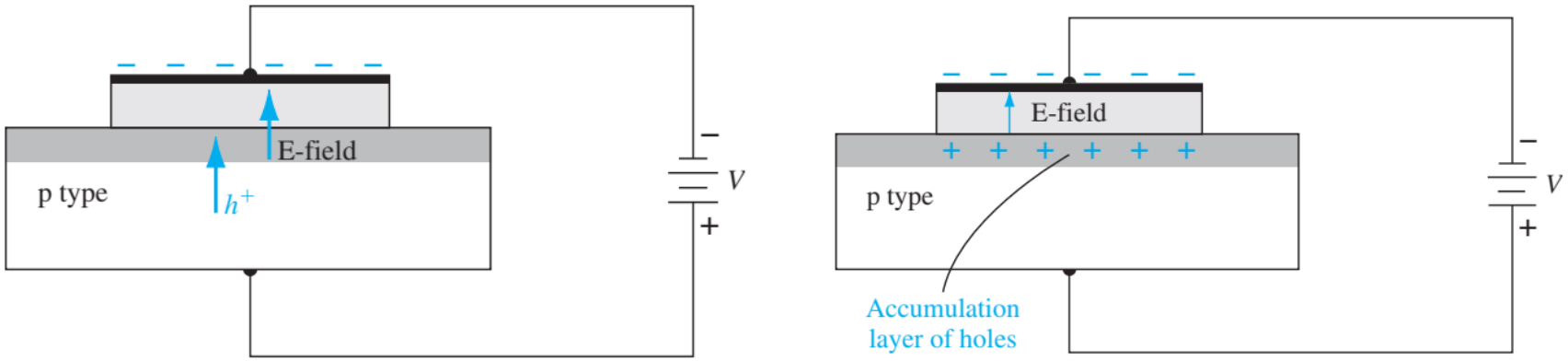
MOSFET

- The physics of the MOS structure can be more easily explained with the aid of the simple parallel-plate capacitor.



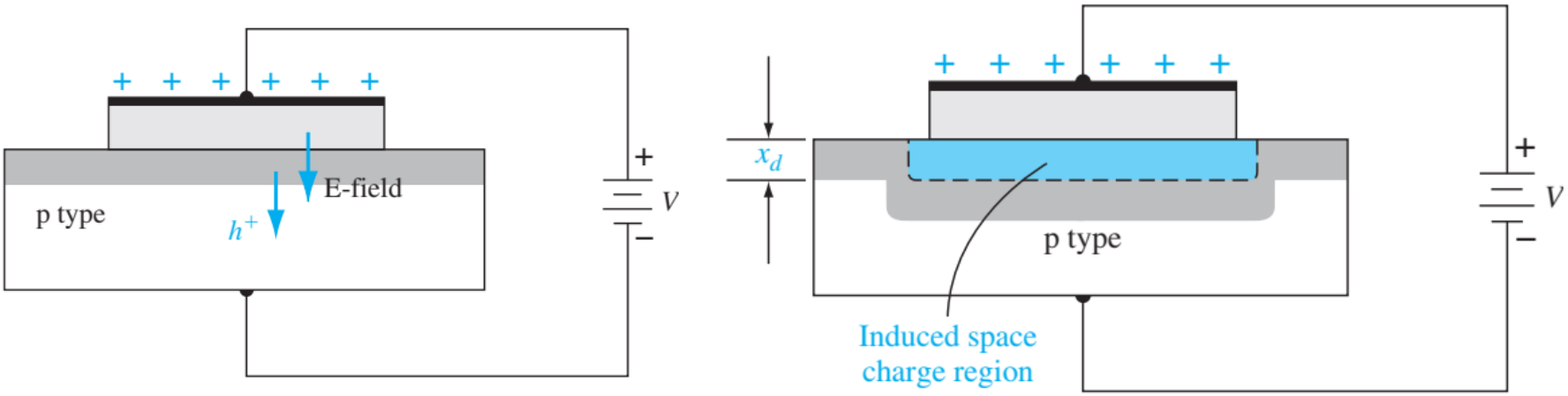
The basic MOS capacitor structure.

Accumulation Mode ($V_G<0$)



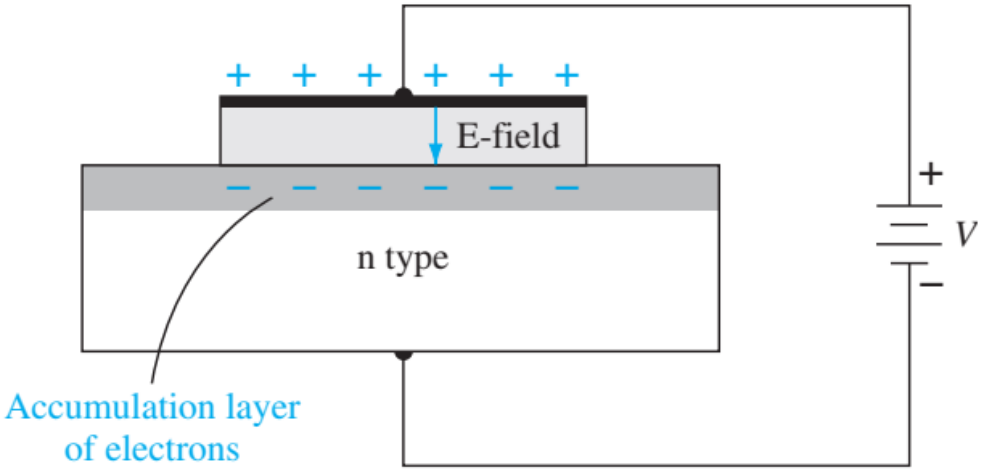
- The top metal gate is at a negative voltage with respect to the semiconductor substrate.
- Negative charge will exist on the top metal plate and an electric field will be induced with
- the direction bottom to top.
- If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide– semiconductor interface.
- A pile of holes of holes at the oxide–semiconductor junction has occurred is called as *accumulation*

Depletion ($0 < V_G < V_{TH}$)



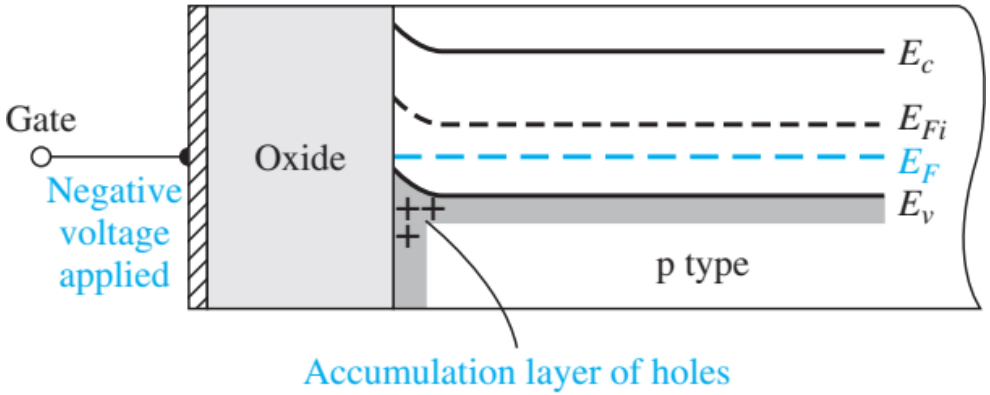
- The top metal gate is at a positive with respect to the semiconductor substrate.
- If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a force away from the oxide–semiconductor interface.
- As the holes are pushed away from the interface, a negative space charge region is created because of the fixed ionized acceptor atoms.
- This is known as Depletion.

Inversion ($V_G > V_{TH}$)

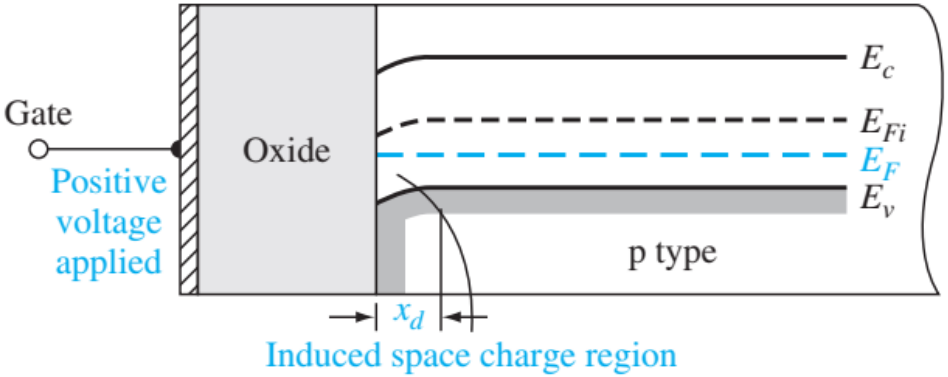


- We consider the case when a larger positive voltage is applied to the top metal gate of the MOS capacitor
- The p-region near to interface is converted into n-region and hence is called inversion.

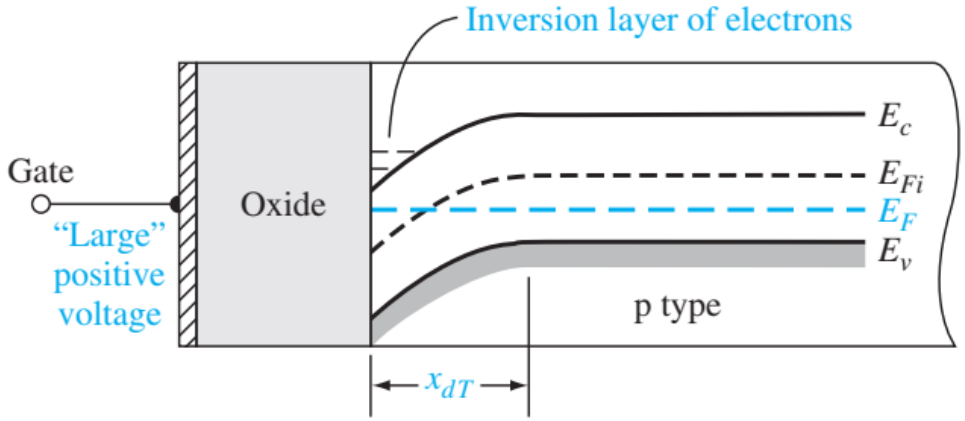
Accumulation Mode ($V_G<0$)



Depletion ($0 < V_G < V_{TH}$)



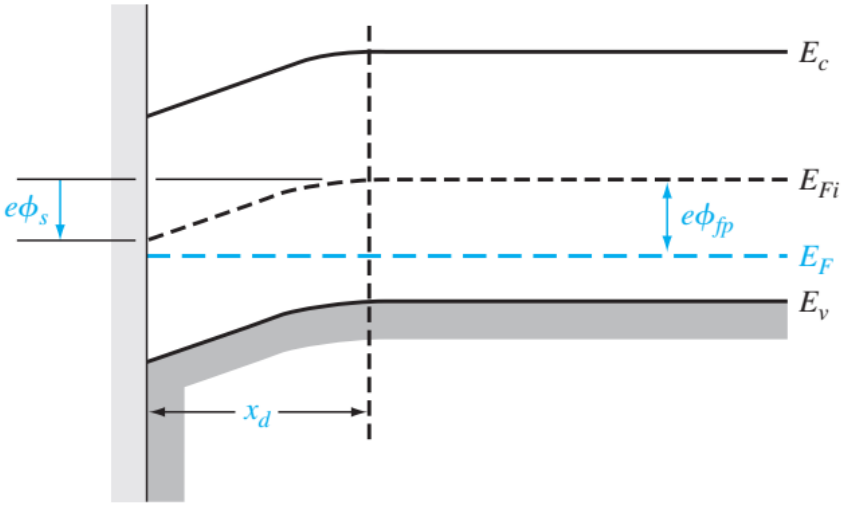
Inversion ($V_G > V_{TH}$)



Depletion Width

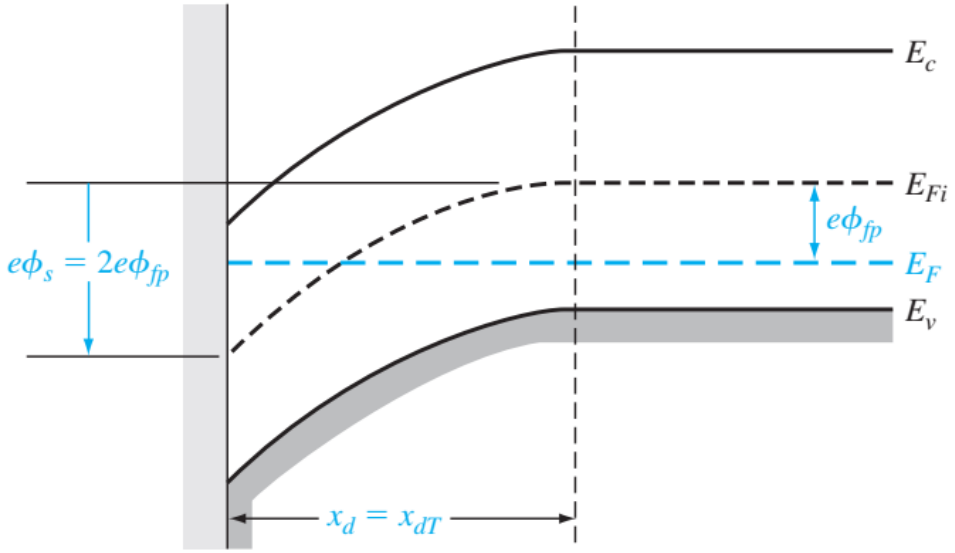
$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a}\right)^{1/2}$$



Maximum Depletion Width (x_{dT})

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a}\right)^{1/2}$$



Objective: Calculate the maximum space charge width for a given semiconductor doping concentration.

Consider silicon at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}. The intrinsic carrier concentration is $n_i = 1.5 \times 10^{10}$ cm^{-3}.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.3473 \text{ V}$$

Then the maximum space charge width is

$$x_{dT} = \left[\frac{4\epsilon_s \phi_{fp}}{eN_a}\right]^{1/2} = \left[\frac{4(11.7)(8.85 \times 10^{-14})(0.3473)}{(1.6 \times 10^{-19})(10^{16})}\right]^{1/2}$$

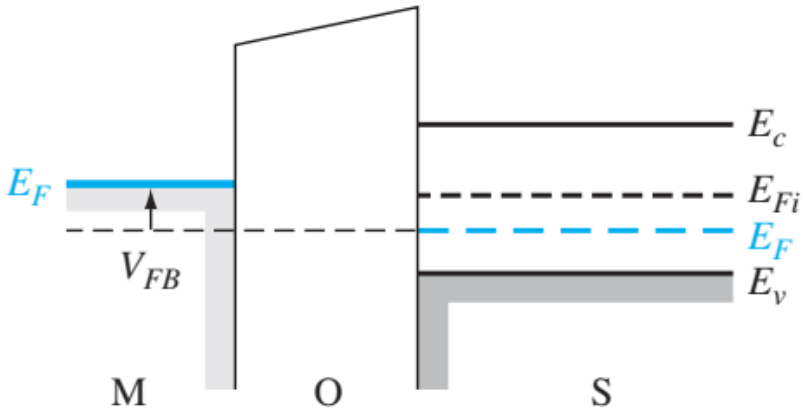
or

$$x_{dT} \cong 0.30 \times 10^{-4} \text{ cm} = 0.30\ \mu\text{m}$$

Consider an oxide-to-p-type silicon junction at $T = 300$ K. The impurity doping concentration in the silicon is $N_a = 2 \times 10^{15}$ cm^{-3}. Calculate the maximum space charge width. Does the space charge width increase or decrease as the p-type doping concentration decreases?

(Ans. $x_{dT} = 0.629\ \mu$m, increase)

The *flat-band voltage* is defined as the applied gate voltage such that there is no band bending in the semiconductor and, as a result, zero net space charge in this region.



Energy-band diagram of a MOS capacitor at flat band.

- In an ideal scenario, it is considered that there is zero net charge density in the oxide material.
- Work function difference and possible trapped charge in the oxide may make the net fixed charge density usually positive, which may exist in the insulator.

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

V_{FB} is the flat-band voltage, C_{ox} is oxide capacitance per unit area and Q'_{ss} is equivalent trapped charge per unit area, ϕ_{ms} is metal semiconductor work function.

Objective: Calculate the flat-band voltage for a MOS capacitor with a p-type semiconductor substrate.

Consider a MOS capacitor with a p-type silicon substrate doped to $N_a = 10^{16}$ cm^{-3}, a silicon dioxide insulator with a thickness of $t_{ox} = 20$ nm $= 200$ Å, and an n$^+$ polysilicon gate. Assume that $Q'_{ss} = 5 \times 10^{10}$ electronic charges per cm^2. $\phi_{ms} \cong -1.1$V

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{200 \times 10^{-8}} = 1.726 \times 10^{-7} \text{ F/cm}^2$$

The equivalent oxide charge density is

$$Q'_{ss} = (5 \times 10^{10})(1.6 \times 10^{-19}) = 8 \times 10^{-9} \text{ C/cm}^2$$

The flat-band voltage is then determined to be

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} = -1.1 - \frac{8 \times 10^{-9}}{1.726 \times 10^{-7}} = -1.15 \text{ V}$$

The applied gate voltage required to achieve the flat-band condition for this p-type substrate is negative. If the amount of fixed oxide charge increases, the flat-band voltage becomes even more negative.

The threshold voltage is defined as the applied gate voltage required to achieve the threshold inversion point.

The threshold inversion point, in turn, is defined as the condition when the surface potential is $\phi_s = 2\phi_{fp}$ for the p-type semiconductor

$$V_{TN} = \frac{|Q'_{SD}\,(\max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp}$$

$$V_{TN} = \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\phi_{fp}$$

$$V_{TN} = \left(|Q'_{SD}(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$V_{TN} = V_{FB} + 2\phi_{fp} + \frac{eN_a x_{dT}}{C_{ox}}$$

$$V_{TP} = \left(-|Q'_{SD}\,(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

$$V_{TP} = V_{FB} - 2\phi_{fn} - \frac{eN_d x_{dT}}{C_{ox}}$$

Objective: Calculate the threshold voltage of a MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{15}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 12$ nm $= 120$ Å, and assume the oxide is silicon dioxide. $\phi_{ms} \cong -0.88$ V

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{15}}{1.5 \times 10^{10}}\right) = 0.2877 \text{ V}$$

and

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.2877)}{(1.6 \times 10^{-19})(10^{15})}\right\}^{1/2} = 8.63 \times 10^{-5} \text{ cm}$$

Then

$$|Q'_{SD}(\max)| = eN_a x_{dT} = (1.6 \times 10^{-19})(10^{15})(8.63 \times 10^{-5}) = 1.381 \times 10^{-8} \text{ C/cm}^2$$

The threshold voltage is now found to be

$$V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$= [(1.381 \times 10^{-8}) - (10^{10})(1.6 \times 10^{-19})] \cdot \left[\frac{120 \times 10^{-8}}{(3.9)(8.85 \times 10^{-14})}\right]$$

$$+ (-0.88) + 2(0.2877)$$

or

$$V_{TN} = -0.262 \text{ V}$$

In this example, the semiconductor is fairly lightly doped, which, in conjunction with the positive charge in the oxide and the work function difference, is sufficient to induce an electron inversion layer charge even with zero applied gate voltage. This condition makes the threshold voltage negative.

Determine the threshold voltage for a silicon MOS device at $T = 300$ K for the following parameters: p^+ polysilicon gate, $\phi_{ms} \cong +0.28$ V, $N_a = 2 \times 10^{16}$ cm^{-3}, $t_{ox} = 8$ nm $= 80$ Å, and $Q'_{ss} = 2 \times 10^{10}$ cm^{-2}.

(Ans. $V_{TN} = +1.16$ V)

Consider a MOS capacitor with silicon dioxide and an n-type silicon substrate at $T = 300$ K with the following parameters: p^+ polysilicon gate, $N_d = 2 \times 10^{16}$ cm^{-3}, $t_{ox} = 20$ nm $= 200$ Å, and $Q'_{ss} = 5 \times 10^{10}$ cm^{-2}. Determine the threshold voltage. Is the capacitor an enhancement mode or depletion mode device?

$$\phi_{ms} \cong 0.35\,\text{V}.$$

$$V_{TN} = -0.83, \textit{Enhancement Mode}$$

Consider a MOS device with a p-type silicon substrate with $N_a = 2 \times 10^{16}$ cm^{-3}. The oxide thickness is $t_{ox} = 15$ nm $= 150$ Å and the equivalent oxide charge is $Q'_{ss} = 7 \times 10^{10}$ cm^{-2}. Calculate the threshold voltage for (*a*) an n$^+$ polysilicon gate, (*b*) a p$^+$ polysilicon gate, and (*c*) an aluminum gate.

$$\text{n}^+ \text{ poly gate on p-type: } \phi_{ms} \cong -1.12 \text{ V}$$

$$\text{p}^+ \text{ poly gate on p-type: } \phi_{ms} \cong +0.28 \text{ V}$$

$$\text{Al gate on p-type: } \phi_{ms} \cong -0.95 \text{ V}$$

$$\phi_{fp} = (0.0259)\ln\left(\frac{2\times10^{16}}{1.5\times10^{10}}\right) = 0.3653 \text{ V}$$

$$x_{dT} = \left[\frac{4(11.7)(8.85\times10^{-14})(0.3653)}{(1.6\times10^{-19})(2\times10^{16})}\right]^{1/2}$$

$$= 2.174\times10^{-5} \text{ cm}$$

$$|Q'_{SD}(\max)| = eN_a x_{dT}$$

$$= (1.6\times10^{-19})(2\times10^{16})(2.174\times10^{-5})$$

$$= 6.958\times10^{-8} \text{ C/cm}^2$$

$$C_{ox} = \frac{(3.9)(8.85\times10^{-14})}{150\times10^{-8}} = 2.301\times10^{-7} \text{ F/cm}^2$$

$$V_{TN} = \frac{|Q'_{SD}(\max)| - Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp}$$

$$= \frac{6.958\times10^{-8} - (7\times10^{10})(1.6\times10^{-19})}{2.301\times10^{-7}} + \phi_{ms} + 2(0.3653)$$

$$= 0.9843 + \phi_{ms}$$

(a) n$^+$ poly gate on p-type: $\phi_{ms} \cong -1.12$ V

$$V_{TN} = 0.9843 - 1.12 = -0.136 \text{ V}$$

(b) p$^+$ poly gate on p-type: $\phi_{ms} \cong +0.28$ V

$$V_{TN} = 0.9843 + 0.28 = +1.26 \text{ V}$$

(c) Al gate on p-type: $\phi_{ms} \cong -0.95$ V

$$V_{TN} = 0.9843 - 0.95 = +0.0343 \text{ V}$$

(*a*) Calculate the maximum space charge width x_{dT} and the maximum space charge density $|Q'_{SD}(\max)|$ in a MOS capacitor with a p-type silicon substrate at $T = 300$ K for doping concentrations of (*i*) $N_a = 7 \times 10^{15}$ cm^{-3} and (*ii*) $N_a = 3 \times 10^{16}$ cm^{-3}.
(*b*) Repeat part (*a*) for $T = 350$ K.

(i)

$$\phi_{fp} = 0.3381\,\text{V}$$

$$x_{dT} = 0.354\,\mu\,\text{m}$$

(ii)

$$\phi_{fp} = 0.3758\,\text{V}$$

$$x_{dT} = 0.180\,\mu\,\text{m}$$

(i)

$$\phi_{fp} = 0.3173\,\text{V}$$

$$x_{dT} = 0.343\,\mu\,\text{m}$$

(ii)

$$\phi_{fp} = 0.3613\,\text{V}$$

$$x_{dT} = 0.177\,\mu\,\text{m}$$

$$C'(\text{acc}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

$$\frac{1}{C'(\text{depl})} = \frac{1}{C_{\text{ox}}} + \frac{1}{C'_{SD}}$$

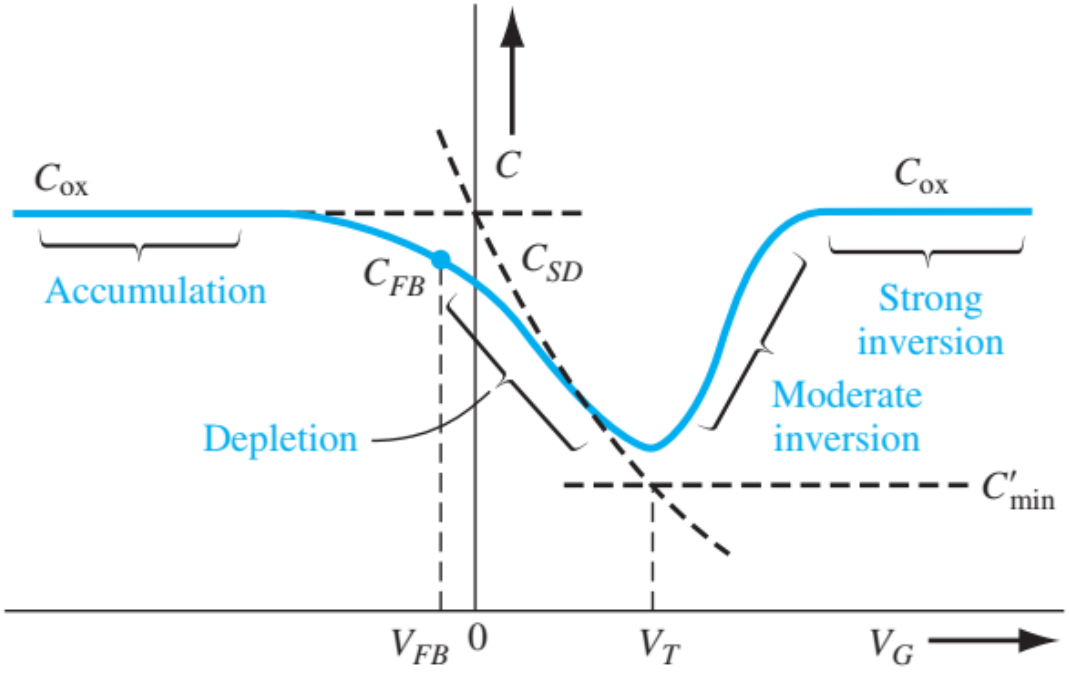
$$C'(\text{depl}) = \frac{C_{\text{ox}} C'_{SD}}{C_{\text{ox}} + C'_{SD}}$$

$$C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}} \text{ and } C'_{SD} = \epsilon_s/x_d$$

$$C'(\text{depl}) = \frac{C_{\text{ox}}}{1 + \dfrac{C_{\text{ox}}}{C'_{SD}}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \left(\dfrac{\epsilon_{\text{ox}}}{\epsilon_s}\right) x_d}$$

$$C'_{\text{min}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \left(\dfrac{\epsilon_{\text{ox}}}{\epsilon_s}\right) x_{dT}}$$

$$C'(\text{inv}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$



$$C'_{FB} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \left(\dfrac{\epsilon_{\text{ox}}}{\epsilon_s}\right)\sqrt{\left(\dfrac{kT}{e}\right)\left(\dfrac{\epsilon_s}{eN_a}\right)}}$$

Objective: Calculate C_{ox}, $C'_{\min}$, and C'_{FB} for a MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}.

The oxide is silicon dioxide with a thickness of $t_{ox} = 18$ nm $= 180$ Å, and the gate is aluminum.

The oxide capacitance is

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8}} = 1.9175 \times 10^{-7} \text{ F/cm}^2$$

To find the minimum capacitance, we need to calculate

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.3473 \text{ V}$$

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.3473)}{(1.6 \times 10^{-19})(10^{16})}\right\}^{1/2}$$

$$\cong 0.30 \times 10^{-4} \text{ cm}$$

$$C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)x_{dT}} = \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8} + \left(\frac{3.9}{11.7}\right)(0.30 \times 10^{-4})}$$

$$= 2.925 \times 10^{-8} \text{ F/cm}^2$$

The flat-band capacitance is

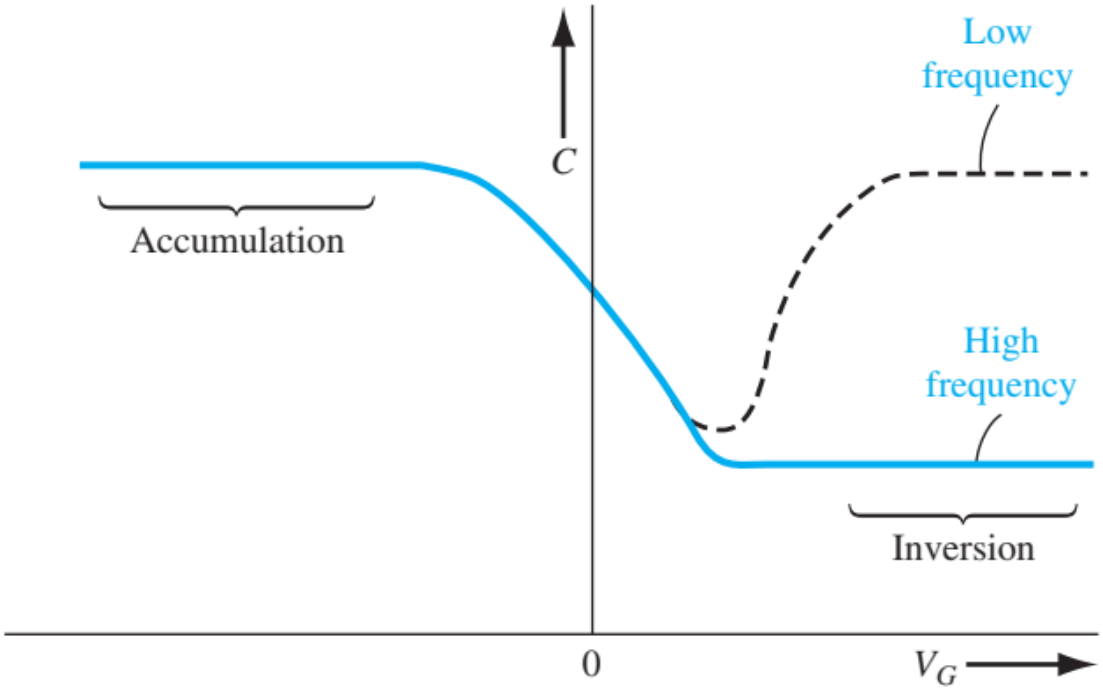
$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{V_t \epsilon_s}{eN_a}}}$$

$$= \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8} + \left(\frac{3.9}{11.7}\right)\sqrt{\frac{(0.0259)(11.7)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(10^{16})}}}$$

$$= 1.091 \times 10^{-7}\ \text{F/cm}^2$$

Consider a MOS capacitor with the following parameters: n^+ polysilicon gate, $N_a = 3 \times 10^{16}\ \text{cm}^{-3}$, $t_{ox} = 8\ \text{nm} = 80\ \text{Å}$, and $Q'_{ss} = 2 \times 10^{10}\ \text{cm}^{-2}$. Determine the ratios C'_{min}/C_{ox} and C'_{FB}/C_{ox}.

(Ans. $C'_{\text{min}}/C_{ox} = 0.118$, $C'_{FB}/C_{ox} = 0.504$)



Low-frequency and high-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate.

- The electron concentration in the inversion layer, then, cannot change instantaneously.
- If the ac voltage across the MOS capacitor changes rapidly, the change in the inversion layer charge will not be able to respond.
- The inversion layer charge will not respond to a differential change in capacitor voltage.

An ideal MOS capacitor with an n^+ polysilicon gate has a silicon dioxide thickness of $t_{ox} = 12$ nm $= 120$ Å on a p-type silicon substrate doped at $N_a = 10^{16}$ cm^{-3}. Determine the capacitance C_{ox}, C'_{FB}, C'_{min}, and $C'(\text{inv})$ at (a) $f = 1$ Hz and (b) $f = 1$ MHz. (c) Determine V_T.

(a) For $f = 1$ Hz (low freq),

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{120\times10^{-8}}$$

$$= 2.876\times10^{-7}\ \text{F/cm}^2$$

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{V_t\,\epsilon_s}{eN_a}}}$$

$$= \frac{(3.9)(8.85\times10^{-14})}{120\times10^{-8} + \left(\frac{3.9}{11.7}\right)\sqrt{\frac{(0.0259)(11.7)(8.85\times10^{-14})}{(1.6\times10^{-19})(10^{16})}}}$$

$$C'_{FB} = 1.346\times10^{-7}\ \text{F/cm}^2$$

$$C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\cdot x_{dT}}$$

Now

$$\phi_{fp} = (0.0259)\ln\left(\frac{10^{16}}{1.5\times10^{10}}\right) = 0.3473\ \text{V}$$

$$x_{dT} = \left[\frac{4(11.7)(8.85\times10^{-14})(0.3473)}{(1.6\times10^{-19})(10^{16})}\right]^{1/2}$$

$$= 3.00\times10^{-5}\ \text{cm}$$

$$C'_{\min} = \frac{(3.9)(8.85\times10^{-14})}{120\times10^{-8} + \left(\frac{3.9}{11.7}\right)(3.00\times10^{-5})}$$

$$= 3.083\times10^{-8}\ \text{F/cm}^2$$

$$C'(\text{inv}) = C_{ox} = 2.876\times10^{-7}\ \text{F/cm}^2$$

(b) $f = 1$ MHz (high freq),

$C_{ox} = 2.876\times10^{-7}$ F/cm^2 (unchanged)

$C'_{FB} = 1.346\times10^{-7}$ F/cm^2 (unchanged)

$C'_{\min} = 3.083\times10^{-8}$ F/cm^2 (unchanged

$C'(\text{inv}) = C'_{\min} = 3.083\times10^{-8}$ F/cm^2

(c) $V_{FB} = \phi_{ms} \cong= -1.10$ V

$$V_{TN} = \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\phi_{fp}$$

Now

$$|Q'_{SD}(\max)| = eN_a x_{dT}$$

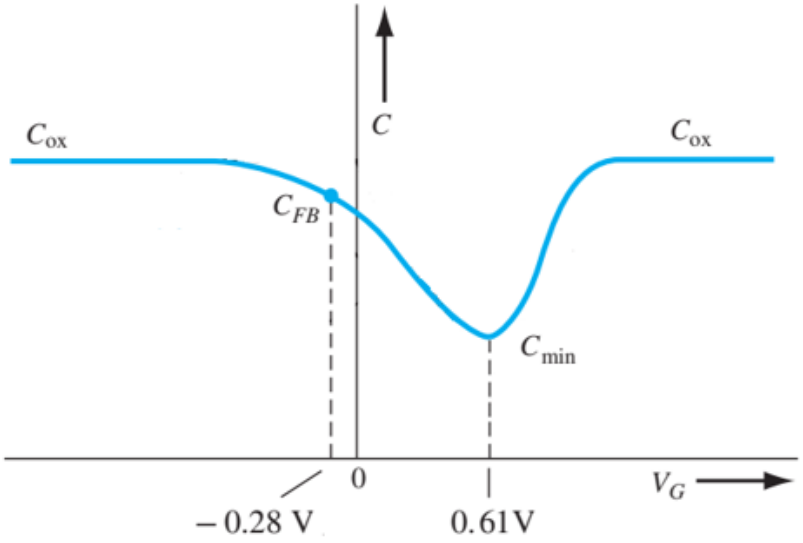
$$= (1.6\times10^{-19})(10^{16})(3.00\times10^{-5})$$

$$= 4.80\times10^{-8}\ \text{C/cm}^2$$

$$V_{TN} = \frac{4.80\times10^{-8}}{2.876\times10^{-7}} - 1.10 + 2(0.3473)$$

$$V_{TN} = -0.2385\ \text{V}$$

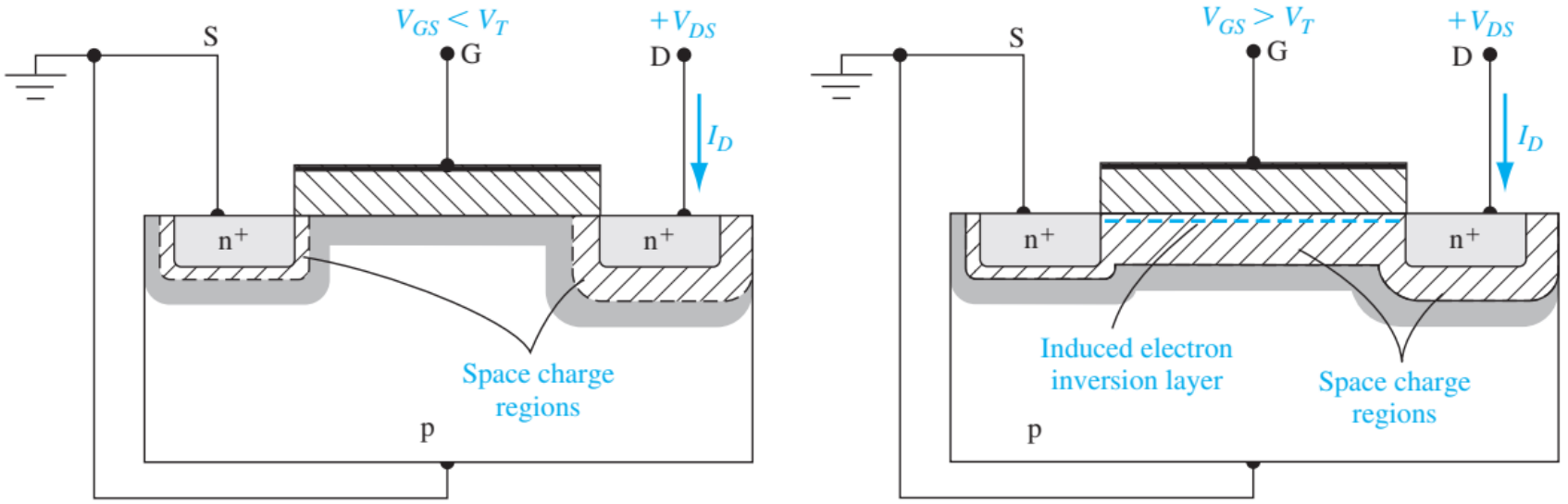
Calculate the oxide capacitance and oxide thickness. Consider the figure shown below for an n-channel silicon MOSFET at T=300 K. Assume the substrate doping as $N_a = 2\times10^{16}$ cm^{-3}.



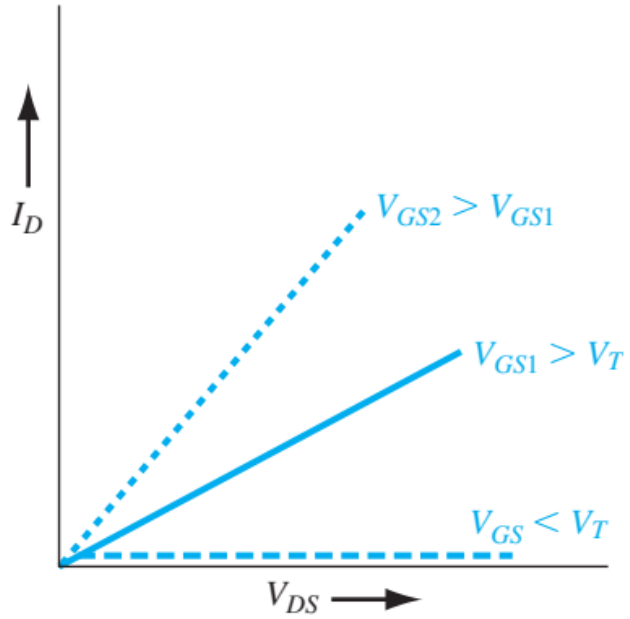
$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) \qquad x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} \qquad V_{TN} = V_{FB} + 2\phi_{fp} + \frac{eN_a x_{dT}}{C_{ox}}$$

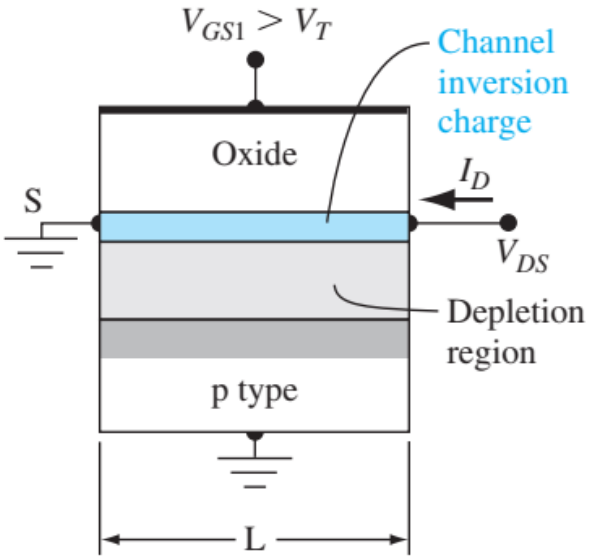
$$Cox = 4.36 \times 10^{-7} F/cm^2$$

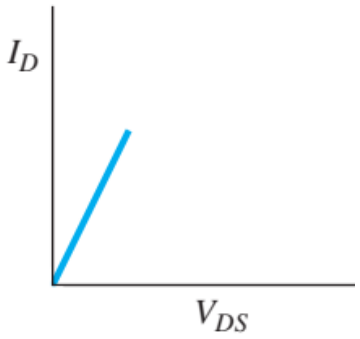
$$tox = 7.9163nm$$

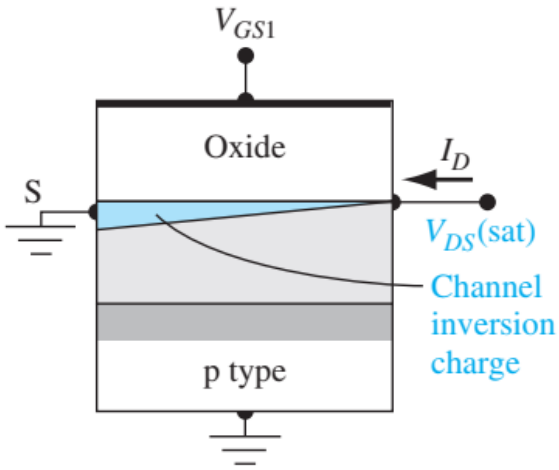


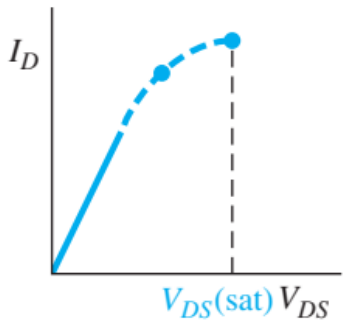
The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ and (b) with an applied gate voltage $V_{GS} > V_T$.

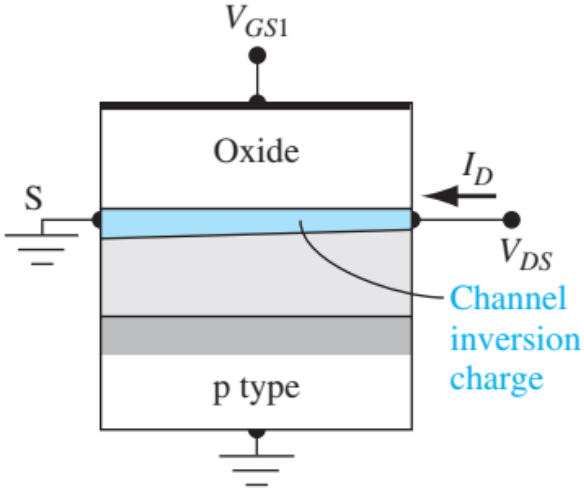


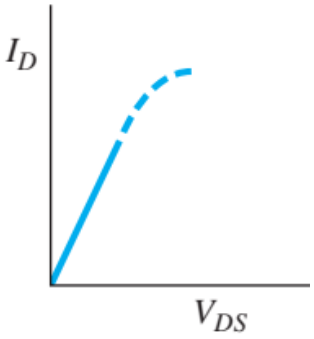

$V_{GS1} > V_T$
Channel inversion charge
Oxide
I_D
S
V_{DS}
Depletion region
p type
L

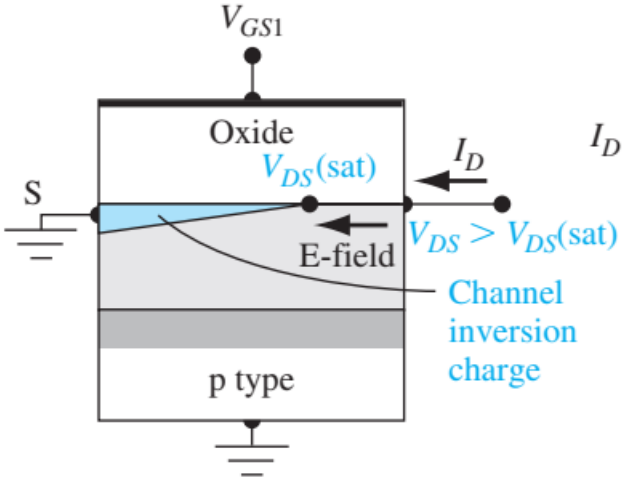

I_D
V_{DS}

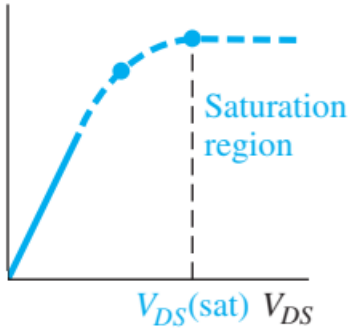

V_{GS1}
Oxide
I_D
S
V_{DS}(sat)
Channel inversion charge
p type

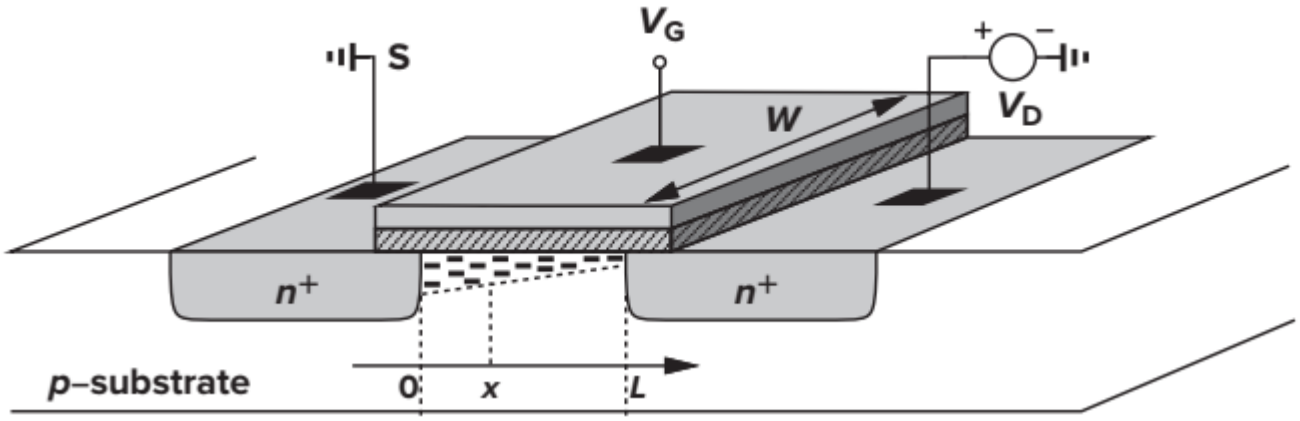

I_D
V_{DS}(sat) V_{DS}


V_{GS1}
Oxide
I_D
S
V_{DS}
Channel inversion charge
p type


I_D
V_{DS}


V_{GS1}
Oxide
V_{DS}(sat)
I_D
S
$V_{DS} > V_{DS}$(sat)
E-field
Channel inversion charge
p type


I_D
Saturation region
V_{DS}(sat) V_{DS}



$$I = Q_d \cdot v$$

$$Q_d = WC_{ox}(V_{GS} - V_{TH})$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}]$$

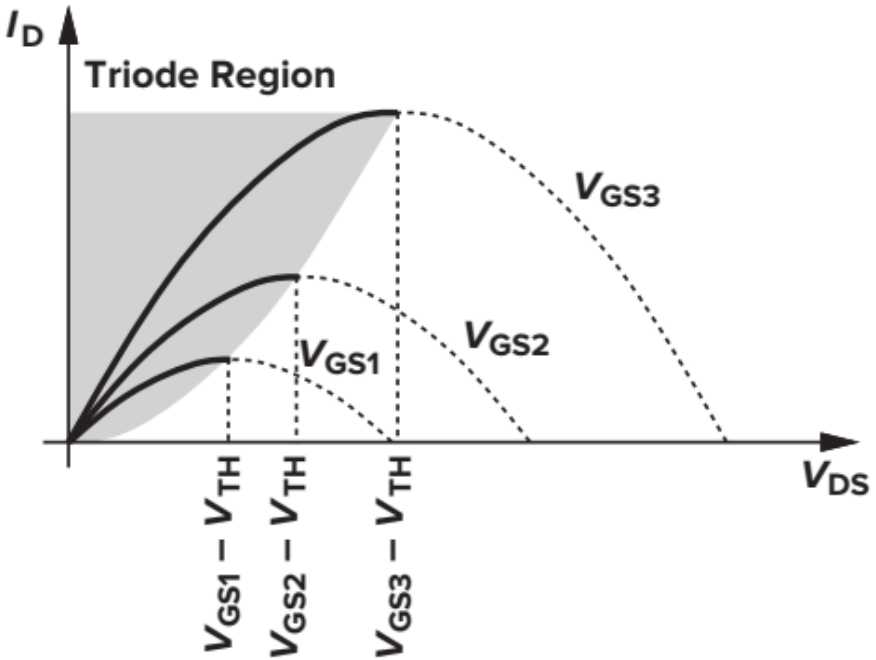
$$V_{DS} = V_{GS} - V_{TH}$$

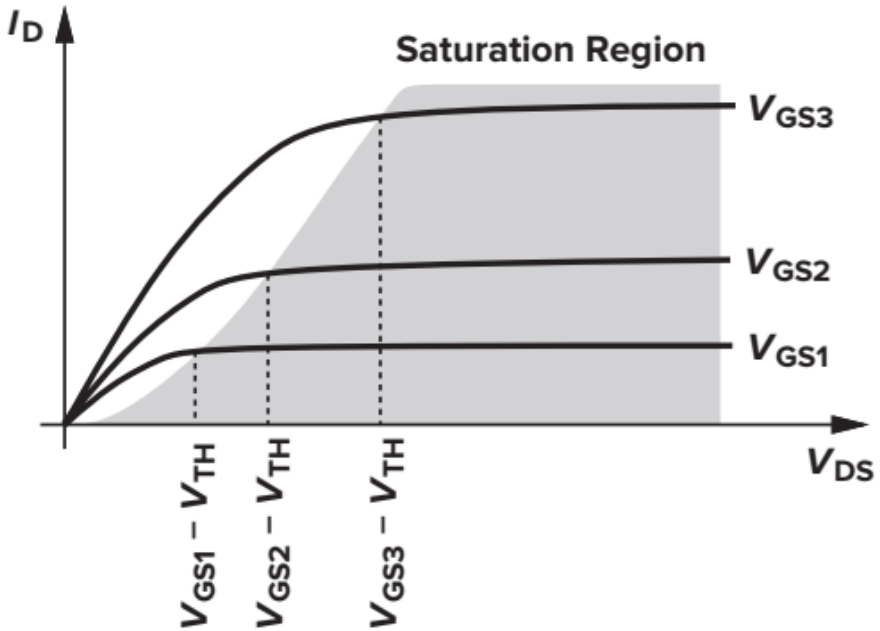
$$v = \mu E$$

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

$$I_{D,\,max} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV$$


I_D
Triode Region
V_{GS3}
V_{GS2}
V_{GS1}
V_{DS}
$V_{GS1} - V_{TH}$
$V_{GS2} - V_{TH}$
$V_{GS3} - V_{TH}$


I_D
Saturation Region
V_{GS3}
V_{GS2}
V_{GS1}
V_{DS}
$V_{GS1} - V_{TH}$
$V_{GS2} - V_{TH}$
$V_{GS3} - V_{TH}$

Objective: Design the width of a MOSFET such that a specified current is induced for a given applied bias.

Consider an ideal n-channel MOSFET with parameters $L = 1.25\ \mu\text{m}$, $\mu_n = 650\ \text{cm}^2/\text{V-s}$, $C_{ox} = 6.9 \times 10^{-8}\ \text{F/cm}^2$, and $V_T = 0.65\ \text{V}$. Design the channel width W such that $I_D(\text{sat}) = 4\ \text{mA}$ for $V_{GS} = 5\ \text{V}$.

$$I_D(\text{sat}) = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$$

or

$$4 \times 10^{-3} = \frac{W(650)(6.9 \times 10^{-8})}{2(1.25 \times 10^{-4})} \cdot (5 - 0.65)^2 = 3.39\ W$$

Then

$$W = 11.8\ \mu\text{m}$$

The current capability of a MOSFET is directly proportional to the channel width W. The current handling capability can be increased by increasing W.

The parameters of an n-channel silicon MOSFET are $\mu_n = 650$ cm^2/V-s, $t_{ox} = 8$ nm $= 80$ Å, $W/L = 12$, and $V_T = 0.40$ V. If the transistor is biased in the saturation region, find the drain current for (*a*) $V_{GS} = 0.8$ V, (*b*) $V_{GS} = 1.2$ V, and (*c*) $V_{GS} = 1.6$ V.

[Ans. (*a*) 0.269 mA; (*b*) 1.077 mA; (*c*) 2.423 mA]

Objective: Determine the inversion carrier mobility from experimental results.

Consider an n-channel MOSFET with $W = 15\ \mu$m, $L = 2\ \mu$m, and $C_{ox} = 6.9 \times 10^{-8}$ F/cm^2. Assume that the drain current in the nonsaturation region for $V_{DS} = 0.10$ V is $I_D = 35\ \mu$A at $V_{GS} = 1.5$ V and $I_D = 75\ \mu$A at $V_{GS} = 2.5$ V.

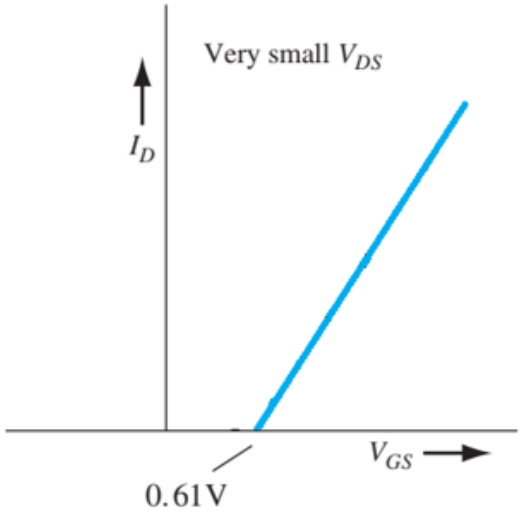
$$I_{D2} - I_{D1} = \frac{W\mu_n C_{ox}}{L}(V_{GS2} - V_{GS1})V_{DS}$$

$$\mu_n = 773 \text{ cm}^2/\text{V-s}$$

$$75 \times 10^{-6} - 35 \times 10^{-6} = \left(\frac{15}{2}\right)\mu_n(6.9 \times 10^{-8})(2.5 - 1.5)(0.10)$$

$$V_T = 0.625 \text{ V}$$

Calculate the aspect ratio W/L of the MOSFET and drain current of MOSFET at V_{GS}=1V. Consider the figure shown for an n-channel silicon MOSFET at T=300 K, the straight line has a slope of 4×10^{-5}. Assume Cox = 6.9×10^{-8} F /cm^2, μ_n = 773 cm^2/V-s and V_D= 0.10V.



For the small value of V_{DS},

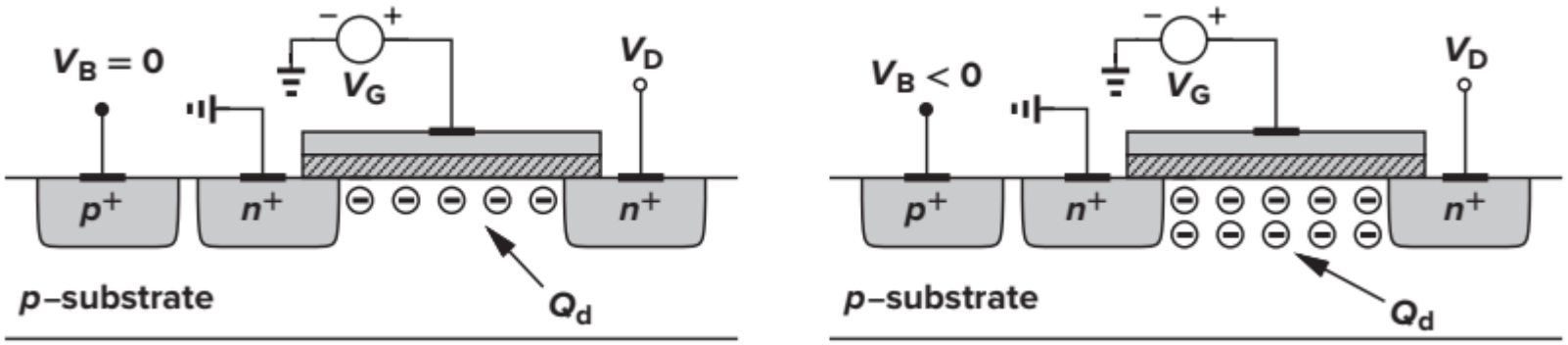
$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}$$

From the diagram and above equation

$$V_{TH} = 0.61V \text{ and } \mu_n C_{ox} \frac{W}{L} V_{DS} = 4 \times 10^{-5}$$

$$\frac{W}{L} = \frac{4 \times 10^{-5}}{\mu_n C_{ox} V_{DS}} = \frac{4 \times 10^{-5}}{773 \times 6.9 \times 10^{-8} \times 0.10} = 7.5$$

$$I_D = 773 \times 6.9 \times 10^{-8} \times 7.5 \times (1 - 0.61) \times 0.10 = 15.6\mu A$$



- When $V_S = V_D = 0$, and V_G is somewhat less than V_{TH}, a depletion region is formed under the gate but no inversion layer exists.
- As V_B becomes more negative, more holes are attracted to the substrate connection, leaving a larger negative charge behind; the depletion region becomes wider.
- Threshold voltage is a function of the total charge in the depletion region. Thus, as V_B drops and Q_D increases, V_{TH} also increases.

$$V_T = V_{T_0} + \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

$$\Delta V_T = \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

γ is defined as the *body-effect coefficient*. $\gamma = \dfrac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}$

Objective: Calculate the body-effect coefficient and the change in the threshold voltage due to an applied source-to-body voltage.

Consider an n-channel silicon MOSFET at $T = 300$ K. Assume the substrate is doped to $N_a = 3 \times 10^{16}$ cm^{-3} and assume the oxide is silicon dioxide with a thickness of $t_{ox} = 20$ nm $= 200$ Å. Let $V_{SB} = 1$ V.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259) \ln\left(\frac{3 \times 10^{16}}{1.5 \times 10^{10}}\right) = 0.3758 \text{ V}$$

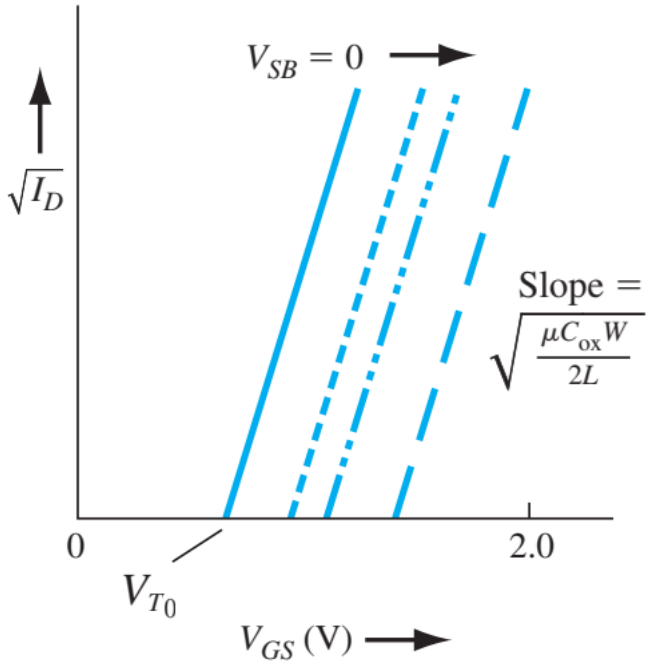
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{200 \times 10^{-8}} = 1.726 \times 10^{-7} \text{ F/cm}^2$$

$$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} = \frac{[2(1.6 \times 10^{-19})(11.7)(8.85 \times 10^{-14})(3 \times 10^{16})]^{1/2}}{1.726 \times 10^{-7}}$$

$$\gamma = 0.5776 \text{ V}^{1/2}$$

The change in threshold voltage for $V_{SB} = 1$ V is found to be

$$\begin{aligned}\Delta V_T &= \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right] \\ &= (0.5776)\left[\sqrt{2(0.3758) + 1} - \sqrt{2(0.3758)}\right] \\ &= (0.5776)[1.3235 - 0.8669] = 0.264 \text{ V}\end{aligned}$$



$$\sqrt{I_D(\text{sat})} = \sqrt{\frac{W\mu_n C_{\text{ox}}}{2L}}(V_{GS} - V_{T_0})$$

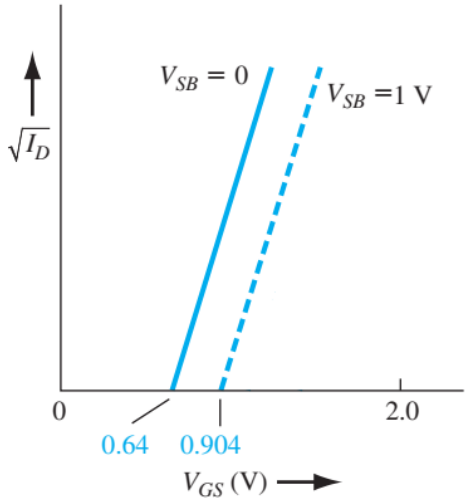
Intercept = V_{T_0}

$$V_T = V_{T_0} + \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

$$\sqrt{I_D(\text{sat})} = \sqrt{\frac{W\mu_n C_{\text{ox}}}{2L}}\left(V_{GS} - \left(V_{T_0} + \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]\right)\right)$$

Intercept = $\left(V_{T_0} + \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]\right)$

Calculate the body coefficient, oxide capacitance (C_{ox}), and the oxide thickness. Consider the figure shown below for an n-channel silicon MOSFET at T=300 K. Assume the substrate is doped to Na=3×10^{16} cm.



$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{3\times10^{16}}{1.5\times10^{10}}\right) = 0.3758 \text{ V}$$

$$\Delta V_T = \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

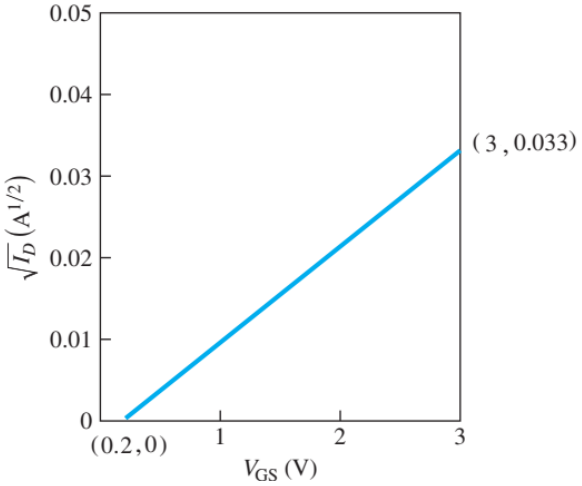
$$\gamma = 0.5783$$

$$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}$$

$$C_{ox} = 1.726\times10^{-7} \text{ F/cm}^2$$

$$t_{ox} = 20 \text{ nm}$$

The experimental characteristics of an ideal n-channel MOSFET biased in the saturation region are shown. If $W/L = 10$ and $t_{ox} = 425$ Å, determine V_T and μ_n.



We find that $V_T \cong 0.2$ V

Now

$$\sqrt{I_D(sat)} = \sqrt{\frac{W\mu_n C_{ox}}{2L}} \cdot (V_{GS} - V_T)$$

where

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{425\times10^{-8}}$$

or

$$C_{ox} = 8.12\times10^{-8}\ \text{F/cm}^2$$

We are given $W/L = 10$. From the graph, $V_{GS} = 3$ V, we have

$$\sqrt{I_D(sat)} \cong 0.033,$$

$$0.033 = \sqrt{\frac{W\mu_n C_{ox}}{2L}} \cdot (3 - 0.2)$$

or

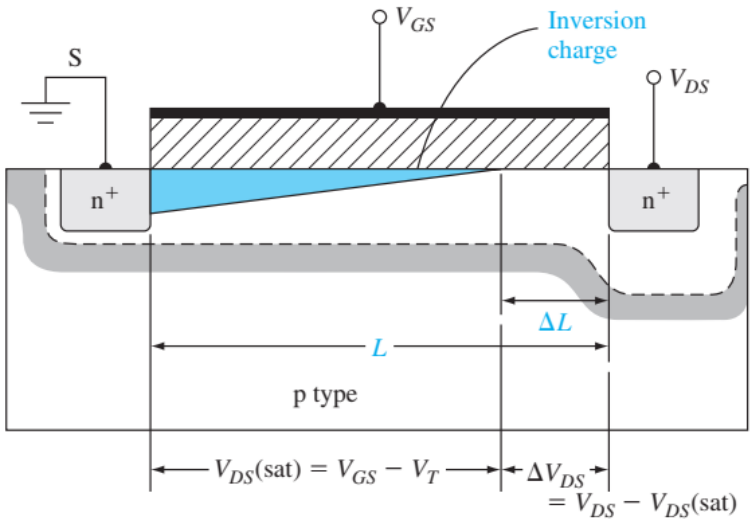
$$\frac{W\mu_n C_{ox}}{2L} = 0.139\times10^{-3}$$

or

$$\frac{1}{2}(10)\mu_n(8.12\times10^{-8}) = 0.139\times10^{-3}$$

which yields

$$\mu_n = 342\ \text{cm}^2/\text{V-s}$$



$$x_p = \sqrt{\frac{2\epsilon_s \phi_{fp}}{eN_a}}$$

$$x_p = \sqrt{\frac{2\epsilon_s}{eN_a}(\phi_{fp} + V_{DS})}$$

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}}\left[\sqrt{\phi_{fp} + V_{DS}(\text{sat}) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(\text{sat})}\right]$$

$$\Delta V_{DS} = V_{DS} - V_{DS}(\text{sat})$$

Since the drain current is inversely proportional to the channel length, we may write

$$I'_D = \left(\frac{L}{L - \Delta L}\right) I_D$$

where I'_D is the actual drain current and I_D is the ideal drain current. Since ΔL is a function of V_{DS}, I'_D is now also a function of V_{DS} even though the transistor is biased in the saturation region.

Objective: Determine the increase in drain current due to short channel modulation.

Consider an n-channel MOSFET with a substrate doping concentration of $N_a = 2 \times 10^{16}$ cm^{-3}, a threshold voltage of $V_T = 0.4$ V, and a channel length of $L = 1$ μm. The device is biased at $V_{GS} = 1$ V and $V_{DS} = 2.5$ V. Determine the ratio of actual drain current compared to the ideal value.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{2 \times 10^{16}}{1.5 \times 10^{10}}\right) = 0.3653 \text{ V}$$

$$V_{DS}(\text{sat}) = V_{GS} - V_T = 1.0 - 0.4 = 0.6 \text{ V}$$

$$\Delta V_{DS} = V_{DS} - V_{DS}(\text{sat}) = 2.5 - 0.6 = 1.9 \text{ V}$$

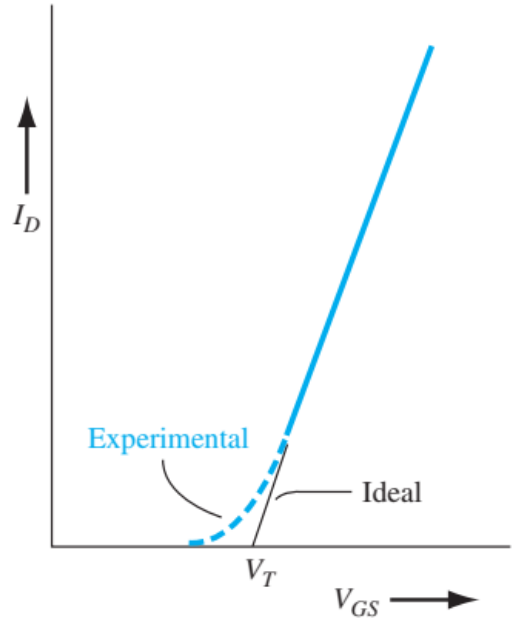
$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}}\left[\sqrt{\phi_{fp} + V_{DS}(\text{sat}) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(\text{sat})}\right]$$

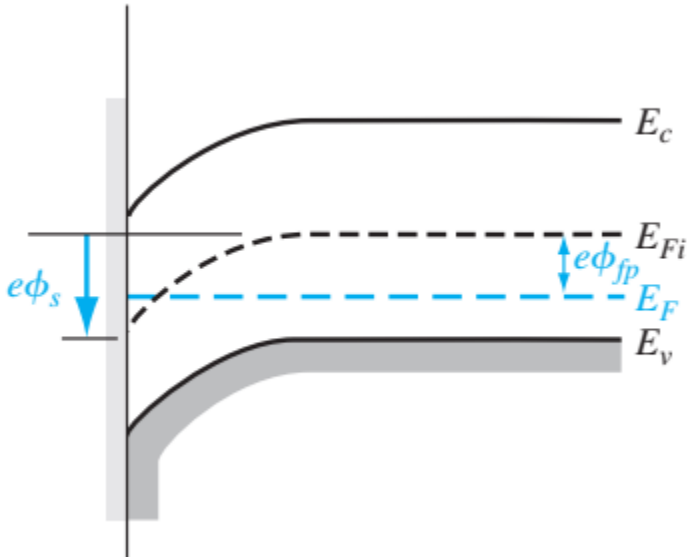
$$= \sqrt{\frac{2(11.7)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(2 \times 10^{16})}}\left[\sqrt{0.3653 + 0.6 + 1.9} - \sqrt{0.3653 + 0.6}\right]$$

$$= 1.807 \times 10^{-5} \text{ cm}$$

$$\Delta L = 0.1807 \ \mu\text{m}$$

$$\frac{I'_D}{I_D} = \frac{L}{L - \Delta L} = \frac{1}{1 - 0.1807} = 1.22$$





condition for $\phi_{fp} < \phi_s < 2\phi_{fp}$ is known as *weak inversion*

$$I_D(\text{sub}) \propto \left[\exp\left(\frac{eV_{GS}}{kT}\right)\right] \cdot \left[1 - \exp\left(\frac{-eV_{DS}}{kT}\right)\right]$$

If V_{DS} is larger than a few (kT/e) volts, then the subthreshold current is independent of V_{DS}.