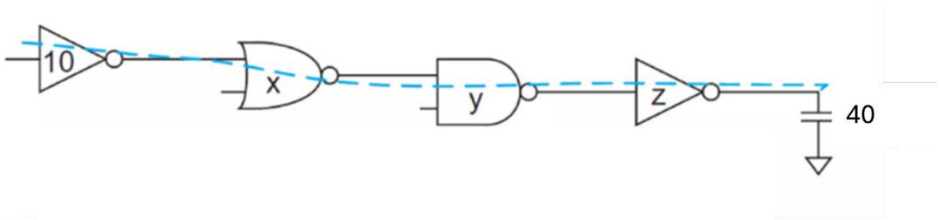
Assignment-4

1. Consider the 3 input CMOS NAND gate and calculate the best- and worst-case Elmore delay at output node.
2. Consider the following circuit, which is driving a large capacitor of 40C. Calculate the size of each stage using a linear delay model.



3. For Q2, after obtaining the correct size calculate the delay.
4. Explain the working of 3-T DRAM and draw its stick diagram
5. Implement 0101 overlapping sequence detector using NMOS PLA and TFF.

$$T_1 = Q_1Q_2'x + Q_1'Q_2x + Q_1Q_2x'$$

$$T_2 = Q_2'x' + Q_2x$$

$$n = Q_1Q_2x$$