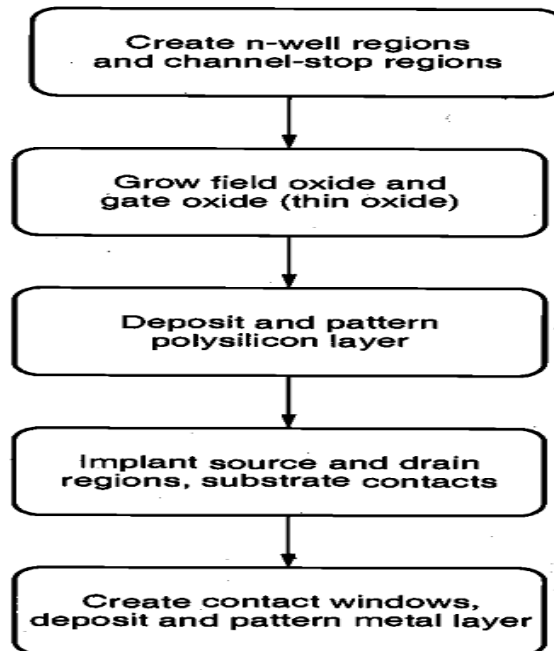


## **UNIT -2**

### **FABRICATION OF MOSFET**

#### **SIMPLIFIED PROCESS SEQUENCE FOR FABRICATION-**

- CMOS fabrication technology requires both NMOS and PMOS transistor to be built on the same chip substrate.
- To accommodate both NMOS & PMOS devices, special regions must be created in which the semiconductor type is opposite to the substrate type. These special regions are called wells or tubs.
- So, a n well is formed in a P substrate and a P well is formed in a n substrate.  
The simplified process sequence for the fabrication of CMOS-
- The process starts with the creation of the n well regions for PMOS and p well regions for NMOS by ion implantation into the substrate.
- Ion implantation is the process of adding impurities to a silicon wafer.
- Then a thick oxide is grown in the regions surrounding the NMOS and PMOS active regions. The thin gate oxide is subsequently grown on the surface through thermal oxidation.
- Again a polysilicon layer is deposited on the surface of the oxide layers and selectively removed to form the gate.
- These steps are followed by the creation of n+ and P+ regions.
- At last metallization is done means creation of metal interconnects.
- Metallization is the process by which the components of IC's are interconnected by aluminum conductor.
- Channel stop implant is used to prevent the formation of any unwanted channels between two neighboring regions. Hence channel stop implants act to electrically isolate neighboring devices built on the same substrate.

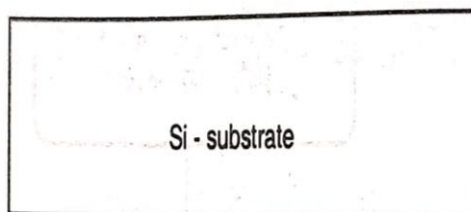


#### **BASIC STEPS OF FABRICATION-**

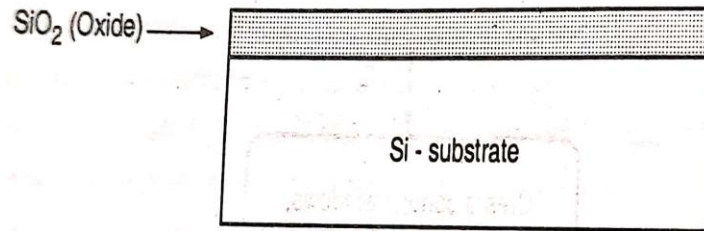
- The fabrication cycle of VLSI chips consists of a sequential set of basic steps which are wafer preparation, oxidation, lithography and etching.
- During fabrication process, the devices are created on the chip. So, IC may be viewed as a set of patterned layers.
- A layer must be patterned before the next layer of material is applied on the chip.
- Patterning uses the process of lithography. The process used to transfer a pattern to a layer on the chip is called lithography.
- The lithography sequence must be repeated for every layer.

Steps:

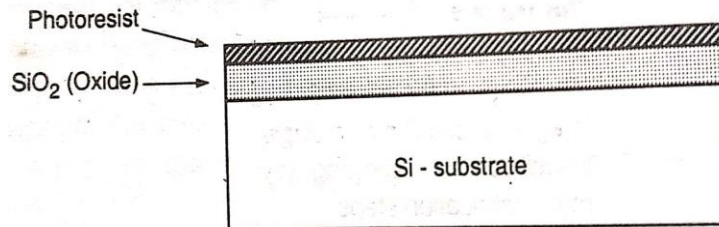
- First we take a Si substrate.



- The sequence starts with the thermal oxidation of the silicon surface. Due to which oxide layer formed of 1mm thickness.



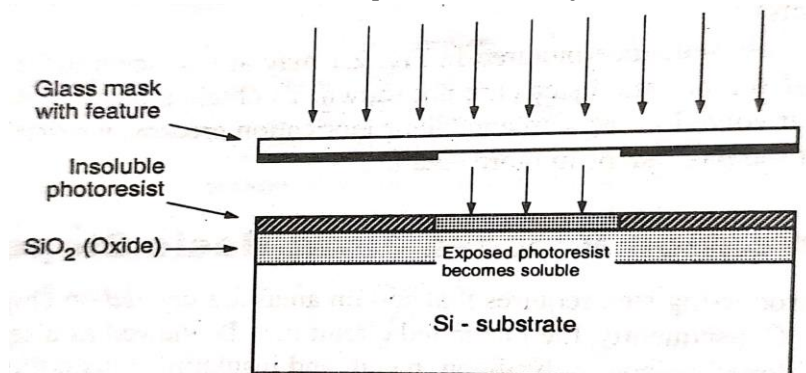
- The entire oxide surface is then covered with a layer of photoresist.



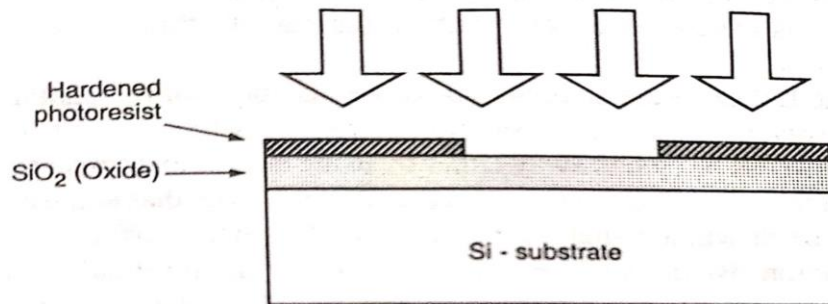
- Photoresist is a light sensitive material. It is of 2 types.

- 1) Positive photoresist
- 2) Negative photoresist

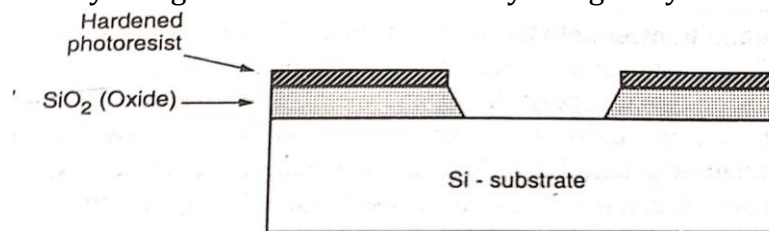
- Positive photoresist is initially insoluble and becomes soluble after exposure to UV light.
- Negative photoresist is initially soluble and becomes insoluble after exposure to UV light.
- Here we use positive photoresist. So, we have to cover some of the areas on the surface and selectively expose the photoresist.
- The areas becomes soluble, which are exposed to UV rays.



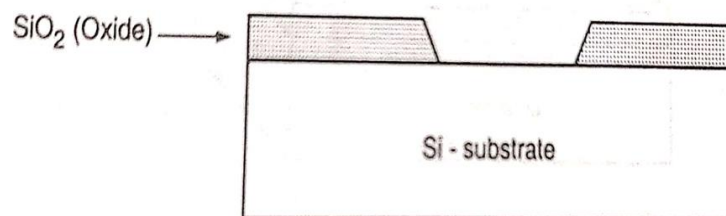
- Then the soluble areas can be etched away. Etching is the process of material being removed from the surface.



- The two major types of etching are wet etching and dry etching.
- The etching process that involves using liquid chemicals to take off the substrate material is called wet etching. Ex- Hydrofluoric Acid, Nitric acid, Acetic acid
- The dry etching is known as plasma etching. Etchant gases are used to remove the substrate material. Ex. Tetra fluoromethane, sulfur hexafluoride, Nitrogen trifluoride, Chlorine gas, Fluorine gas
- **Negative photoresists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photoresists. Therefore, negative photoresists are used less commonly.**
- The silicon dioxide regions which are not covered by hardened photoresist can be etched away either by using a chemical solvent or by using a dry etching process.

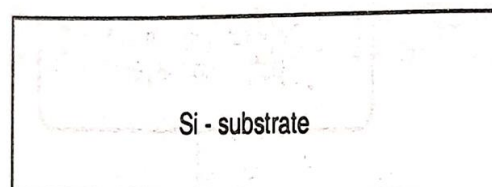


- After that the unexposed portions of the photoresist can be removed by a chemical leaving the patterned SiO<sub>2</sub>.

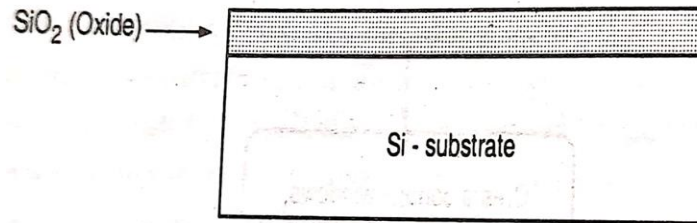


### FABRICATION PROCESS OF NMOS TRANSISTOR-

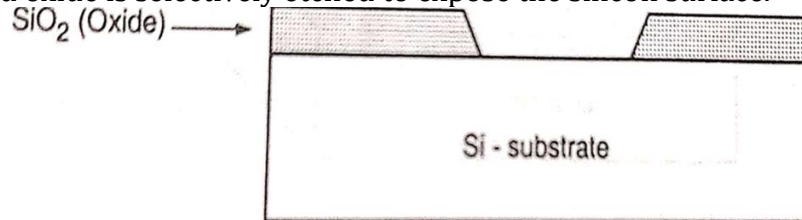
- First we take a p type silicon substrate.



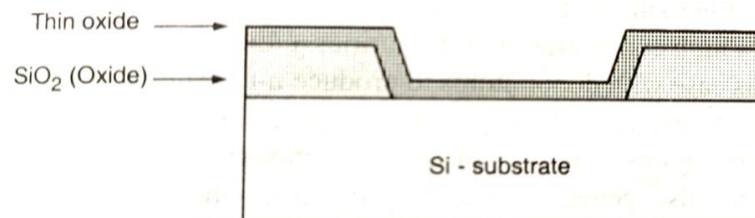
- The process starts with the oxidation of the silicon substrate



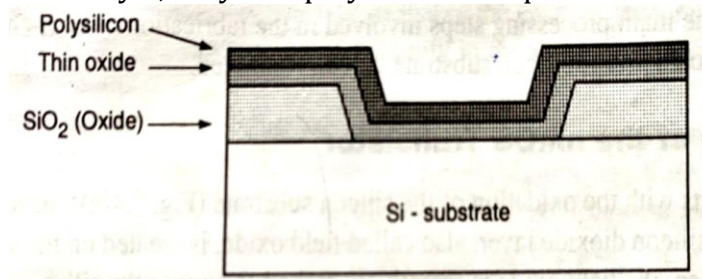
- Then the field oxide is selectively etched to expose the silicon surface.



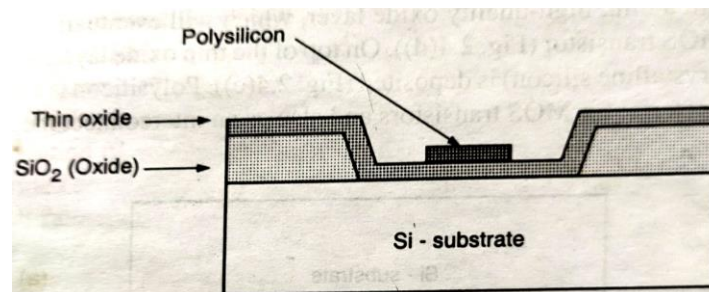
- Again the surface is covered with a thin oxide layer.



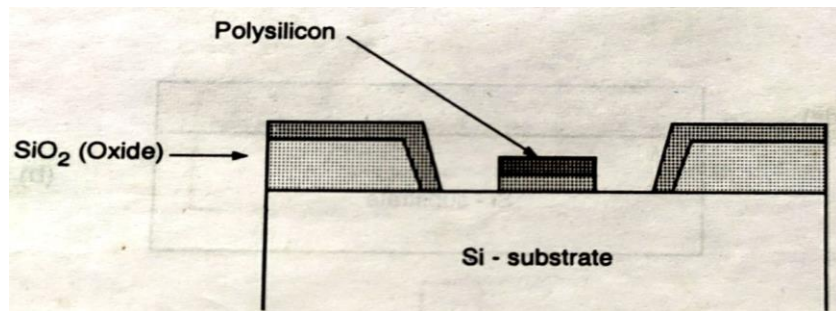
- On top of the thin oxide layer, a layer of polysilicon is deposited.



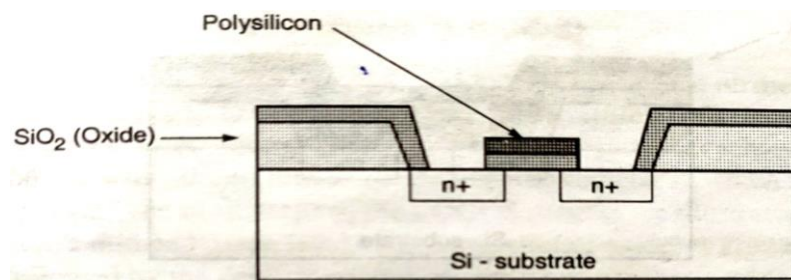
- After deposition, the polysilicon layer is patterned and etched to form gate of the MOSFET.



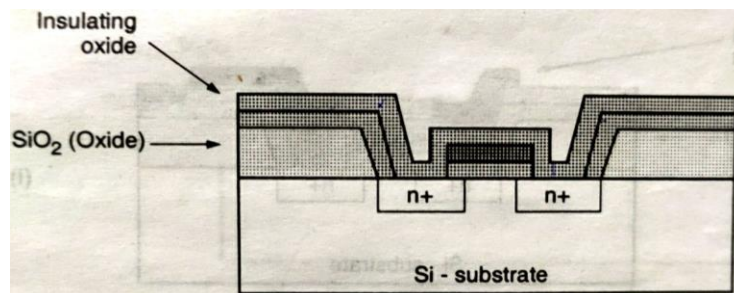
- The thin gate oxide not covered by polysilicon is also etched away, which exposes the silicon surface on which the source and drain junctions are to be formed.



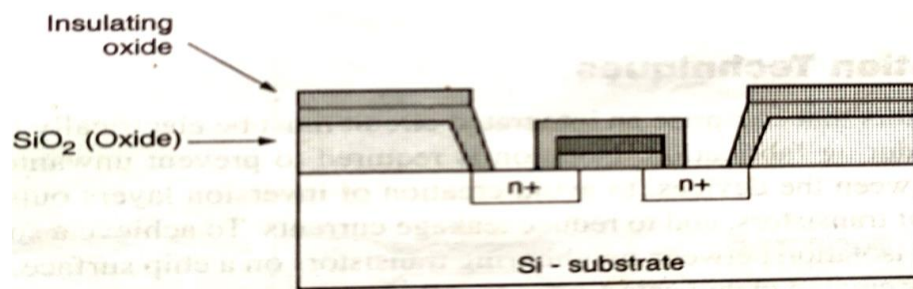
- The entire silicon surface is then doped with a high concentration of impurities, ultimately creating two n type regions.



- Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide.

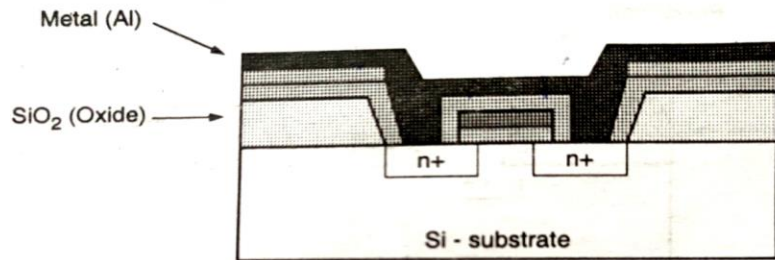


- The insulating oxide layer is then patterned in order to provide contact windows for the drain and source.

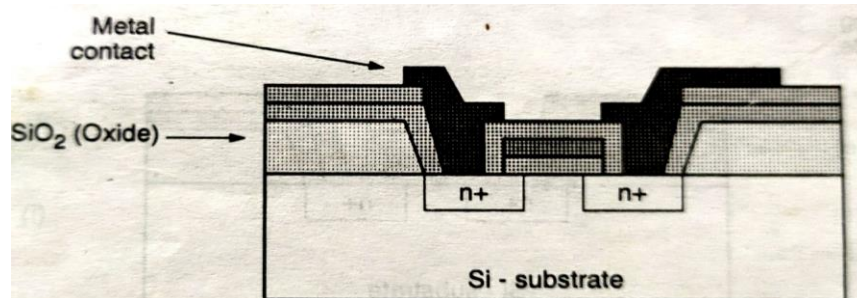


- Then the surface is covered with evaporated aluminum which will form the interconnects.





- Finally the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface.

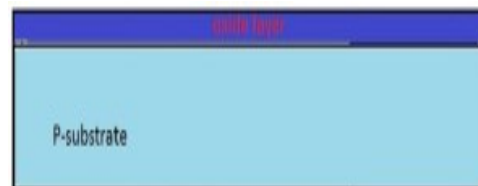


#### CMOS N-WELL FABRICATION PROCESS FLOW-

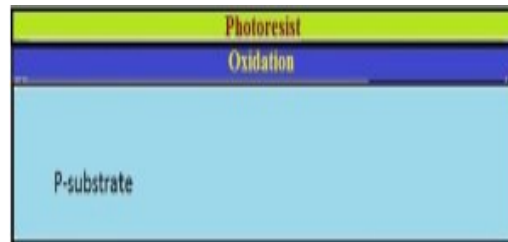
- For less power dissipation requirement CMOS technology is used for implementing transistor.
- The n-well technology and p-well technologies are used for fabrication of CMOS.  
Now let's discuss the steps of CMOS n-well fabrication.
- First we select a substrate as a base for fabrication. So, here we select a p-type substrate.



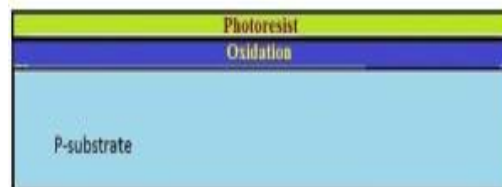
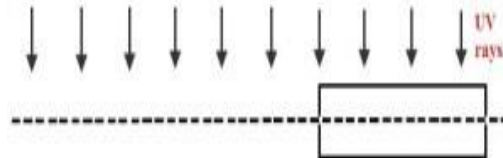
- Silicon dioxide layer formed by oxidation process on the Si substrate.



- For selective etching the SiO<sub>2</sub> layer is subjected to photolithography process. In this process, the wafer is coated with a uniform film of a photosensitive material known as photoresist.



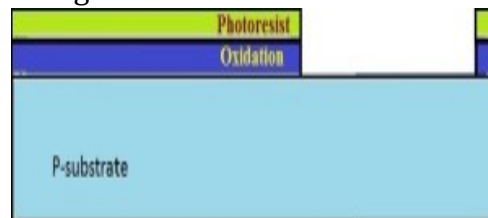
- The photoresist layer selectively exposed to UV rays.



- The soluble photoresist is removed.



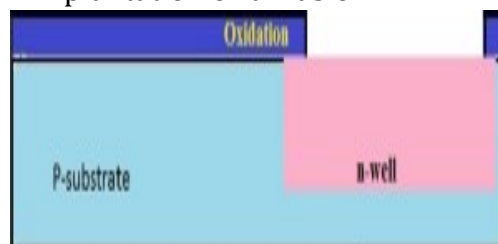
- The exposed silicon dioxide region is removed.



- The remaining photoresist layer is removed.

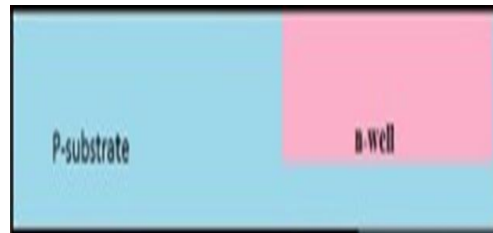


- N well is formed using ion implantation or diffusion.





- The remaining silicon dioxide is removed.

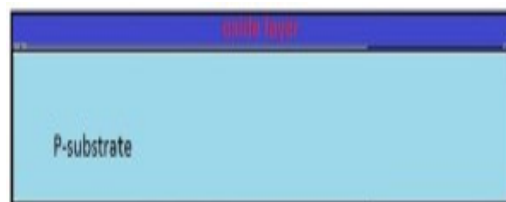


## CMOS FABRICATION PROCESS BY N-WELL ON P SUBSTRATE-

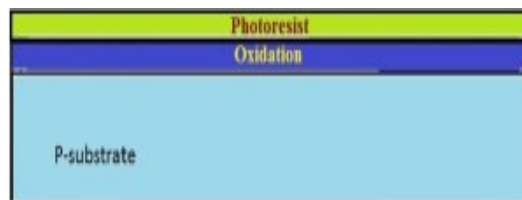
- For N well process first we take a P type substrate.



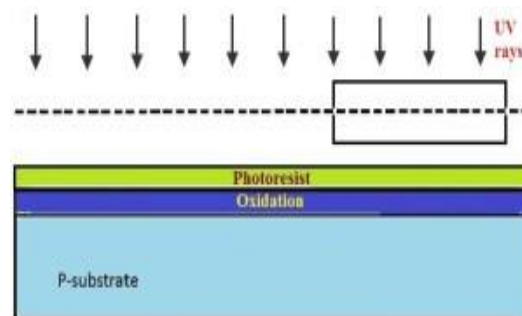
- Substrate is oxidized in high temperature.



- Apply photoresist on the surface of the silicon dioxide.



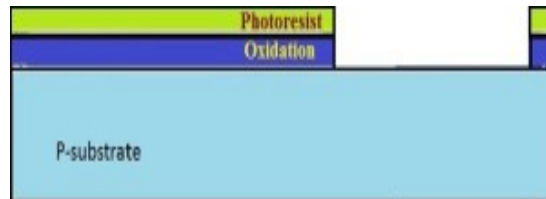
- Selectively expose the photoresist to the UV rays.



- The soluble photoresist is removed.



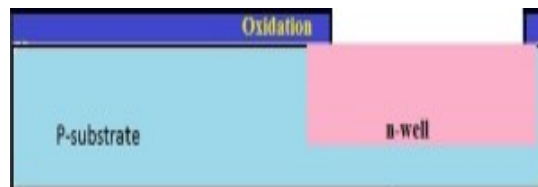
- The exposed Silicon dioxide region is removed.



- The entire photoresist layer is stripped off.



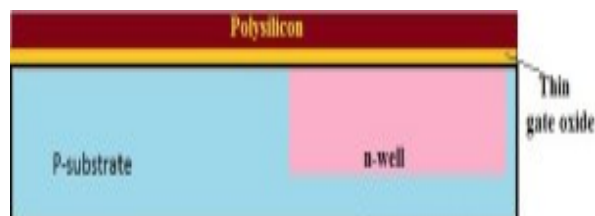
- By using ion implantation or diffusion process N-well is formed.



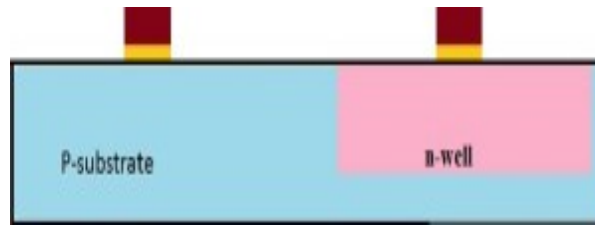
- The remaining silicon dioxide is removed.



- A thin layer of gate oxide is deposited on the surface of the substrate. Then apply the polysilicon on the surface.



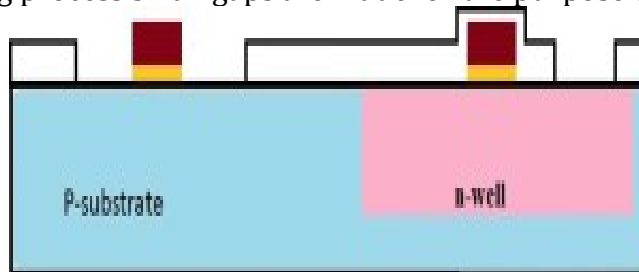
- Gate oxide and polysilicon layers are selectively removed.



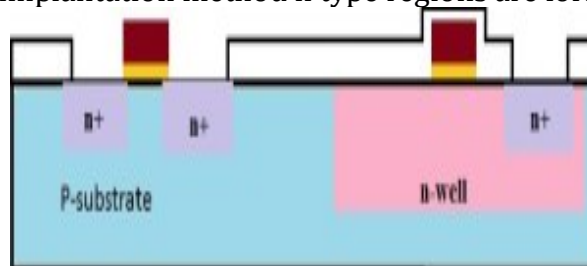
- An oxide layer is formed on the surface.



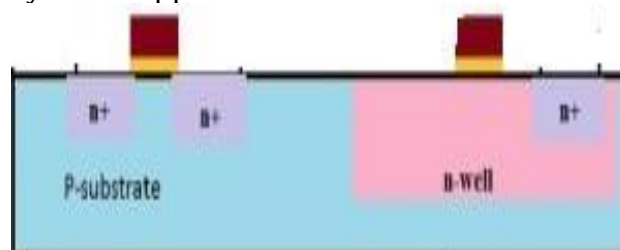
- By using the masking process small gaps are made for the purpose of N-diffusion.



- Using diffusion or ion implantation method n type regions are formed.



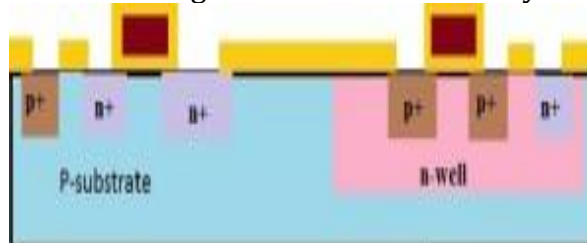
- The remaining oxide layer is stripped off.



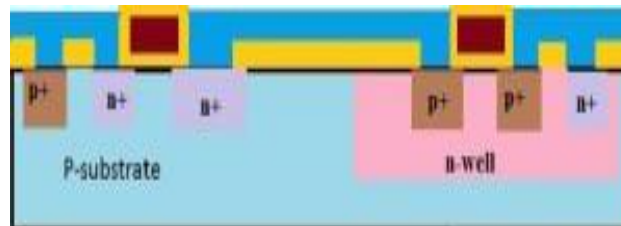
- Similar to the above process, the p type regions are formed.



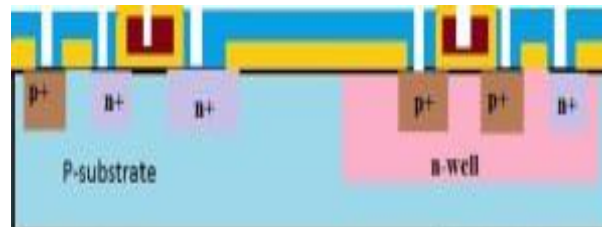
- A thick-field oxide is formed in all regions and then selectively removed.



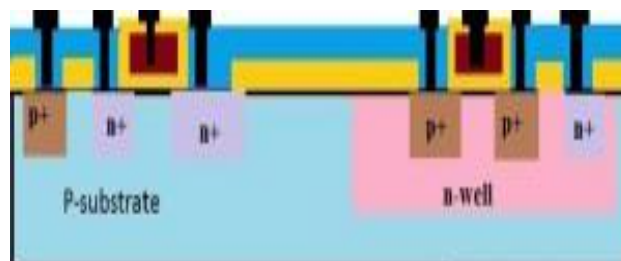
- Then the surface is covered with evaporated aluminum.



- The excess metal is removed from the surface.

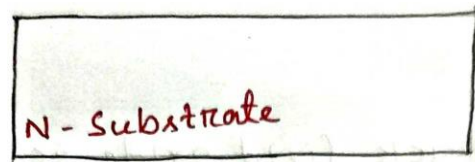


- The terminals of the PMOS and NMOS are made from respective gaps.

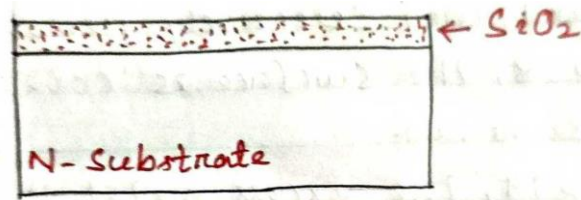


## CMOS FABRICATION PROCESS BY P-WELL ON N SUBSTRATE-

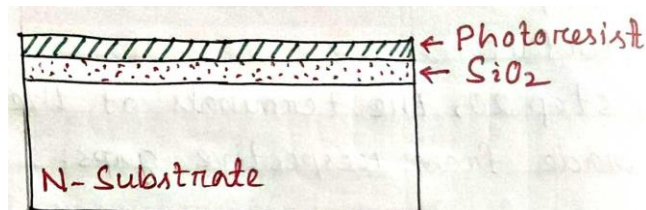
- For P well process first we take an N type substrate.



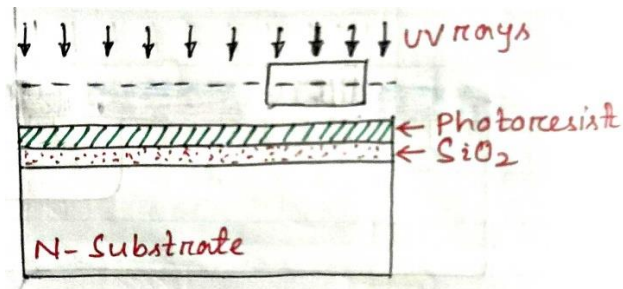
- Substrate is oxidized in high temperature.



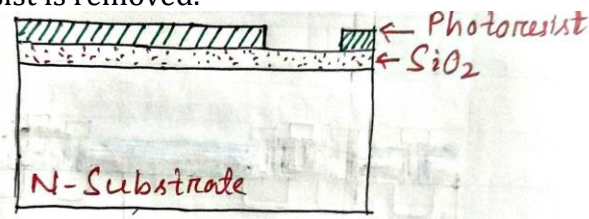
- Apply photoresist on the surface of the silicon dioxide.



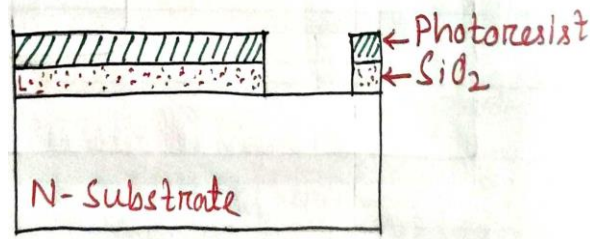
- Selectively expose the photoresist to the UV rays.



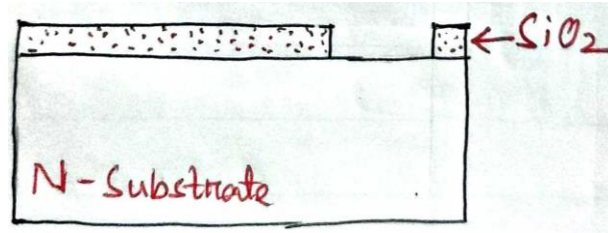
- The soluble photoresist is removed.



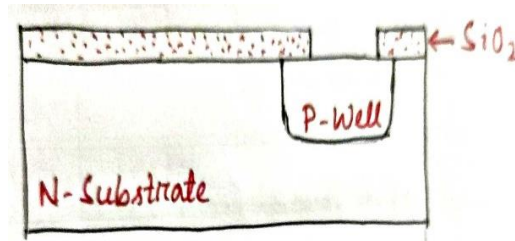
- The exposed Silicon dioxide region is removed.



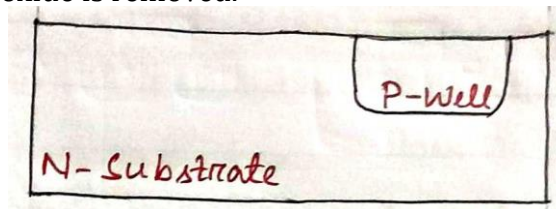
- The entire photoresist layer is stripped off.



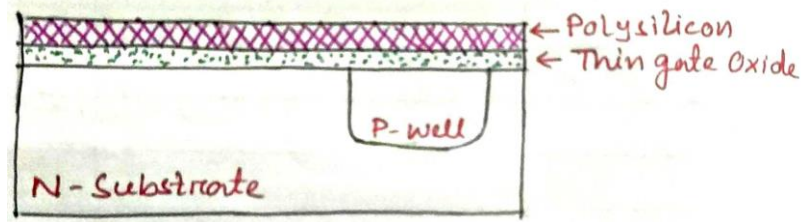
- By using ion implantation or diffusion process P-well is formed.



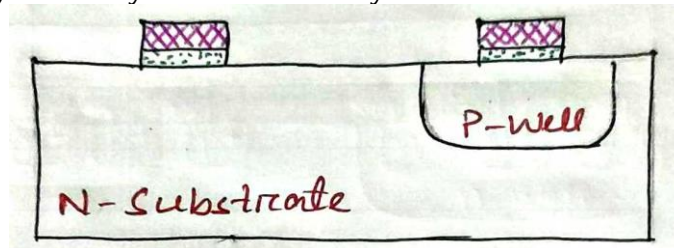
- The remaining silicon dioxide is removed.



- A thin layer of gate oxide is deposited on the surface of the substrate. Then apply the polysilicon on the surface.

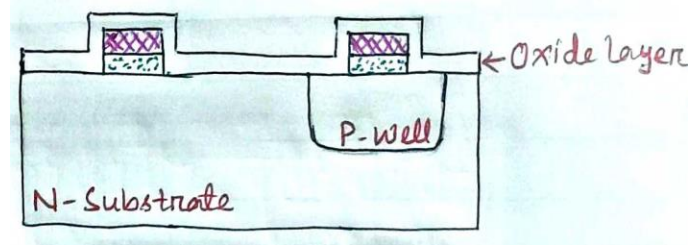


- Gate oxide and polysilicon layers are selectively removed.

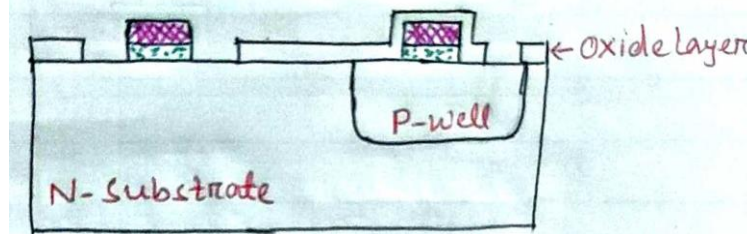


- An oxide layer is formed on the surface.

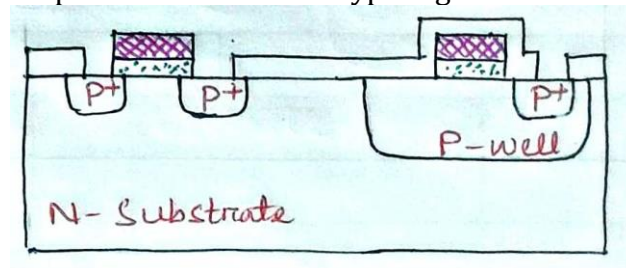




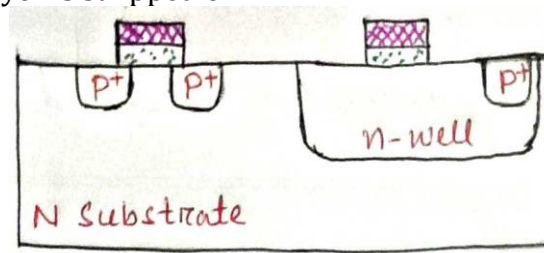
- By using the masking process small gaps are made for the purpose of P-diffusion.



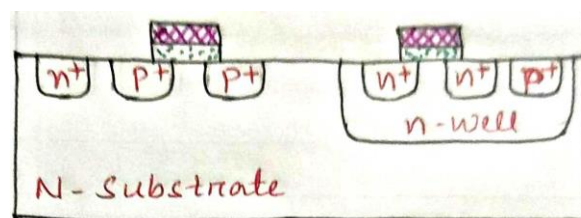
- Using diffusion or ion implantation method P type regions are formed.



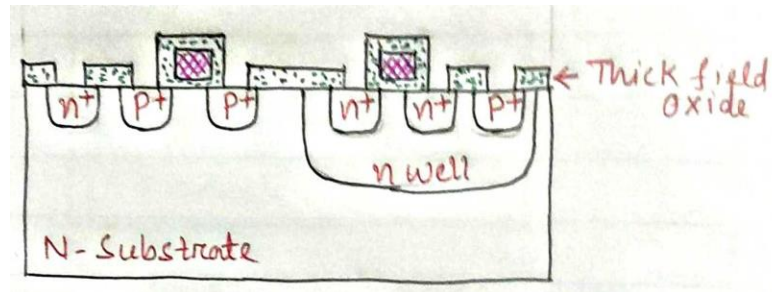
- The remaining oxide layer is stripped off.



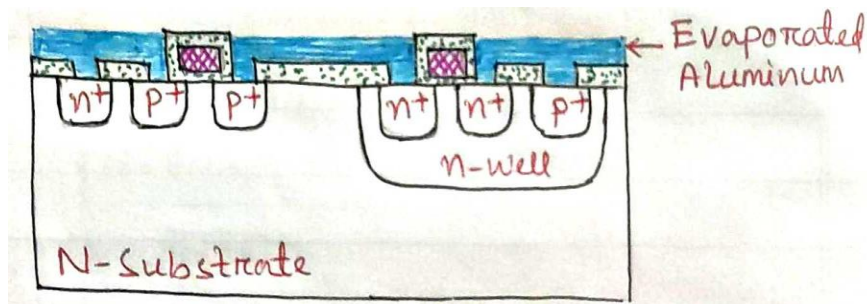
- Similar to the above process, the n type regions are formed.



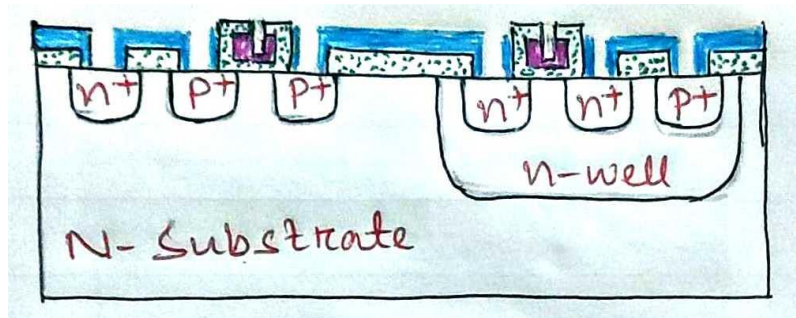
- A thick-field oxide is formed in all regions and then selectively removed.



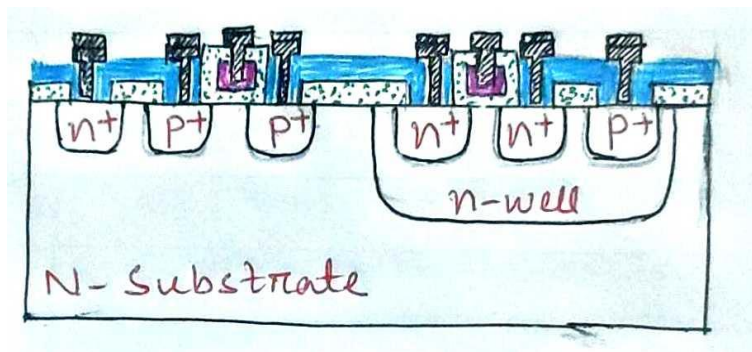
- Then the surface is covered with evaporated aluminum.



- The excess metal is removed from the surface.



- The terminals of the PMOS and NMOS are made from respective gaps.



## LAYOUT DESIGN RULES-

The physical mask layout of any circuit to be manufactured using a particular process must confirm to set of geometric constraints or rules, which are generally called layout design rules.

The design rules are described in two ways-

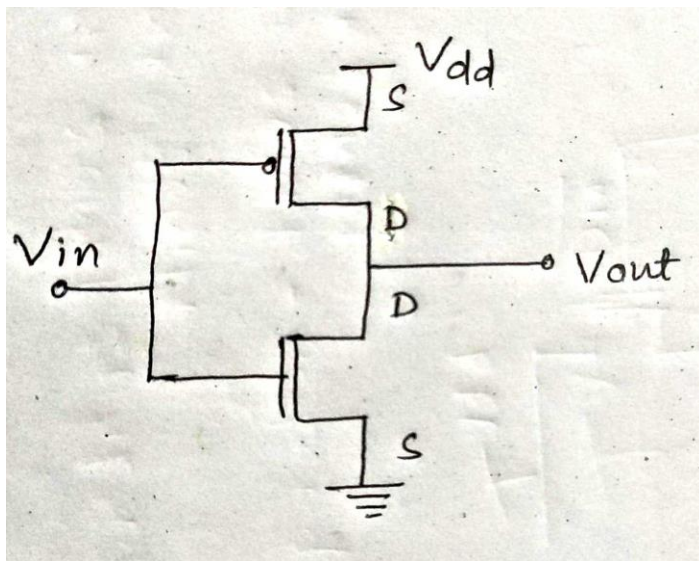
1) Micron rules-

Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

2) Lambda rules-

Lambda rules specify the layout constraints in terms of a single parameter ( $\lambda$ ) and thus allow linear, proportional scaling of all geometrical constraints.

### STICK DIAGRAM OF CMOS INVERTER-



### Stick Diagram-

