Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
MARCH 2021
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 2152)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the stack based machine organization. Using a minimum number instructions, write a program that is equivalent to Z:= A*A+E*A+A*B+E*B for the stack machine. Show the stack operation while instruction execution.

1B. Explain base and index register addressing with the help of an example.

1C. The CPU of a computer contains 8 registers R0 through R7. The register R7 is a read only register and it always contains a zero. X is a memory location. The instruction set of this machine includes the following instructions:
ADD Rj, Ri, X ; (Rj)<- (Ri)+X where i=0,1,2,….7 but j=0,1,2,4,5 or 6.
ADD X, Ri, Rj ; (X)<- (Ri)+(Rj) where i,j=0,1,2,…..6,7
Write a program segment that will add the content of memory locations 2400 and 2500 and save the sum in memory location 2600.

(4+3+3)

2A. What is the process of Opcode Encoding? Explain the basic principle of block code technique. Using the expanding opcode techniques, discuss the possibility to encode all of the following instructions. Justify your answer.
14 double address instructions, 127 single address instructions, 60 zero address instructions

2B. Add 0.5 and 0.4375 using 32-bit IEEE floating point representation and write the result in 32-bit IEEE format.

2C. Perform the multiplication on $-20_{(10)}$ and $12_{(10)}$ using a) Booth's algorithm b) Modified Booth algorithm.

(4+3+3)

3A. Design a 4 bit, 8 function arithmetic unit that will meet the specifications given in **Table 3A.**

3B. What is DMA system and how it functions? Explain in detail with necessary control signals. Discuss the types of DMA.

3C. A computer follows a set associative cache memory organization with size of main memory, cache memory is 16MB, 64KB respectively. Cache memory maintains 32 blocks as a set where each block size is 16bytes. Show the format of main memory address.

(4+3+3)

4A. Write the microprogram for 4X 4 Booth's multiplier to perform signed data multiplication. With the help of program, draw the microprogrammed control unit with condition select MUX design and binary encoding control instructions for the same. The declarations are: A[4]; M[4]; Q[5]; L[3]; Inbus[4]; Outbus[4].

4B. Design a carry save adder for 6 operand summation and calculate the total delay involved. Compare the delay if Wallace tree structure is used for the same. Assume CSA add time is half of the CPA add time.

(5+5)

5A. Explain the following: i. Port structure ii. Pipelining

5B. With help of a diagram explain the principle of working of MAC unit in Digital signal processor. Write the significance of guard bits.

5C. Explain the bit reversed and circular addressing modes used in digital signal processor with an example.

(4+3+3)

Table. 3A

S_2	S_1	S_0	F
0	0	0	2A
0	0	1	A+B'
0	1	0	A+B
0	1	1	A-1
1	0	0	2A+1
1	0	1	A+B'+1
1	1	0	A+B+1
1	1	1	A