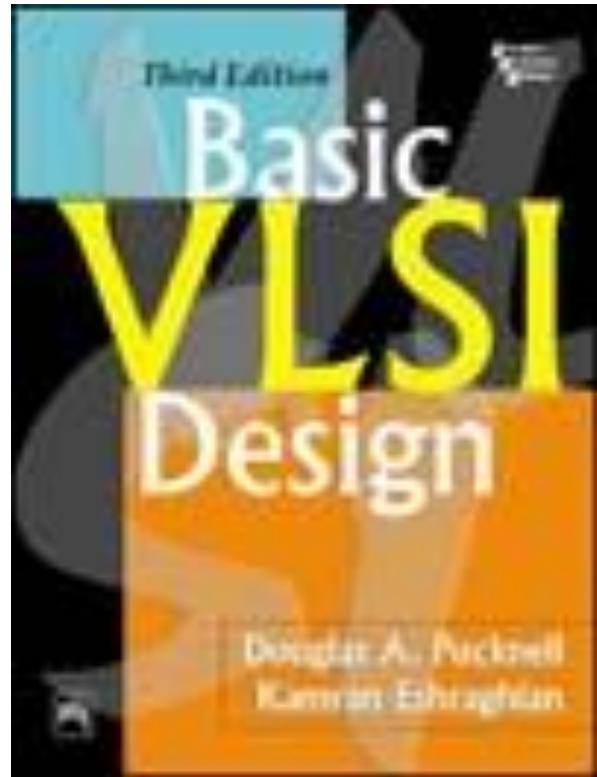


# VLSI Design

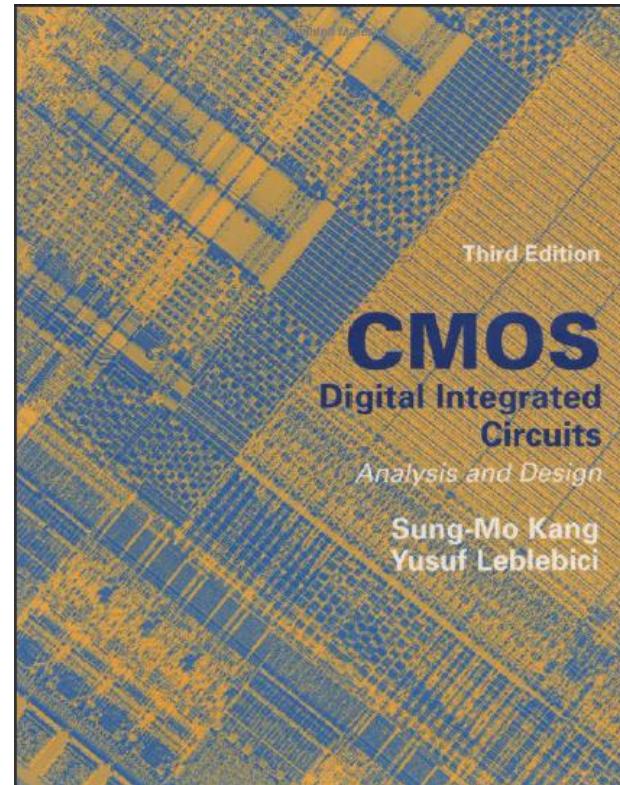
# Course Outcome

- Analyze NMOS & CMOS inverter circuits
- Analyze and Design combinational and sequential circuits using MOS devices.
- Describe the process of fabrication of NMOS and CMOS devices
- Draw the stick diagrams and layouts for different MOS circuits.
- Describe various issues involved in subsystem design and estimate performance parameters.
- Analyze the impact of interconnects on the circuit performance

# Reference Books

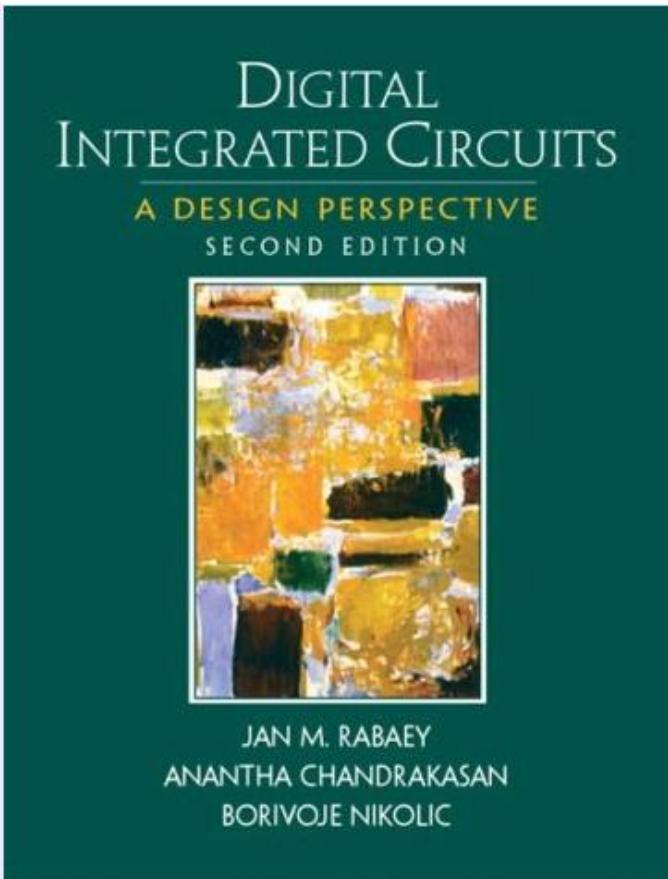


**"Basic VLSI Design", 3<sup>rd</sup> Ed., PHI**  
**By: PUCKNELL DOUGLAS A.ESHRAGHIAN,**  
**KAMRAN**

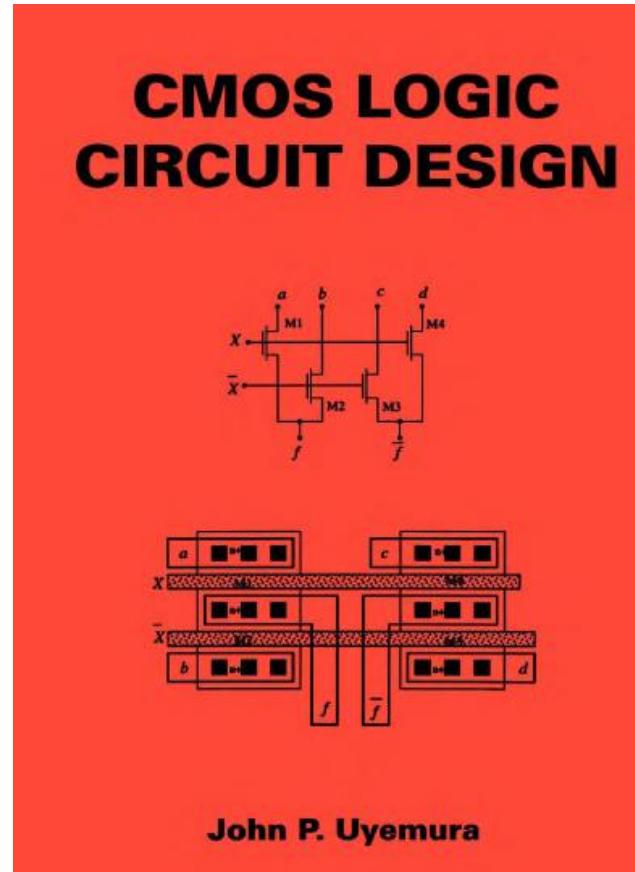


**"CMOS DIGITAL INTEGRATED CIRCUITS:Analysis and Design"**  
**3<sup>rd</sup> Ed. McGraw-Hill.**  
**By:SUNG-MO (STEVE) KANG**

# Reference Books

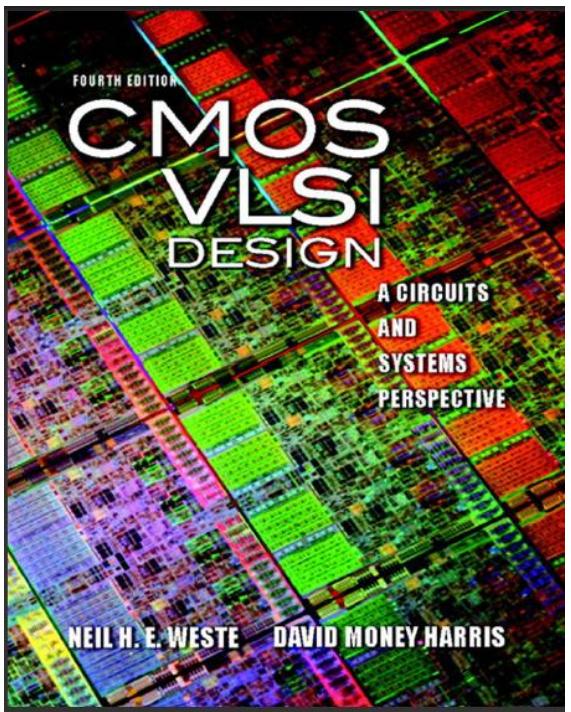


**Digital Integrated Circuits – A Design Perspective”,  
2nd ed. by J. Rabaey, A. Chandrakasan, B. Nikolic**



**“CMOS LOGIC CIRCUIT DESIGN”  
KLUWER ACADEMIC PUBLISHERS  
By: John P. Uyemura**

# Reference Books



**"CMOS VLSI Design:A Circuits and Systems Perspective"** 4<sup>th</sup> ed. Addison-Wesley  
**By: Neil H. E. Weste, David Money Harris**

# Introduction

## What is expected ?

**Complexity**   $\infty$

Intel 4004 Processor: 2300 Transistor  $\rightarrow$  10 $\mu$ m Technology

Intel i7 Processor : 3,200,000,000 Transistors  $\rightarrow$  14nm Technology

**Power**  Min

Intel 4004 Processor: 1 W

Intel i7 Processor : 47W

**Delay**  Min

Intel 4004 Processor: 740KHz

Intel i7 Processor : 3.6 GHz

**Cost**  Min

Intel 4004 Processor: \$60

Intel i7 Processor : \$366

**Size**  Min

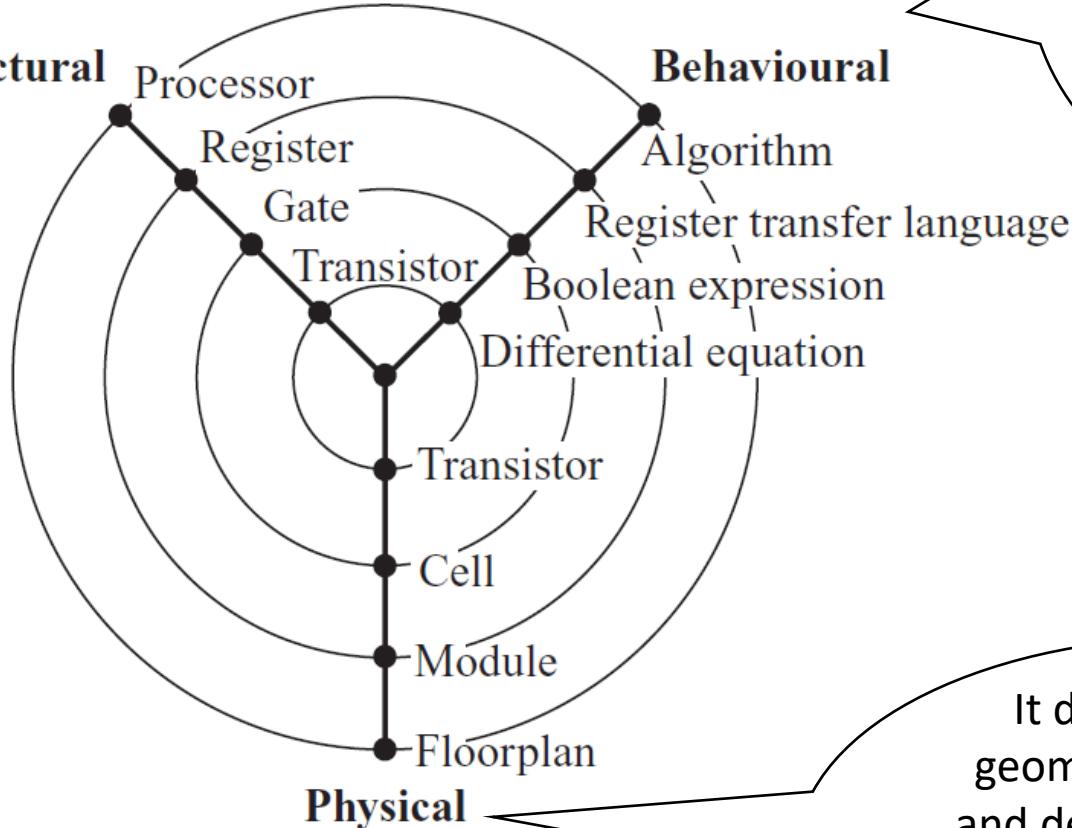
Intel 4004 Processor: 12 mm<sup>2</sup>

Intel i7 Processor : 246 mm<sup>2</sup>

# Introduction

Circuit is described by its components and their interconnections

**Structural**



Circuit is described fully by its behaviour without describing its physical implementation or structure

It deals with actual geometry of the circuit and describes the shape, size, and locations of its components.

# VLSI Design Styles

- Field programmable gate array (FPGA) design
- Gate array design
- Standard cell-based design
- Full-custom design
- Semi-custom design
- Programmable logic device (PLD)

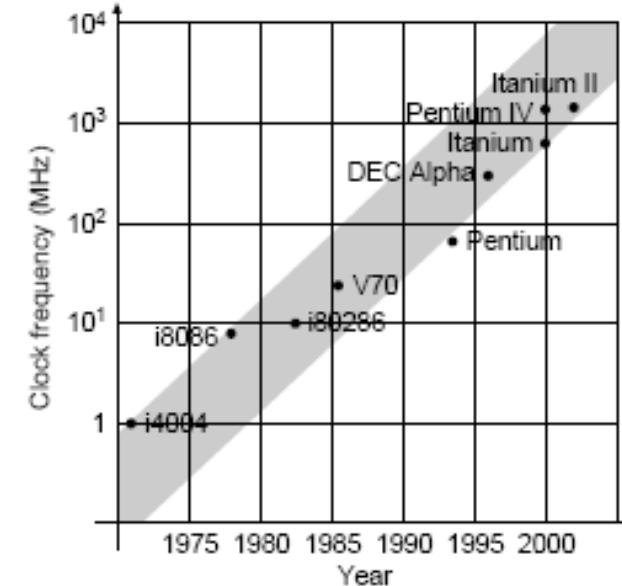
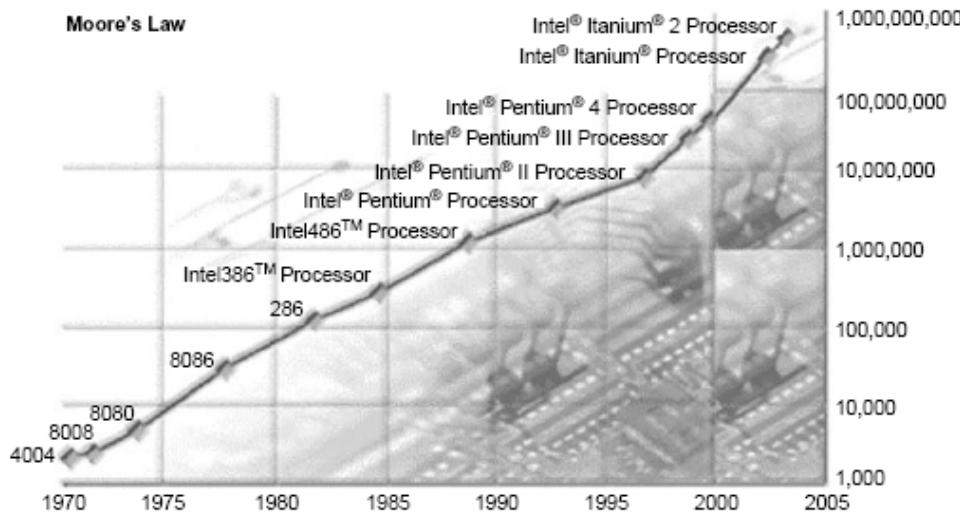
# TECHNOLOGY GENERATIONS

Integration level	Year	No. of transistors	DRAM Integration
SSI	1950s	Less than $10^2$	
MSI	1960s	$10^2 \approx 10^3$	
LSI	1970s	$10^3 \approx 10^5$	4K, 16K, 64K
VLSI	1980s	$10^5 \approx 10^7$	256K, 1M, 4M
ULSI	1990s	$10^7 \approx 10^9$	16M, 64M, 256M
SLSI	2000s	Over $10^9$	1G, 4G and Above

$$\text{Regularity} = \frac{\text{Total number of transistors on the chip}}{\text{Number of transistor circuits that must be designed in detail}}$$

# Moore's law

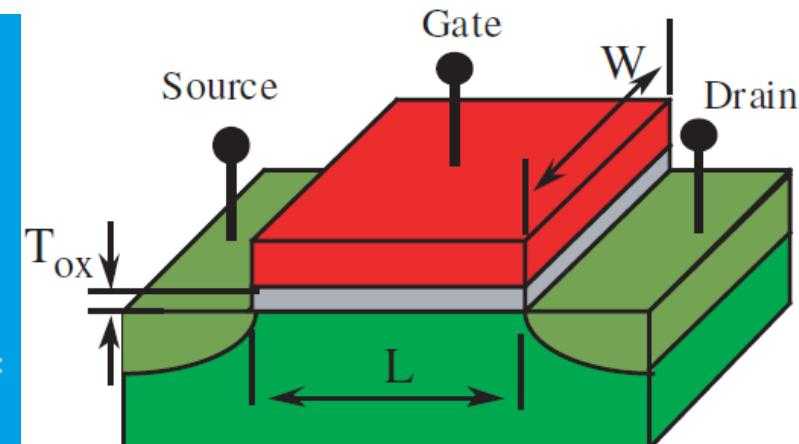
The evolution of MOS technology has followed the famous Moore's law that predicts a steady decrease in gate length. As predicted by Gordon Moore in the 1960s, integrated circuit (IC) densities have been doubling approximately every 18 months, and this doubling in size has been accompanied by a similar exponential increase in circuit speed (or more precisely, clock frequency).



On-chip transistor count increase for the Intel processors (Source: Intel).

# Moore's Law and our expectation

<b>1</b> <b>1971</b> <b>Intel® 4004 processor</b> Initial clock speed: 108KHz Transistors: 2,300 Manufacturing technology: 10 micron	<b>2</b> <b>1972</b> <b>Intel® 8008 processor</b> Initial clock speed: 800KHz Transistors: 3,500 Manufacturing technology: 10 micron	<b>3</b> <b>1974</b> <b>Intel® 8080 processor</b> Initial clock speed: 2MHz Transistors: 4,500 Manufacturing technology: 6 micron	<b>4</b> <b>1978</b> <b>Intel® 8086 processor</b> Initial clock speed: 5MHz Transistors: 29,000 Manufacturing technology: 3 micron	<b>5</b> <b>1982</b> <b>Intel® 286™ processor</b> Initial clock speed: 6MHz Transistors: 134,000 Manufacturing technology: 1.5 micron
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Assume initial  $L=1, W=1$  and  $T_{ox}=1$

$$W=0.7, L=0.7, T_{ox}=0.7$$

=> Lateral and vertical dimensions reduce 30 %

$$\text{Area Cap} = C = \frac{0.7 \times 0.7}{0.7} = 0.7$$

- **Area reduced by 50%**
- **Capacitance reduced by 30%**

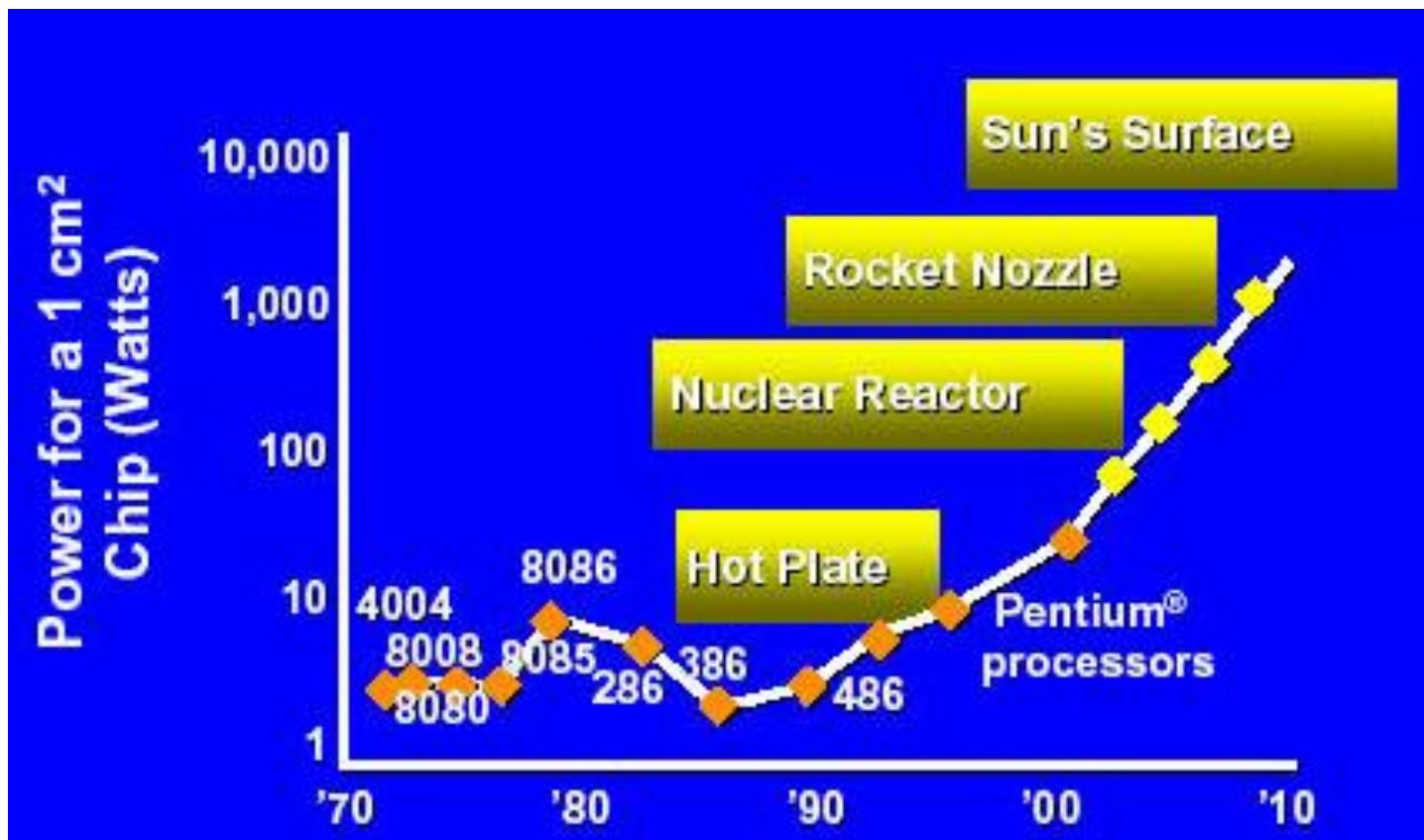
Assume initial  $V_{dd}=1, V_t=1$  and  $T_{ox}=1$

$$V_{dd}=0.7, V_t=0.7, T_{ox}=0.7,$$

$$T = \frac{C \times V_{dd}}{I} = 0.7, \text{ Power} = CV^2f = \frac{0.7 \times 0.7^2}{0.7} = 0.7^2$$

=> **Delay reduces by 30 % and Power reduces by 50 %**

# Power Extrapolation



Melting point of Silicon is 1,414 °C

# VLSI : Very Large Scale Integration

- Integration: Integrated Circuits
  - multiple devices on one substrate
- How large is Very Large?
  - SSI (small scale integration)
    - 7400 series, 10-100 transistors
  - MSI (medium scale)
    - 74000 series 100-1000
  - LSI 1,000-10,000 transistors
  - VLSI > 10,000 transistors
  - ULSI (some disagreement)

# WHY VLSI?

## Integration Improves the Design

- Lower parasitics, higher clocking speed
- Lower power
- Physically small

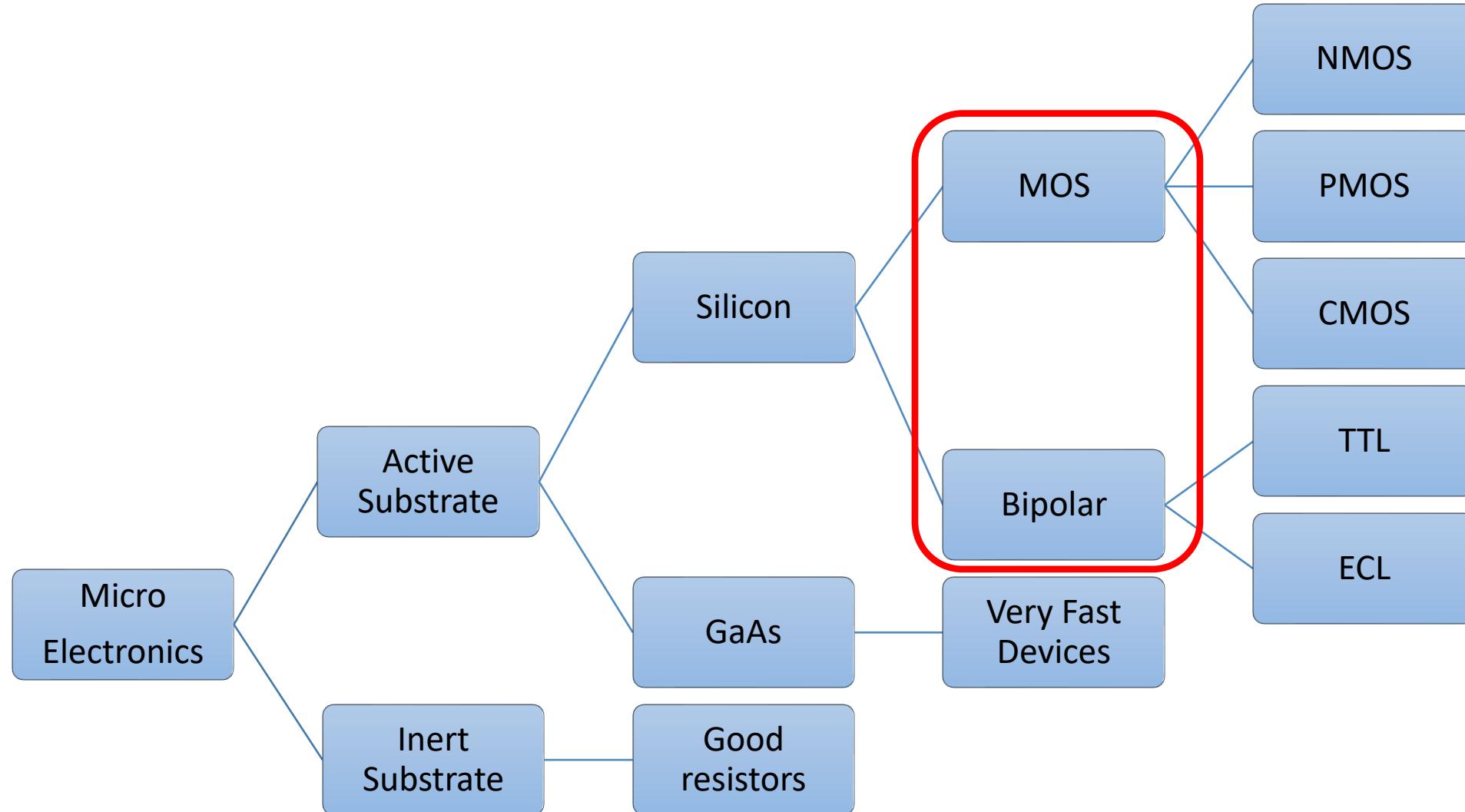
## Integration Reduces Manufacturing Costs

- (almost) no manual assembly
- About \$1-5billion/fab
- Typical Fab  $\approx$ 1 city block, a few hundred people
- Packaging is largest cost
- Testing is second largest cost
- For low volume ICs, Design Cost may swamp all manufacturing cost

# What is “CMOS VLSI”?

- MOS = Metal Oxide Semiconductor (This used to mean a Metal gate over Oxide insulation)
- Now we use polycrystalline silicon which is deposited on the surface of the chip as a gate. We call this “poly” or just “red stuff” to distinguish it from the body of the chip, the substrate, which is a single crystal of silicon.
- We do use metal (aluminum) for interconnection wires on the surface of the chip.

# Microelectronics Technology

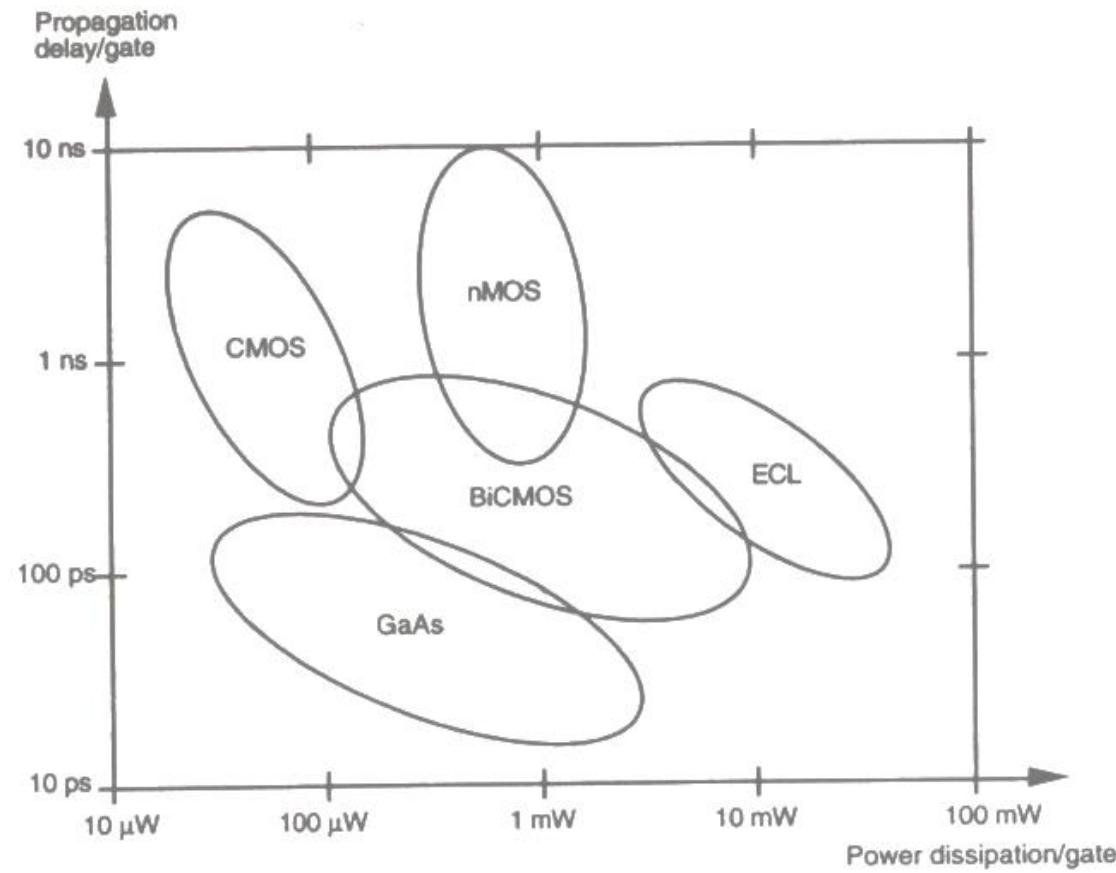


# MOS Vs. BJT

Factors	CMOS	Bipolar
Static Power Dissipation	Low	High
Input Impedance	High	Low
Noise Margin	High	Low
Packing Density	High	Low
Fan-out	Low	High
Direction	Bidirectional	Unidirectional

**CMOS is superior!**

# Power Dissipation Vs. Delay



**CMOS offers low powers dissipation with large delay**

# VLSI Design

- The real issue in VLSI is about designing systems on chips.
- The designs are complex, and we need to use structured design techniques and sophisticated design tools to manage the complexity of the design.
- We also accept the fact that any technology we learn the details of will be out of date soon.
- We are trying to develop and use techniques that will transcend the technology, but still respect it.
- The real issue in VLSI is about designing systems on chips.

# Design Styles

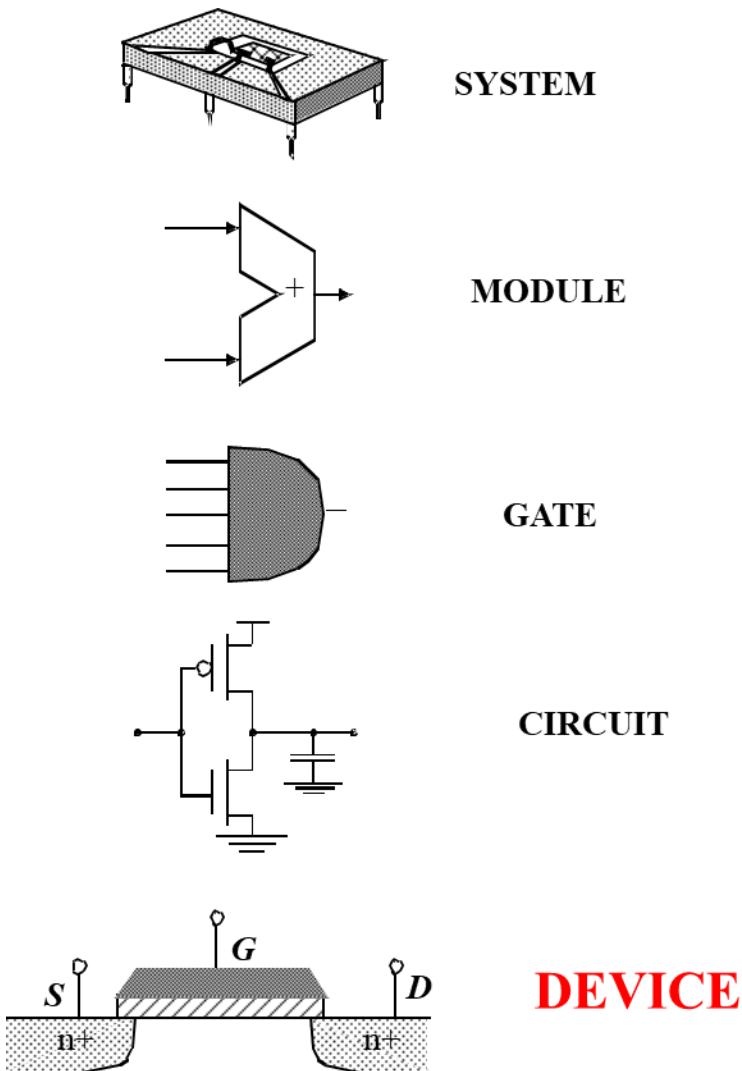
- Full custom
- Standard cell
- Gate-array
- Macro-cell
- “FPGA”
- Combinations

# Comparison

	FPGA	Gate array	Standard cell	Full custom	Macro cell
<b>Density</b>	Low	Medium	Medium	High	High
<b>Flexibility</b>	Low (high)	Low	Medium	High	Medium
<b>Analog</b>	No	No	No	Yes	Yes
<b>Performance</b>	Low	Medium	High	Very high	Very high
<b>Design time</b>	Low	Medium	Medium	High	Medium
<b>Design costs</b>	Low	Medium	Medium	High	High
<b>Tools</b>	Simple	Complex	Complex	Very complex	Complex
<b>Volume</b>	Low	Medium	High	High	High
<b>Device cost</b>	High	Medium	Low	Low	Low

# Levels of Design

- Specifications
  - IO, Function, Costs
- Architectural Description
  - VHDL, Verilog, Behavioral, Large Blocks
- Logic Design
  - Gates plus Registers
- Circuit Design
  - Transistors sized for power and speed
  - Discrete Logic, Technology Mapping
- Layout
  - Size, Interconnect, Parasitics



# Design Methodology

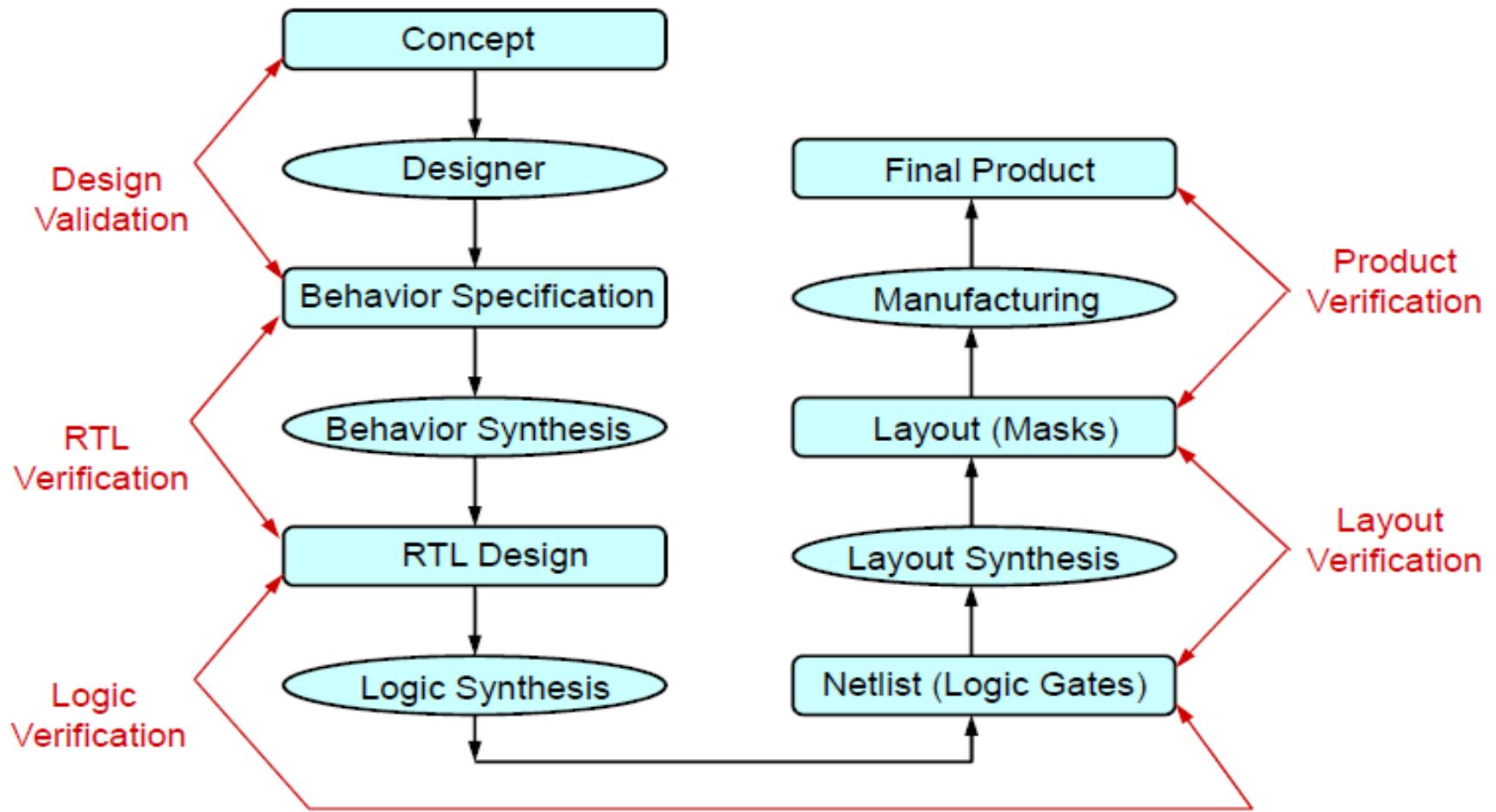
## ➤ Design methodology

- Process for creating a design

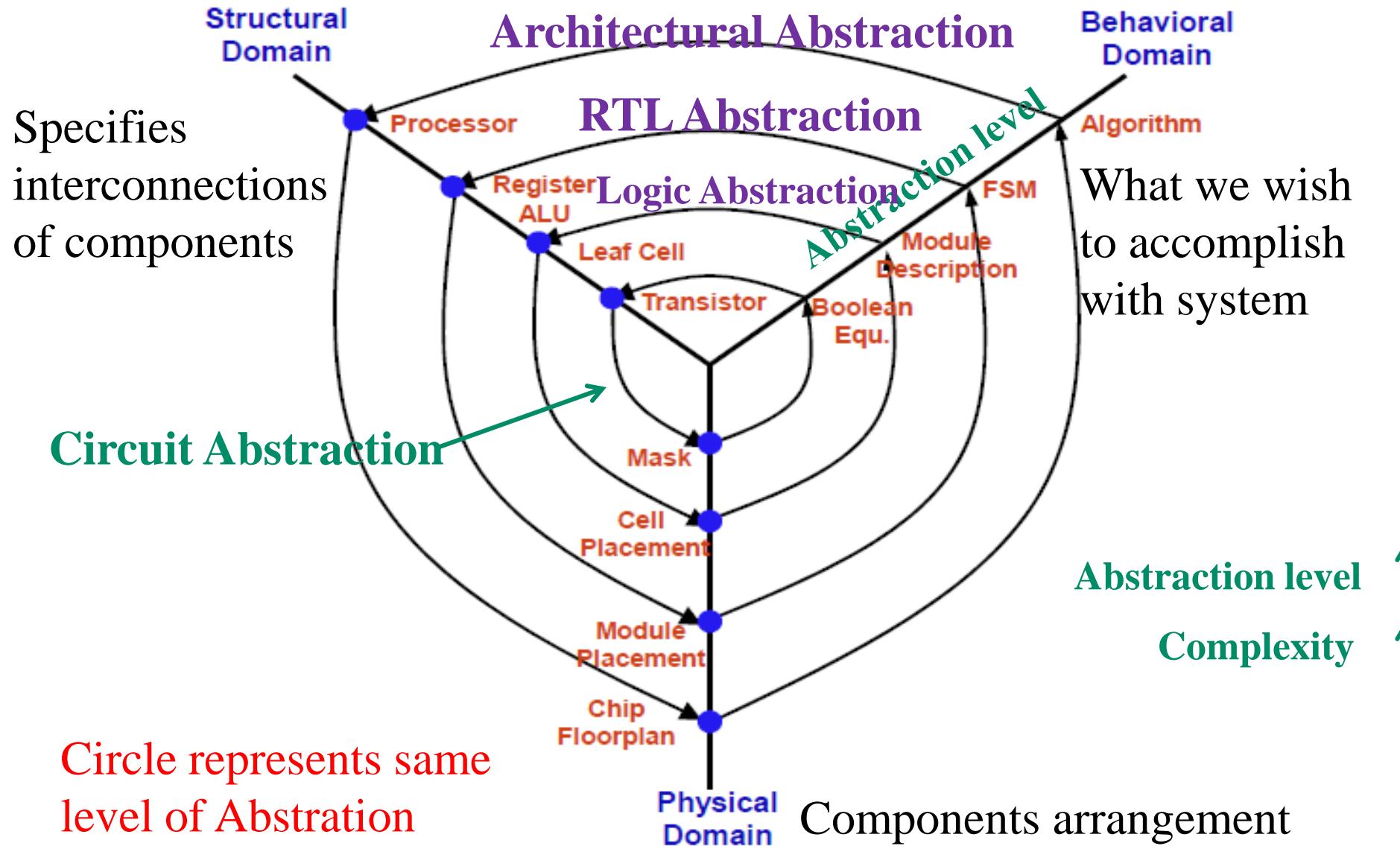
## ➤ Methodology Goals

- Design cycle
- Complexity
- Performance
- Reuse
- Reliability

# VLSI Design Flow



# Gajski Y Chart



# VLSI Design Hierarchy

## Works on Divide and Conquer

- Regularity
- Modularity
- Locality

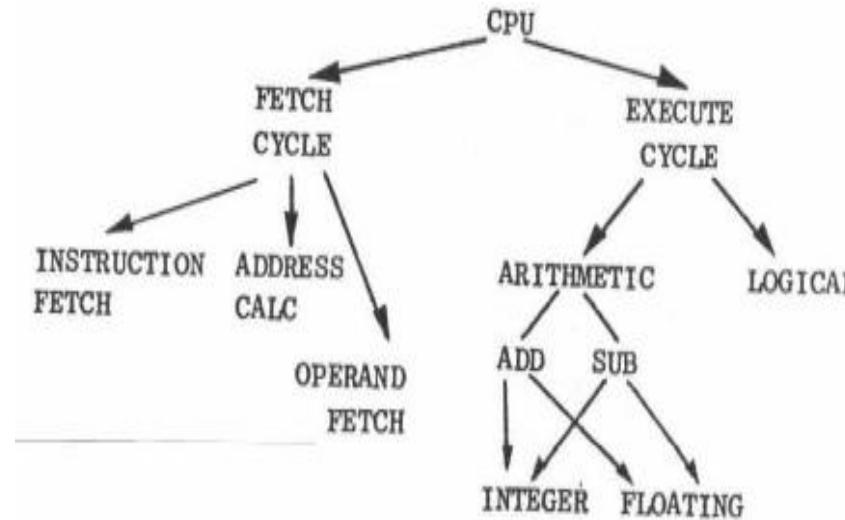
Hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible

Various functional blocks which make up the larger system must have well-defined functions and interfaces. **Independent of each other**

Internals of each module become unimportant to the exterior modules. **Internal details remain at the local level.**

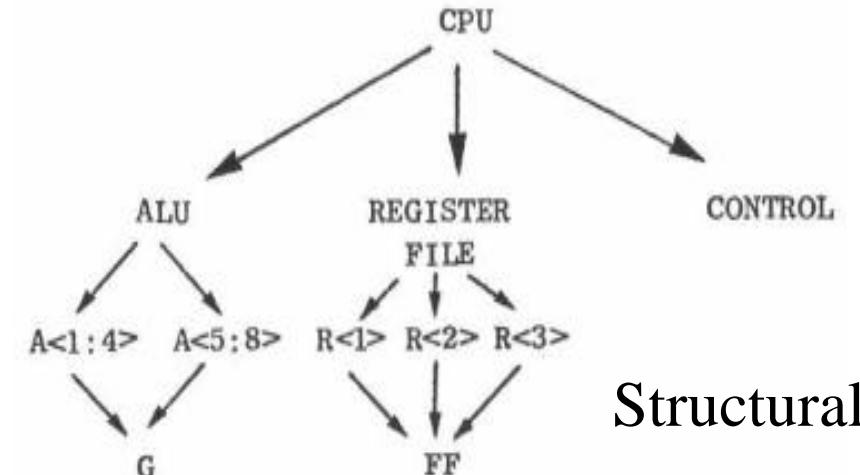
# VLSI Design Hierarchy

Exist at all level of Abstraction

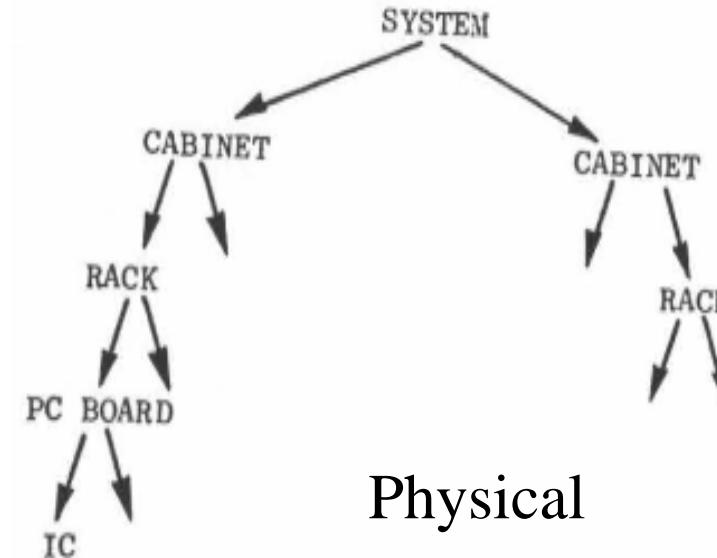


Behavioral

Example of a Computer



Structural



Physical

# VLSI Design Hierarchy

Regularity exist at all level of Abstraction

- Transistor Level: All are of same size
- Logic Level : All Gate are of same type

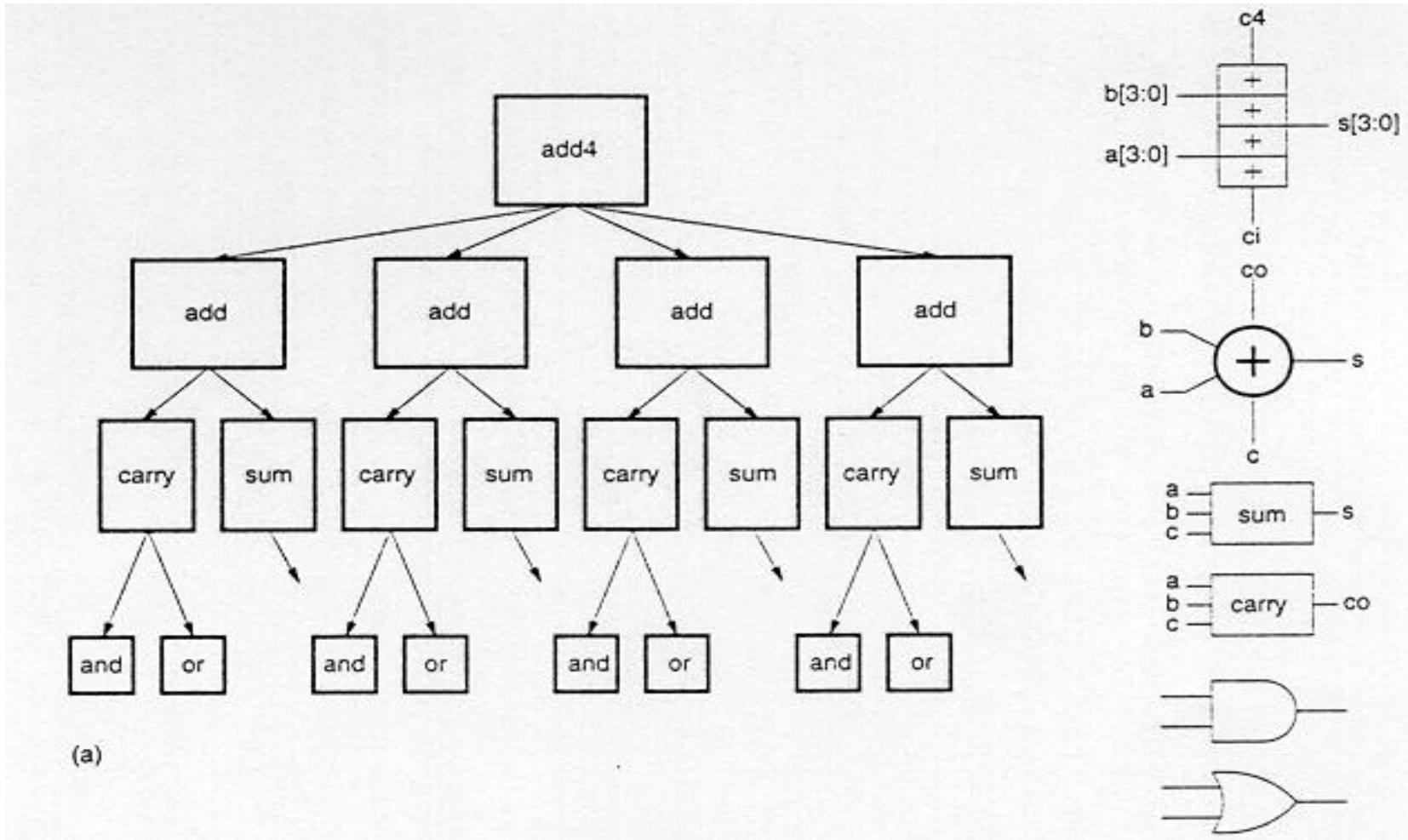
## VLSI Design Hierarchy (Advantage)

Regularity usually reduces the number of different **modules** that need to be designed and verified, at all levels of abstraction.

Modularity enables the **parallelization** of the design process. It also allows the use of generic modules in various designs.

Time-critical operations should be performed locally, without the need to access distant modules or signals.

# VLSI Design Hierarchy (Example)



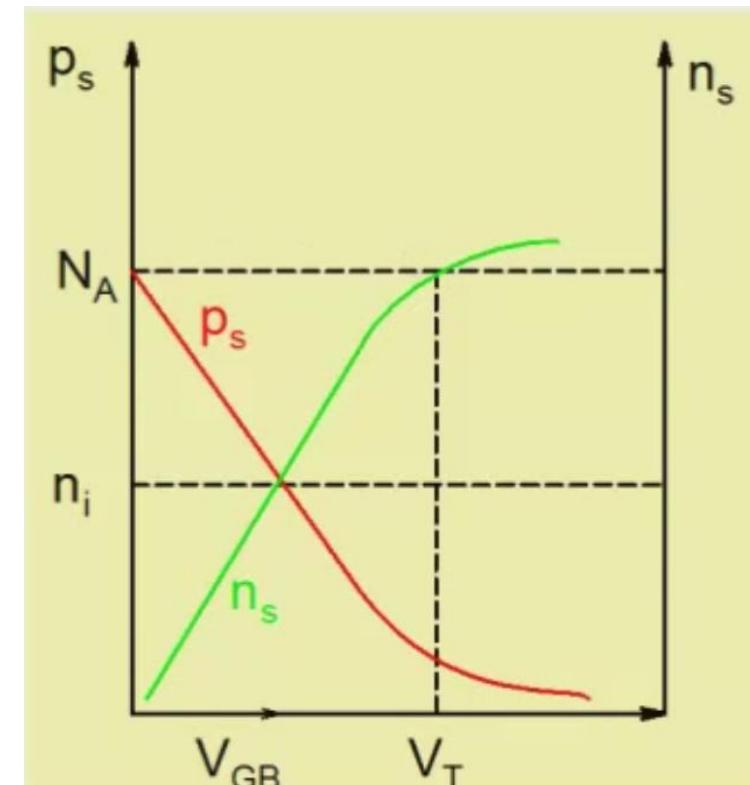
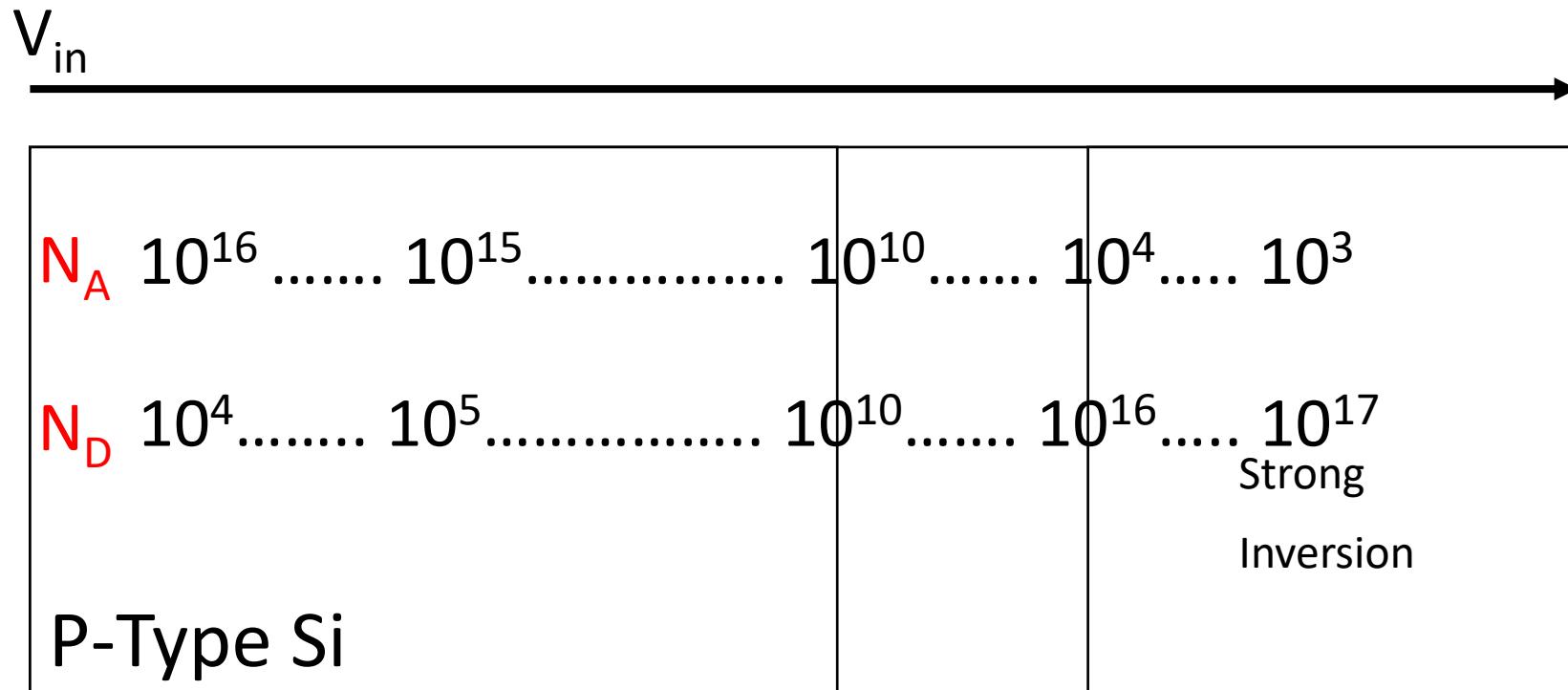
Structural decomposition of a CMOS four-bit adder into its components

# Field Effect

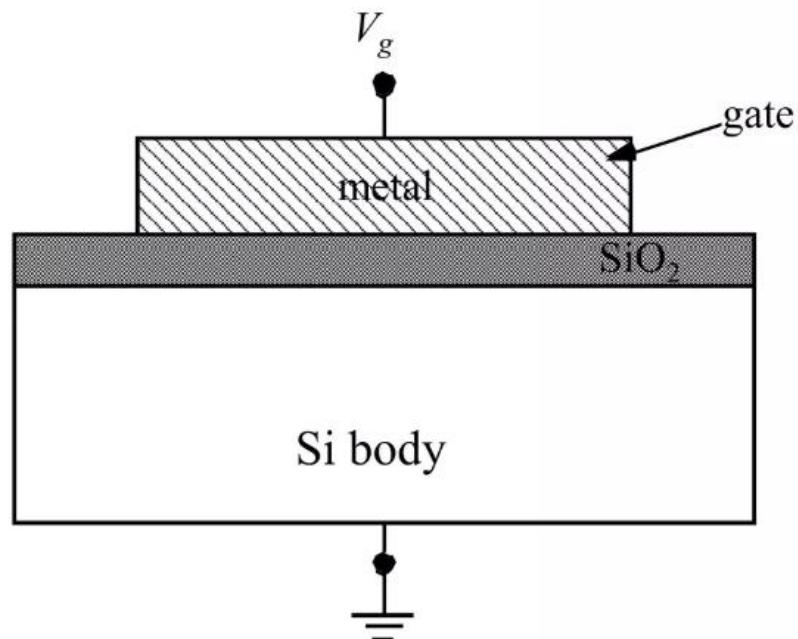
# Mass Action Law

Under thermal equilibrium the product of the free electron concentration and the free hole concentration is equal to a constant equal to the square of intrinsic carrier concentration.

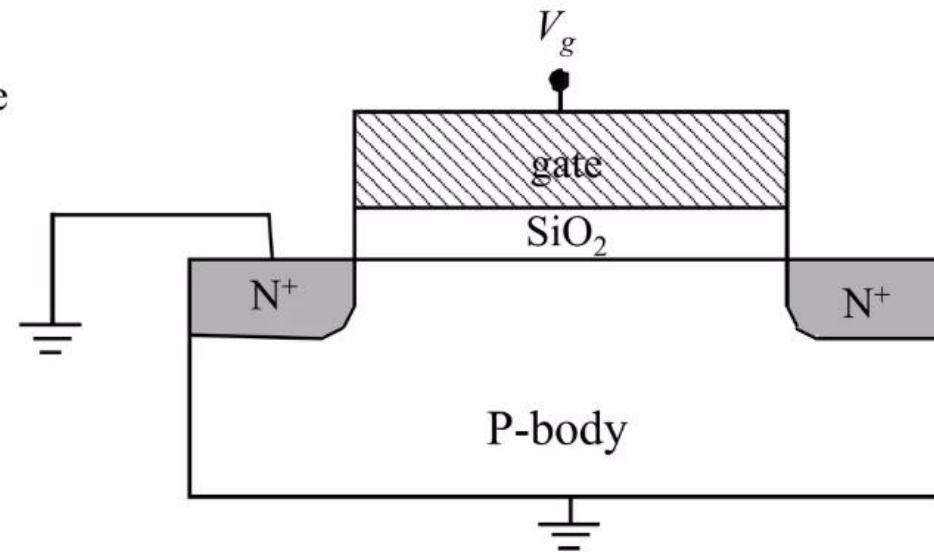
$$N_A N_D = n_i^2$$



# MOS: Metal-Oxide-Semiconductor

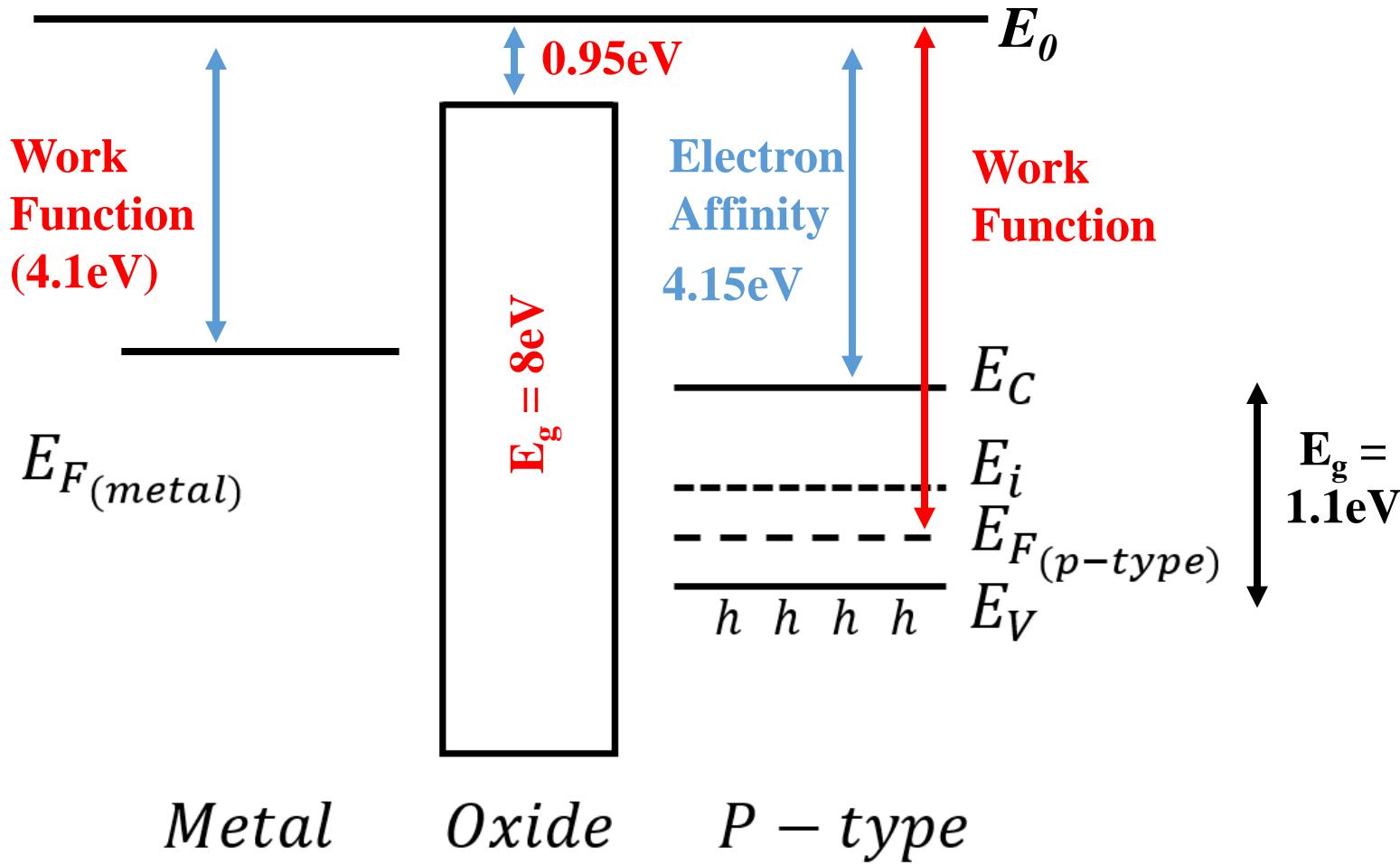


MOS capacitor

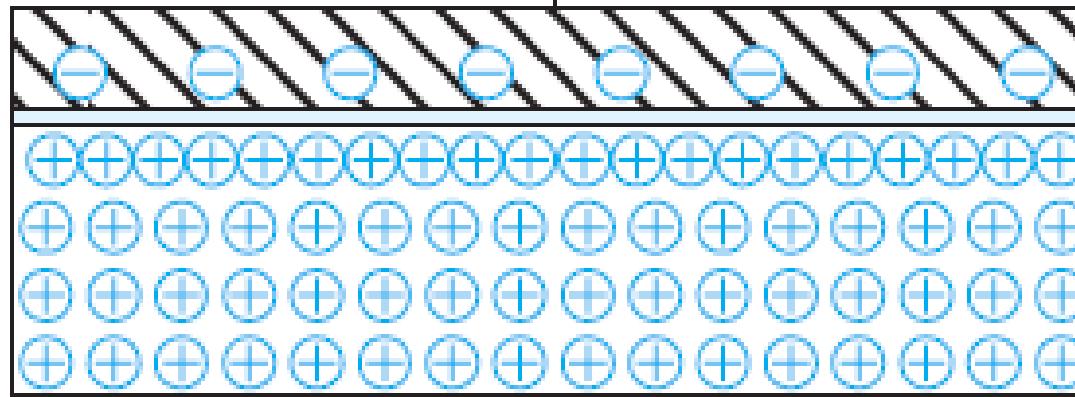


MOS transistor

# MOS Capacitor



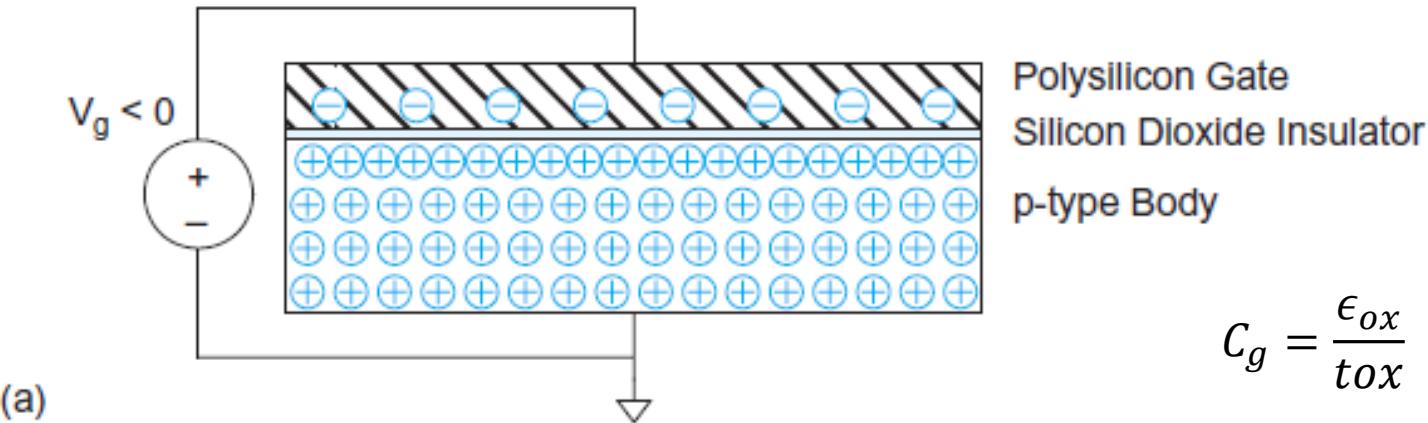
# MOS Capacitor



Oxide thickness, Threshold voltage, and Doping levels, depend on the fabrication process, and cannot be changed by design; they are technology parameters.

# MOS Capacitor

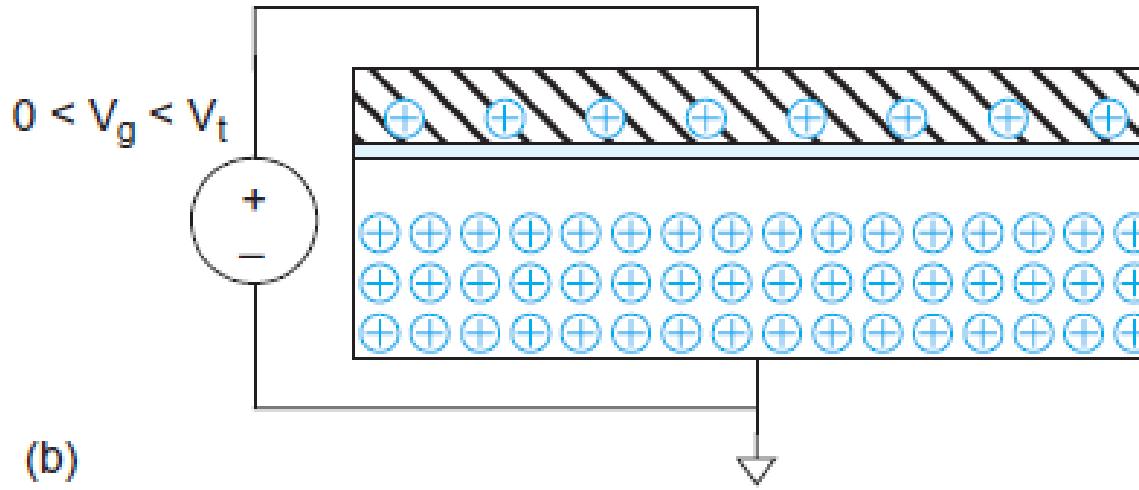
## i. Accumulation



A negative voltage is applied to the gate, so there is negative charge on the gate. The mobile positively charged holes are attracted to the region beneath the gate. This is called the *accumulation* mode

# MOS Capacitor

## ii. Depletion



Depletion Region

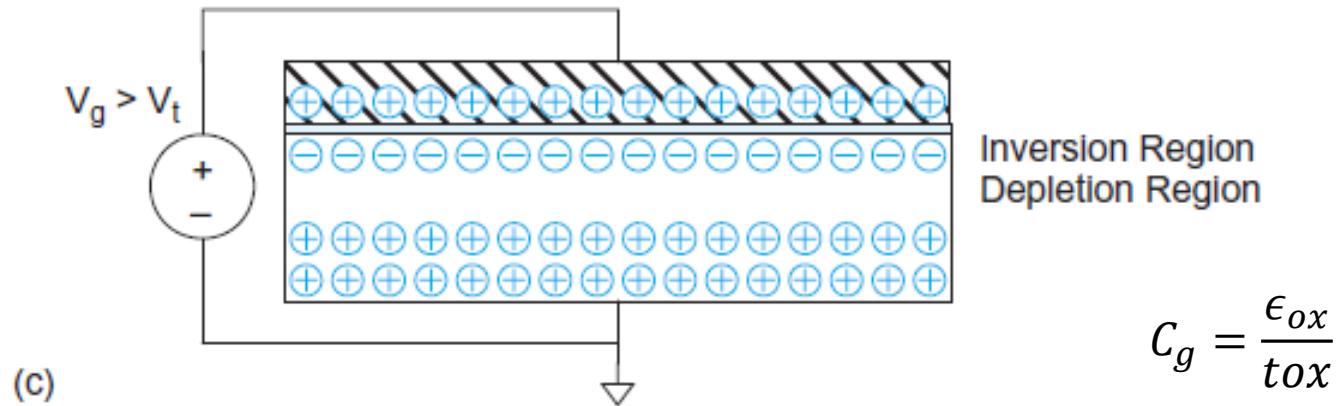
$$C_{dep} = \frac{\epsilon_{si}}{X_d}$$

$$C_g = \frac{\epsilon_{ox}}{t_{ox}}$$

A small positive voltage is applied to the gate, resulting in some positive charge on the gate. The holes in the body are repelled from the region directly beneath the gate, resulting in a *depletion* region forming below the gate.

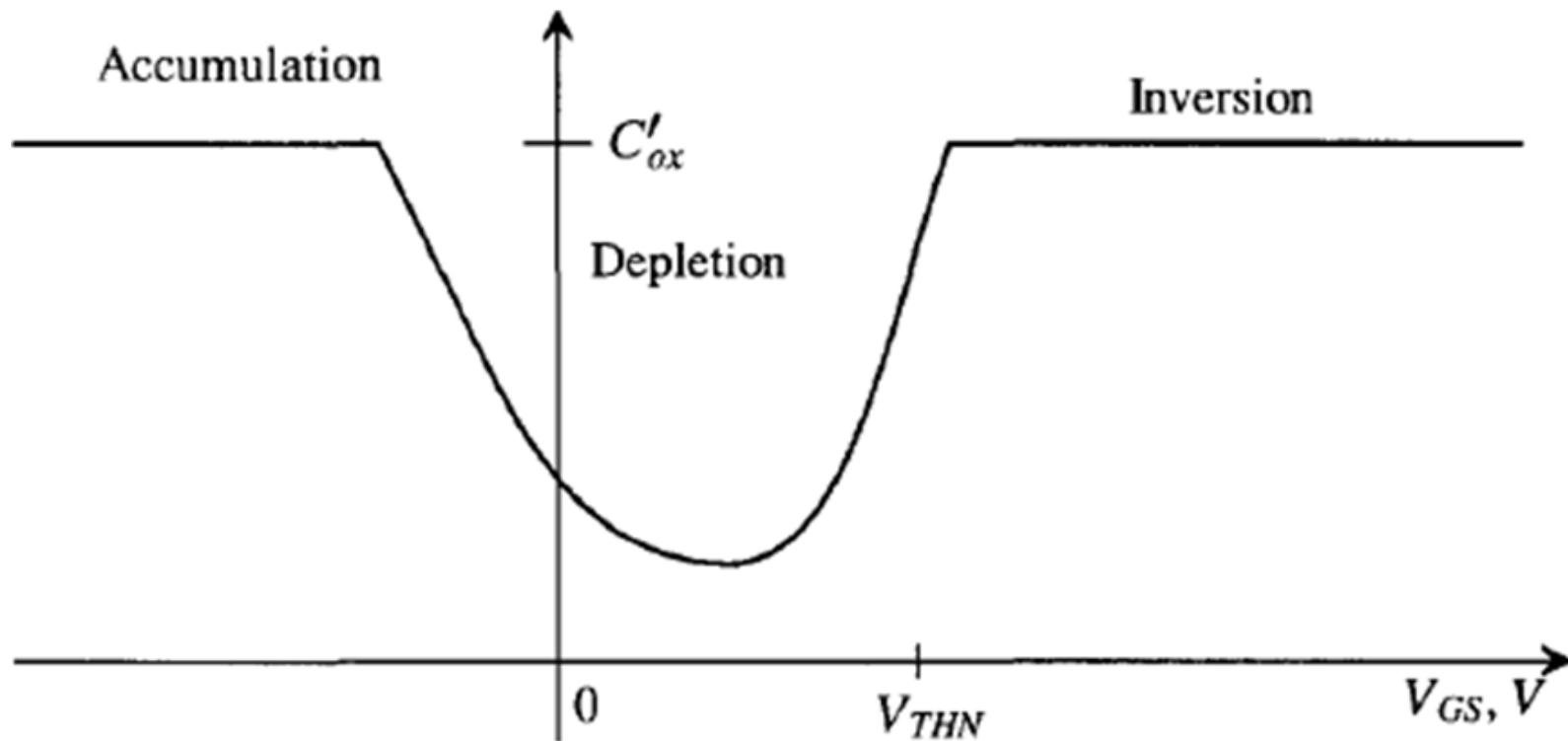
# MOS Capacitor

*iii. inversion*



A higher positive potential exceeding a critical threshold voltage  $V_t$  is applied, attracting more positive charge to the gate. The holes are repelled further and some free electrons in the body are attracted to the region beneath the gate. This conductive layer of electrons in the p-type body is called the *inversion* layer

# MOS Capacitor



# MOSFET

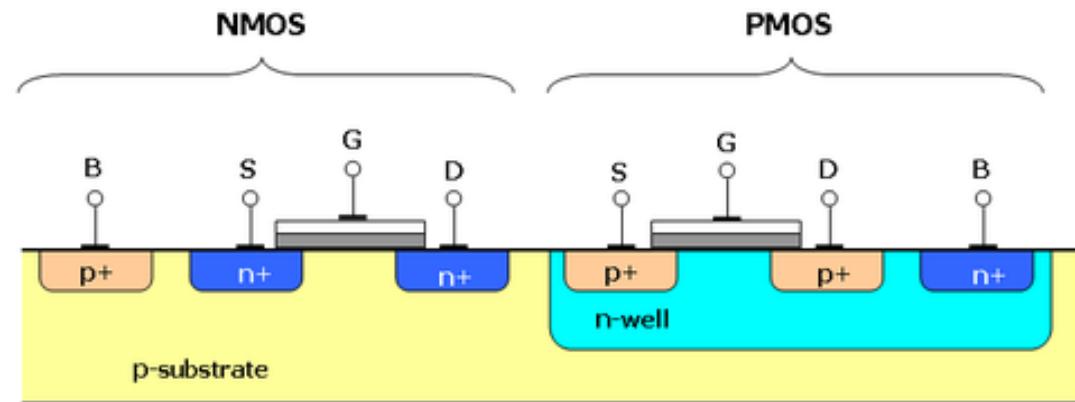
- Enhancement type MOSFET
  1. N-Channel MOSFET
  2. P-Channel MOSFET
- Depletion type MOSFET
  1. N-Channel MOSFET
  2. P-Channel MOSFET

# MOSFET

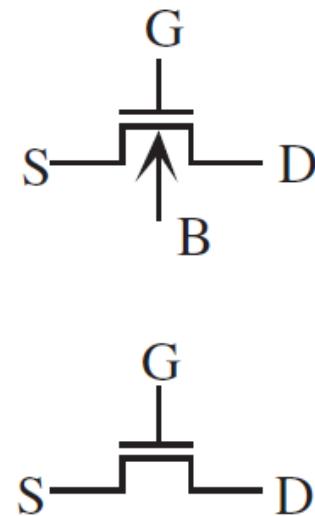
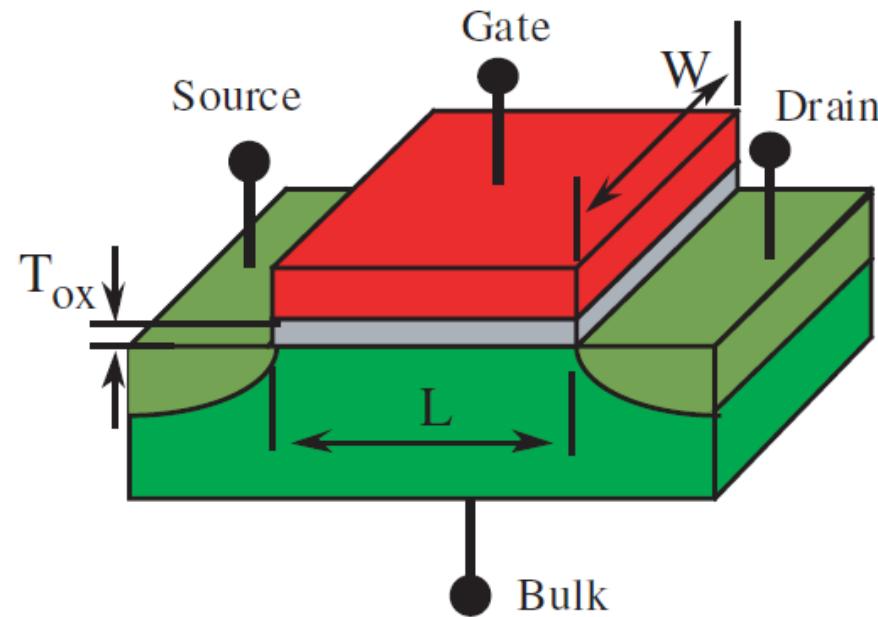
- Enhancement type MOSFET
  1. N-Channel MOSFET
  2. P-Channel MOSFET

## Device Structure

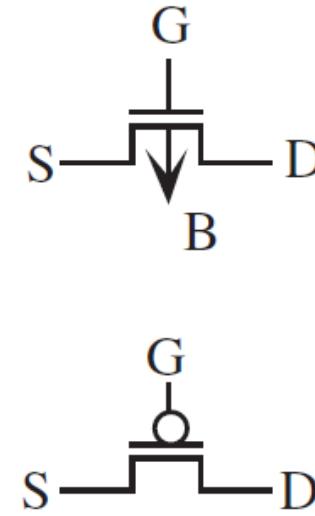
- Depletion type MOSFET
  1. N-Channel MOSFET
  2. P-Channel MOSFET



# Enhancement MOSFET



*n*MOS

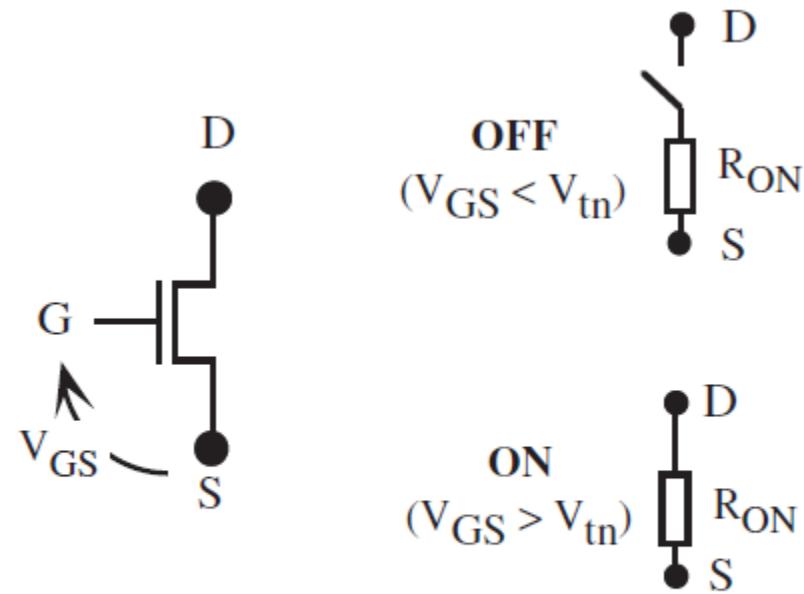


*p*MOS

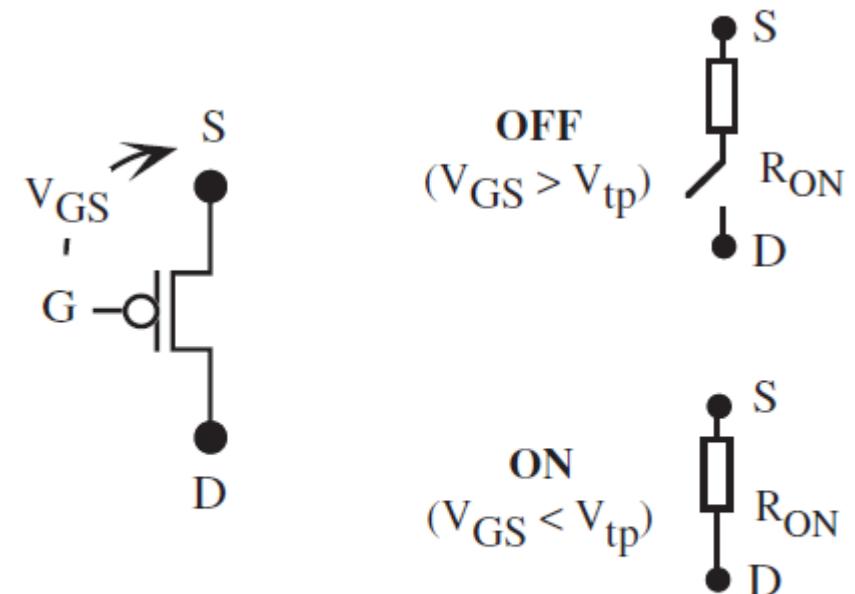
$T_{ox} = 15\text{\AA}$  to  $100\text{\AA}$  (Diameter of  $\text{SiO}_2$  molecule is about  $3.2\text{\AA}$ )

Arrows always point from P to N, so an NMOS (N-channel in P-well or P-substrate) has the arrow pointing in (from the bulk to the channel)

# Enhancement MOSFET



$n\text{MOS } (V_{tn} > 0, V_{DS} \geq 0, V_{GS} \geq 0)$



$p\text{MOS } (V_{tp} < 0, V_{DS} \leq 0, V_{GS} \leq 0)$

**$V_{Th}$  is fixed for NMOS and PMOS devices for given fabrication process**

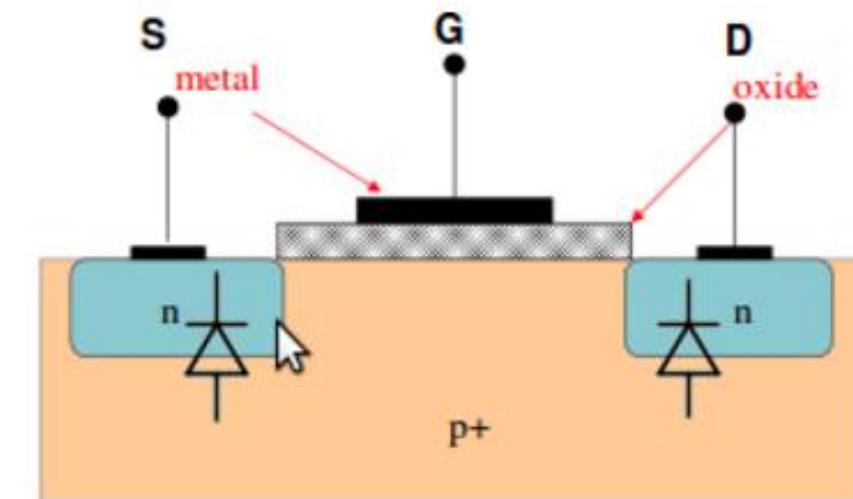
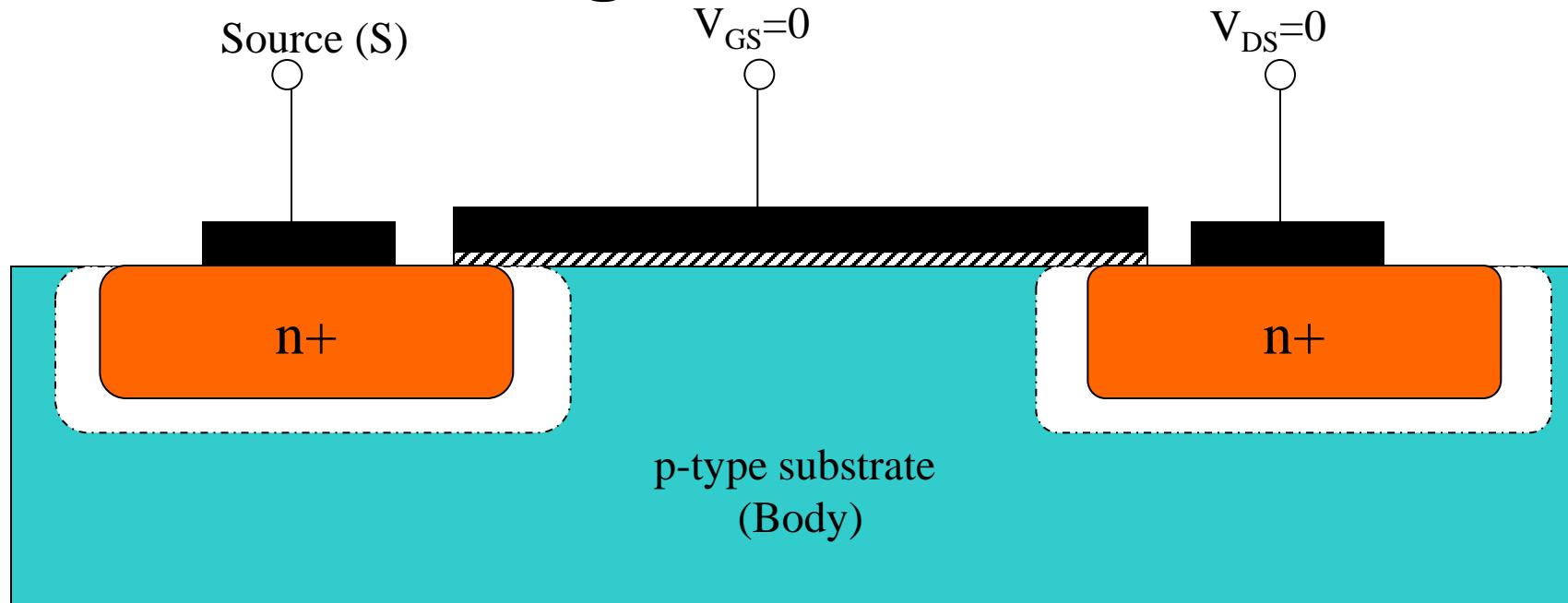
# Enhancement NMOS Transistor

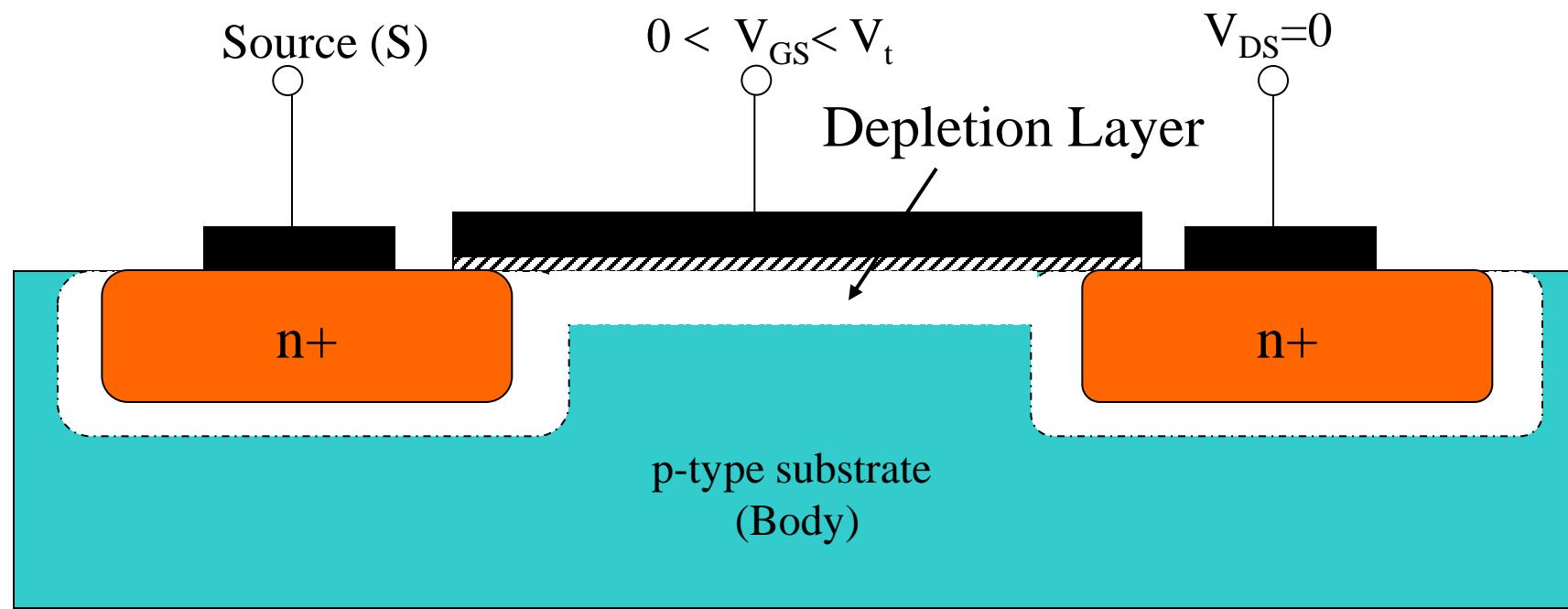
# Operation Of N-MOS Transistor

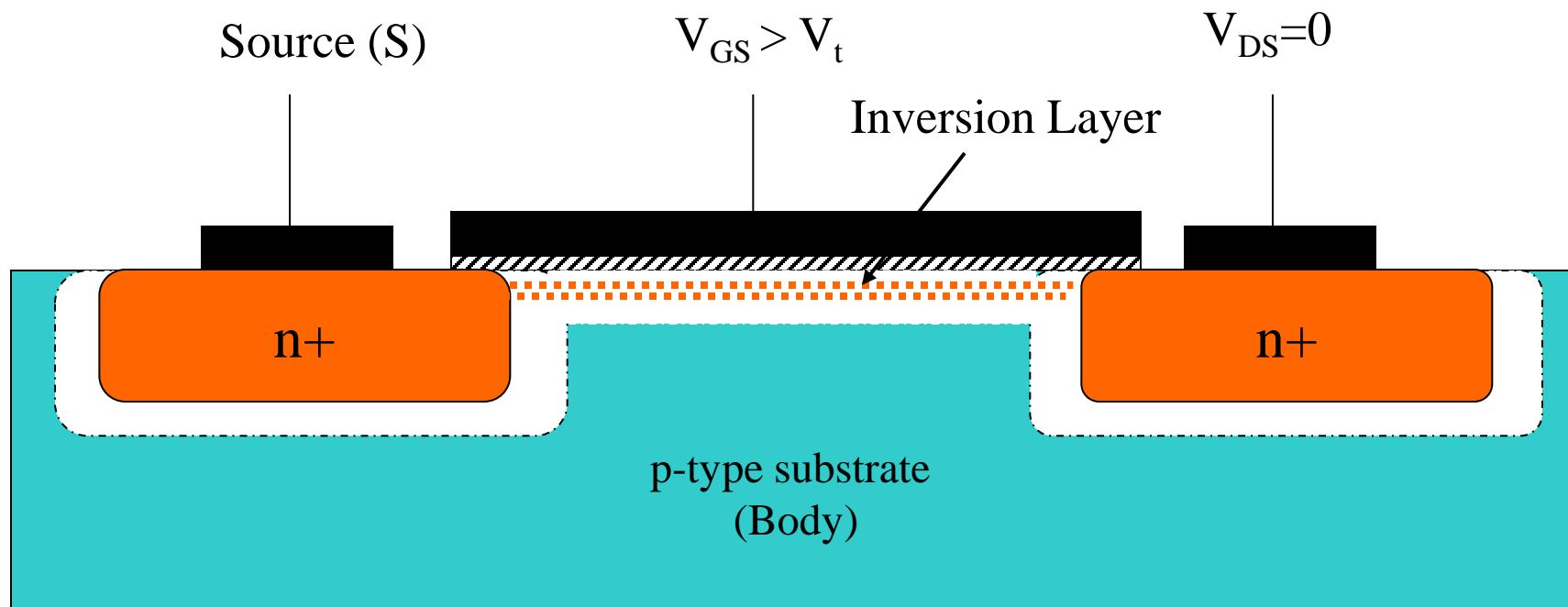
Depending on the relative voltages of the source, drain and gate, the NMOS transistor may operate in any of three regions viz :

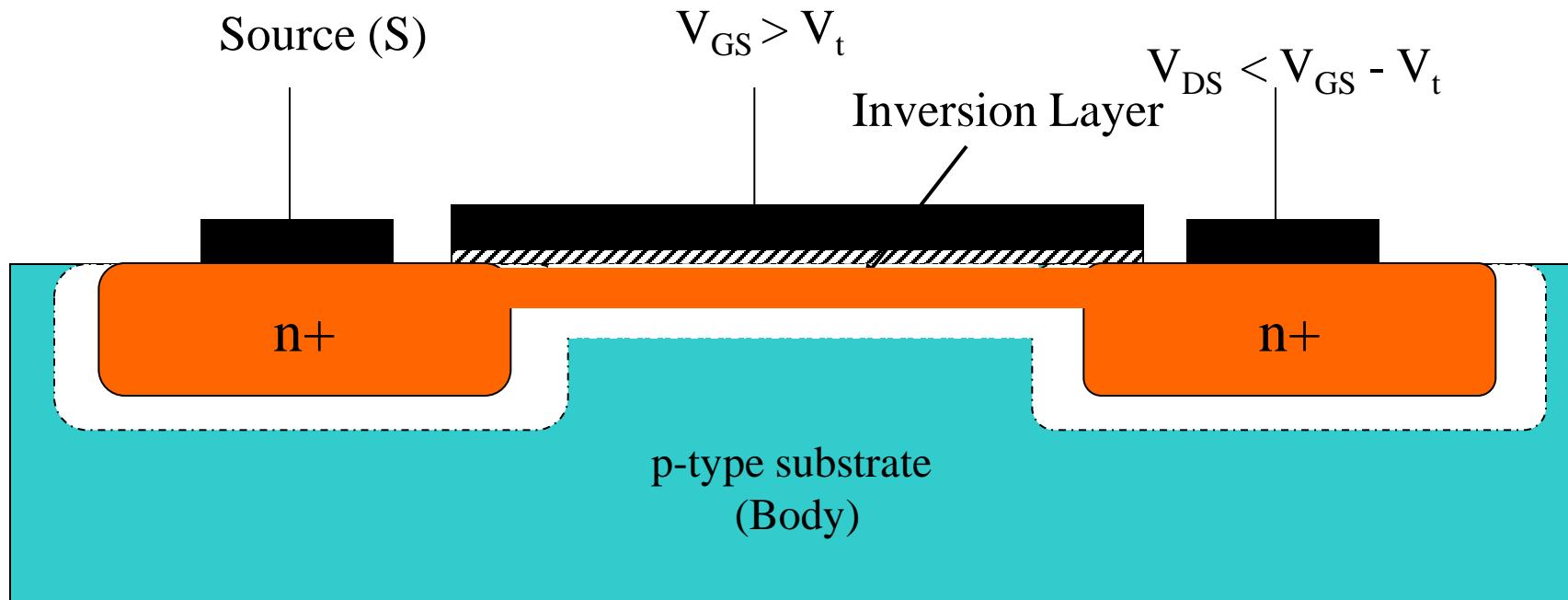
- Cut off : Current flow is essentially zero (also called accumulation region)
- Linear : (Non saturated region)-It is weak inversion region drain current depends on gate and drain voltage.
- Saturation : It is strong inversion region where drain current is independent of drain-source voltage.

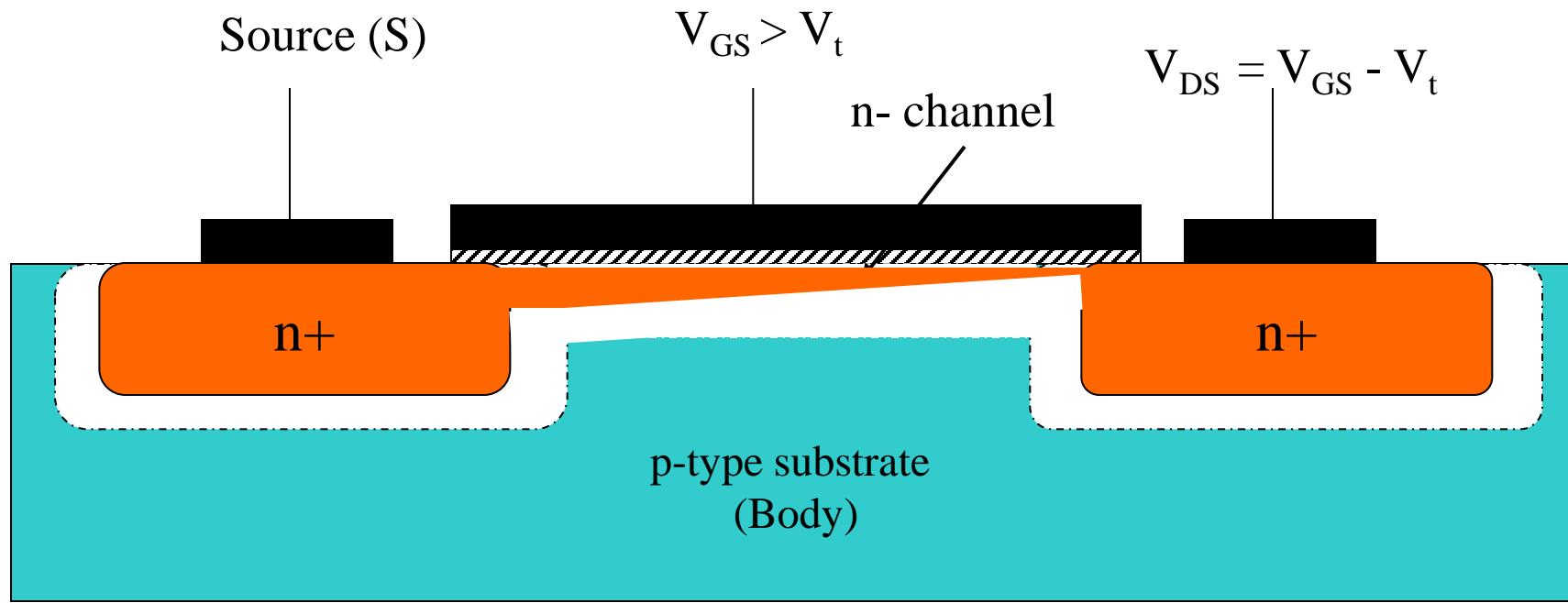
# Cut-off Region



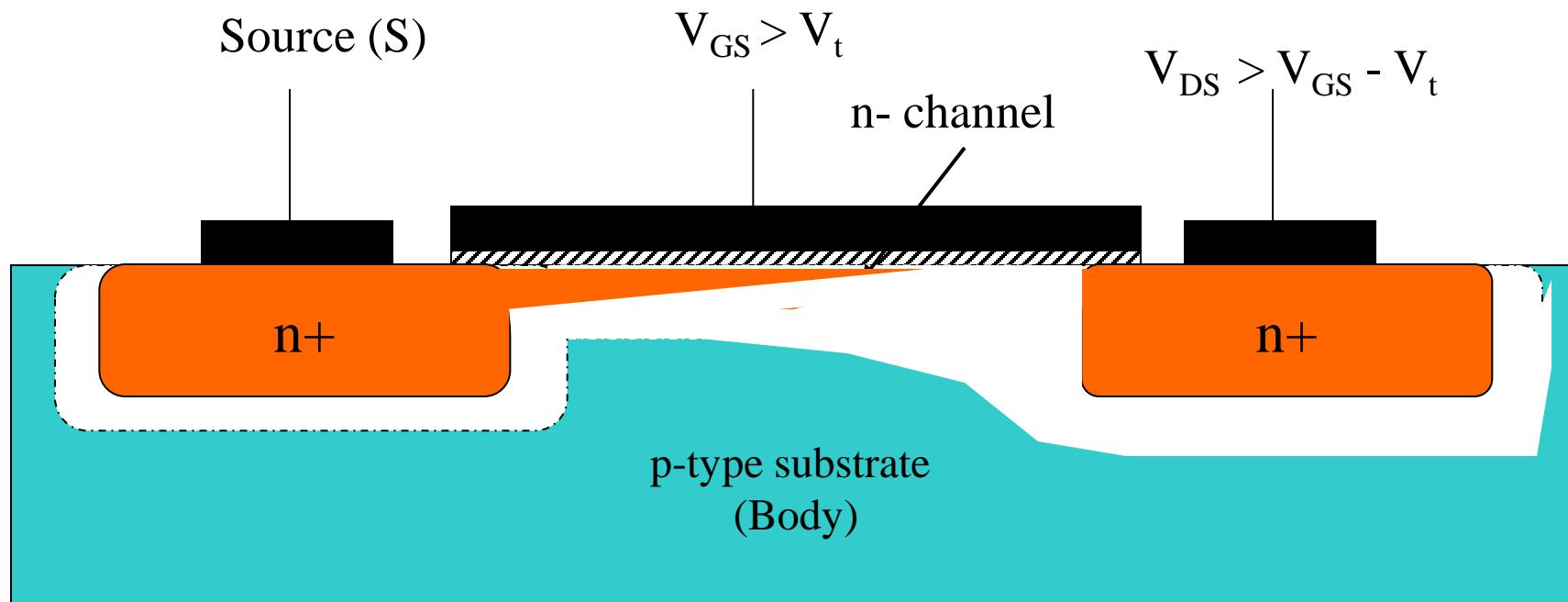






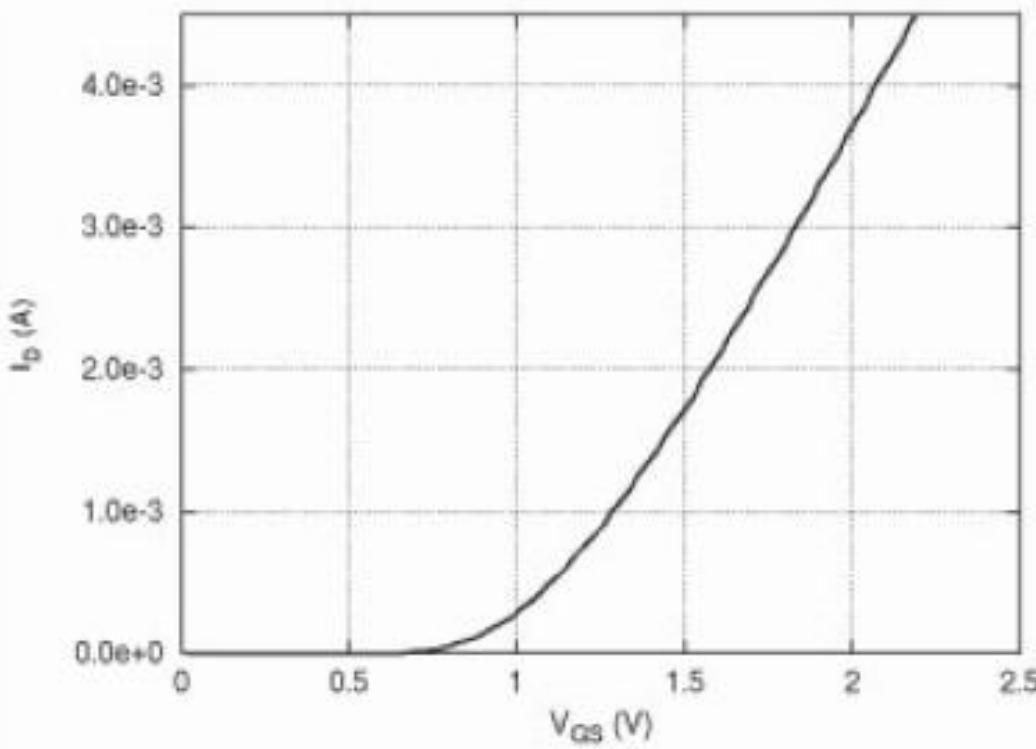


# Saturation Region

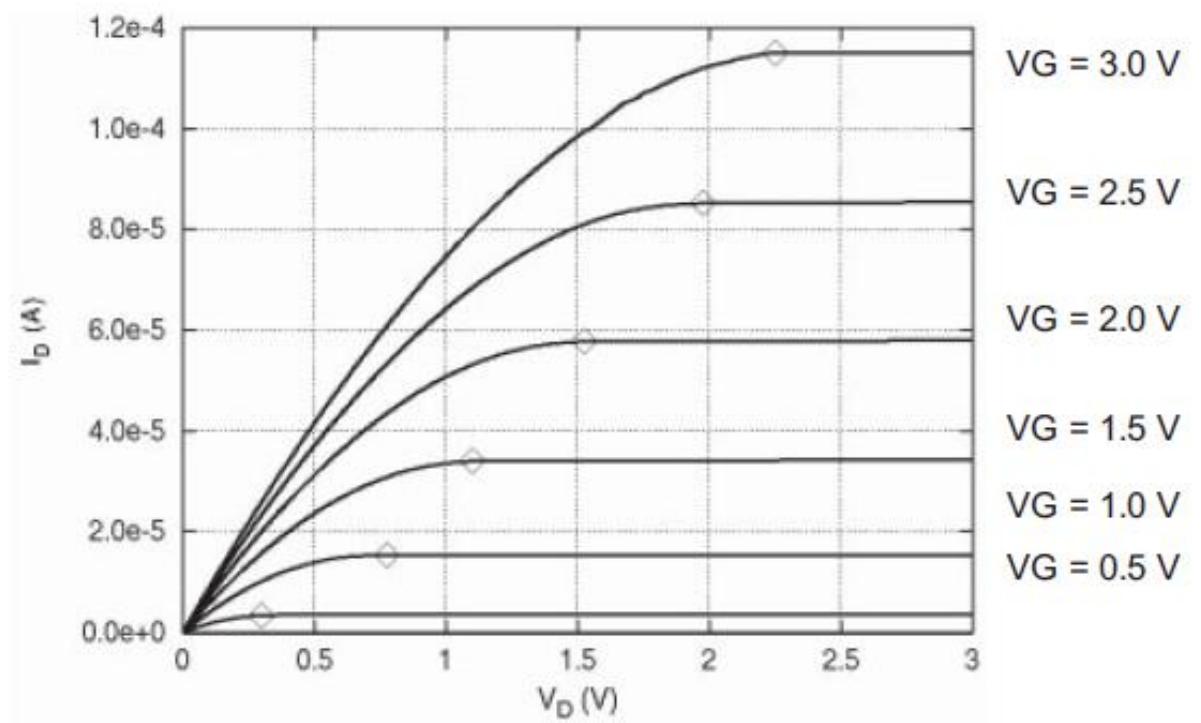


# Important Observations

- The bulk or substrate of *n*MOS transistors must always be connected to the lower voltage that is the reference terminal.
- The positive convention current in an *n*MOS device is from the drain to the source, and is referred to as  $I_{DS}$  or just  $I_D$ , since drain and source current are equal.
- When a positive voltage is applied to the drain terminal, the drain current depends on the voltage applied to the gate control terminal.



input characteristics ( $I_D$  vs.  $V_{GS}$ ) for an nMOS,



nMOS transistor output characteristics

# NMOS Threshold Voltage

$$V_t = V_{t0} + \gamma \left( \sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

$V_{t0}$  is the threshold voltage when the source is at the body potential.

$\phi_s$  is the *surface potential* at threshold

$\gamma$  is the *body effect coefficient*

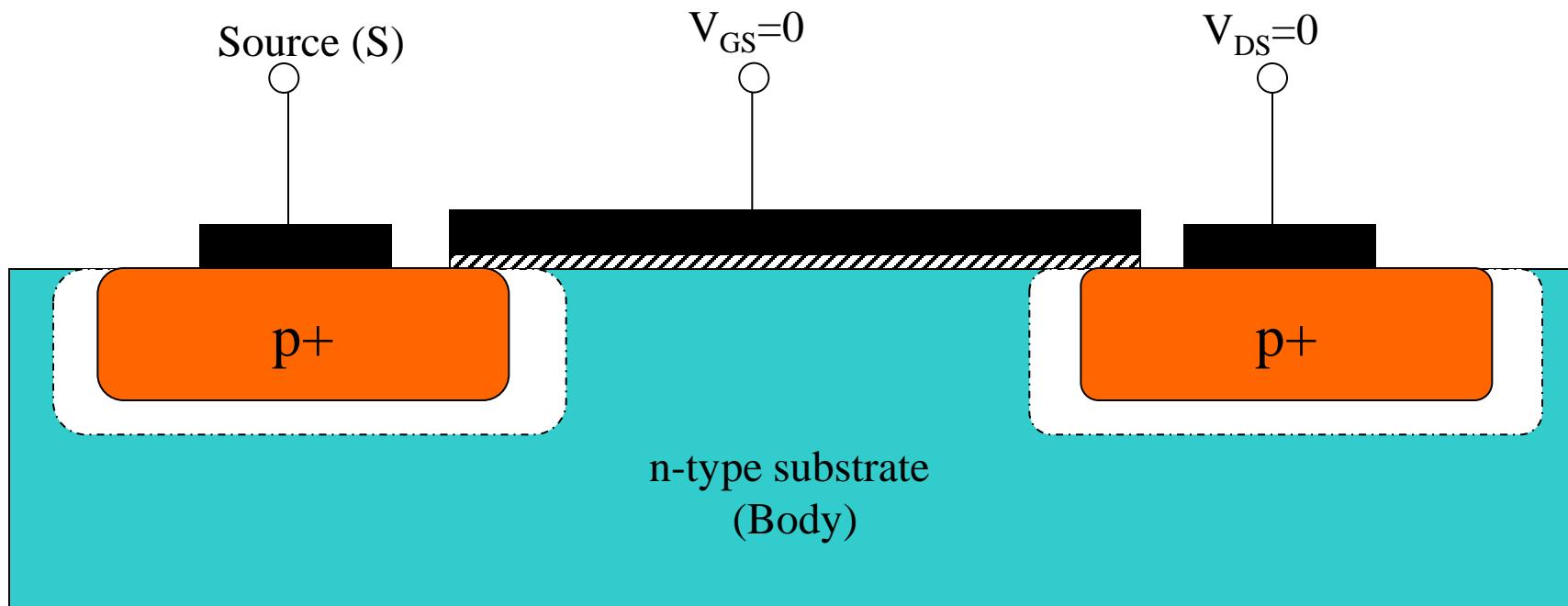
$$\gamma = \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \sqrt{2q\epsilon_{\text{si}}N_A} = \frac{\sqrt{2q\epsilon_{\text{si}}N_A}}{C_{\text{ox}}} \quad \text{and}$$

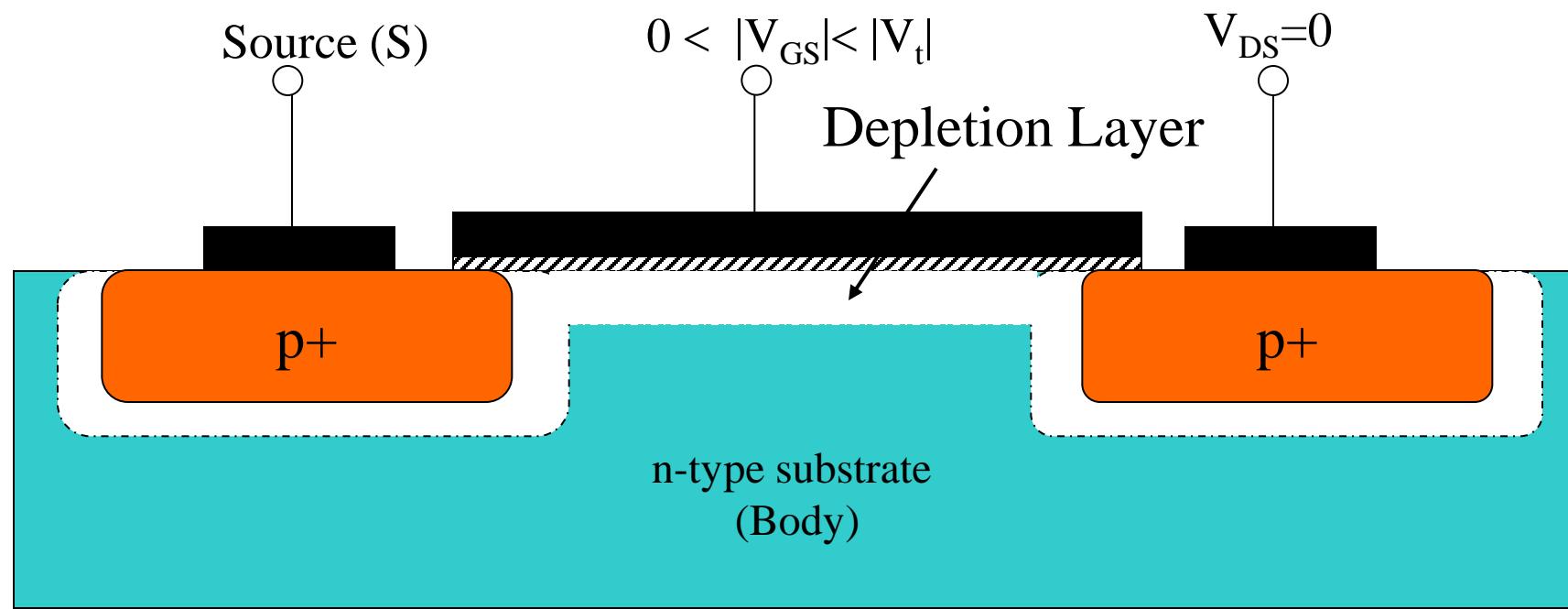
$$\phi_s = 2v_T \ln \frac{N_A}{n_i}$$

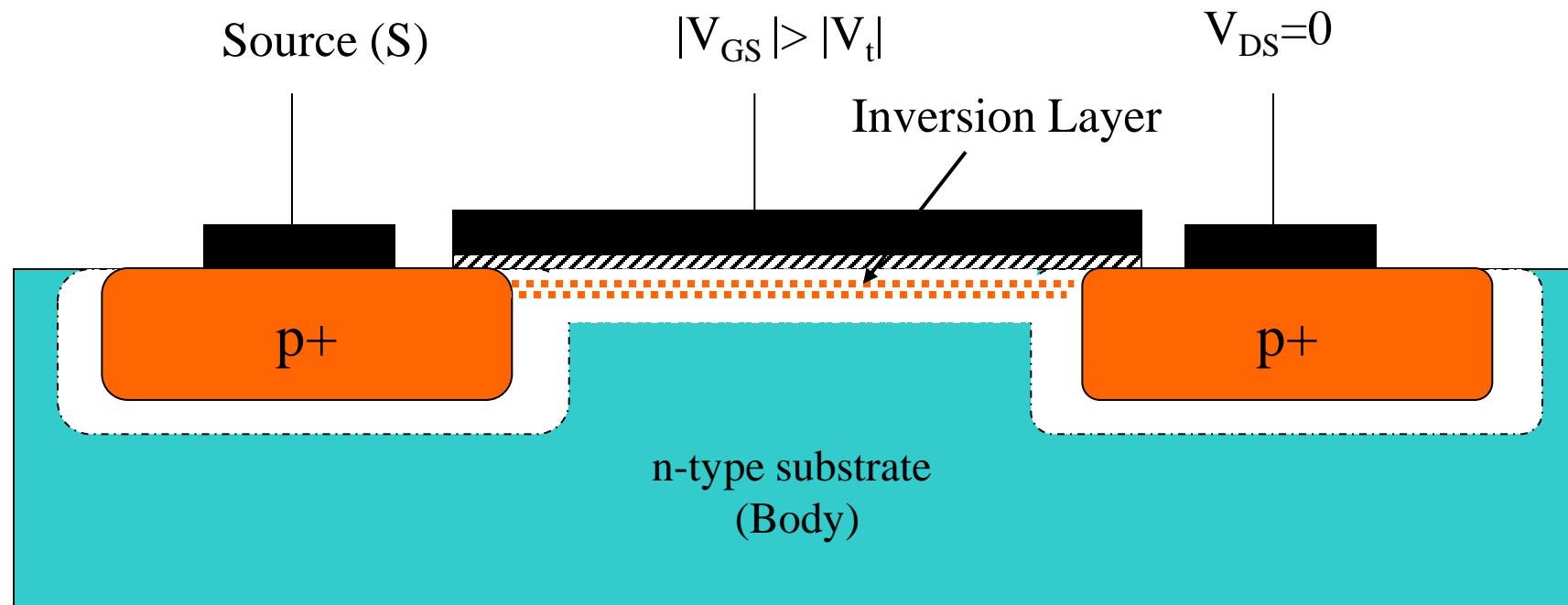
$v_T$  is thermal voltage, which is around 26mV at room temperature.

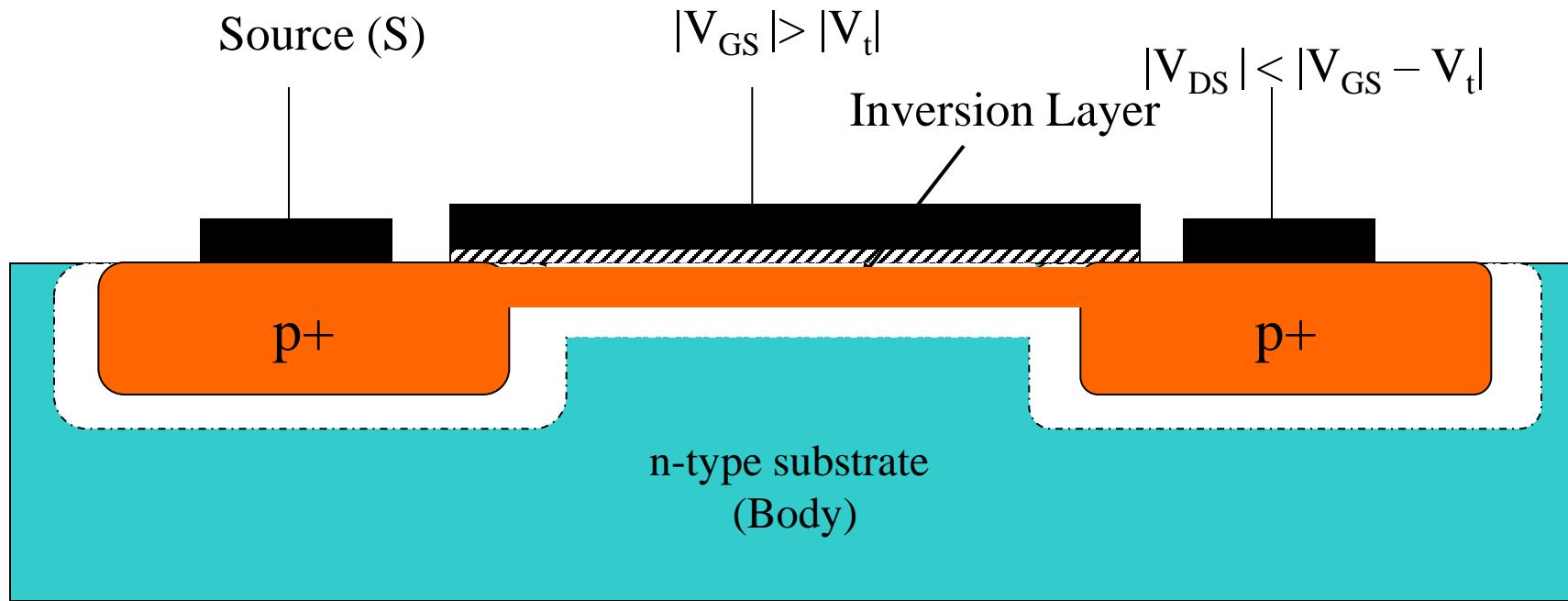
# Enhancement PMOS Transistor

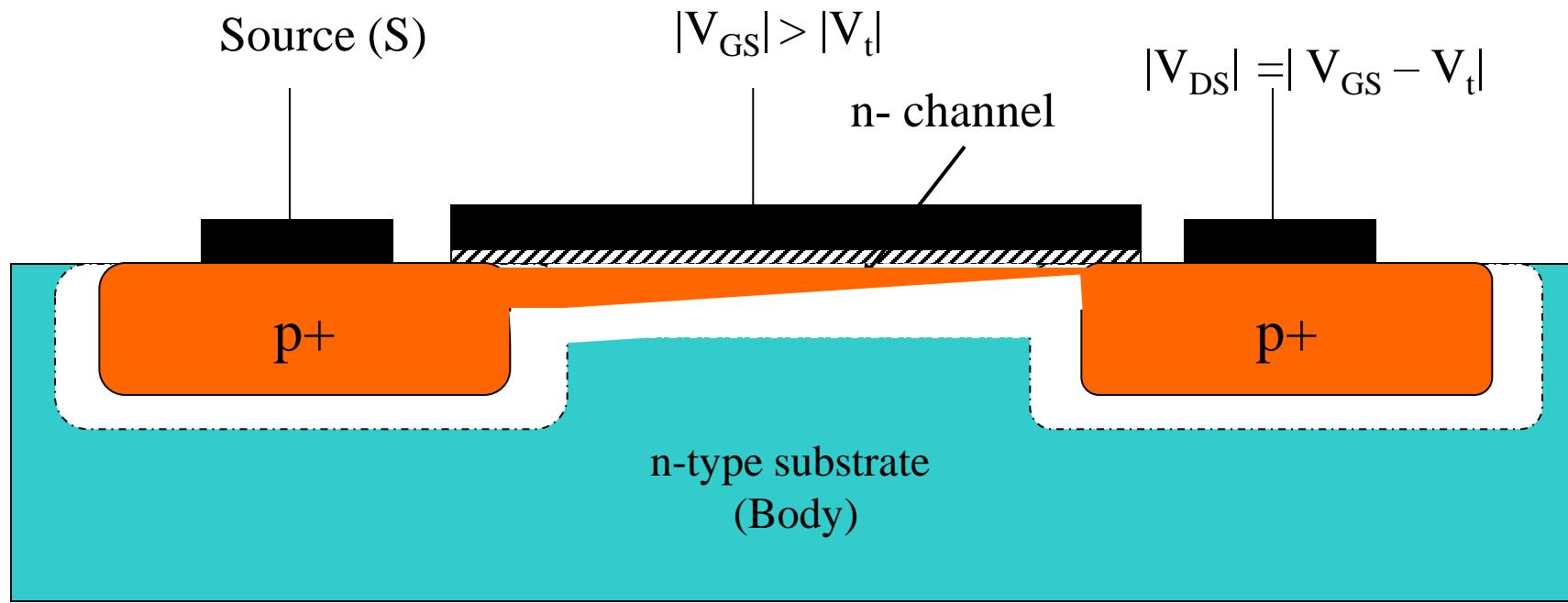
# Cut-off Region



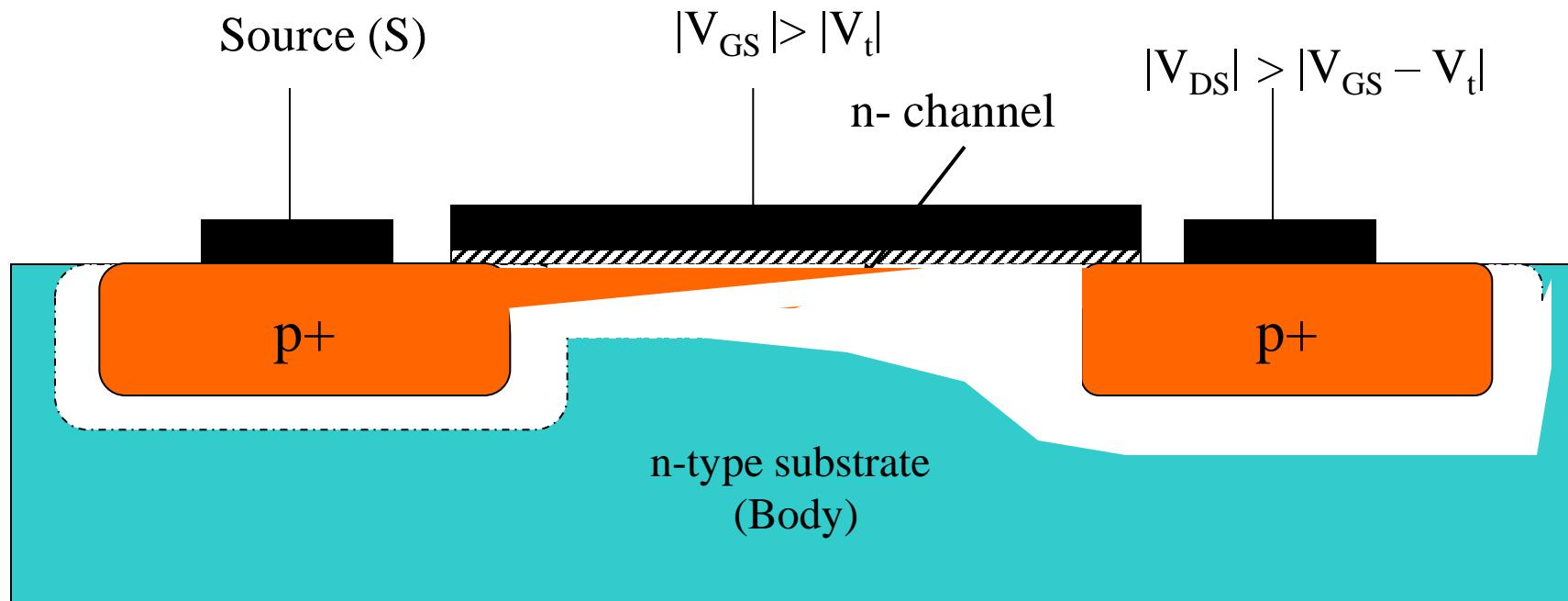


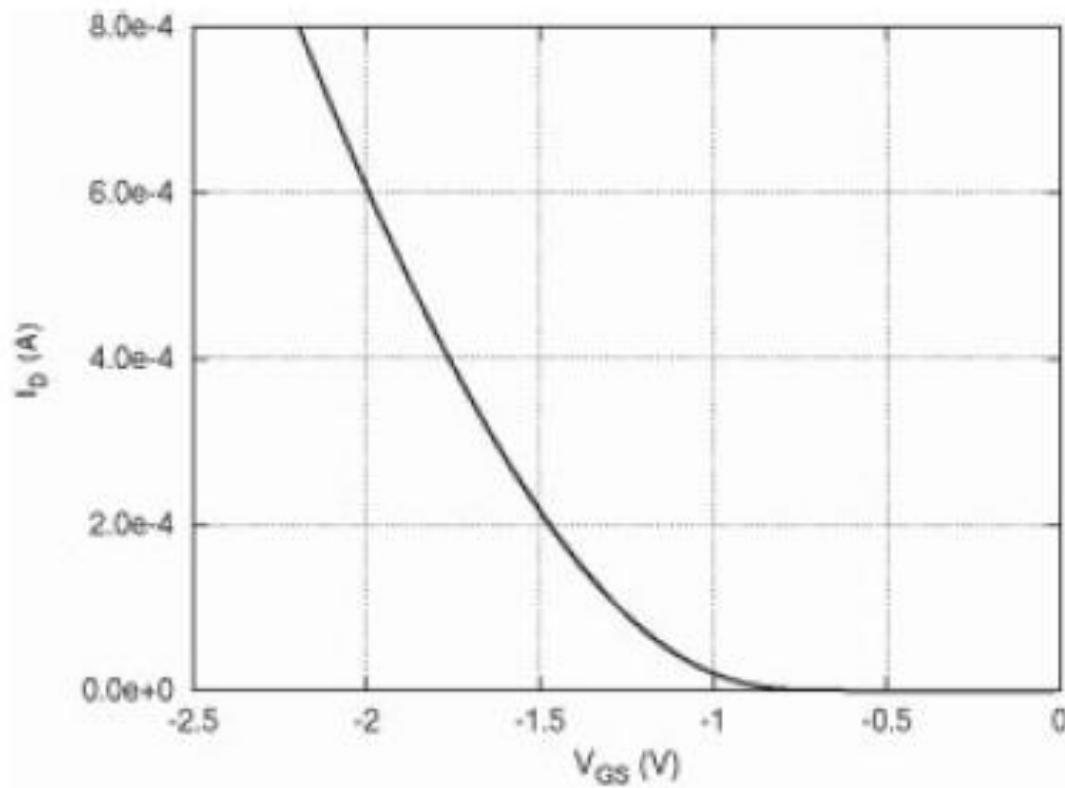




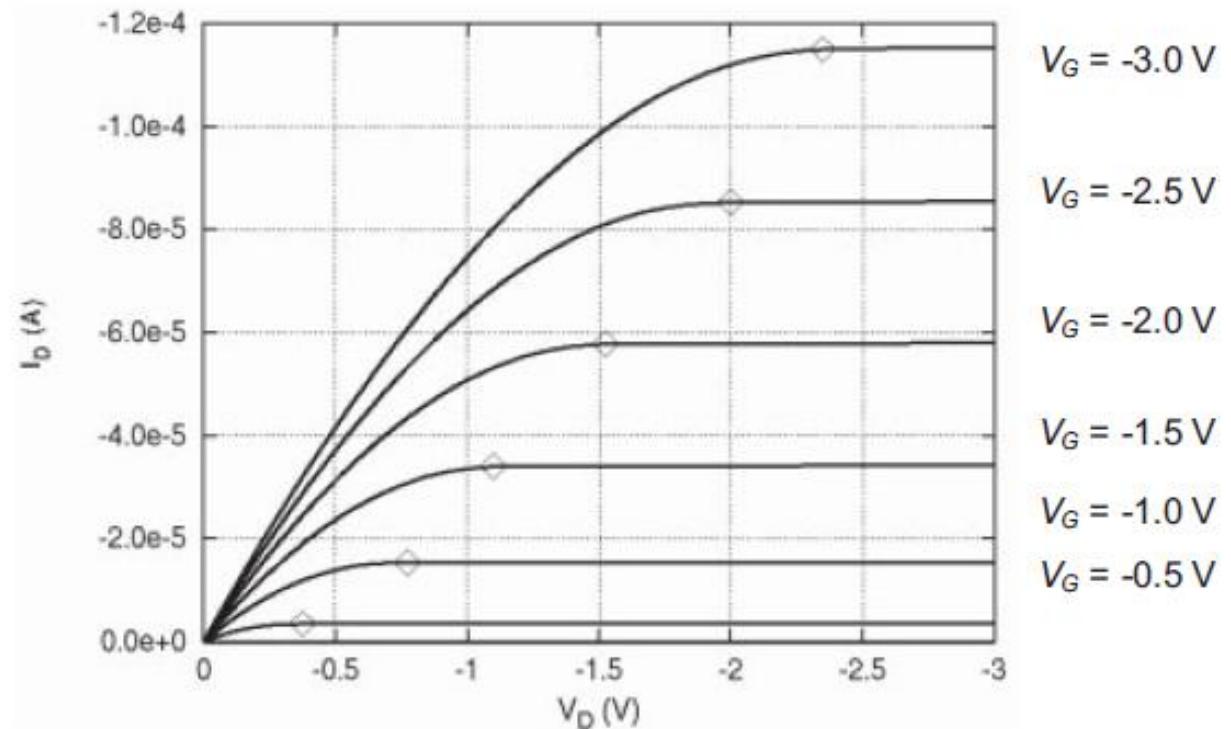


# Saturation Region





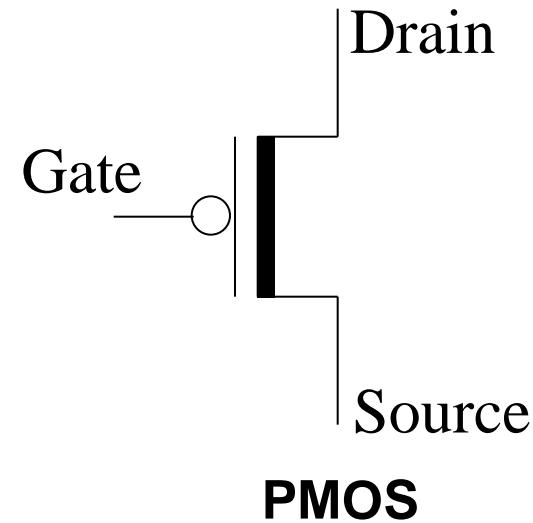
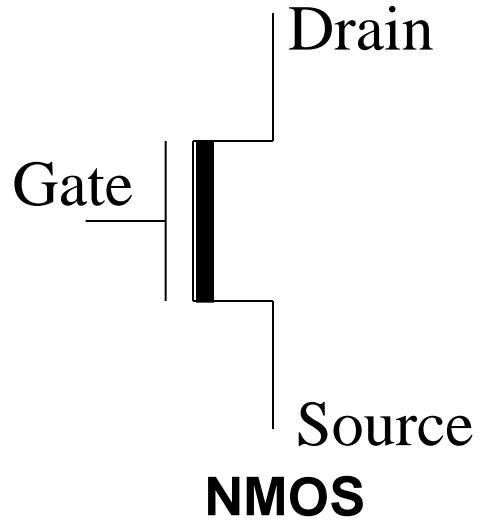
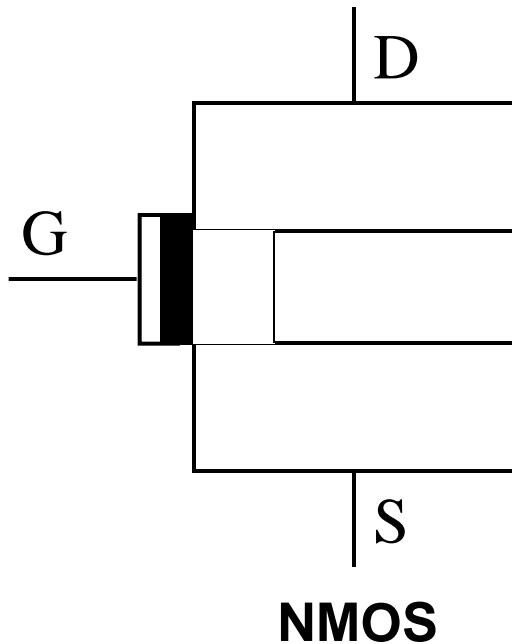
input characteristics ( $I_D$  vs.  $V_{GS}$ ) for an *p*MOS,



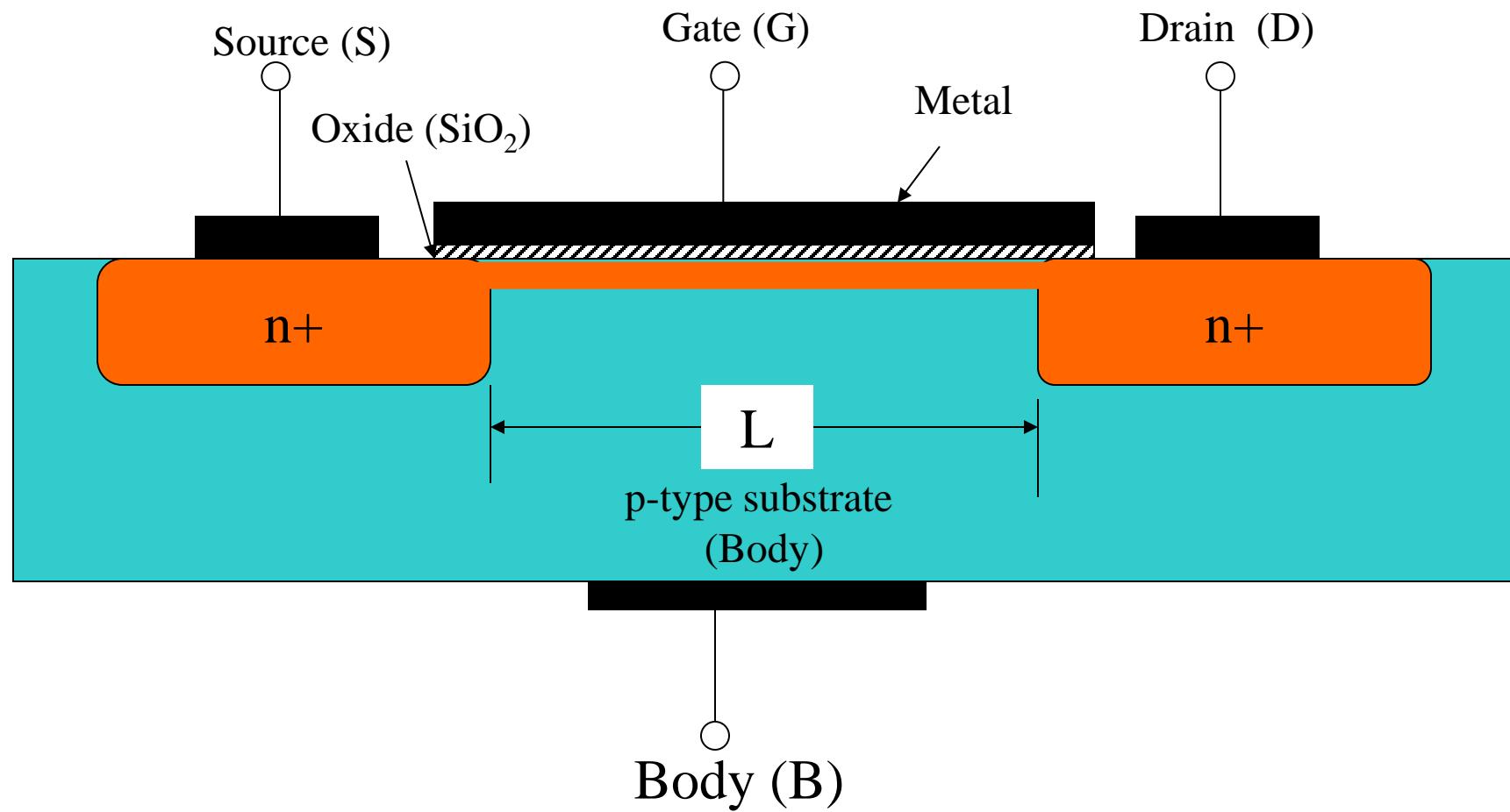
*p*MOS transistor output characteristics

# Depletion NMOS Transistor

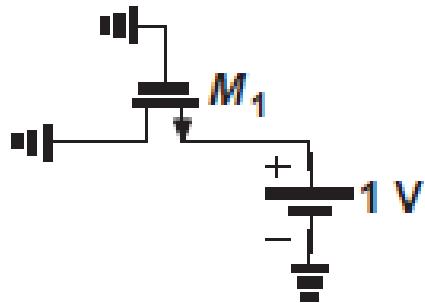
# Depletion Type MOS



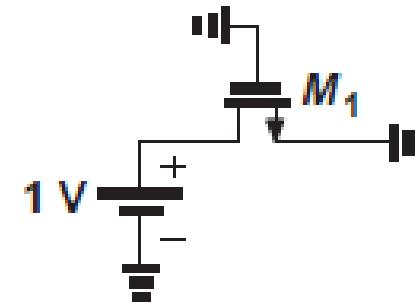
- In Depletion MOS structure, the source & drain are diffused on P- substrate as shown above.
- Positive voltages enhances number of electrons from source to drain.
- Negative voltage applied to gate reduces the drain current
- This is called as 'normally ON' MOS.



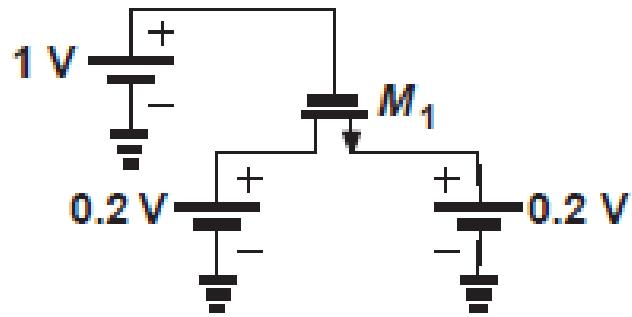
Determine the region of operation of  $M_1$  in each of the circuits shown in Fig.



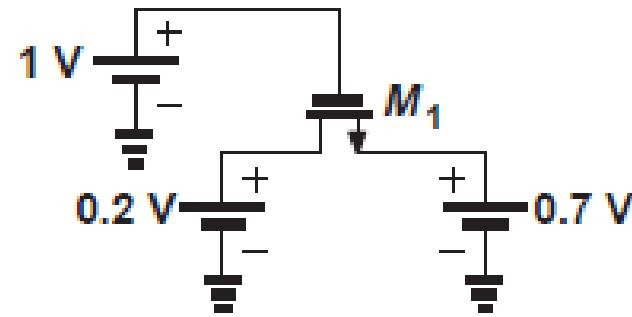
(a)



(b)

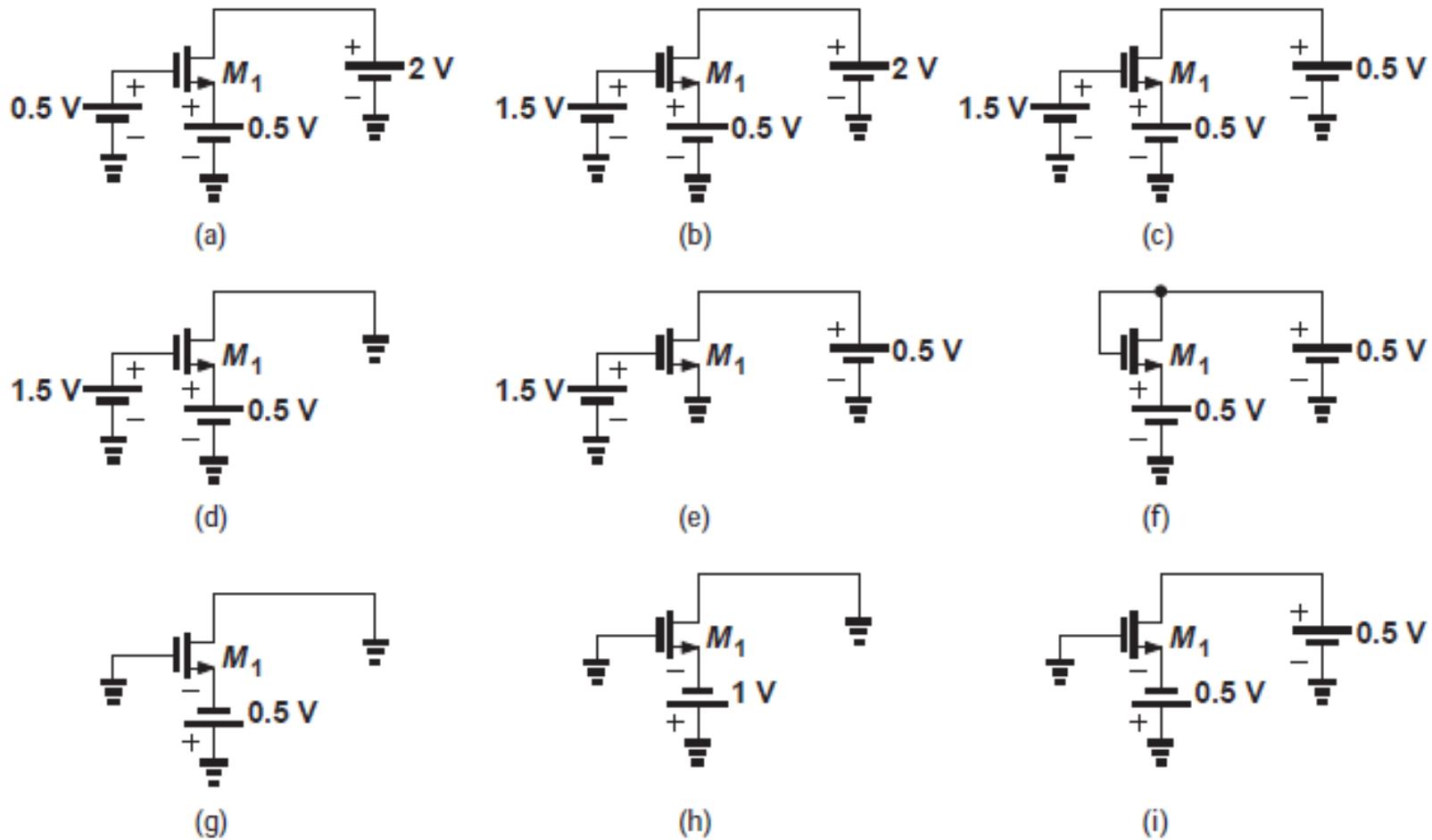


(c)



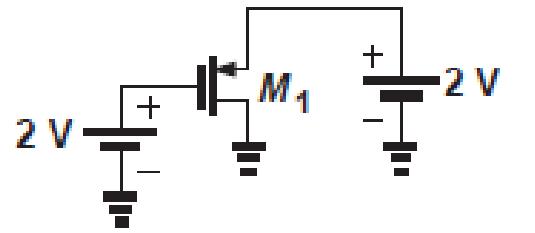
(d)

$V_{TH} = 0.4 \text{ V}$  for NMOS devices and  $-0.4 \text{ V}$  for PMOS devices.

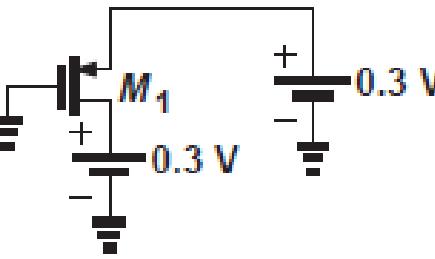


$V_{TH} = 0.4 \text{ V}$  for NMOS devices and  $-0.4 \text{ V}$  for PMOS devices.

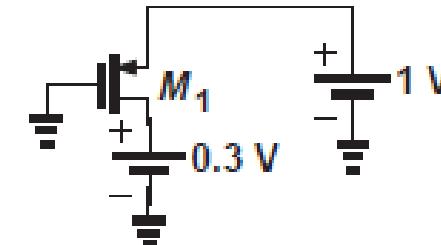
Determine the region of operation of  $M_1$  in each of the circuits shown in Fig.



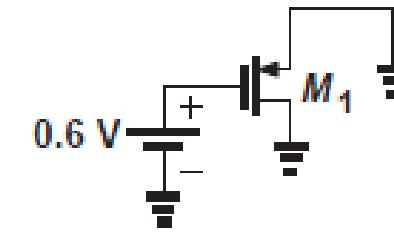
(a)



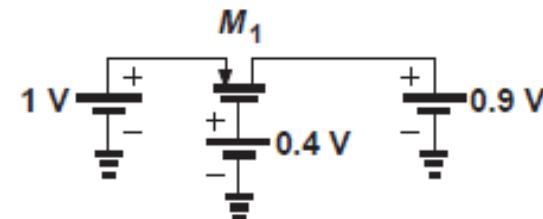
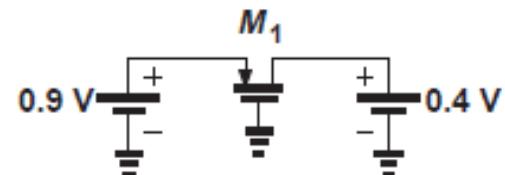
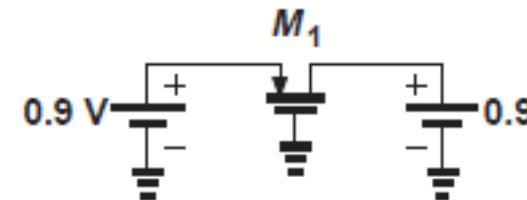
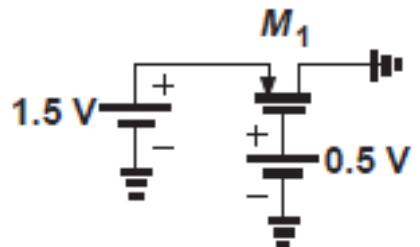
(b)



(c)



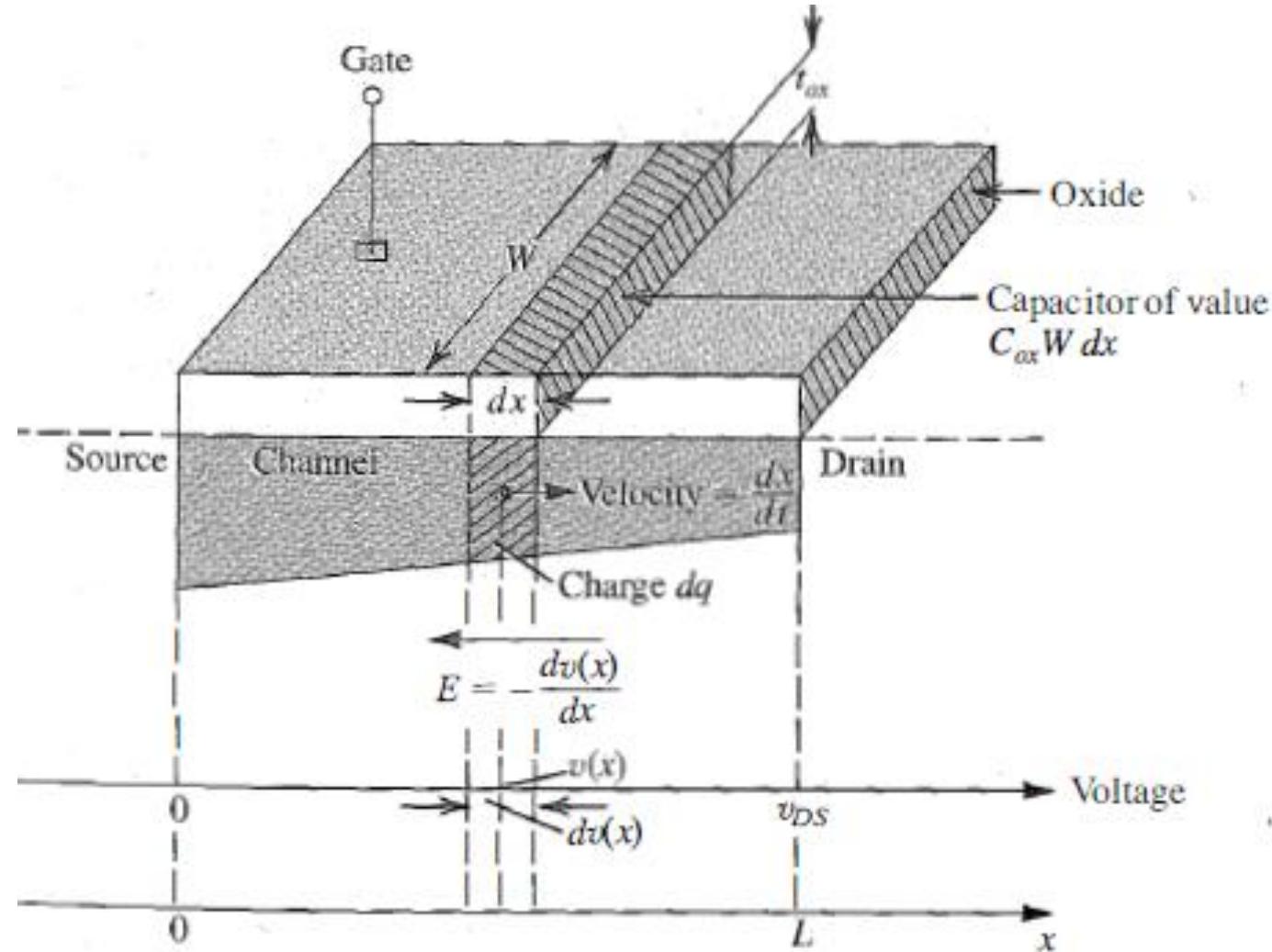
(d)



Current Derivation For Enhancement NMOS

**Follow Weste Book Convention**

# Drain to Source Current $I_{DS}$



the gate and the channel region form a parallel plate capacitor for which the oxide layer serves as a dielectric.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

consider the infinitesimal strip of the gate at distance  $x$  from the source. The capacitance of this strip is

$$C_{ox} W dx$$

To find the charge stored on this infinitesimal strip of the gate capacitance, we multiply the capacitance by the effective voltage between the gate and the channel at point  $x$ ,

$$V_{GS} - V(x) - V_t$$

Charge  $dq$  in the infinitesimal portion of the channel at point  $x$  is

$$dq = -C_{ox}Wdx[V_{GS} - V(x) - V_t]$$

Negative sign accounts for the fact that  $dq$  is a negative charge

The voltage  $V_{DS}$  produces an electric field along the channel in the negative  $x$  direction

$$E(x) = -\frac{dV(x)}{dx}$$

The electric field  $E(x)$  causes the electron charge  $dq$  to drift toward the drain with a velocity  $\frac{dx}{dt}$

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dx}$$

Where  $\mu_n$  is the mobility of electrons in the channel (called surface mobility).

The resulting drift current i

$$i = \frac{dq}{dt} = \frac{dq}{dx} \frac{dx}{dt}$$

$$i = -\mu_n C_{ox} W [V_{GS} - V(x) - V_t] \frac{dV(x)}{dx}$$

Thus  $i$  must be equal to the source-to-drain current. Since we are interested in the drain-to-source current  $i_D$ , we can find it as

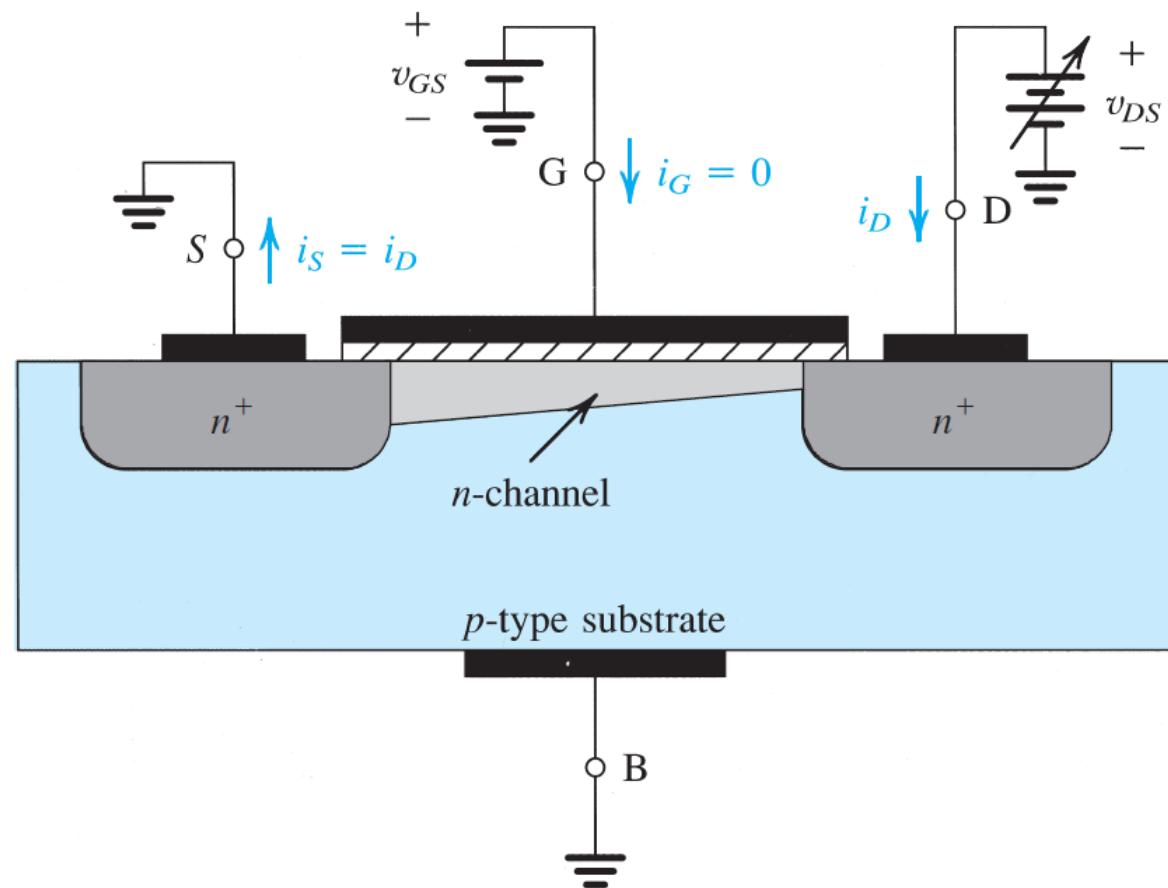
$$i_D = \mu_n C_{ox} W [V_{GS} - V(x) - V_t] \frac{dV(x)}{dx}$$

$$i_D dx = \mu_n C_{ox} W [V_{GS} - V(x) - V_t] dV(x)$$

Integrating both sides of this equation from  $x = 0$  to  $x = L$  and, correspondingly, for  $V(0) = 0$  to  $V(L) = V_{DS}$ ,

$$\int_0^L i_D dx = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{GS} - V(x) - V_t] dV(x)$$

$$I = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}]$$



# Drain to Source Current $I_{DS}$

$$C_G = \frac{\varepsilon_{ins} \varepsilon_0 W L}{t_{ox}}$$

$$K' = \frac{\mu C_G}{WL}$$

$$I_{DS} = \frac{C_G \mu}{L^2} \left( (V_{GS} - V_T) - \frac{V_{DS}}{2} \right) V_{DS}$$

$$C_G = C_{ox} WL$$

$$I_{DS} = \frac{C_{ox} \mu W}{L} \left( (V_{GS} - V_T) - \frac{V_{DS}}{2} \right) V_{DS}$$

Continued .....

# Drain to Source Current $I_{DS}$

Saturation Region  $V_{DS} \geq (V_{GS} - V_T)$

$$I_{DS} = K' \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2}$$

$$I_{DS} = \frac{K}{2} (V_{GS} - V_T)^2$$

$$I_{DS} = \frac{C_G \mu}{2L^2} (V_{GS} - V_T)^2$$

$$I_{DS} = \frac{C_0 \mu W}{2L} (V_{GS} - V_T)^2$$

# Current Summary

Current-voltage equations of the n-channel MOSFET :

$$I_D = 0, \quad \text{for } V_{GS} < V_T \quad (3.54)$$

$$I_D(\text{lin}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \begin{aligned} &\text{for } V_{GS} \geq V_T \\ &\text{and } V_{DS} < V_{GS} - V_T \end{aligned} \quad (3.55)$$

$$I_D(\text{sat}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \begin{aligned} &\text{for } V_{GS} \geq V_T \\ &\text{and } V_{DS} \geq V_{GS} - V_T \end{aligned} \quad (3.56)$$

Current-voltage equations of the p-channel MOSFET :

$$I_D = 0, \quad \text{for } V_{GS} > V_T \quad (3.57)$$

$$I_D(\text{lin}) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \begin{aligned} &\text{for } V_{GS} \leq V_T \\ &\text{and } V_{DS} > V_{GS} - V_T \end{aligned} \quad (3.58)$$

$$I_D(\text{sat}) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \begin{aligned} &\text{for } V_{GS} \leq V_T \\ &\text{and } V_{DS} \leq V_{GS} - V_T \end{aligned} \quad (3.59)$$

A 0.18- $\mu\text{m}$  fabrication process is specified to have  $t_{\text{ox}} = 4\text{nm}$ ,  $\mu_n = 450\text{cm}^2/\text{Vs}$  and  $V_T = 0.5\text{V}$ . Find the value of  $\mu_n C_{\text{ox}}$  (Also known as  $k_n'$  process transconductance) For a MOSFET with minimum length fabricated in this process, find the required value of  $W$  so that the device exhibits a channel resistance  $r_{\text{DS}}$  of 1K at  $V_{\text{GS}} = 1\text{V}$ . Given  $e_{\text{ox}} = 3.45 \times 10^{-11}\text{ F/m}^2$

$$K_n' = 388\mu\text{A/V}^2$$

$$W = 0.93\mu\text{m}$$

Consider a process technology for which  $L_{min} = 0.4 \mu\text{m}$ ,  $t_{ox} = 8 \text{ nm}$ ,  $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_t = 0.7 \text{ V}$ .

- (a) Find  $C_{ox}$  and  $K_n'$ .  $C_{ox} = 4.31 \times 10^{-3} \text{ F/m}^2$   $K_n' = 194.1 \mu\text{A/V}^2$
- (b) For a MOSFET with  $W/L = 8 \mu\text{m} / 0.8 \mu\text{m}$  calculate the values of  $V_{ov}$ ,  $V_{GS}$ , and  $V_{DSmin}$  needed to operate the transistor in the saturation region with a dc current  $I_D = 100 \mu\text{A}$ .  $V_{DSmin} = V_{ov} = 0.32 \text{ V}$   $V_{GS} = 1.015 \text{ V}$
- (c) For the device in (b), find the values of  $V_{ov}$  and  $V_{GS}$  required to cause the device to operate as a 1000-resistor for very small  $v_D$   $V_{ov} = 0.51 \text{ V}$   $V_{GS} = 1.215 \text{ V}$

Consider a process technology for which  $L_{\min} = 0.4 \mu\text{m}$ ,  $t_{ox} = 8 \text{ nm}$ ,  $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_t = 0.7 \text{ V}$ .

- Find  $C_{ox}$  and  $k'_n$ .
- For a MOSFET with  $W/L = 8 \mu\text{m}/0.8 \mu\text{m}$ , calculate the values of  $V_{ov}$ ,  $V_{GS}$ , and  $V_{DSmin}$  needed to operate the transistor in the saturation region with a dc current  $I_D = 100 \mu\text{A}$ .
- For the device in (b), find the values of  $V_{ov}$  and  $V_{GS}$  required to cause the device to operate as a  $1000\text{-}\Omega$  resistor for very small  $v_{DS}$ .

### Solution

(a)

$$\begin{aligned}C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3} \text{ F/m}^2 \\&= 4.32 \text{ fF}/\mu\text{m}^2\end{aligned}$$

$$\begin{aligned}k'_n &= \mu_n C_{ox} = 450 (\text{cm}^2/\text{V}\cdot\text{s}) \times 4.32 (\text{fF}/\mu\text{m}^2) \\&= 450 \times 10^8 (\mu\text{m}^2/\text{V}\cdot\text{s}) \times 4.32 \times 10^{-15} (\text{F}/\mu\text{m}^2) \\&= 194 \times 10^{-6} (\text{F}/\text{V}\cdot\text{s}) \\&= 194 \mu\text{A/V}^2\end{aligned}$$

(b) For operation in the saturation region,

$$i_D = \frac{1}{2} k'_n \frac{W}{L} v_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} V_{OV}^2$$

which results in

$$V_{OV} = 0.32 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 1.02 \text{ V}$$

and

$$V_{DSmin} = V_{OV} = 0.32 \text{ V}$$

(c) For the MOSFET in the triode region with  $v_{DS}$  very small,

$$r_{DS} = \frac{1}{k' n \frac{W}{L} V_{OV}}$$

Thus

$$1000 = \frac{1}{194 \times 10^{-6} \times 10 \times V_{OV}}$$

which yields

$$V_{OV} = 0.52 \text{ V}$$

Thus,

$$V_{GS} = 1.22 \text{ V}$$

Q. For a 0.8- $\mu\text{m}$  process technology for which  $t_{ox} = 15 \text{ nm}$  and  $\mu_n = 550 \text{ cm}^2/\text{V}\cdot\text{s}$ , find  $C_{ox}$ ,  $K'_n$ , and the overdrive voltage  $V_{ov}$  required to operate a transistor having  $W/L=20$  in saturation with  $I_D = 0.2 \text{ mA}$ . What is the minimum value of  $V_{DS}$  needed?

$$C_{ox} = 2.301 \times 10^{-3} \text{ F/m}^2 \quad K'_n = 126.5 \mu\text{A/V}^2 \quad V_{DSmin} = V_{ov} = .397 \text{ V} \approx 0.4 \text{ V}$$

Q. A circuit designer intending to operate a MOSFET in saturation is considering the effect of changing the device dimensions and operating voltages on the drain current  $I_D$ . Specifically, by what factor does  $I_D$  change in each of the following cases?

- (a) The channel length is doubled.
- (b) The channel width is doubled.
- (c) The overdrive voltage is doubled.
- (d) The drain-to-source voltage is doubled.

**Ans. 0.5; 2; 4; no change**

Q. An enhancement type NMOS transistor with  $V_t = 0.7V$  has its source terminal grounded and a 1.5-V DC is applied to the gate. In what region does the device operate :for (a)  $V_D = +0.5 V$  (b)  $V_D = +0.9 V$  (c)  $V_D = +3 V$

If the NMOS device in  $\mu_nC_{ox} = 100 \mu\text{A/V}^2$  ,  $W = 10 \mu\text{m}$ , and  $L = 1 \mu\text{m}$ , find the value of drain current that results in each of the three cases (a), (b), and (c).

- (a) Non Sat<sup>n</sup>→275 μA
- (b) Sat<sup>n</sup>→320 μA
- (c) Sat<sup>n</sup>→320 μA

## Examples:

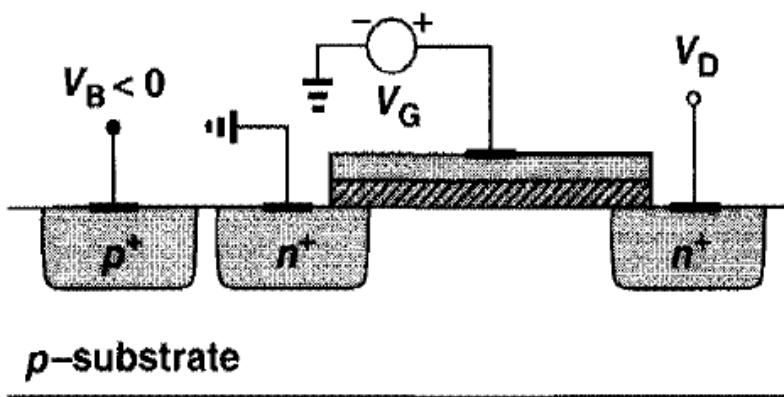
1. Consider an n-MOSFET that has a gate oxide thickness  $t_{ox}=12$  nm and an electron mobility of  $\mu_n=540 \text{ cm}^2/\text{V}\cdot\text{sec}$ . Find the process transconductance.
2. An n-MOSFET with  $W=20 \mu\text{m}$  and  $L=0.5 \mu\text{m}$  is built in a process where  $k'_n=120 \mu\text{A}/\text{V}^2$  and  $V_{Tn}=0.65 \text{ V}$ . The voltages are set to a value of  $V_{GS} = V_{DS} = 5 \text{ V}$ .
  - (a) Is the transistor saturated or non-saturated?
3. Consider an n-MOSFET with the following characteristics:  
 $t_{ox}=10 \text{ nm}$ ,  $\mu_n=520 \text{ cm}^2/\text{V}\cdot\text{sec}$ ,  $W/L=8$ ,  $V_{Tn}=0.7 \text{ V}$ 
  - (a) Calculate the drain current for  $V_{GS}=2 \text{ V}$ ,  $V_{DS}= 2 \text{ V}$ .
  - (b) If the voltage values are  $V_{DS}=1.2 \text{ V}$  and  $V_{GS}=2 \text{ V}$ , find the operating region and current
4. Consider an n-MOSFET where  $V_{Ton}=0.7 \text{ V}$ ,  $\gamma=0.08 \text{ V}^{1/2}$  and  $2|Φ_F|=0.58 \text{ V}$ . Calculate the threshold voltage for the given body-bias voltage  $V_{SB} = 1 \text{ V}$ ,  $2 \text{ V}$  and  $3 \text{ V}$ .
5. An n-MOSFET has a gate oxide with a thickness of  $t_{ox}=120 \text{ Å}$ . The p-type bulk region is Doped with boron at a density of  $N_a=8\times10^{14} / \text{cm}^3$ . It is given that  $V_{Ton}=0.55 \text{ V}$ . Calculate the body-bias coefficient  $\gamma$ .

# Second-order Effects

- Body Effect.
- Sub threshold conduction
- Channel length modulation
- Mobility variation
- Fowler-Nordheim tunneling
- Drain punchthrough
- Impact Ionization-Hot electrons.

# Body Effect

What happens if the bulk voltage of an N-MOSFET drops below the source voltage ?



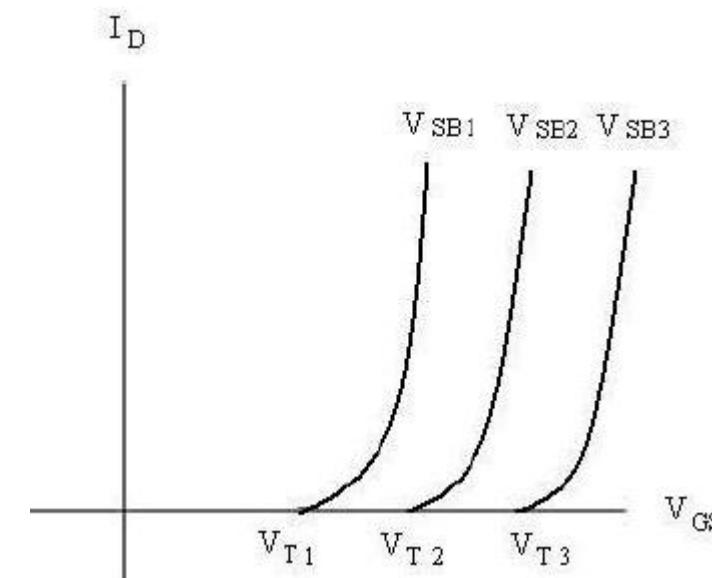
$$V_{TH} = V_{TH0} + \gamma \left( \sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right)$$

$$\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$

$$V_{TH0} = \varphi_{MS} + 2\varphi_F + \frac{Q_{Dep}}{C_{OX}}$$

where  $\varphi_{MS}$  is the difference between the work functions of the polysilicon gate and the silicon substrate

$\varphi_F$ = Fermi potential



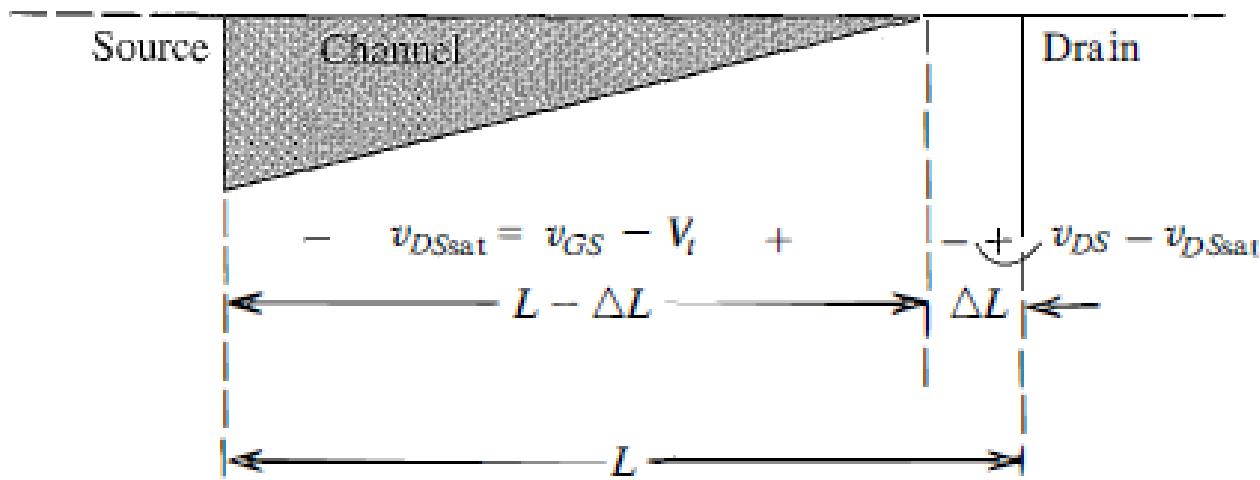
# Sub threshold conduction

For  $V_{GS} \approx V_{TH}$ , a "weak" inversion layer still exists and some current flows from D to S. Even for  $V_{GS} < V_{TH}$ ,  $I_D$  is finite, but it exhibits an *exponential* dependence on  $V_{GS}$ . Called "subthreshold conduction". This effect can be formulated for  $V_{DS}$  greater than roughly 200 mV as

$$I_D = I_0 \exp \frac{V_{GS}}{\xi V_T},$$

$\xi > 1$  is a nonideality factor

# Channel length modulation



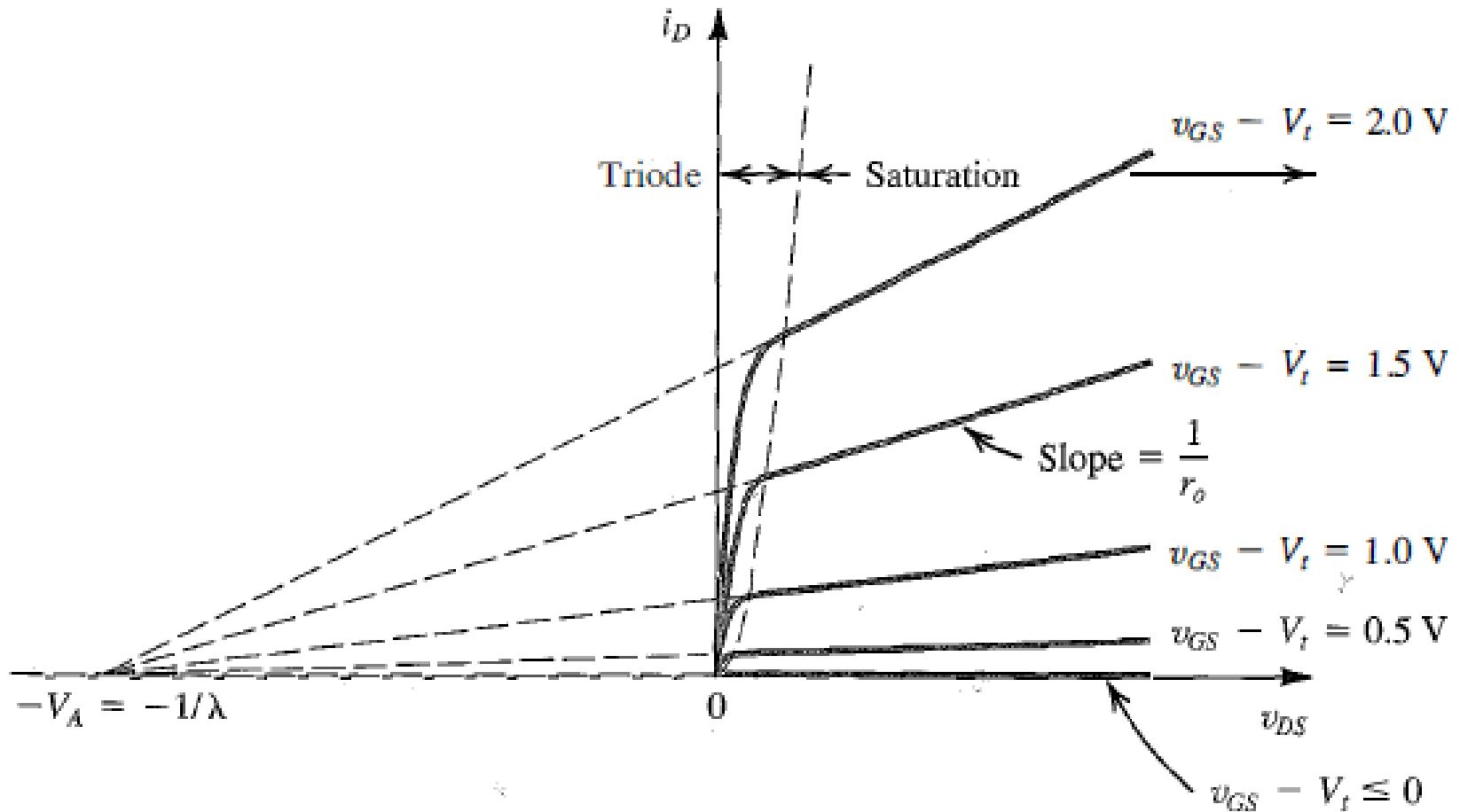
$$\begin{aligned}
 i_D &= \frac{1}{2} k'_n \frac{W}{L - \Delta L} (v_{GS} - V_t)^2 \\
 &= \frac{1}{2} k'_n \frac{W}{L} \frac{1}{1 - (\Delta L/L)} (v_{GS} - V_t)^2 \\
 &\approx \frac{1}{2} k'_n \frac{W}{L} \left(1 + \frac{\Delta L}{L}\right) (v_{GS} - V_t)^2 \\
 \Delta L &= \lambda' v_{DS}
 \end{aligned}$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} \left(1 + \frac{\lambda'}{L} v_{DS}\right) (v_{GS} - V_t)^2$$

$$\lambda = \frac{\lambda'}{L}$$

$\lambda$  is a process-technology parameter  
with the dimensions of  $V^{-1}$

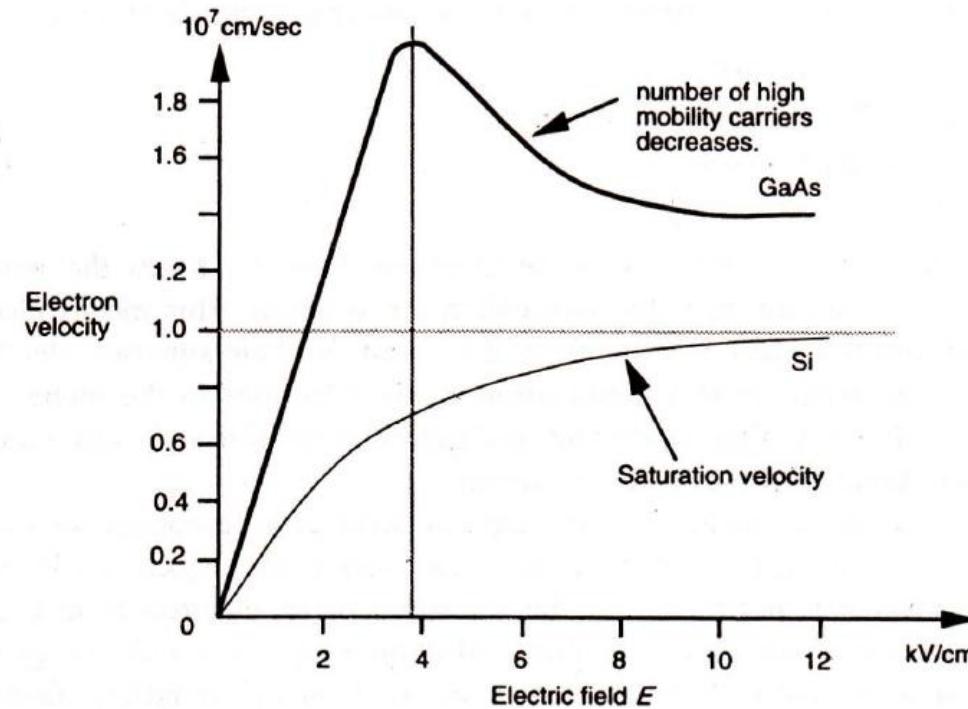
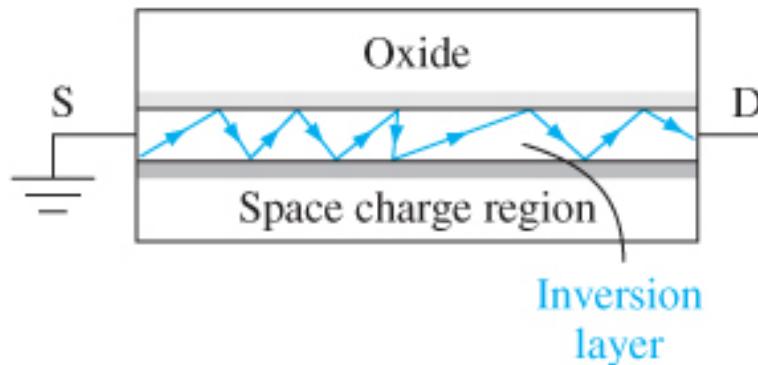
$$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$



$V_A$  is a process-technology parameter with the dimensions of V.

# Mobility variation

Mobility is defined as the ease with which the charge carriers drift in the substrate material. Mobility decreases with increase in doping concentration and increase in temperature. Mobility is the ratio of average carrier drift velocity and electric field. Mobility is represented by the symbol  $\mu$ .



# Fowler Nordhiem tunneling:

When the gate oxide is very thin there can be a current between gate and source or drain by electron tunneling through the gate oxide. This current is proportional to the area of the gate of the transistor.

# Drain punchthrough

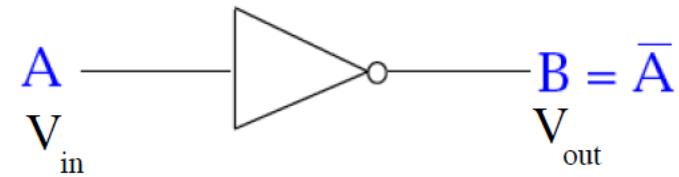
When the drain is at a high voltage, the depletion region around the drain may extend to the source, causing the current to flow even if the gate voltage is zero. This is known as Punchthrough condition.

# Impact Ionization-Hot electrons

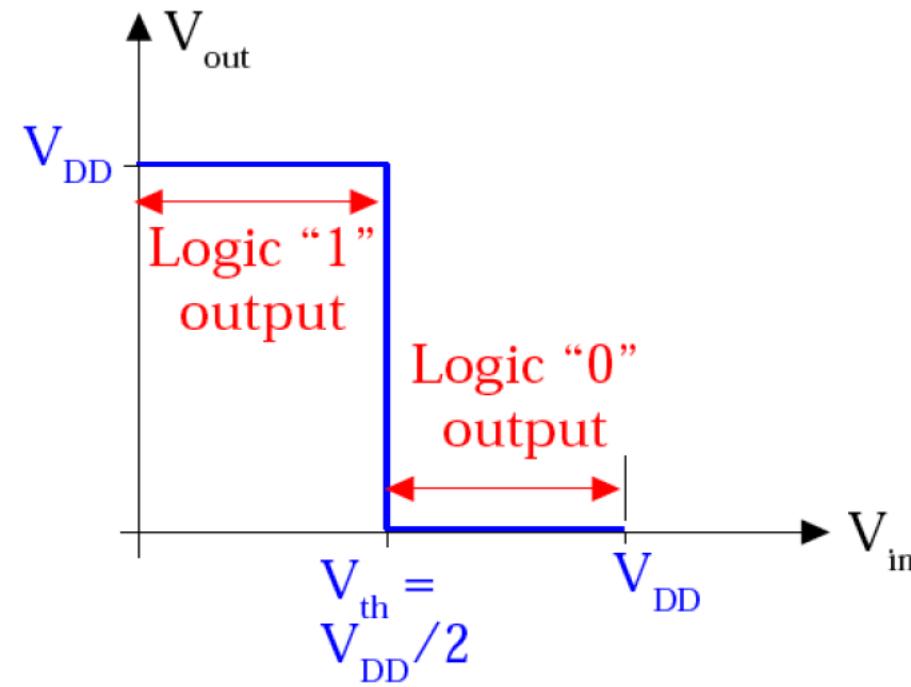
When the length of the transistor is reduced, the electric field at the drain increases. The field can become so high that electrons are imparted with enough energy we can term them as hot. These hot electrons impact the drain, dislodging holes that are then swept toward the negatively charged substrate and appear as a substrate current. This effect is known as Impact Ionization.

# Inverters

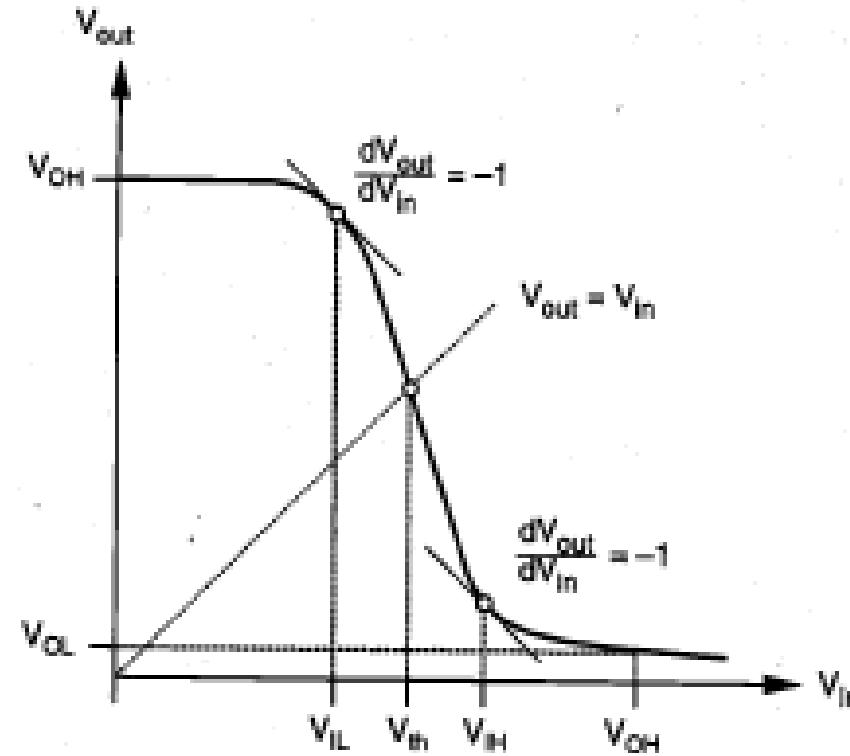
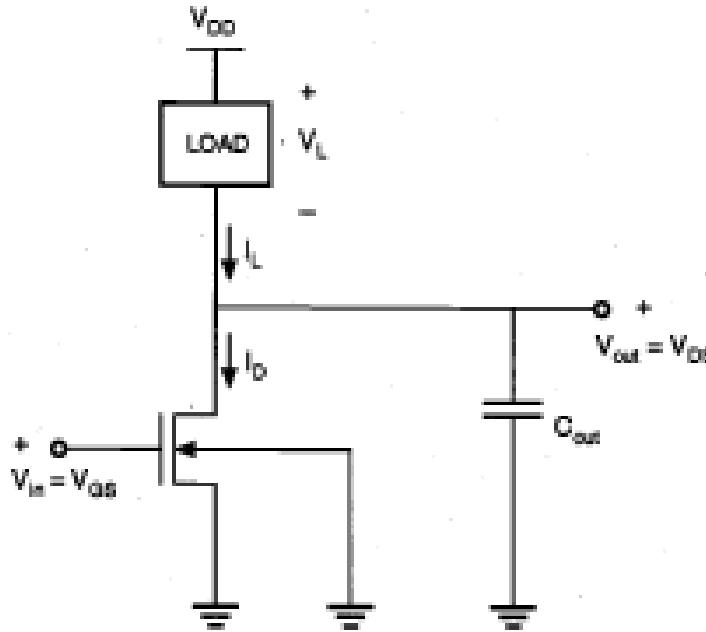
# Inverters



A	B
0	1
1	0



# Inverters



$V_{OH}$ : Maximum output voltage when the output level is logic "1"

$V_{OL}$ : Minimum output voltage when the output level is logic "0"

$V_{IL}$ : Maximum input voltage which can be *interpreted* as logic "0"

$V_{IH}$ : Minimum input voltage which can be *interpreted* as logic "1"

# Inverters

- ❖ Resistive Load Inverter
- ❖ Enhancement-load Inverter
- ❖ Depletion-load Inverter
- ❖ CMOS Inverter

# Inverters

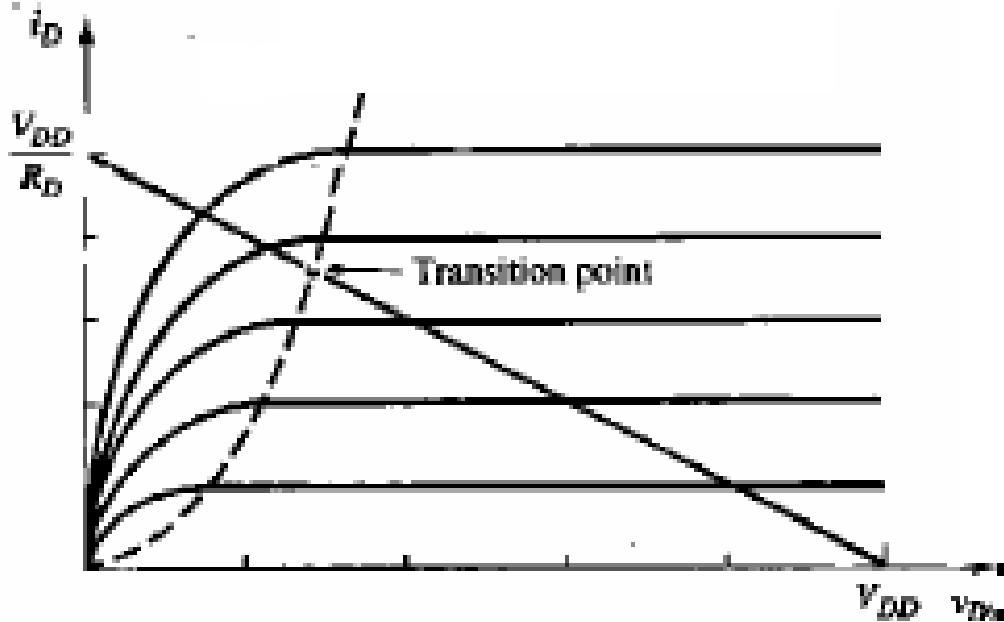
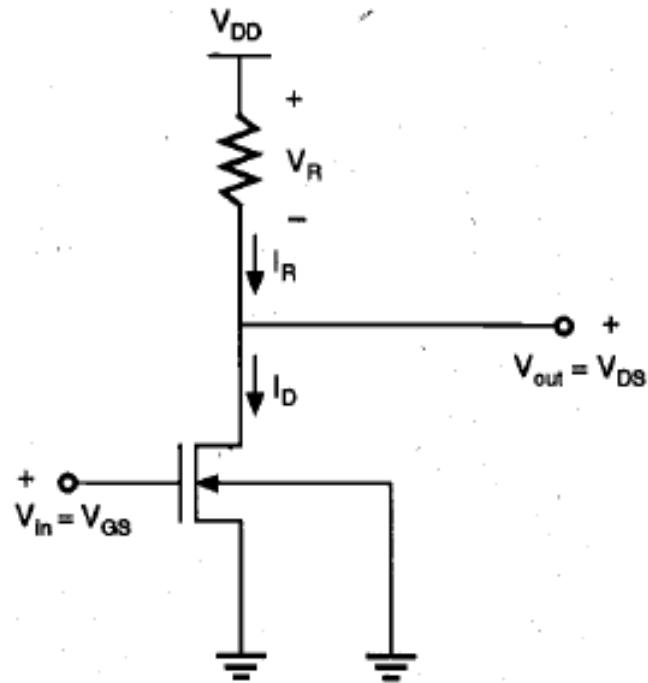
$V_{OH}$ : Maximum output voltage when the output level is logic "1"

$V_{OL}$ : Minimum output voltage when the output level is logic "0"

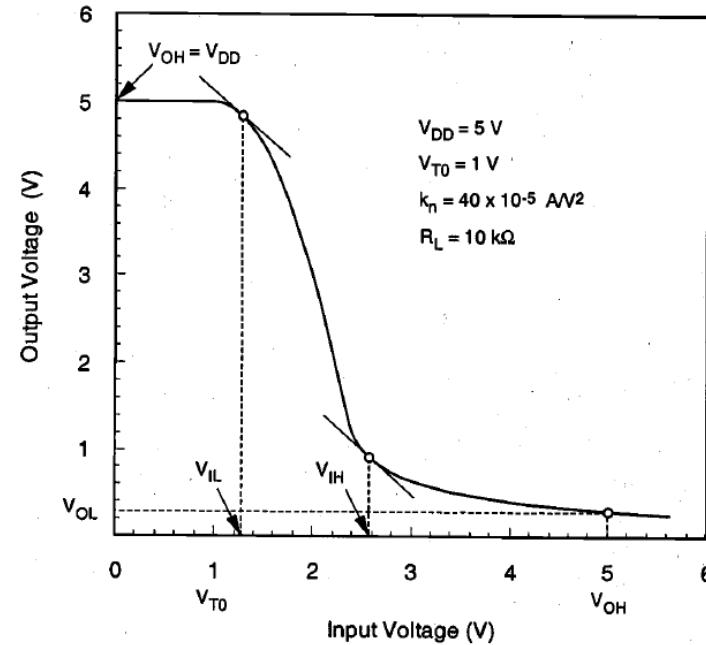
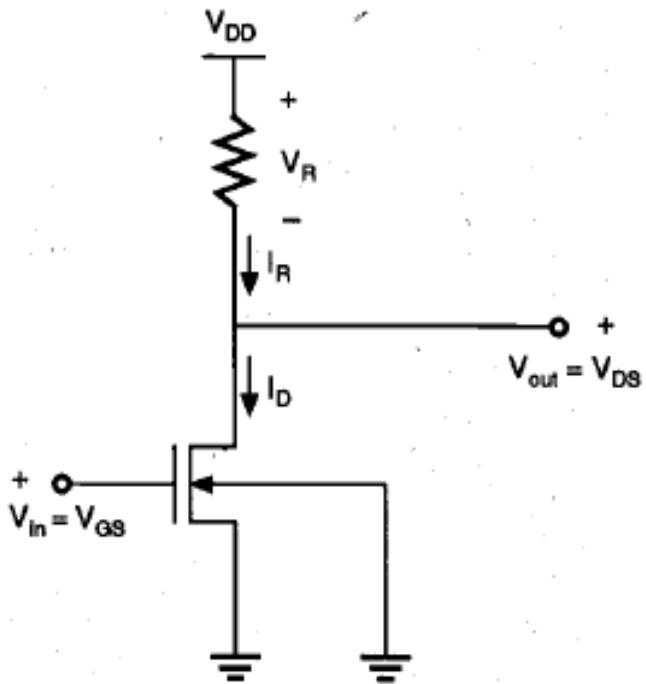
$V_{IL}$ : Maximum input voltage which can be *interpreted* as logic "0"

$V_{IH}$ : Minimum input voltage which can be *interpreted* as logic "1"

# Resistive Load Inverter



# Resistive-load Inverters



Saturation Current:

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

Linear Current:

$$I_R = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2]$$

Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	cut-off
$V_{T0} \leq V_{in} < V_{out} + V_{T0}$	saturation
$V_{in} \geq V_{out} + V_{T0}$	linear

# Resistive-load Inverters

**V<sub>OH</sub>**

$$V_{out} = V_{DD} - R_L \cdot I_R$$

$$V_{OH} = V_{DD}$$

**V<sub>OL</sub>**

$$I_R = \frac{V_{DD} - V_{out}}{R_L}$$

Using KCL for the output node, i.e.,  $I_R = I_D$ , we can write the following equation:

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{DD} - V_{T0}) \cdot V_{OL} - V_{OL}^2]$$

$$V_{OL}^2 - 2 \cdot \left( V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right) \cdot V_{OL} + \frac{2}{k_n R_L} \cdot V_{DD} = 0$$

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left( V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$

# Resistive-load Inverters

**V<sub>IL</sub>**

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

Differentiate w.r.t. V =

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = k_n \cdot (V_{in} - V_{T0})$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

$$\begin{aligned} V_{out}(V_{in} = V_{IL}) &= V_{DD} - \frac{k_n R_L}{2} \cdot \left( V_{T0} + \frac{1}{k_n R_L} - V_{T0} \right)^2 \\ &= V_{DD} - \frac{1}{2 k_n R_L} \end{aligned}$$

**V<sub>IH</sub>**

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2]$$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \cdot \left[ 2 \cdot (V_{in} - V_{T0}) \cdot \frac{dV_{out}}{dV_{in}} + 2 V_{out} - 2 V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$V_{IH} = V_{T0} + 2 V_{out} - \frac{1}{k_n R_L}$$

# Resistive-load Inverters

**V<sub>IH</sub>**

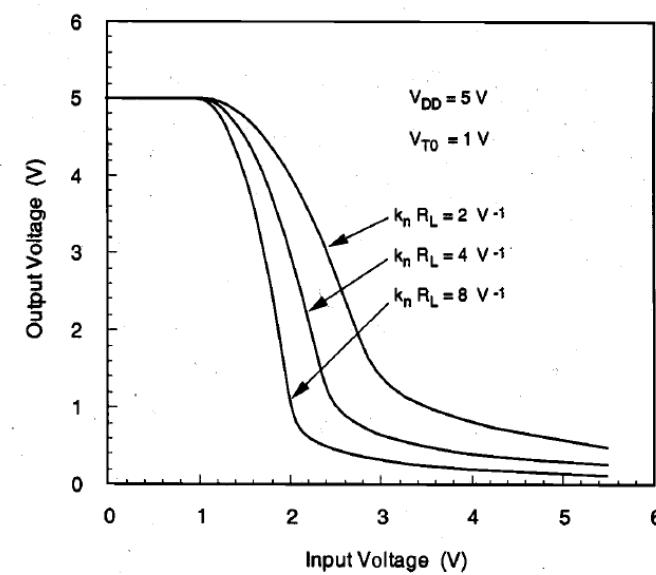
$$V_{IH} = V_{T0} + 2V_{out} - \frac{1}{k_n R_L}$$

Utilize  $\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2]$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot \left[ 2 \cdot \left( V_{T0} + 2V_{out} - \frac{1}{k_n R_L} - V_{T0} \right) \cdot V_{out} - V_{out}^2 \right]$$

$$V_{out} (V_{in} = V_{IH}) = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$



Consider a resistive-load inverter circuit with  $V_{DD} = 5$  V,  $k_n' = 20 \mu\text{A/V}^2$ ,  $V_{T0} = 0.8$  V,  $R_L = 200 \text{ k}\Omega$ , and  $W/L = 2$ . Calculate the critical voltages ( $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ ,  $V_{IH}$ ) on the VTC and find the noise margins of the circuit.

**Solution:**

$$V_{OH} = V_{DD} = 5 \text{ V}$$

Note that in this resistive-load inverter example, the transconductance of the driver transistor is  $k_n = k_n' (W/L) = 40 \mu\text{A/V}^2$  and, hence,  $(k_n R_L) = 8 \text{ V}^{-1}$ .

$$\begin{aligned} V_{OL} &= V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left( V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right)^2 - \frac{2 V_{DD}}{k_n R_L}} \\ &= 5 - 0.8 + \frac{1}{8} - \sqrt{\left( 5 - 0.8 + \frac{1}{8} \right)^2 - \frac{2 \cdot 5}{8}} \\ &= 0.147 \text{ V} \end{aligned}$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L} = 0.8 + \frac{1}{8} = 0.925 \text{ V}$$

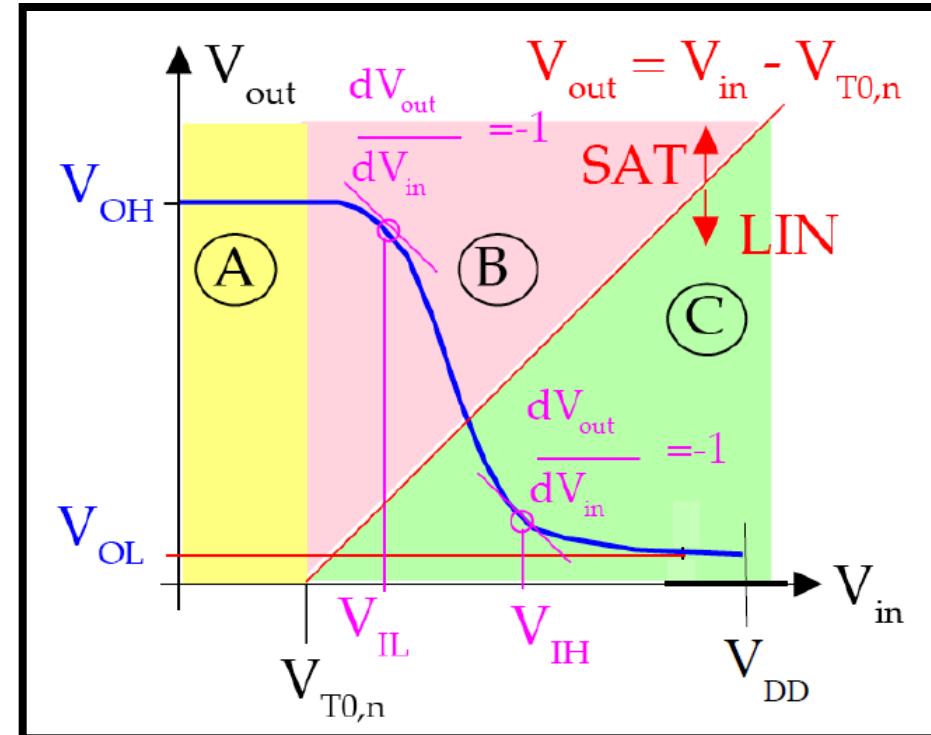
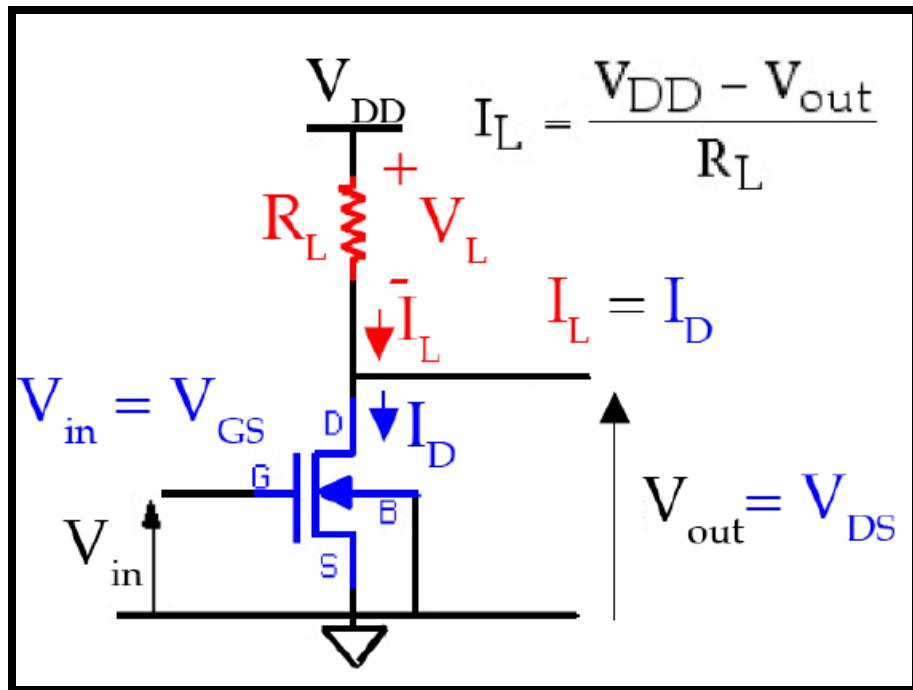
$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} = 0.8 + \sqrt{\frac{8}{3} \cdot \frac{5}{8}} - \frac{1}{8} = 1.97 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.93 - 0.15 = 0.78 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.97 = 3.03 \text{ V}$$

For better noise immunity, the  $NM_L$  should be at least about 25% of the power supply voltage  $VDD$ , i.e., about 1.25 V.

# Resistive-load Inverters

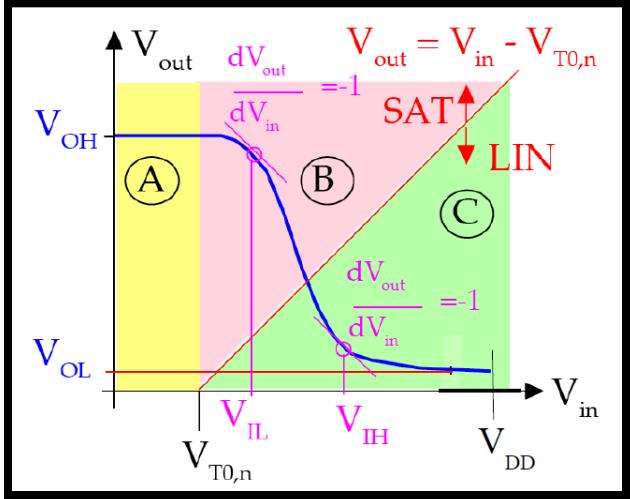
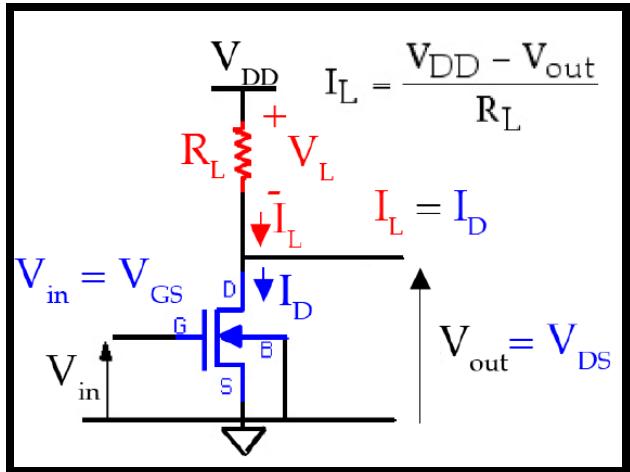


$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}}$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

# Resistive-load Inverters



$$V_{in} = V_{out} = V_{th} \Rightarrow V_{DS} = V_{GS} > V_{GS} - V_{T0,n} \longrightarrow B$$

$$I_L = I_D \rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} (V_{in} - V_{T0,n})^2$$

$$\frac{V_{DD} - V_{th}}{R_L} = \frac{k_n}{2} (V_{th} - V_{T0,n})^2$$

$$V_{th}^2 - 2 \left( V_{T0,n} - \frac{1}{k_n R_L} \right) V_{th} + V_{T0,n}^2 - \frac{2 V_{DD}}{k_n R_L} = 0$$

$$V_{th} = V_{T0,n} - \frac{1}{k_n R_L} \pm \sqrt{\left( V_{T0,n} - \frac{1}{k_n R_L} \right)^2 + \frac{2 V_{DD}}{k_n R_L} - V_{T0,n}^2}$$

## SUMMARY - RESISTIVE LOAD INVERTER

$$\rightarrow V_{th} = V_{T0,n} - \frac{1}{k_n R_L} + \sqrt{\left(V_{T0,n} - \frac{1}{k_n R_L}\right)^2 + \frac{2V_{DD}}{k_n R_L} - V_{T0,n}^2}$$

$$\rightarrow V_{IL} = V_{T0,n} + \frac{1}{k_n R_L} \quad V_{out}(V_{in} = V_{IL}) = V_{DD} - \frac{1}{2k_n R_L}$$

$$\rightarrow V_{IH} = V_{T0,n} + 2\sqrt{\frac{2V_{DD}}{3k_n R_L}} - \frac{1}{k_n R_L} \quad V_{out}(V_{in} = V_{IH}) = \sqrt{\frac{2V_{DD}}{3k_n R_L}}$$


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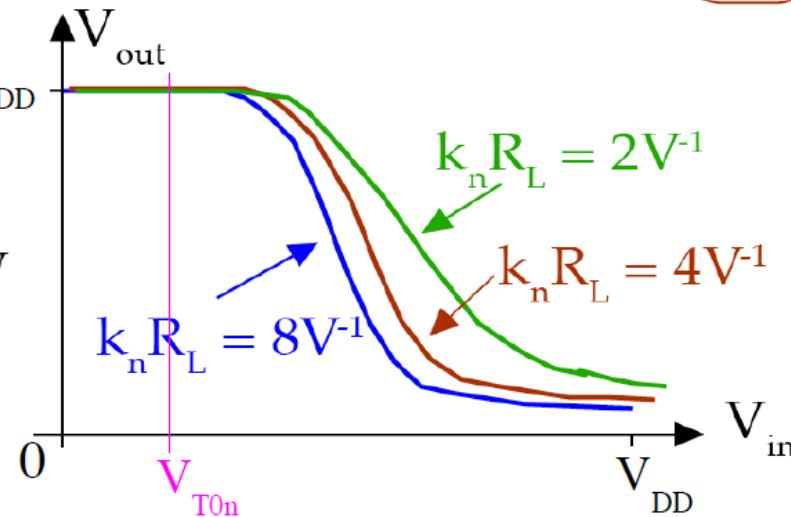

$$\rightarrow V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} \pm \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L} V_{DD}}$$

$$\rightarrow V_{OH} = V_{DD}$$

Units

$$\begin{aligned} V_{DD} &= 5V \\ V_{T0,n} &= 1V \end{aligned}$$

$$k_n R_L = \left( \frac{A}{V^2} \right) \left( \frac{V}{A} \right) = V^{-1}$$



Take Limit as  $k_n R_L \rightarrow \infty$

$$V_{th} = V_{T0,n} - \frac{1}{k_n R_L} + \sqrt{\left(V_{T0,n} - \frac{1}{k_n R_L}\right)^2 + \frac{2V_{DD}}{k_n R_L} - V_{T0,n}^2} \rightarrow V_{T0n}$$

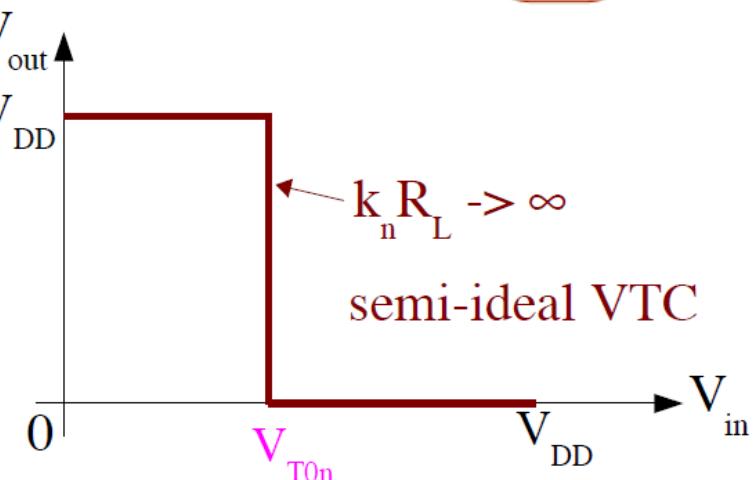
$$V_{IL} = V_{T0,n} + \frac{1}{k_n R_L} \rightarrow V_{T0n}$$

$$V_{III} = V_{T0,n} + 2\sqrt{\frac{2V_{DD}}{3k_n R_L} - \frac{1}{k_n R_L}} \rightarrow V_{T0n}$$

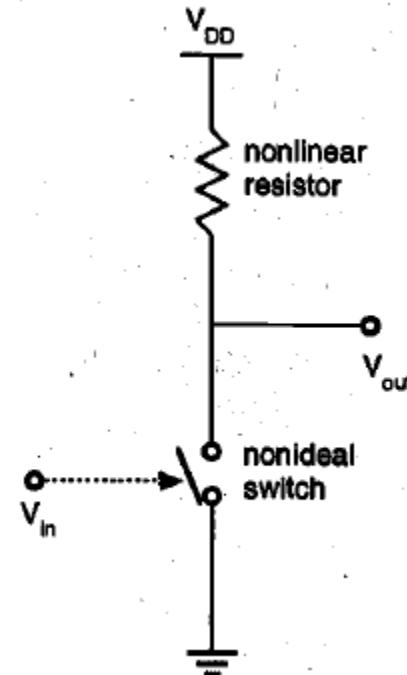
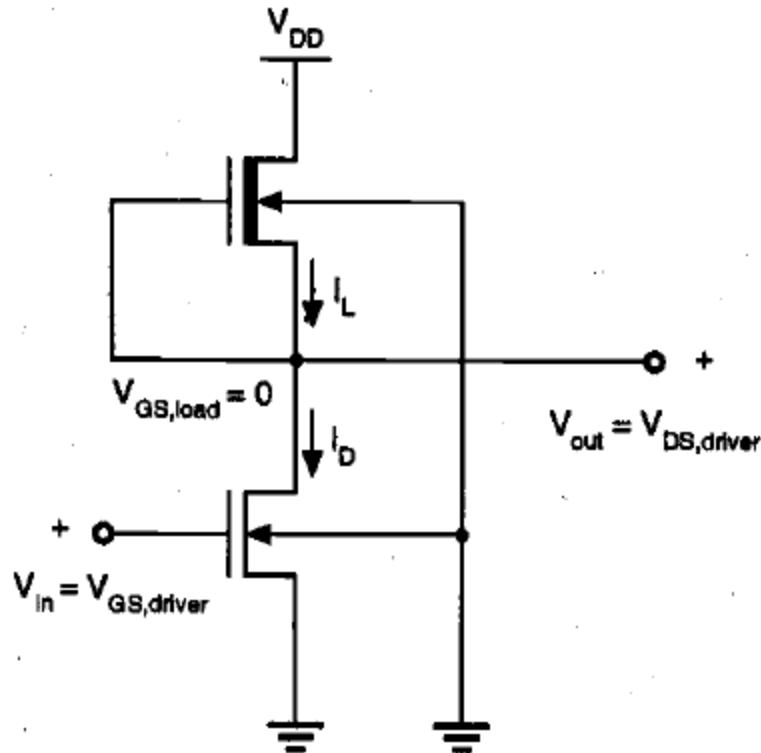
$$V_{OL} = V_{DD} - V_{T0,n} + \frac{1}{k_n R_L} \pm \sqrt{\left(V_{DD} - V_{T0,n} + \frac{1}{k_n R_L}\right)^2 - \frac{2}{k_n R_L} V_{DD}} \rightarrow 0$$

Units

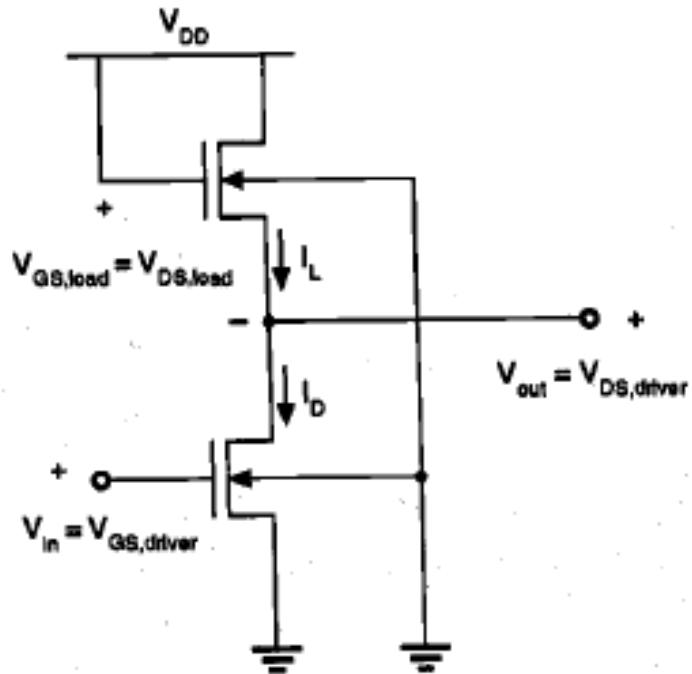
$$k_n R_L = \left(\frac{A}{V^2}\right) \left(\frac{V}{A}\right) = V^{-1}$$



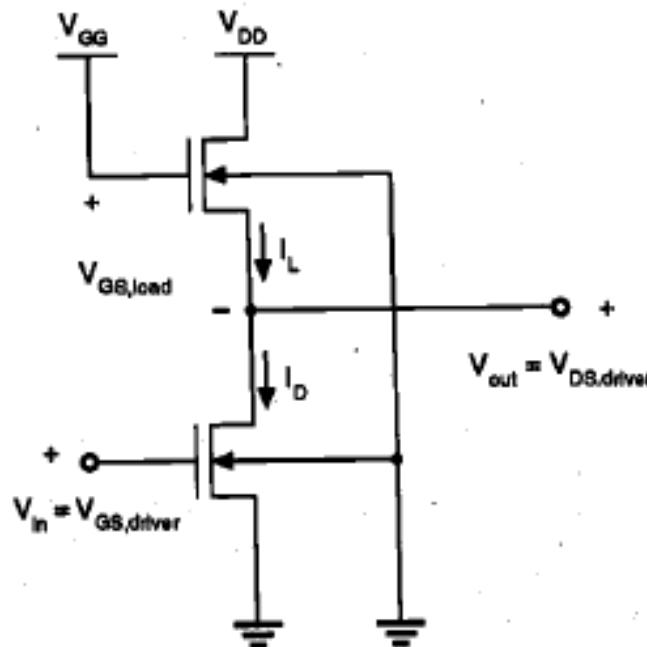
# Depletion Load NMOS Inverter



# Enhancement load NMOS inverter

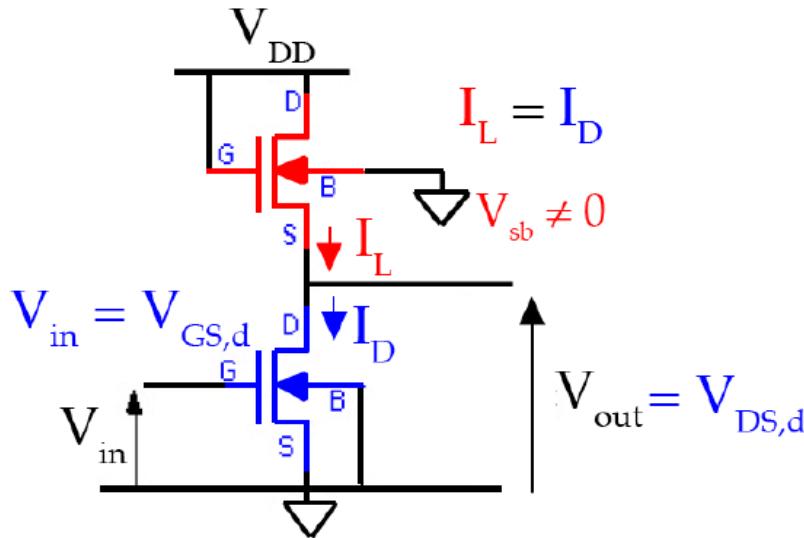


(A)



(B)

# SATURATED NMOS ENHANCEMENT-LOAD INVERTER



Load  $\rightarrow$  Sat, Driver  $\rightarrow$  Cutoff (A)  $V_{OH}$

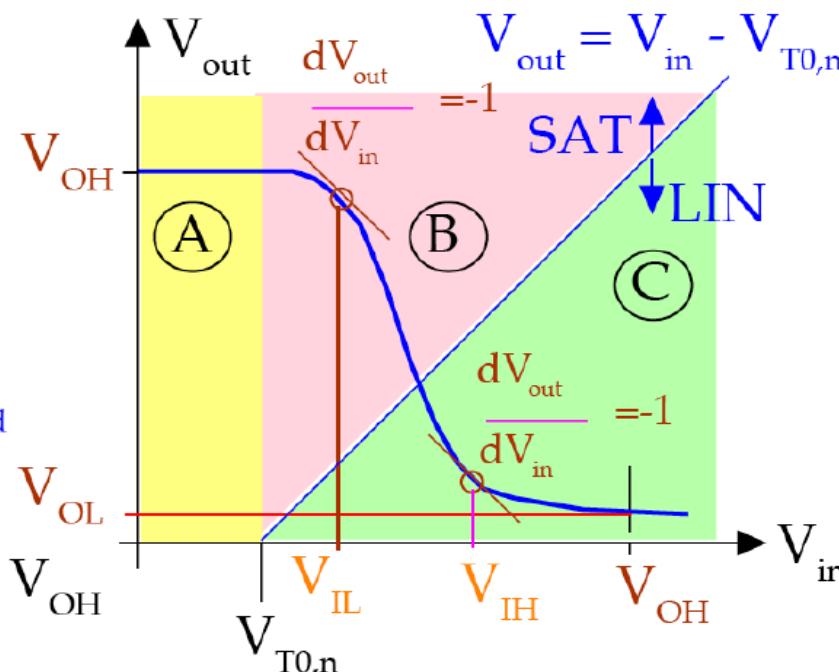
$$\frac{k_n}{2} \left( \frac{W}{L} \right)_L (V_{DD} - V_{out} - V_{T,L})^2 = 0$$

Load  $\rightarrow$  Sat, Driver  $\rightarrow$  Sat (B)  $V_{IL}$

$$\frac{k_n}{2} \left( \frac{W}{L} \right)_L (V_{DD} - V_{out} - V_{T,L})^2 = \frac{k_n}{2} \left( \frac{W}{L} \right)_d (V_{in} - V_{T0,n})^2$$

Load  $\rightarrow$  Sat, Driver  $\rightarrow$  Lin (C)  $V_{IH}, V_{OL}$

$$\frac{k_n}{2} \left( \frac{W}{L} \right)_L (V_{DD} - V_{out} - V_{T,L})^2 = \frac{k_n}{2} \left( \frac{W}{L} \right)_d (2[V_{in} - V_{T0,n}]V_{out} - V_{out}^2)$$



$$\begin{cases} V_{OH} < V_{DD} \\ V_{OL} > 0 \end{cases}$$

# Examples

Q1. Consider a resistive-load inverter circuit with  $V_{DD}=5$  V,  $k'n= 20 \mu\text{A}/\text{V}^2$ ,  $V_{t0}= 0.8$  V,  $R_L= 200 \text{ k}\Omega$ , and  $W/L = 2$ . Calculate the critical voltages- $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ ,  $V_{IH}$  find the noise margins of the circuit.

Q2. Determine the value of ( $W/L$ ) of nMOS for resistive load inverter, if

$$V_{OL}=0.6\text{V}, R=10 \text{ k}\Omega, V_{DD}=5\text{V}, V_{th,n}=1\text{V}, \mu_n C_{ox}=22\mu\text{A}/\text{V}^2$$

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left( V_{DD} - V_{T0} + \frac{1}{k_n R_L} \right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}}$$

# THE nMOS INVERTER

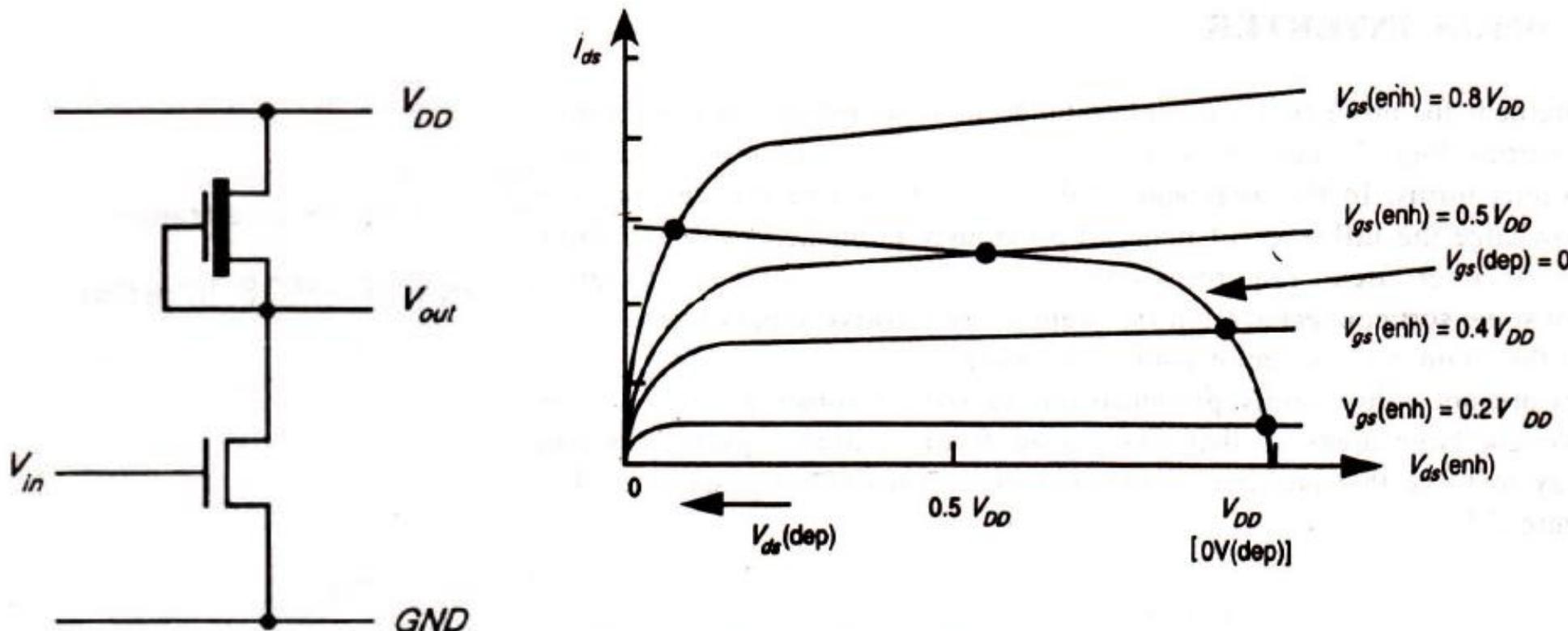
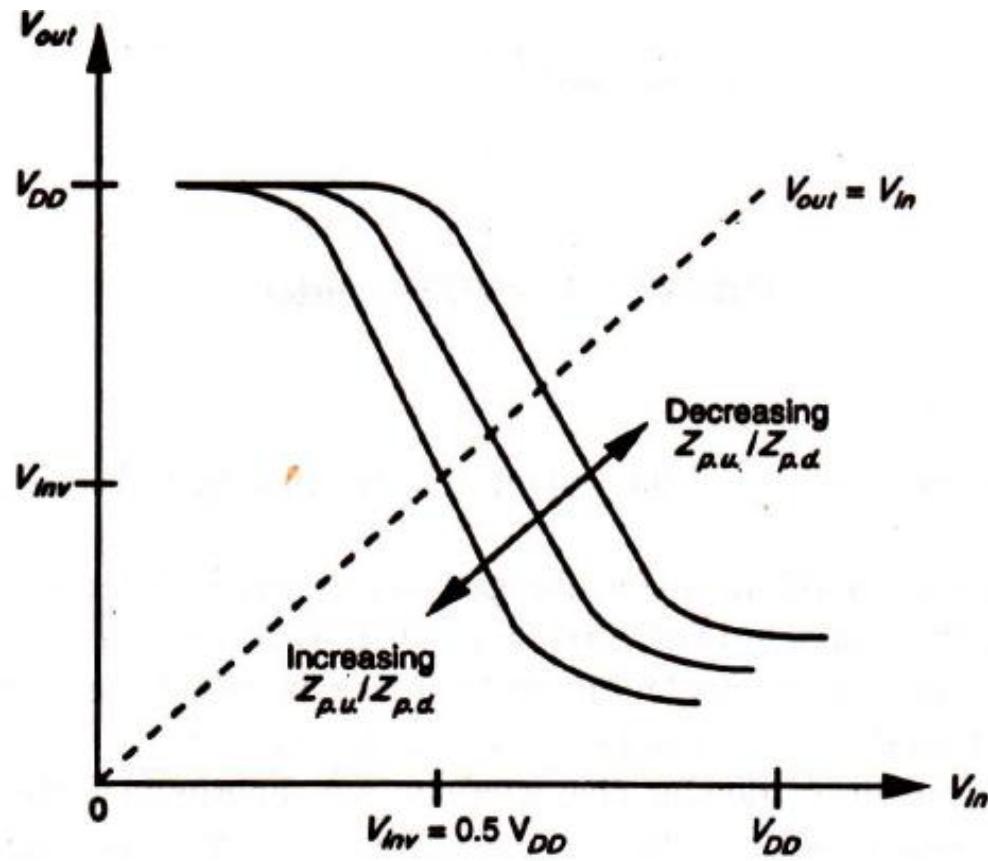


FIGURE 2.5 nMOS inverter.

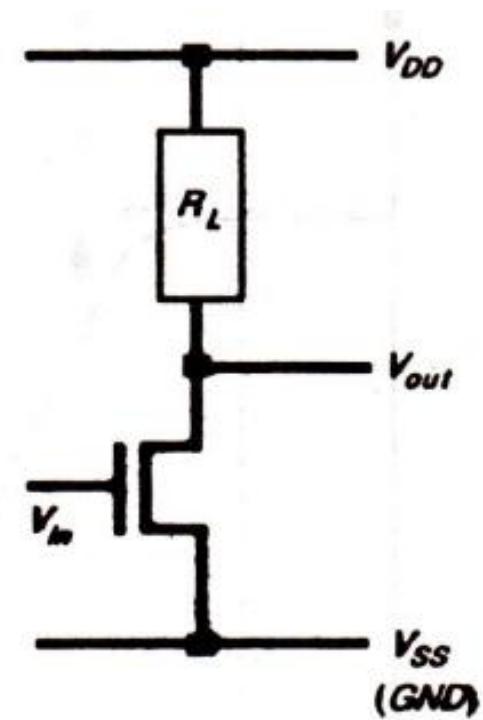
$$V_{ds(\text{enh})} = V_{DD} - V_{ds(\text{dep})} = V_{out}$$

$V_{gs(\text{enh})} = V_{in}$  . . . intersection points give transfer characteristic

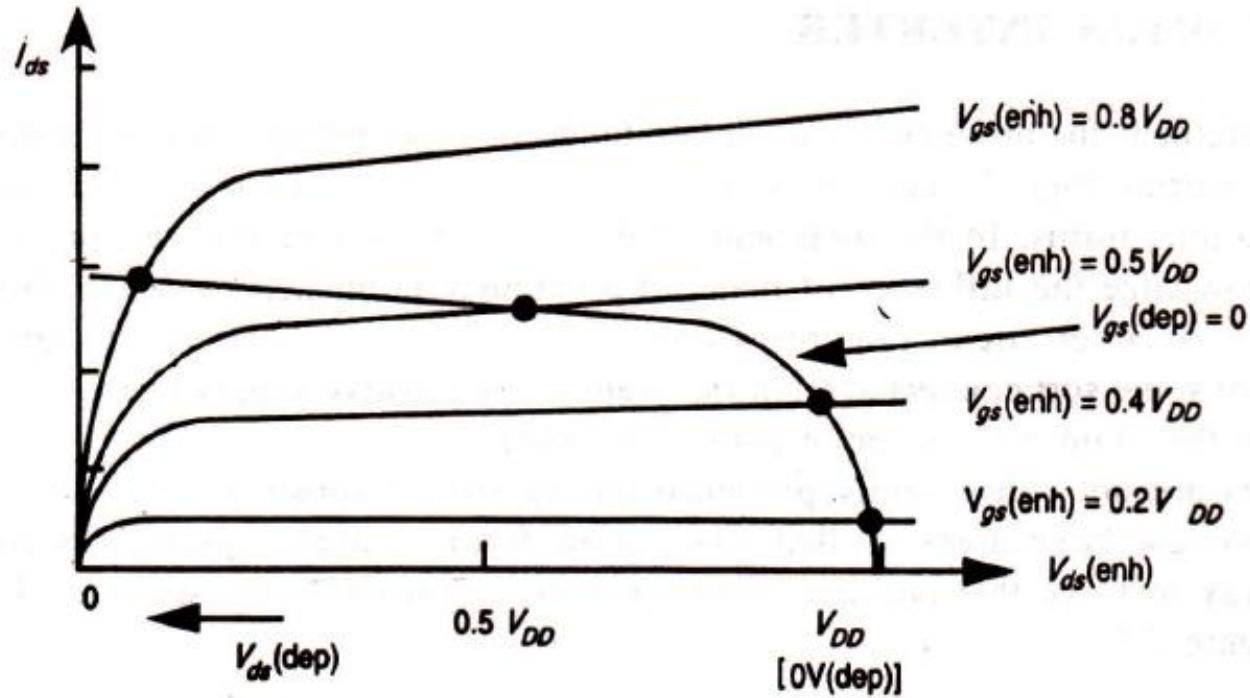


**FIGURE 2.7** nMOS Inverter transfer characteristic.

$$\text{Gain} = \frac{\delta V_{out}}{\delta V_{in}}$$

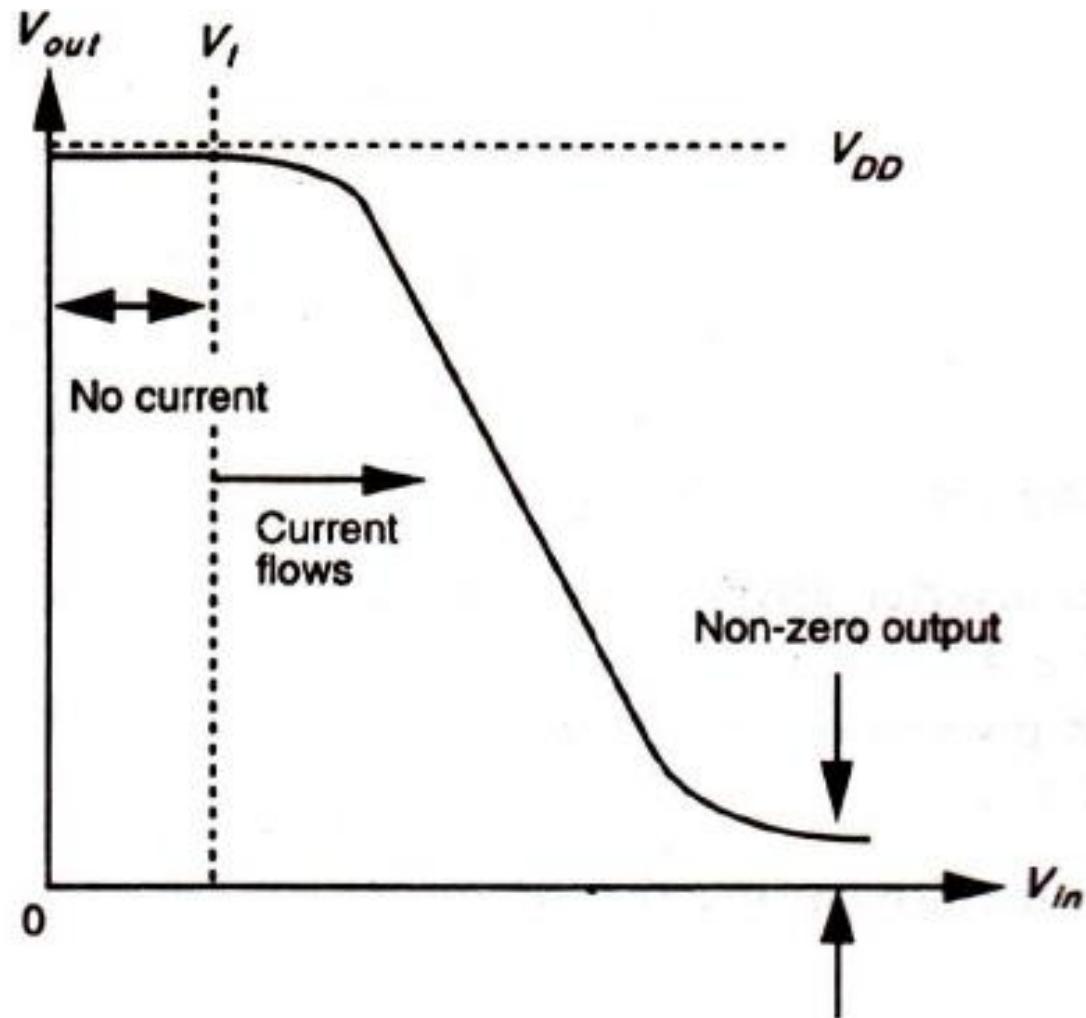


**FIGURE 2.11** Resistor pull-up.



$$V_{ds}(\text{enh}) = V_{DD} - V_{ds}(\text{dep}) = V_{out}$$

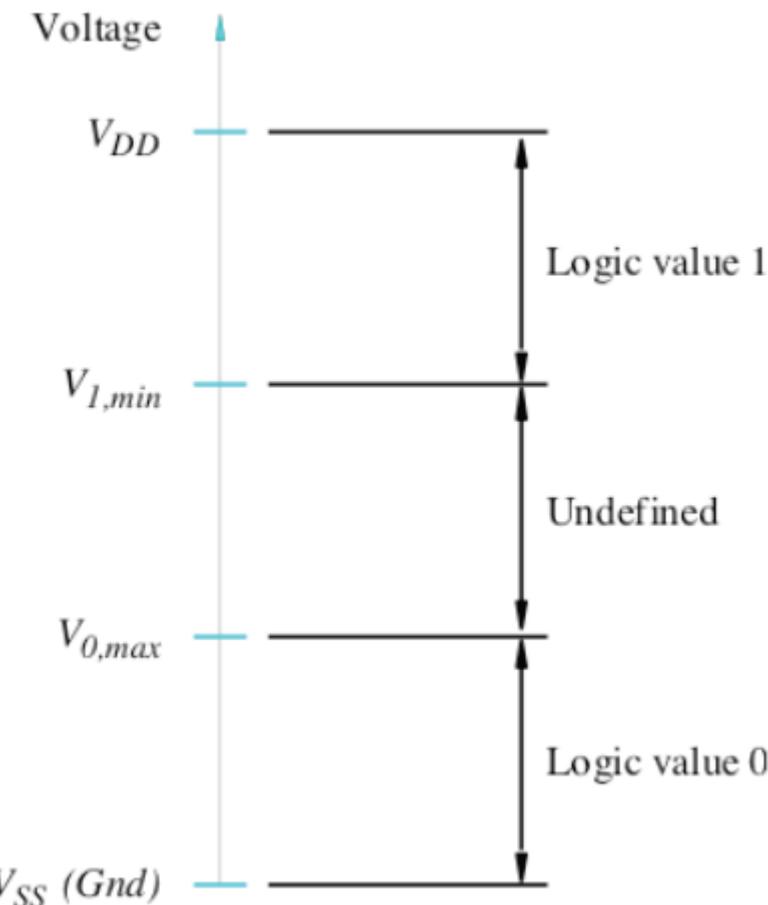
$V_{gs}(\text{enh}) = V_{in} \dots$  intersection points give transfer characteristic



# Pass Transistors

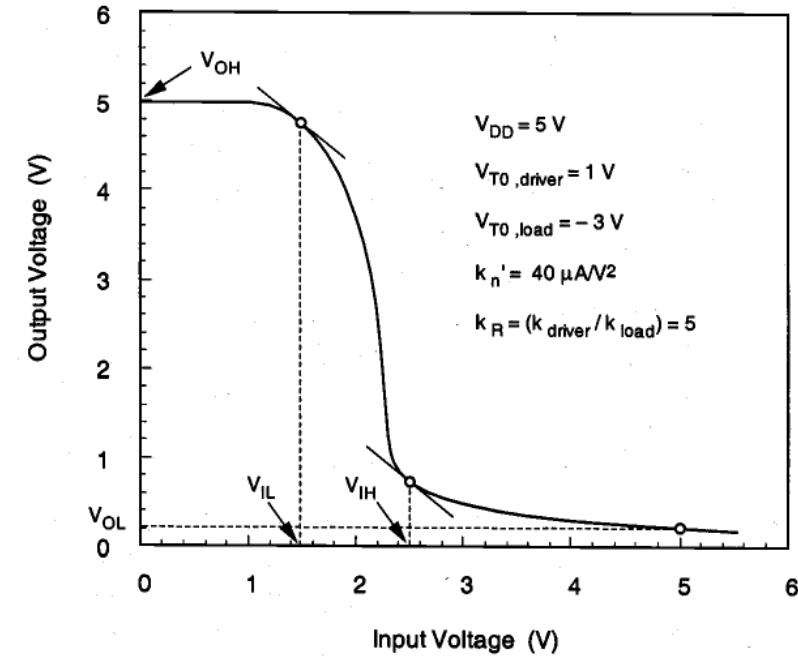
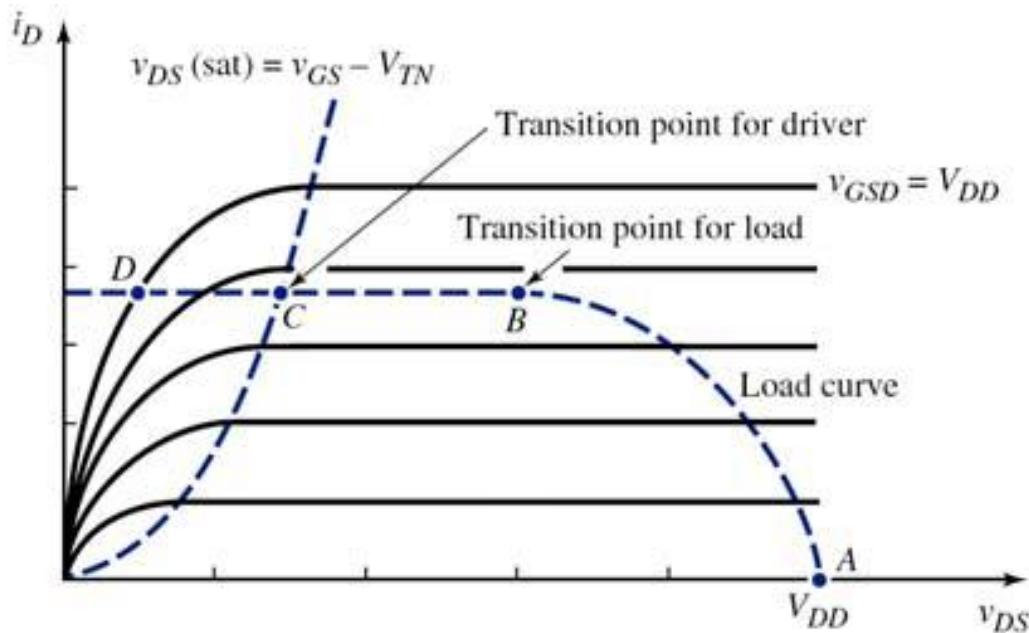
Ref:-CMOS LOGIC CIRCUIT DESIGN by John P. Uyemura

## Transistor as a Switch

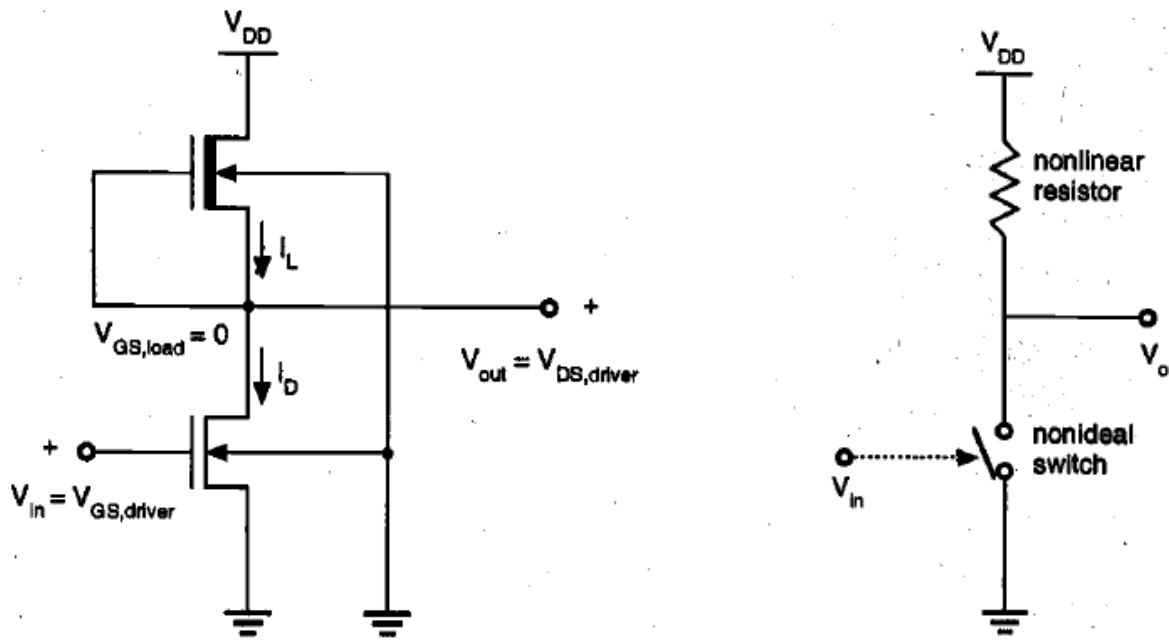


# Depletion Load NMOS Inverter

$V_{in}$	$V_{out}$	Driver operating region	Load operating region
$V_{OL}$	$V_{OH}$	cut-off	linear
$V_{IL}$	$\approx V_{OH}$	saturation	linear
$V_{IH}$	small	linear	<i>saturation</i>
$V_{OH}$	$V_{OL}$	linear	saturation



# Depletion Load NMOS Inverter



$V_{in}$	$V_{out}$	Driver operating region	Load operating region
$V_{OL}$	$V_{OH}$	cut-off	linear
$V_{IL}$	$\approx V_{OH}$	saturation	linear
$V_{IH}$	small	linear	<i>saturation</i>
$V_{OH}$	$V_{OL}$	linear	saturation

# Depletion Load NMOS Inverter

## Calculation of $V_{OH}$

When the input voltage  $V_{in}$  is smaller than the driver threshold voltage  $V_{T0}$ , the driver transistor is turned off and does not conduct any drain current. Consequently, the load device, which operates in the linear region, also has zero drain current.

Substituting  $V_{OH}$  for  $V_{out}$

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[ 2|V_{T,load}(V_{OH})| \cdot (V_{DD} - V_{OH}) - (V_{DD} - V_{OH})^2 \right] = 0$$

The only valid solution in the linear region is  $V_{OH} = V_{DD}$ .

# Depletion Load NMOS Inverter

## Calculation of $V_{OL}$

We assume that the input voltage  $V_{in}$  of the inverter is equal to  $V_{OH} = V_{DD}$

**Driver transistor** → linear region

**Depletion-type load** → saturation region

$$\frac{k_{driver}}{2} \cdot [2 \cdot (V_{OH} - V_{T0}) \cdot V_{OL} - V_{OL}^2] = \frac{k_{load}}{2} \cdot [-V_{T,load}]^2$$

This second-order equation in  $V_{OL}$  can be solved by temporarily neglecting the dependence of  $V_{T,load}$  on  $V_{OL}$ , as follows.

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot |V_{T,load}|^2}$$

# Depletion Load NMOS Inverter

## Calculation of $V_{IL}$

By definition, the slope of the VTC is equal to  $(-1)$ , i.e.,  $dV_{out}/dV_{in} = -1$  when the input voltage is  $V_{in} = V_{IL}$ . Note that in this case, the driver transistor operates in saturation while the load transistor operates in the linear region. Applying KCL for the output node, we obtain the following current equation:

$$\frac{k_{driver}}{2} \cdot (V_{in} - V_{T0})^2 = \frac{k_{load}}{2} \cdot [2|V_{T,load}(V_{out})| \cdot (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2] \quad (5.39)$$

To satisfy the derivative condition at  $V_{IL}$ , we differentiate both sides of (5.39) with respect to  $V_{in}$ .

$$k_{driver} \cdot (V_{in} - V_{T0}) = \frac{k_{load}}{2} \cdot \left[ 2|V_{T,load}(V_{out})| \left( -\frac{dV_{out}}{dV_{in}} \right) + 2(V_{DD} - V_{out}) \left( -\frac{dV_{T,load}}{dV_{in}} \right) - 2(V_{DD} - V_{out}) \left( -\frac{dV_{out}}{dV_{in}} \right) \right] \quad (5.40)$$

# Depletion Load NMOS Inverter

Calculation of  $V_{IL}$

In general, we can assume that the term  $(dV_{T,load}/dV_{in})$  is negligible with respect to the others. Substituting  $V_{IL}$  for  $V_{in}$ , and letting  $dV_{out}/dV_{in} = -1$ , we obtain  $V_{IL}$  as a function of the output voltage  $V_{out}$ .

$$V_{IL} = V_{T0} + \left( \frac{k_{load}}{k_{driver}} \right) \cdot [V_{out} - V_{DD} + |V_{T,load}|] \quad (5.41)$$

# Depletion Load NMOS Inverter

## Calculation of $V_{IH}$

$V_{IH}$  is the larger of the two voltage points on the VTC at which the slope is equal to  $(-1)$ . Since the output voltage corresponding to this operating point is relatively small, the driver transistor is in the linear region and the load transistor is in saturation.

$$\frac{k_{\text{driver}}}{2} \cdot [2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2] = \frac{k_{\text{load}}}{2} \cdot [-\beta_{I, \text{load}}(V_{out})]^2 \quad (5.42)$$

Differentiating both sides of (5.42) with respect to  $V_{in}$ , we obtain :

# Depletion Load NMOS Inverter

Calculation of  $V_{IH}$

$$\begin{aligned} k_{driver} \cdot & \left[ V_{out} + (V_{in} - V_{T0}) \left( \frac{dV_{out}}{dV_{in}} \right) - V_{out} \left( \frac{dV_{out}}{dV_{in}} \right) \right] \\ = k_{load} \cdot & \left[ -V_{T,load}(V_{out}) \right] \cdot \left( \frac{dV_{T,load}}{dV_{out}} \right) \cdot \left( \frac{dV_{out}}{dV_{in}} \right) \end{aligned} \quad (5.43)$$

Now, substitute  $dV_{out} / dV_{in} = -1$  into (5.43), and solve for  $V_{in} = V_{IH}$

$$V_{IH} = V_{T0} + 2V_{out} + \left( \frac{k_{load}}{k_{driver}} \right) \cdot \left[ -V_{T,load}(V_{out}) \right] \cdot \left( \frac{dV_{T,load}}{dV_{out}} \right) \quad (5.44)$$

Note that the derivative of the load threshold voltage with respect to the output voltage cannot be neglected in this case.

$$\frac{dV_{T,load}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{out}}} \quad (5.45)$$

# Depletion Load NMOS Inverter

$$V_{OH} = V_{DD}$$

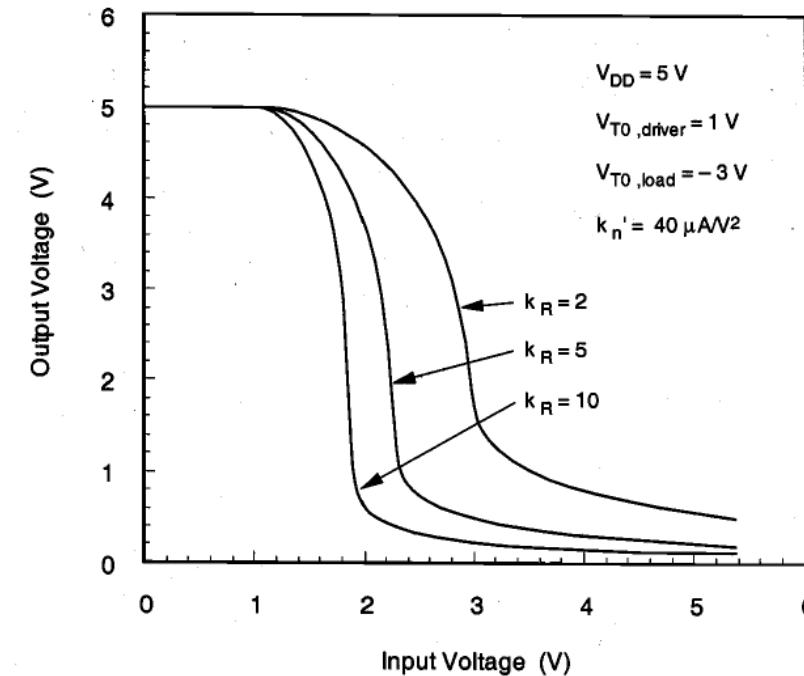
$$V_{OL} = V_{OH} - V_{T0} - \sqrt{\left(V_{OH} - V_{T0}\right)^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot |V_{T,load}|^2}$$

$$V_{IL} = V_{T0} + \left(\frac{k_{load}}{k_{driver}}\right) \cdot \left[V_{out} - V_{DD} + |V_{T,load}|\right]$$

$$V_{IH} = V_{T0} + 2V_{out} + \left(\frac{k_{load}}{k_{driver}}\right) \cdot \left[-V_{T,load}(V_{out})\right] \cdot \left(\frac{dV_{T,load}}{dV_{out}}\right)$$

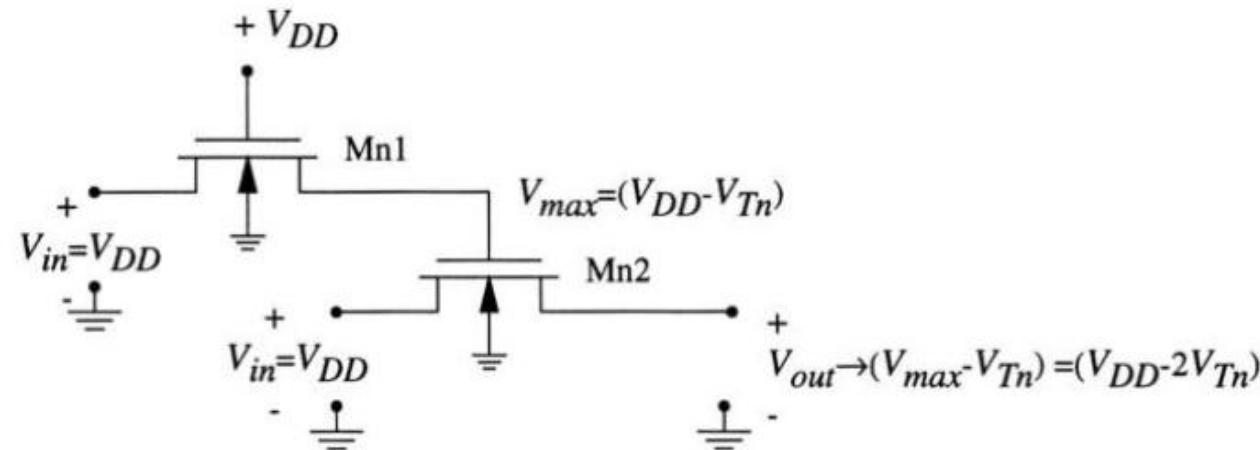
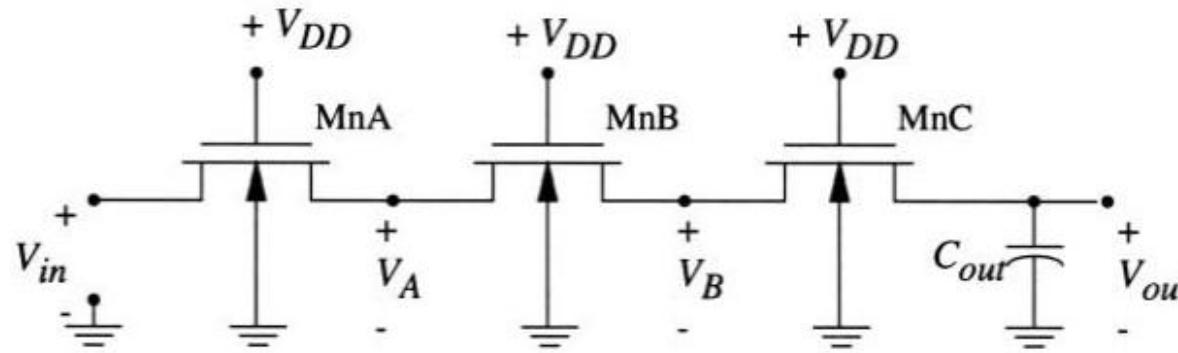
$$k_R = \frac{k'_{n,driver} \cdot \left(\frac{W}{L}\right)_{driver}}{k'_{n,load} \cdot \left(\frac{W}{L}\right)_{load}} \quad \text{Where}$$

$$k' = \mu_n \cdot C_{ox} \quad k = k' \cdot \frac{W}{L}$$

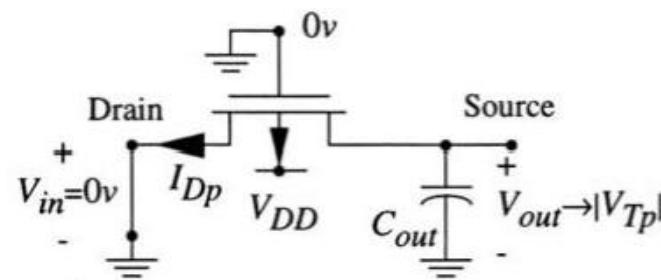
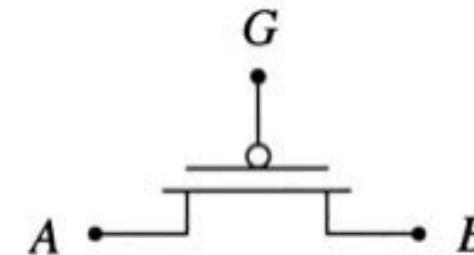
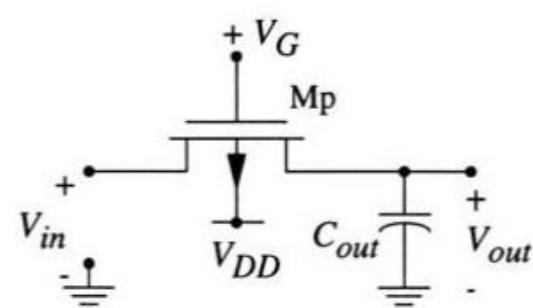


# Pass Transistor and Transmission Gate

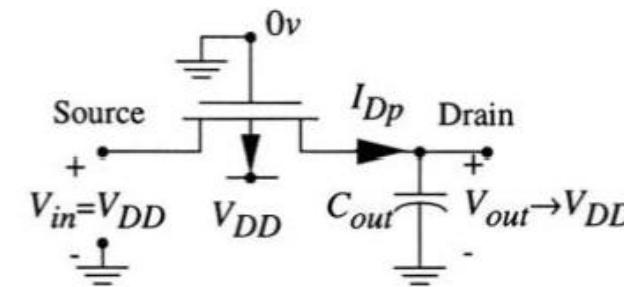
# Pass Transistors (NMOS)



# Pass Transistors (PMOS)

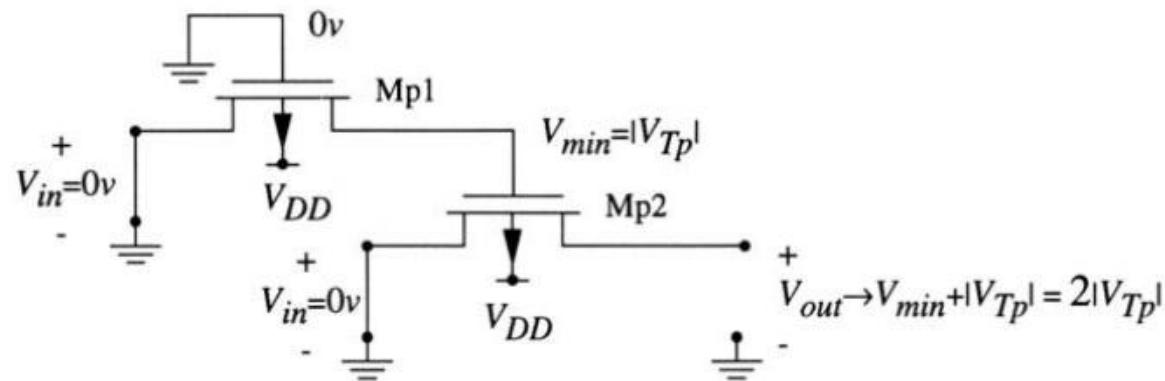
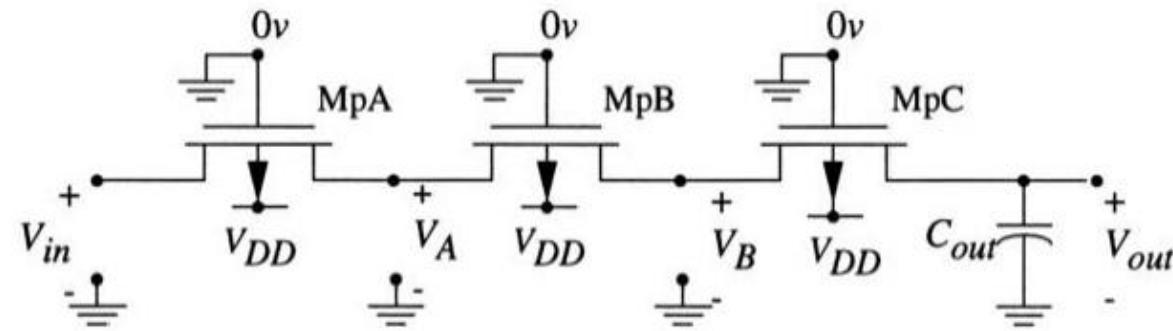


(a) Logic 0 input



(b) Logic 1 input

# Pass Transistors (NMOS)

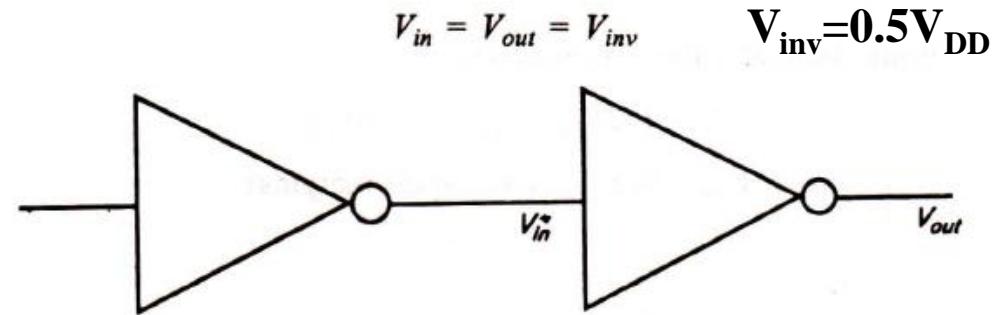
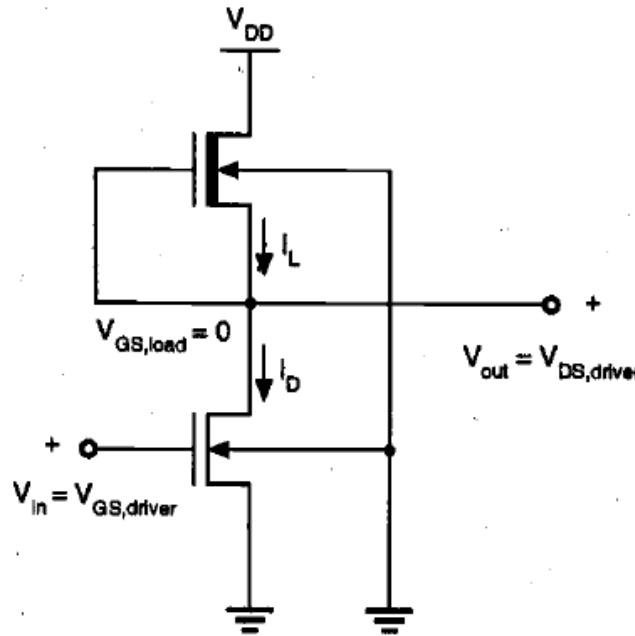


# Pass Transistors: Summary

- PMOS Pass transistor passes weak logic 0.
- PMOS Pass transistor passes strong logic 1.
- NMOS Pass transistor passes strong logic 0.
- NMOS Pass transistor passes weak logic 1.

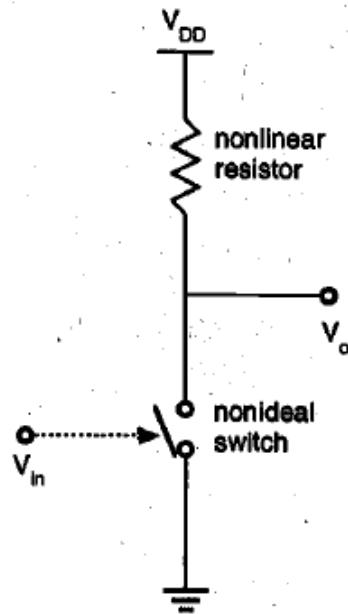
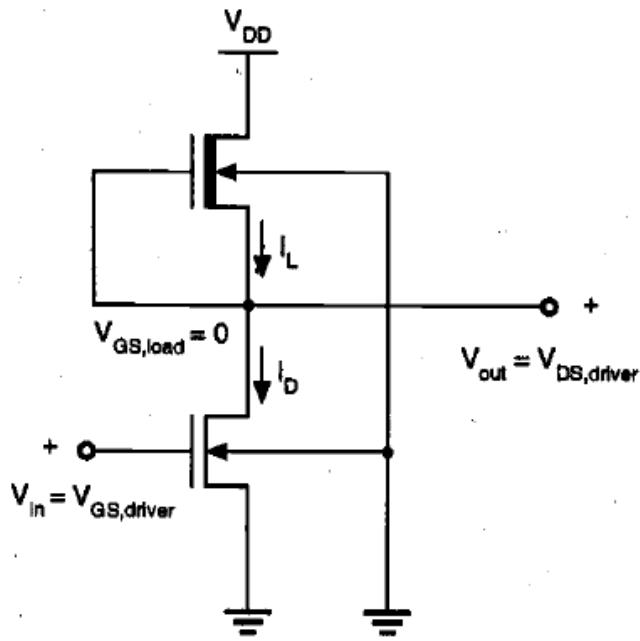
# Cascade Inverter

Determination of pull-up to pull-down ratio ( $Z_p.U / Z_p.D.$ ) For An NMOS Inverter Driven By Another NMOS Inverter



$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2} \quad \text{Note} \rightarrow K = \frac{\mu \epsilon_{ins} \epsilon_0}{t_{ox}}$$

# Depletion Load NMOS Inverter



$V_{in}$	$V_{out}$	Driver operating region	Load operating region
$V_{OL}$	$V_{OH}$	cut-off	linear
$V_{IL}$	$\approx V_{OH}$	saturation	linear
$V_{IH}$	small	linear	<i>saturation</i>
$V_{OH}$	$V_{OL}$	linear	saturation

# Cascade Inverter

In the depletion mode

$$I_{ds} = K \frac{W_{p.u.}}{L_{p.u.}} \frac{(-V_{td})^2}{2} \text{ since } V_{gs} = 0$$

and in the enhancement mode

$$I_{ds} = K \frac{W_{p.d.}}{L_{p.d.}} \frac{(V_{inv} - V_t)^2}{2} \text{ since } V_{gs} = V_{inv}$$

Equating (since currents are the same) we have

$$\frac{W_{p.d.}}{L_{p.d.}} (V_{inv} - V_t)^2 = \frac{W_{p.u.}}{L_{p.u.}} (-V_{td})^2$$

# Cascade Inverter

$$Z_{p.d.} = \frac{L_{p.d.}}{W_{p.d.}}; Z_{p.u.} = \frac{L_{p.u.}}{W_{p.u.}}$$

$$\frac{1}{Z_{p.d.}} (V_{inv} - V_t)^2 = \frac{1}{Z_{p.u.}} (-V_{td})^2$$

$$V_{inv} = V_t - \frac{V_{td}}{\sqrt{Z_{p.u.}/Z_{p.d.}}}$$

substitute typical values as follows

$$V_t = 0.2V_{DD}; V_{td} = - 0.6V_{DD}$$

$$V_{inv} = 0.5V_{DD} \text{ (for equal margins)}$$

# Cascade Inverter

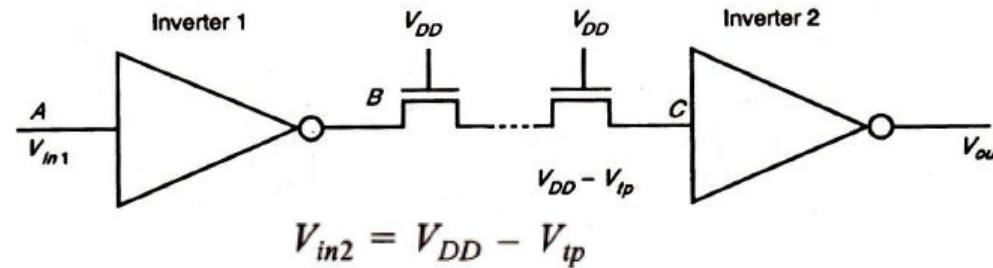
$$0.5 = 0.2 + \frac{0.6}{\sqrt{Z_{p.u.}/Z_{p.d.}}}$$

$$\sqrt{Z_{p.u.}/Z_{p.d.}} = 2$$

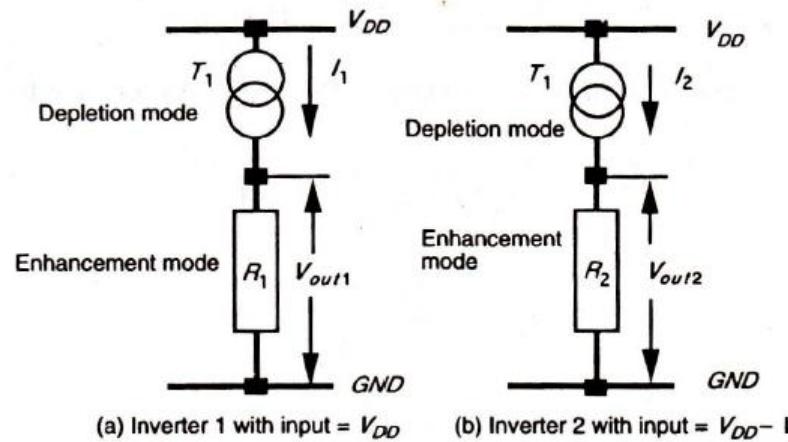
$$Z_{p.u.}/Z_{p.d.} = 4/1$$

# Cascade Inverter

Pull-up to pull-down ratio for an NMOS inverter driven through one or more pass transistors



$V_{tp}$  = threshold voltage for a pass transistor



# Cascade Inverter

For the p.d. transistor

$$I_{ds} = K \frac{W_{p.d.1}}{L_{p.d.1}} \left( (V_{DD} - V_t) V_{ds1} - \frac{V_{ds1}^2}{2} \right)$$

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{1}{K} \frac{L_{p.d.1}}{W_{p.d.1}} \left( \frac{1}{V_{DD} - V_t - \frac{V_{ds1}}{2}} \right)$$

$$R_1 = \frac{1}{K} Z_{p.d.1} \left( \frac{1}{V_{DD} - V_t} \right)$$

Now, for depletion mode p.u. in saturation with  $V_{GS} = 0$

$$I_1 = I_{ds} = K \frac{W_{p.u.1}}{L_{p.u.1}} \frac{(-V_{td})^2}{2}$$

$$\text{Note} \rightarrow K = \frac{\mu \epsilon_{ins} \epsilon_0}{t_{ox}}$$

# Cascade Inverter

$$I_1 R_1 = V_{out1}$$

$$V_{out1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}} \left( \frac{1}{V_{DD} - V_t} \right) \frac{(V_{td})^2}{2}$$

Consider inverter 2 (Figure 2.10(b)) when input =  $VDD - V_{tp}$ .

$$R_2 = \frac{1}{K} Z_{p.d.2} \frac{1}{((V_{DD} - V_{tp}) - V_t)}$$

$$I_2 = K \frac{1}{Z_{p.u.2}} \frac{(-V_{td})^2}{2}$$

# Cascade Inverter

Taking typical values

$$V_t = 0.2V_{DD}$$

$$V_{tp} = 0.3V_{DD}^*$$

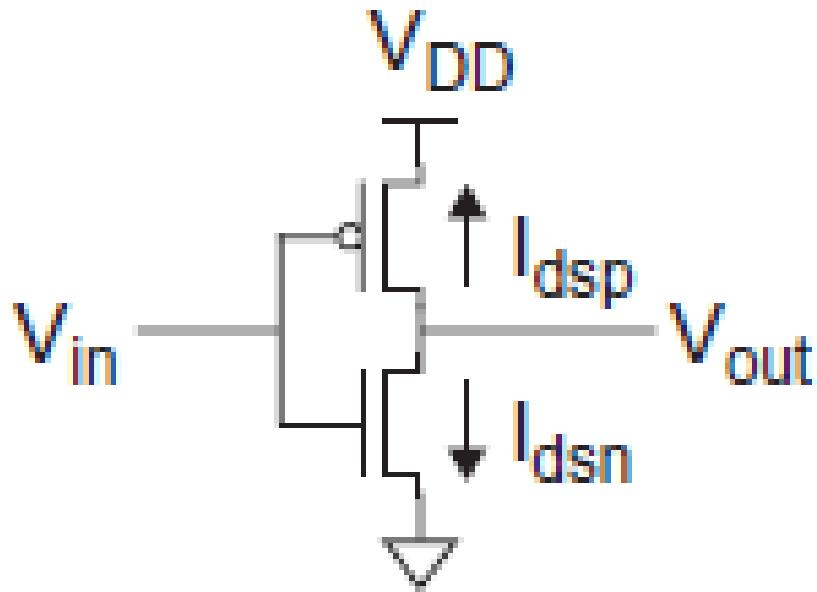
$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{0.8}{0.5}$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} \doteq 2 \quad \frac{Z_{p.u.1}}{Z_{p.d.1}} = \frac{8}{1}$$



# CMOS Inverter

# CMOS Inverter



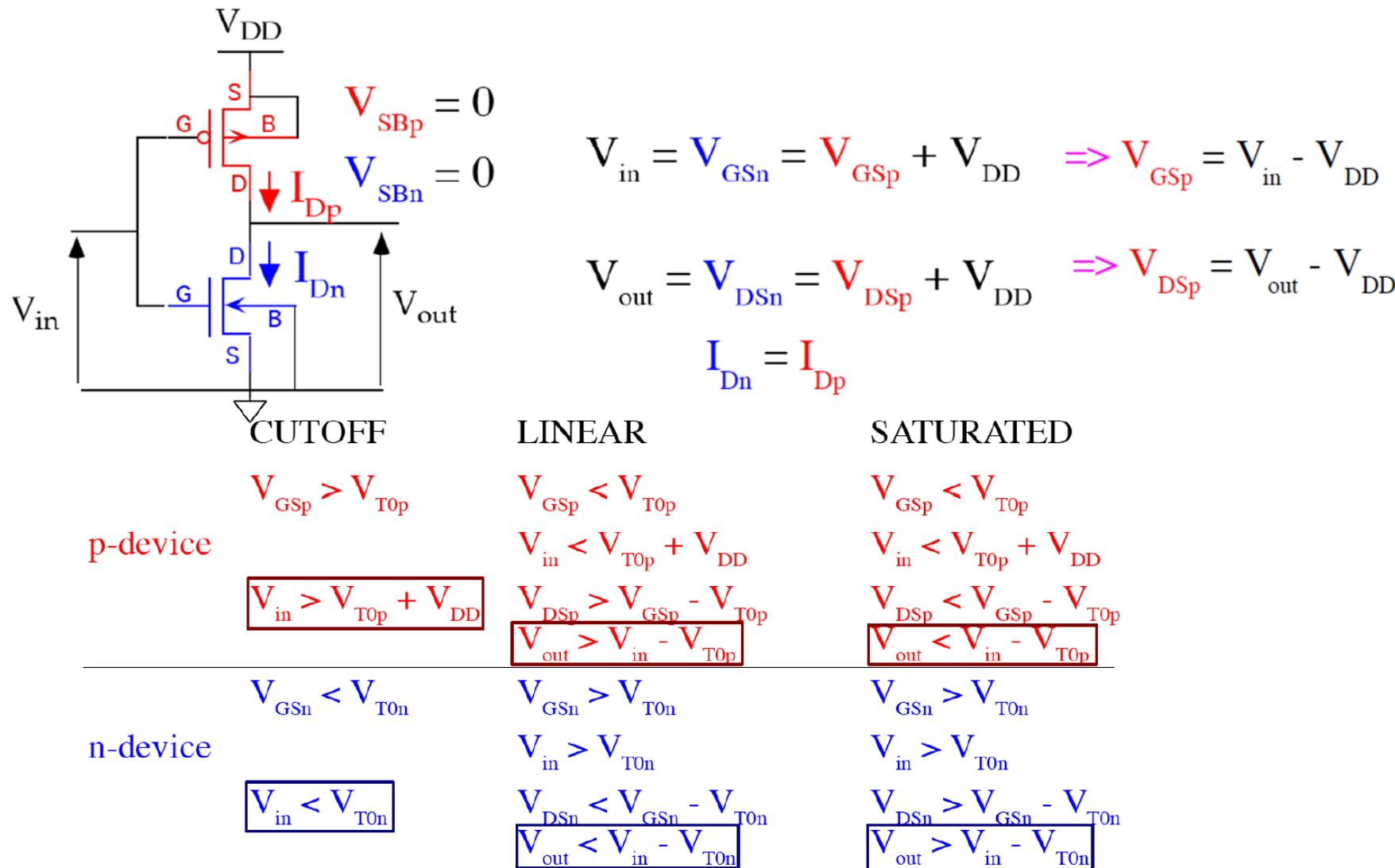
$V_{OH}$ : Maximum output voltage when the output level is logic "1"

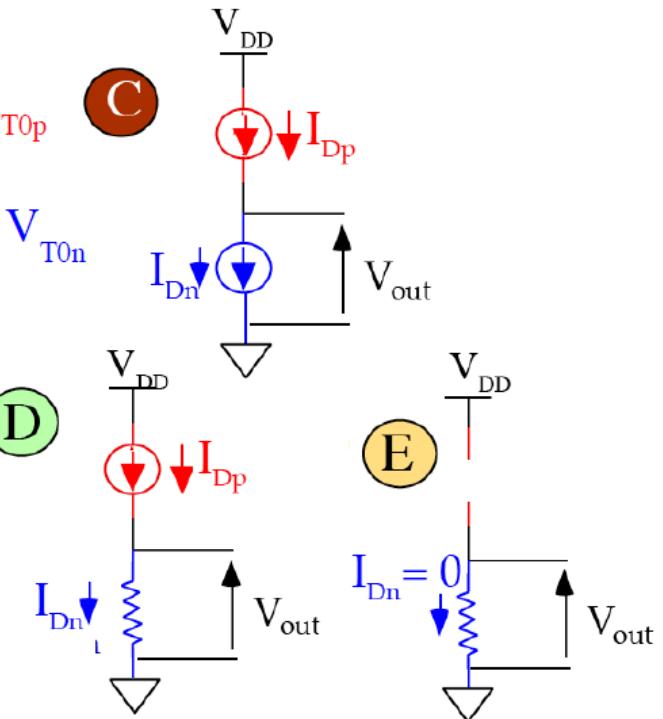
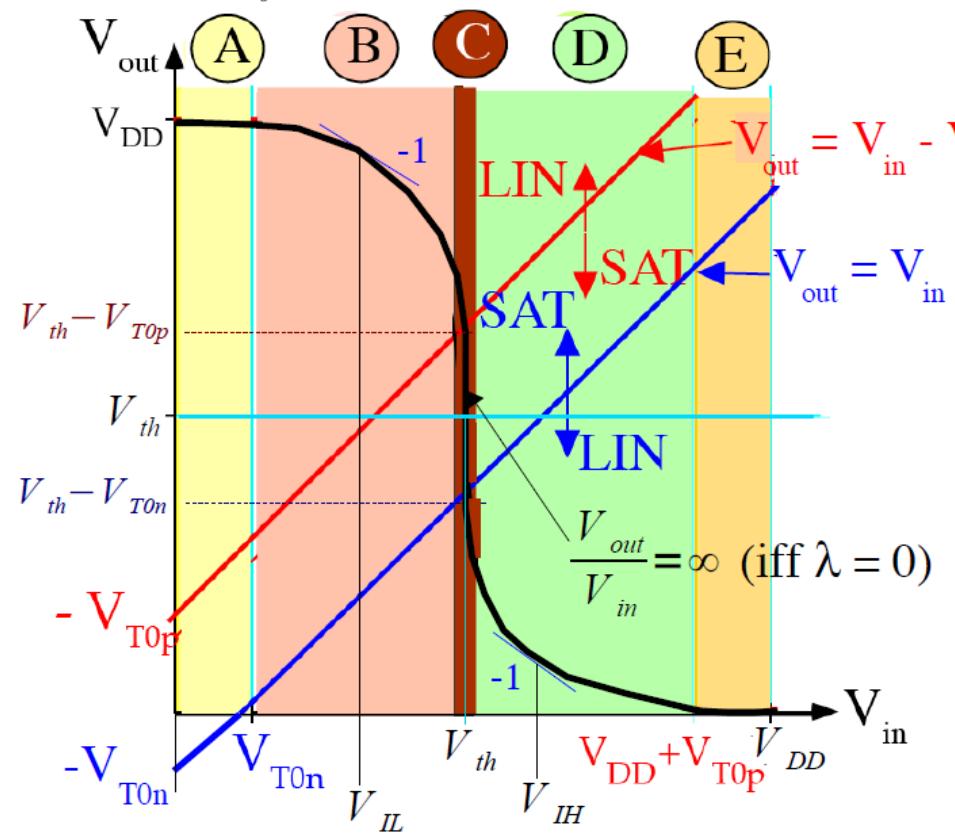
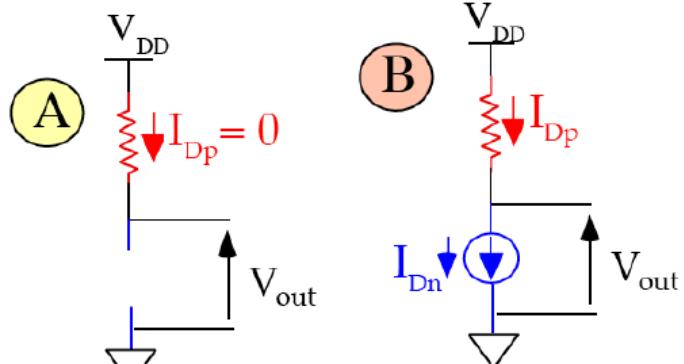
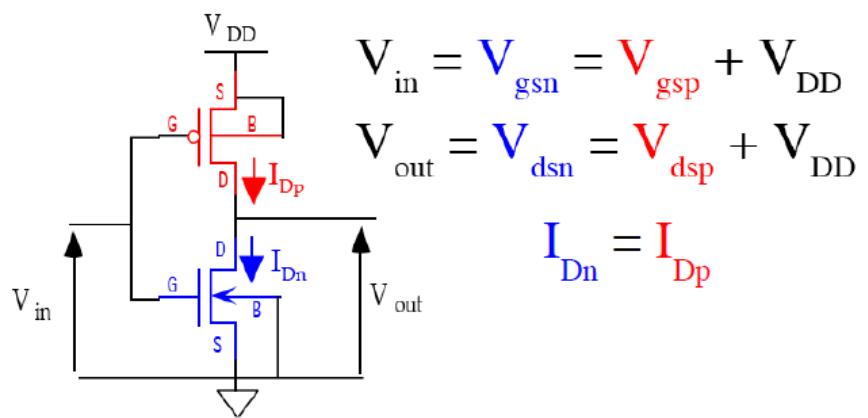
$V_{OL}$ : Minimum output voltage when the output level is logic "0"

$V_{IL}$ : Maximum input voltage which can be *interpreted* as logic "0"

$V_{IH}$ : Minimum input voltage which can be *interpreted* as logic "1"

# CMOS Inverter



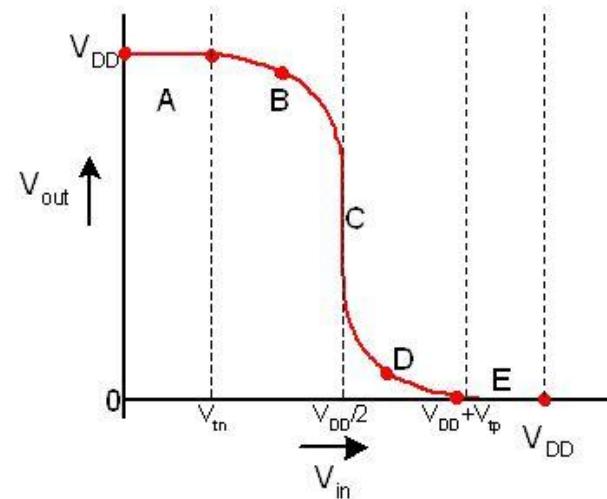


# CMOS Inverter

## Operating Regions

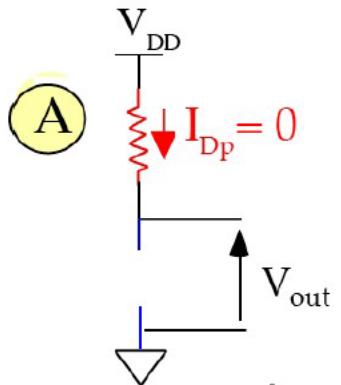
- Revisit transistor operating regions

Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



# CMOS Inverter

CALCULATE  $V_{OH}$

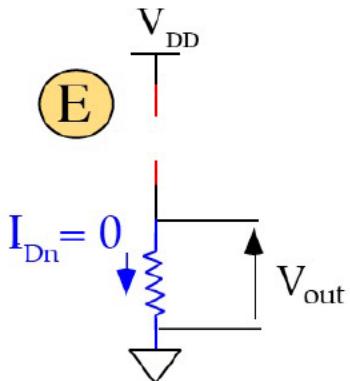


$$I_{Dn} = I_{Dp} = 0$$

$$V_{OH} = V_{DD}$$

$$0 = \frac{k_p}{2} \left( \frac{W}{L} \right)_p [2(v_{in} - V_{DD} - V_{TOp})(v_{out} - V_{DD}) - (v_{out} - V_{DD})^2]$$

CALCULATE  $V_{OL}$



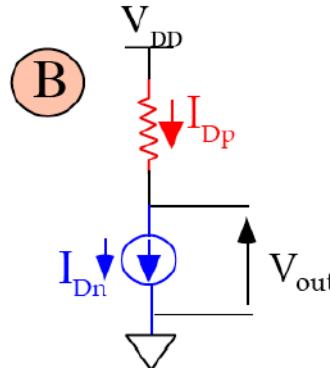
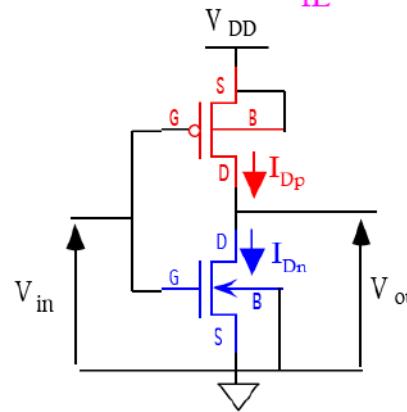
$$I_{Dn} = I_{Dp} = 0$$

$$V_{OL} = 0$$

$$\frac{k_n}{2} \left( \frac{W}{L} \right)_n [2(v_{in} - V_{TOn})(v_{out}) - (v_{out})^2] = 0$$

# CMOS Inverter

CALCULATE  $V_{IL}$



$$I_{Dn} = I_{Dp}$$

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n (V_{GSn} - V_{T0n})^2 = \frac{k_p'}{2} \left( \frac{W}{L} \right)_p [2(V_{GSp} - V_{T0p})V_{DSP} - V_{DSP}^2]$$

$$V_{GSn} = V_{in}, \quad V_{GSp} = V_{in} - V_{DD}, \quad V_{DSP} = V_{out} - V_{DD}$$

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n (V_{in} - V_{T0n})^2$$

Eq.(1)

$$= \frac{k_p'}{2} \left( \frac{W}{L} \right)_p [2(V_{in} - V_{DD} - V_{T0p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

# CMOS Inverter

$$\begin{aligned} & \frac{k'_n}{2} \left( \frac{W}{L} \right)_n (V_{in} - V_{T0n})^2 \\ &= \frac{k'_p}{2} \left( \frac{W}{L} \right)_p [2(V_{in} - V_{DD} - V_{T0p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2] \end{aligned}$$

Eq.(1)

DIFFERENTIATING wrt  $V_{in}$

$$\begin{aligned} \cancel{\frac{k'_n}{2} \left( \frac{W}{L} \right)_n 2(V_{in} - V_{T0n})} &= \cancel{\frac{k'_p}{2} \left( \frac{W}{L} \right)_p [2(V_{out} - V_{DD}) + 2(V_{in} - V_{DD} - V_{T0p}) \frac{dV_{out}}{dV_{in}}]}^{(-1)} \\ & - 2(V_{out} - V_{DD}) \cancel{\frac{dV_{out}}{dV_{in}}}^{(-1)} \end{aligned}$$

$$k'_n \left( \frac{W}{L} \right)_n (V_{IL} - V_{T0n}) = k'_p \left( \frac{W}{L} \right)_p [2V_{out} - V_{IL} + V_{T0p} - V_{DD}]$$

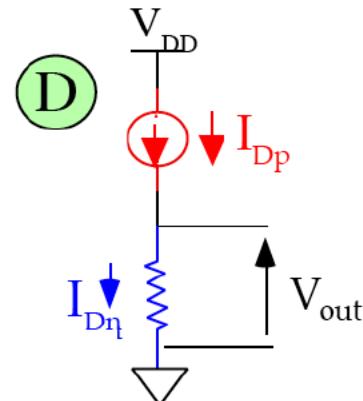
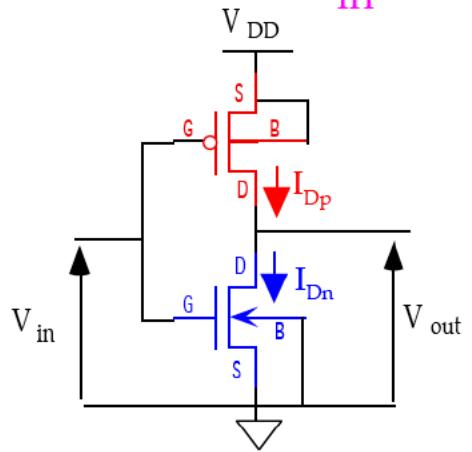
SOLVING FOR  $V_{IL}$

$$V_{IL} = \frac{2V_{out} + V_{T0p} - V_{DD} + k_R V_{T0n}}{1 + k_R} \quad \text{where } k_R = \frac{k'_n (W/L)_n}{k'_p (W/L)_p}$$

SOLVE Eq. (1) and Eq. (2) for  $V_{out}$  and  $V_{IL}$  or use simulation.

# CMOS Inverter

CALCULATE  $V_{IH}$



$$I_{Dn} = I_{Dp}$$

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n [2(V_{GSn} - V_{T0n})V_{DSn} - V_{DSn}^2] = \frac{k_p'}{2} \left( \frac{W}{L} \right)_p (V_{GSp} - V_{T0p})^2$$

$$V_{GSn} = V_{in}, V_{DSn} = V_{out}, V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n [2(V_{in} - V_{T0n})V_{out} - V_{out}^2] = \frac{k_p'}{2} \left( \frac{W}{L} \right)_p (V_{in} - V_{DD} - V_{T0p})^2$$

# CMOS Inverter

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n [2(V_{in} - V_{T0n})V_{out} - V_{out}^2] = \frac{k_p'}{2} \left( \frac{W}{L} \right)_p (V_{in} - V_{DD} - V_{T0p})^2 \quad \text{Eq.(3)}$$

DIFFERENTIATING wrt  $V_{in}$

$$k_n' \left( \frac{W}{L} \right)_n \left[ (V_{in} - V_{T0n}) \frac{dV_{out}}{dV_{in}} + V_{out} - V_{out} \frac{dV_{out}}{dV_{in}} \right] = k_p' \left( \frac{W}{L} \right)_p (V_{in} - V_{DD} - V_{T0p})$$

$$k_n' \left( \frac{W}{L} \right)_n [-V_{IH} + V_{T0n} + 2V_{out}] = k_p' \left( \frac{W}{L} \right)_p (V_{IH} - V_{DD} - V_{T0p})$$

SOLVING FOR  $V_{IH}$

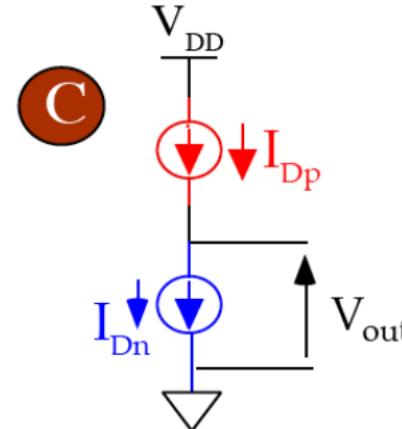
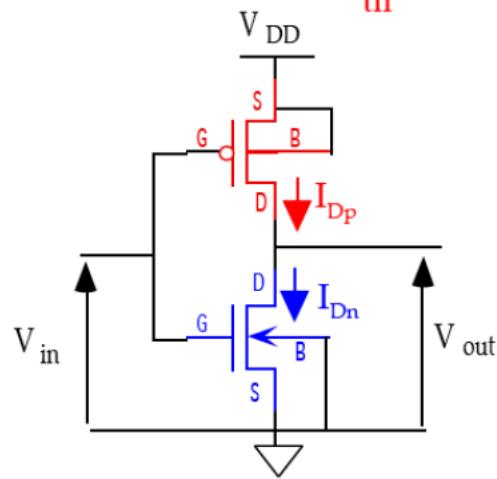
$$V_{IH} = \frac{V_{DD} + V_{T0p} + k_R (2V_{out} + V_{T0n})}{1 + k_R} \quad \text{Eq.(4)}$$

where  $k_R = \frac{k_n' (W/L)_n}{k_p' (W/L)_p}$

SOLVE Eq. (3) and Eq. (4) for  $V_{out}$  and  $V_{IH}$  or use simulation.

# CMOS Inverter

CALCULATE  $V_{th}$



$$I_{Dn} = I_{Dp}$$

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n (V_{GSn} - V_{T0n})^2 = \frac{k_p'}{2} \left( \frac{W}{L} \right)_p (V_{GSp} - V_{T0p})^2$$

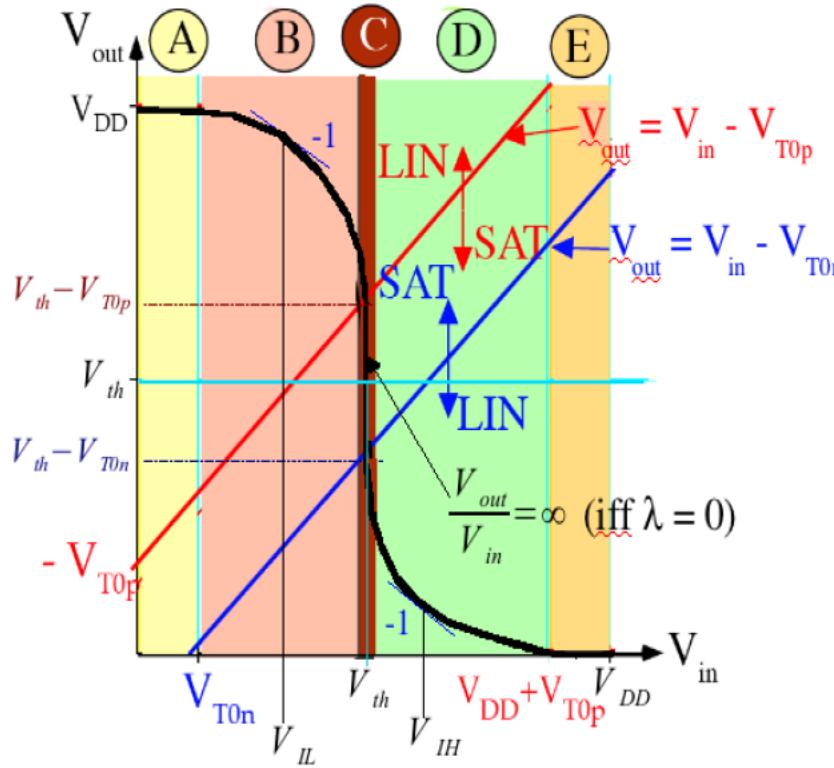
$$V_{GSn} = V_{in}, \quad V_{GSp} = V_{in} - V_{DD}$$

$$\frac{k_n'}{2} \left( \frac{W}{L} \right)_n (V_{in} - V_{T0n})^2 = \frac{k_p'}{2} \left( \frac{W}{L} \right)_p (V_{in} - V_{DD} - V_{T0p})^2$$

# CMOS Inverter

$$\frac{k'_n}{2} \left( \frac{W}{L} \right)_n (V_{in} - V_{T0n})^2 = \frac{k'_p}{2} \left( \frac{W}{L} \right)_p (V_{in} - V_{DD} - V_{T0p})^2$$

Setting for  $V_{in} = V_{th}$  and solving for  $V_{th}$



$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R} (V_{DD} + V_{T0p})}}{1 + \sqrt{\frac{1}{k_R}}} \quad \text{Eq.(5)}$$

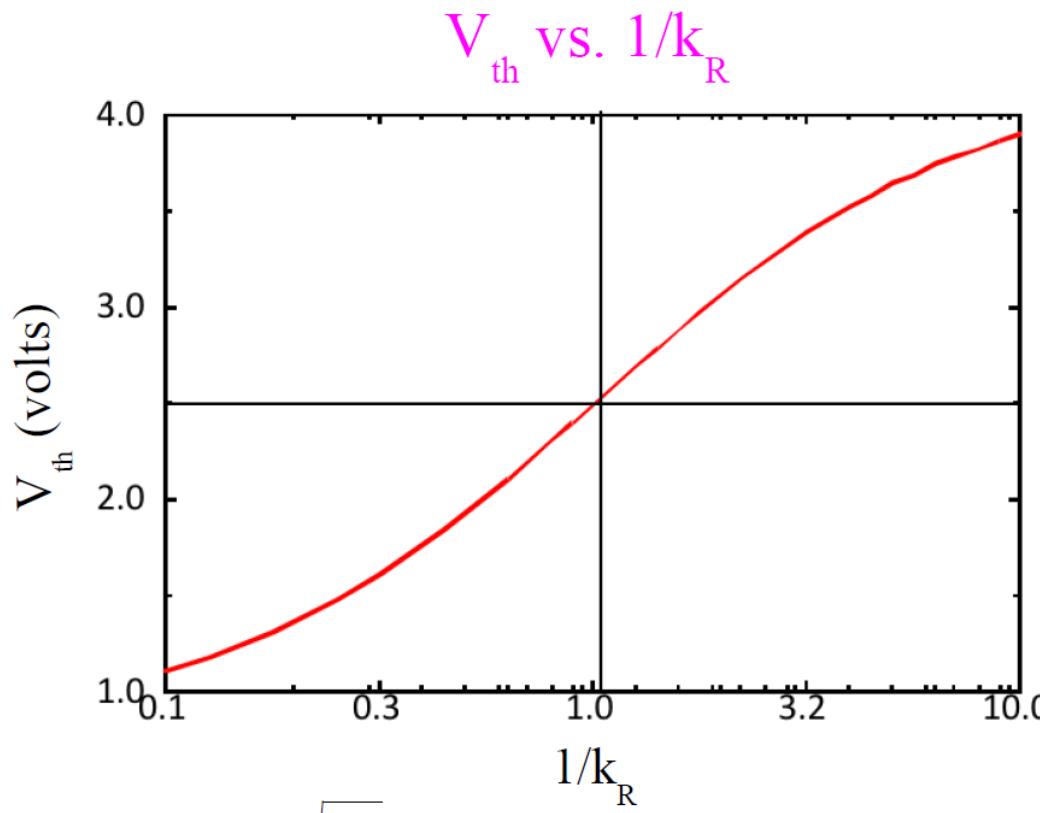
where  $k_R = \frac{k'_n (W/L)_n}{k'_p (W/L)_p} = \frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}$

$$\mu_n > \mu_p$$

Usually  $L_n = L_p$  is set to min  $L$ :

$$k_R = \frac{k'_n (W/L)_n}{k'_p (W/L)_p} = \frac{\mu_n W_n}{\mu_p W_p}$$

# CMOS Inverter



$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}(V_{DD} + V_{T0p})}}{1 + \sqrt{\frac{1}{k_R}}}$$

$V_{DD} = 5V; V_{T0n} = -V_{T0p} = 1 V$

# CMOS Inverter

## DESIGN OF CMOS INVERTERS

$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}(V_{DD} + V_{T0p})}}{1 + \sqrt{\frac{1}{k_R}}} \quad \text{Eq.(5)}$$

Solving Eq.(5) for  $k_R$      $k_R = \left( \frac{V_{DD} + V_{T0p} - V_{th}}{V_{th} - V_{T0n}} \right)^2$     **Important design Eq. for CMOS inverter VTC.**

If  $V_{th}$  is set to  $V_{th} = V_{th(ideal)} = \frac{1}{2}V_{DD}$

$$k_R = \left( \frac{0.5V_{DD} + V_{T0p}}{0.5V_{DD} - V_{T0n}} \right)^2$$

### Symmetric CMOS Inverter

If  $V_{th(ideal)}$  and  $V_{T0n} = -V_{T0p} = V_{T0}$      $\Rightarrow (k_R)_{symmetric} = 1$

# CMOS Inverter

$$k_R = \frac{k_n(W/L)_n}{k_p(W/L)_p} = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{\mu_n(W/L)_n}{\mu_p(W/L)_p}$$

Symmetric CMOS inverter  $V_{th(ideal)}$  and  $V_{T0n} = -V_{T0p} = V_{T0} \Rightarrow (k_R)_{symmetric} = 1$

$$\frac{(W/L)_n}{(W/L)_p} = k_R \frac{\mu_p}{\mu_n} \xrightarrow{k_R=1} \boxed{\frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n}}$$

$$\frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n} = \frac{230 \text{ cm}^2/\text{Vs}}{580 \text{ cm}^2/\text{Vs}} \longrightarrow (W/L)_p \approx 2.52 (W/L)_n$$

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{T0}) \quad \text{FROM Eq. (1) and Eq. (2)}$$

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_{T0}) \quad \text{FROM Eq. (3) and Eq. (4)}$$

NOTE:  $V_{IL} + V_{IH} = V_{DD}$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} = (3/8)V_{DD} + (2/8)V_{T0}$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} = (3/8)V_{DD} + (2/8)V_{T0}$$

# CMOS Inverter

**EXAMPLE:** Compute the noise margins for a symmetric CMOS inverter has been designed to achieve  $V_{th} = V_{DD}/2$ , where  $V_{DD} = 5 \text{ V}$  and  $V_{T0n} = -V_{T0p} = 1 \text{ V}$ .

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} = (3/8)V_{DD} + (2/8)V_{T0}$$

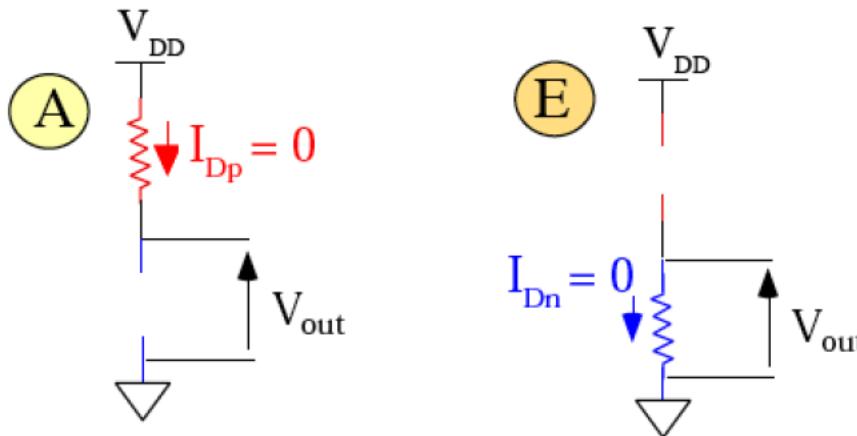
$$NM_L = V_{IL} - V_{OL} = V_{IL} = (3/8)V_{DD} + (2/8)V_{T0}$$

$$NM_H = NM_L = 2.125 \text{ V} > V_{DD}/4$$

**RECALL Preferred Design =>**  $NM_L > V_{DD}/4 = 1.25 \text{ V}$

# CMOS Inverter

## POWER DISSIPATION CONSIDERATIONS



$$P_{DC} = \frac{V_{DD}}{2} [I_{DC}(V_{in} = "0") + I_{DC}(V_{in} = "1")] = \frac{P(V_{in} = 0) + P(V_{in} = 1)}{2}$$

WHEN  $V_{in} = V_{OL}$ :  $I_L = I_D = 0 \Rightarrow P(V_{in} = 0) = 0$

WHEN  $V_{in} = V_{OH}$ :  $I_L = I_D = 0 \Rightarrow P(V_{in} = 1) = 0$

$$P_{DC} = 0$$

