B.Tech. Electronics and Communication Engineering

COURSE PLAN: THEORY COURSE

Department :	**Electronics and Communication Engineering**		
Course Name & code :	**FPGA Based System Design using Verilog & ECE-2243**	**Core**	
Semester & branch :	**IV**	**EE(VLSI Design and Technology)**	
Name of the faculty :	**AKG**		

No of contact hours/week:	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

Course Outcomes (COs) to PO, PSO, BL Mapping

At the end of this course, the student should be able to:		**No. of Contact Hours**	**Marks**	**Program Outcomes (POs)**	**PSOs**	**BL *(Recommended)***
CO1	Explain the various modelling style in Verilog.	10	28	1,2,5	1	2
CO2	Explain the various FPGA architecture and technologies.	5	22	1, 5	1	2
CO3	Develop the ability to model combinational and sequential digital circuits using Verilog HDL.	8	23	2,3,5	1	3
CO4	Implementation of the combinational and sequential digital circuits in FPGA.	8	13	3,4,5	1	3
CO5	Design and implement a system using FPGAs for real-world applications like a traffic light controller or real-time clock.	5	14	3,5,6	1	4
	Total	**36**	**100**			

Course Articulation Matrix

CO	Engineering knowledge	Problem analysis	Design/development of solutions	Investigations of complex problems	Modern tool usage	Engineer and society	Environment and sustainability	Ethics	Individual and team work	Communication	Project management and finance	Life-long learning				
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	3	2			2								3			
CO2	3				3								3			
CO3		3	3		3								3			
CO4			3	2	3								3			
CO5			3		3	2							3			
Average Articulation Level	3	2.5	3	2	2.8	2							3			

ICT Tools used in delivery and assessment

Sl. No	Name of the ICT tool used	Details of how it is used
1	LMS	To share course materials, lecture recordings, and conduct quizzes
2	MS Teams	To share course materials
3	MS Powerpoint	To deliver lectures
4		
5		
6		

Typical tools including LMS, Smart Boards, MS Teams, etc

Mapping of Course Outcomes (COs)/Course Learning Outcomes (CLOs) #

At the end of this course, the student should be able to:		No. of Contact Hours	Marks	Program Outcomes (POs)	Learning Outcomes (LOs)	BL *(Recommended)*
CLO1	Explain the various modelling style in Verilog.	**10**	**28**	**1,2,5**	**1**	**2**
CLO2	Explain the various FPGA architecture and technologies.	**5**	**22**	**1, 5**	**1**	**2**
CLO3	Develop the ability to model combinational and sequential digital circuits using Verilog HDL.	**8**	**23**	**2,3,5**	**1**	**3**
CLO4	Implementation of the combinational and sequential digital circuits in FPGA.	**8**	**13**	**3,4,5**	**1**	**3**
CLO5	Design and implement a system using FPGAs for real-world applications like a traffic light controller or real-time clock.	**5**	**14**	**3,5,6**	**1**	**4**
	Total	**36**	**100**			

 # Applicable to IET Accredited Courses (modules) Only

Delivery and Assessment Plan of LOs #

Learning Outcome (LO) mapped to the course		**Delivery and assessment Plan**
LO	**LO statement**	
1	Explain the various modelling style in Verilog.	Classroom teaching, Quizes, Descriptive exam
2	Explain the various FPGA architecture and technologies.	Classroom teaching, Quizes, Descriptive exam
3	Develop the ability to model combinational and sequential digital circuits using Verilog HDL.	Classroom teaching, Quizes, Descriptive exam
4	Implementation of the combinational and sequential digital circuits in FPGA.	Classroom teaching, Quizes, Descriptive exam
5	Design and implement a system using FPGAs for real-world applications like a traffic light controller or real-time clock.	Classroom teaching, Quizes, Descriptive exam

 # Applicable to IET Accredited Programs Only

Assessment Plan (As communicated from o/o AD-A, in every odd semester)

IN – SEMESTER ASSESSMENTS									
Sl. No.	**Assessment Mode**		**Assessment Method**	****Time Duration**	****Marks**	**** Weightage**	**Typology of Questions *(Recommended)***	****Schedule**	****Topics Covered**
1	**MISAC**	**1**	**Quiz**			**Objective:** 5M 10 MCQs × ½ = 5 marks **Descriptive:** 10 M (2 Questions of 2 marks +2 Questions of 3 marks)	Bloom's taxonomy (B) level of the question should be L3 and above.		
		2	**Mid-Term Test**			10 MCQs × ½ = 5	Bloom's taxonomy (BT) level of the question should be L3 and above.		
		3	**Surprise Assignment**			1 Question × 5M = 5 marks (Minimum 5 questions to be given)	Bloom's taxonomy (BT) level of the question should be L3 and above.		
2	**FISAC**	**1**	*******	******	**5**	*******	Bloom's taxonomy (BT) level of the question should be L3 and above.		
		2	*******	******	**5**	*******	Bloom's taxonomy (BT) level of the question should be L3 and above.		

END – SEMESTER ASSESSMENT							
1	**Regular/Make–Up Exam**	180 Mins	50	Answer all 5 full questions of 10 marks each. Each question can have 3 parts of 2/3/4/5/6 marks.	Bloom's taxonomy (BT) level of the question should be L3 and above.		

******* ***Individual faculty will be entering the details***

****** Individual faculty shall identify the assessment method from FISAC Assessment method (Table 1 below) and fill in the details.***

NOTE: ***Information provided in the Table 1 is as per the In-semester assessment plan notified by Associate Director (Academics).***

Lesson Plan

L No	Topics	CO Addressed
0	*To address OBE philosophy towards NBA and IET accreditation followed by a discussion on Course Plan, Course Outcomes, CO-PO Mapping and Blooms Taxonomy, with prerequisites for the course, if any.*	
1	Introduction to the Course, Structure, Scope, Assessment and evaluation	1
2	Introduction to the system design approach and need of HDL	1
3	Coding Style: Lexical Conventions	1
4	Ports and Modules	1
5	Operators	1
6	Structural Modeling and examples	1
7	Data Flow Modeling and examples	1
8	Behavioral level Modeling and examples	1
9	Tasks & Functions and examples	1
10	System Tasks & Compiler Directives - Test Bench.	1
11	Verilog Modelling of Combinational circuits - Adders	3
12	Verilog Modelling of Combinational circuits - Multipliers	3
13	Verilog Modelling of Combinational Circuits - Comparators	3
14	Verilog Modelling of Sequential Circuits - Flip Flops	3
15	Verilog Modelling of Sequential Circuits - Shift Register	3
16	Verilog Modelling of Sequential Circuits – Synchronous Counter	3
17	Verilog Modelling of Sequential Circuits – Asynchronous Counter	3
18	Examples solving and discussing combined design approach	3
19	State diagram-state table –state assignment-choice of flipflops	4
20	Timing diagram –One hot encoding Mealy and Moore state machines	4
21	Mealy and Moore state machines - State minimization	4
22	Sequence detector	4
23	Sequence detector continue	4
24	Serial adder	4
25	Examples solving and discussing advanced design approaches	4
26	Vending machine using One Hot Controller	4
27	FPGA Architectural options, coarse vs fine-grained	2
28	vendor-specific issues (emphasis on Xilinx FPGA)	2
29	SRAM and EPROM-based FPGAs	2
30	FPGA logic cells	2
31	interconnection network and I/O Pad.	2
32	Traffic light Controller	5
33	Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD,	5
34	Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD,	5
35	Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD,	5
36	Embedded Processor Hardware Design.	5

Faculty members teaching the course (if multiple sections exist): Not Applicable

References:

Textbooks	• **M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2000.** • **Peter Ashenden, "Digital Design using Verilog", Elsevier, 2007.** • **Clive Maxfield, "The Design Warriors' Guide to FPGAs", Elsevier, 2004** • **Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis" Prentice Hall, Second Edition, 2003.** • **Wayne Wolf, "FPGA Based System Design", Prentices Hall Modern Semiconductor Design Series, Pearson, 2004.**
Self-Directed Learning: Simulation of various designs using Xilinx Software	
Research Literature/ Case Studies	• •
NPTEL/Coursera/any MOOC-based material	• •

Submitted by: Dr. Amit Kumar Goyal

(Signature of the faculty)

Date: 01/01/2025

Approved by: Prof. (Dr.) Pallavi R Mane

(Signature of HoD)

Flexible In-semester Assessment Component (FISAC):

i) The FISAC 1 & FISAC 2 may be any of the types given in Table 1. However, the two components should be of different type.

ii) The type of assessment should be informed to the students well in advance.

iii) Syllabus for the last component of In-semester Assessment (ISAC) i.e. FISAC 2 should cover the topics mentioned for self-study if any / topics which are not covered till MISAC 4: In-Semester Exam 2.

Table 1: Flexible In-semester Assessment Component (FISAC)

No	Type	Description
A.	Quiz/MCQs	Same as MISAC 2: Quiz/MCQs
B.	Surprise Assignment	Same as MISAC 3: Surprise assignment.
C.	Take Home Assignment	*10 questions are to be given to each student. *Questions must be of Blooms Taxonomy Level 3 for first year and Level 4 for higher semesters. *Questions are to be given TWO weeks in advance. *Students have to write the answers to all the questions.
D.	Group Assignment	*The students are to be grouped in such a way that there are 3 – 4 students in each group. *Each group is to be given one question. *The questions should be of Blooms Taxonomy Level 4 for first year and Level 5 for higher semesters. *Questions are to be given TWO weeks in advance. *The questions may be in the form of case studies, design, report writing, etc.
E.	Seminar	*Students may be given the topics for seminar relevant to the course of study. *Topics are to be given TWO weeks in advance. *Should be of Blooms Taxonomy Level 4 for first year and Level 5 for higher semesters. *Topics should be related to the courses of study. *Topics should be in the field of recent developments in the courses of study. *Students have to collect the data regarding the seminar topic and submit a report. *Students should make a presentation for about TEN minutes using Power Point.
F.	Quiz / Assignment based on invited talks	*Faculty have to arrange for the invited talk in the emerging areas in the courses of study. *Quiz / Assignment is to be conducted on the topic of the invited talk. *Questions should be at Blooms Taxonomy Level 4 for first year and Level 5 for higher semesters.
G.	Development of Software / Apps	*Faculty has to define the problem statement. *Problem Statements are to be given TWO weeks in advance. *Should be at Blooms Taxonomy Level 4 for first year and Level 5 for higher semesters. *Students have to develop the software / mobile apps using the appropriate software language / platform.
H.	Mini Project	*Faculty has to define the problem statement. *Problem Statements are to be given TWO weeks in advance. *Should be at Blooms Taxonomy Level 4 for first year and Level 5 for higher semesters. *Students have to develop prototypes.