Quiz For C2(COA-2021)

1 message

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Quiz For C2(COA-2021)

This quiz is 50 minutes long .

There are 20 questions in this quiz . Worth 25 marks .

Memory mapping based question carry 2 marks(mentioned with questions).

There are 5 parts in this paper, submit button will appear at last page .

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Given a block-set associative cache memory comprising of sets made of 4 blocks for a total of 32 blocks where each block is made of 256 eight bit words and the main memory comprises of 16200 blocks, how many bits would be required to address the main memory?

- ○ 22

- ○ 21
- ○ 20
- ◉ Cannot be determined

What is the avg time required for memory access with a TLB miss rate of 2% and a cache miss rate of 8% given that the cache needs 2 clock cycles and the DRAM needs 30?

- ○ 3.8
- ○ 6.2
- ◉ 7.0
- ○ 3.5

What is the control statement for $Q_0Q\text{-}_1$ which points to A=A+B?

- ○ 10
- ◉ 01
- ○ 00
- ○ 00/11

What will be value of registers in blank space denoted by _____

C code:

```
sum = 0;
for (i=1; i <= 10; i++) sum = sum + i;
```

- sum in $s3, i in $t1

Compiled MIPS code:

```
      addi $s3, $zero, 0
      addi $t1, $zero, 1
loop: add $s3, $s3, $t1
  addi $t1, $t1, _____
  sle $t2, $__, 10
      bne $t2, $zero, loop
```

- (●) $1, $t1
- ( ) $0,$t1
- ( ) 0,t1
- ( ) 0,$t1
- ( ) 10,$t1
- ( ) $t1,0

What will be the registers values for space denoted by _____

- **For The C statement:**

```
if (i == j) f=g+h;
    else f=g-h;
```

  - **Assume the following MIPS register mapping:**

    f: $s0, g: $s1, h: $s2, i: $s3, j: $s4

- **Mips Instructions:**

```
    beq $s3,$s4, True
    sub $s0,$s1,$___
    j Exit
True: add $s0,$s1,____
Exit:
```

- s2,s2
- $s2,$s1
- $s1,s2
- s1,$s1
- s2,$s2

Find out register values for fill in the blanks denoted by ____.

```
int *sumarray(int a[],int b[]) {
    int i, c[100];
    for(i=0;i<100;i=i+1)
      c[i] = a[i] + b[i];
    return c;
}
```

```
        addi  $t0,$a0,400   # beyond end of a[]
        addi  $sp,$sp,-400  # space for c
        addi  $t3,$sp,0     # ptr for c
        addi  $v0,$t3,0     # $v0 = &c[0]
Loop:   beq   $a0,$t0,Exit
        lw    $t1, 0(___)   # $t1=a[i]
        lw    $t2, 0(___)   # $t2=b[i]
        add   $t1,$t1,$___  # $t1=a[i] + b[i]
        sw    $t1, 0($t3)   # c[i]=a[i] + b[i]
        addi  $a0,$a0,4     # $a0++
        addi  $a1,$a1,4     # $a1++
        addi  $t3,$t3,4     # $t3++
        j     Loop
Exit:   addi  $sp,$sp, 400  # pop stack
        jr    $ra
```

- ○ a0,a1,1
- ○ a0,a1,t2
- ◉ $a0,$a1,t2
- ○ $a1,$a1,t2
- ○ $a0,$a0,t1

For special-purpose operating system _____ page replacement is used and it have to satisfy _____ algorithms.

- ○ Optimal Page Replacement, Queue
- ◉ Optimal Page Replacement , Stack
- ○ LRU, Queue
- ○ LRU, Stack

A reference string for page is in order 1, 2, 4, 5, 2, 1, 2, 4 and there are 3 page frames in main memory already has the pages 1 and 2 what will be no of page faults if LRU page replacement is used.(page 1 brought earlier than page 2).

- [ ] 3
- [ ] 6
- [ ] 5
- [x] 4
- [ ] None of these

Following are the reference string for page replacement algos with frame size 3 how many page fault will occur when using LRU , Optimal page replacement policy. Reference string { 1,2,1,3,7,4,5,6,3,1}

- [ ] 7,8
- [x] 9,7
- [ ] 7,9
- [ ] 8,7
- [ ] 0

For Asynchronous data transfer requires that control signals be transmitted between the communicating units to indicate the time at which data is being transmitted. This Problem can be solved using

- [ ] Strobe
- [ ] HandShaking

- Message passing
- (●) Strobe, handshaking
- Strobe, message passing
- handshaking, message passing

HANDSHAKE allows : 1)arbitrary delays from one state to the next 2) Permits each unit to respond at its own data transfer rate 3) The rate of transfer is determined by the faster unit 4) provides a high degree of flexibility and reliability

- 1 , 3, 4
- (●) 1 , 2 ,4
- 1, 2 , 3
- 2, 3, 4
- all 1,2,3,4

2 marks questions.

Consider a direct mapped cache of size 64 KB with block size 64 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively-

- 10, 17
- (●) 10, 16
- 15, 17
- 5, 17

2 marks questions.

Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 64 bytes. Assume that a direct mapped cache having 1024 cache lines is used with this machine. The size of the tag field in bits is _____.

- ○ 12
- ○ 13
- ○ 14
- ○ 15
- ◉ 16

In Direct addressing memory technique main memory is 128 kb and cache size is 16 kb block size is 256 byte then bit used for tag and block offset will be:

- ○ 3,7
- ◉ 3,8
- ○ 4,7
- ○ 4,8

2 marks

A 4 way set associative cache memory with 16 KiloBytes using 8 word block size, 32 bits are word length, 4GB Physical address space , then tag bit size will be _____ .
###2 marks question

- ○ 19
- ◉ 20
- ○ 18
- ○

16

2 marks

A system have 8GB memory with 64 bit word size. Each block can store 16 words .Then a direct-mapped with word level addressing used with cache of 128 blocks address format will _____ . #####2 marks question

- (●) 19 – 7 –4
- ( ) 18 – 8 –4
- ( ) 19 – 6 –5
- ( ) 19 - 5 -6

2 marks

A system have 8GB memory with 64 bit word size. Each block can store 16 words .If using a 4-way set associative cache then address format will _____ . ######2 marks question

- ( ) 18 – 5 – 7
- ( ) 18 – 7 – 5
- ( ) 21 – 6 – 3
- (●) 21 – 5 – 4

If memory access takes 20 ns with cache and 110 ns with out it, then the ratio (cache uses a 10 ns memory) is

- ( ) 95
- ( ) 80

- [x] 90
- [ ] 85

Cache memory works on the principle of

- [ ] Locality of data
- [x] Locality of reference
- [ ] Locality of memory
- [ ] Locality of reference & memory

The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be

- [x] (812) base 10
- [ ] (-12) base 10
- [ ] (12) base 10
- [ ] (-812) base 10