SEMI CONDUCTOR THEORY

	Si	~~Ge~~	
Leakage →	↓	↑	
Peak Inverse Voltage ← PIV →	↑	↓	⇒ (Reverse Breakdown is High for Si)
Availability →	↑	↓	
below this, Quantum Confinement ← Exciton Bohr Radius →	↓	↑	
Bandgap →	↑	↓	⇒ (High Temperature sustainability for Si)

Intrinsic (pure) Semiconductor : ———

✓ Si (14) → $\underbrace{\boxed{1s^2\ 2s^2\ 2p^6}}_{\text{Core}}$ $\underbrace{3s^2\ 3p^2}_{\text{valence electrons}}$

× Ge (32) → $\underbrace{1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6}_{\text{Core}}$ $\underbrace{3d^{10}}_{\text{Semi core}}$ $\underbrace{4s^2\ 4p^2}_{\text{Valence electrons}}$

Si has 4 valence electrons.

Si (4) — Si (4)

Ionic Bonding

$\overset{+}{Na}(11)$ $\xrightarrow{1e^-}$ $\overset{-}{Cl}(17)$

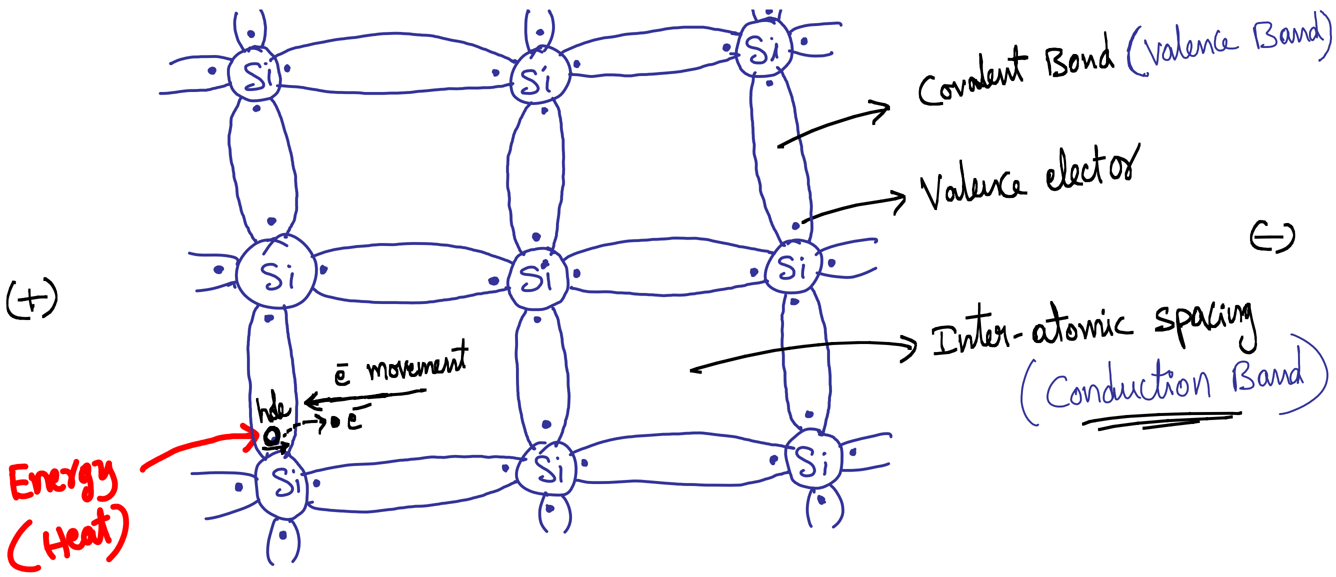
(10e^-) (18e^-)

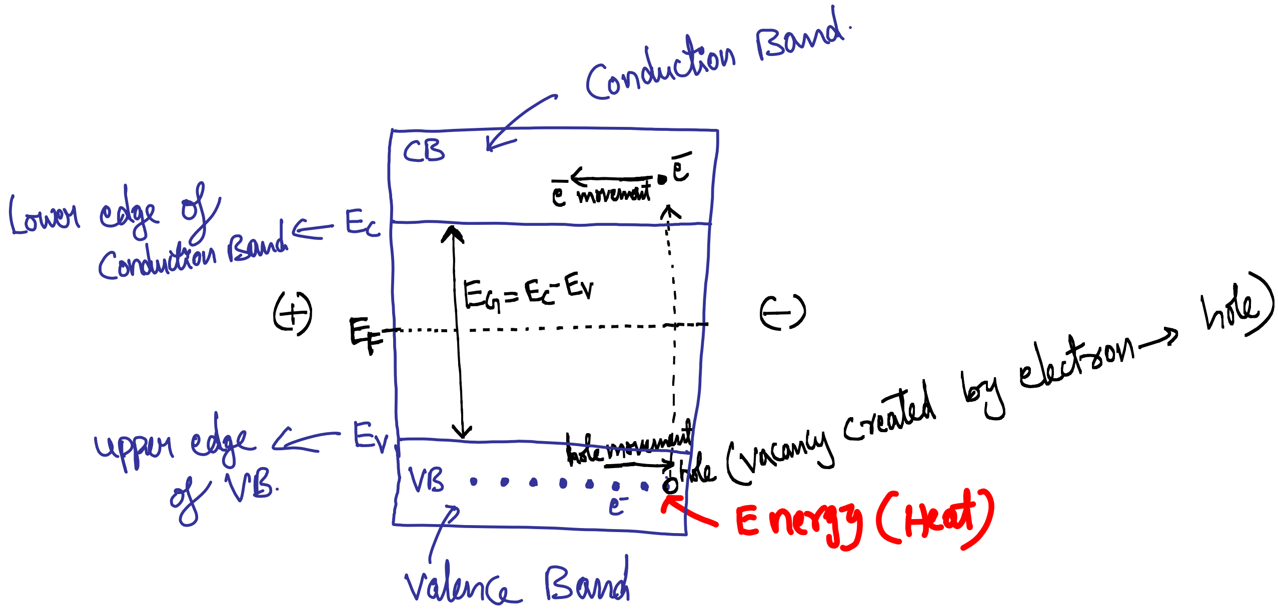
1:7 1:7

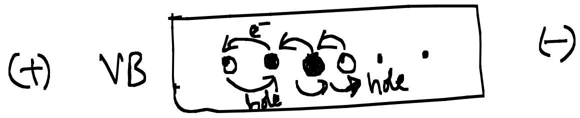
- Ionic Bonding (High Difference in electroneg.)
- Covalent Bonding
- Dative Bonding
- Hydrogen Bonding
- Metallic Bonding
- ⋮

Si: Loss : Gain = 4:4 = 1:1

So, Covalent Bonding in Si.







* movement of electrons in VB Creates the movement of holes
* Electron mobility >> Hole mobility

* <u>Fermi level:</u> maximum occupancy Energy level. All states below the fermi level are filled with ē, All states above fermi level are Empty.

movement

	Si	Ge
Hole mobility (μ_p) →	500 cm^2/Vs	1800 cm^2/Vs (units: $cm^2/V\text{-}s$)
$\bar{e}$ mobility (μ_n) →	1300 cm^2/Vs	3800 cm^2/Vs [(centimeter)^2 / volt-second.]
Band gap (E_G) →	1·21 eV (0°K) 1·1 eV (300°K)	0·78 eV (0°K) 0·72 eV (300°K)
Intrinsic Concentration (n_i) →	$1.5 \times 10^{10} / cm^3$ (300°K)	$2.5 \times 10^{13} / cm^3$ (300°K)

How many atoms are possible per unit volume.

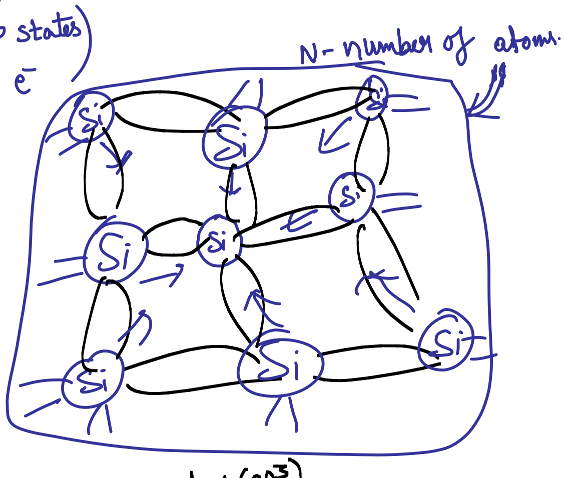
Energy Bands formation in Si – Crystal :—

$Si = [Ne]\, 3s^2\, 3p^2$

$3s^2$ → $\boxed{1\downarrow}$ → (2s states, 2 $\bar{e}$)

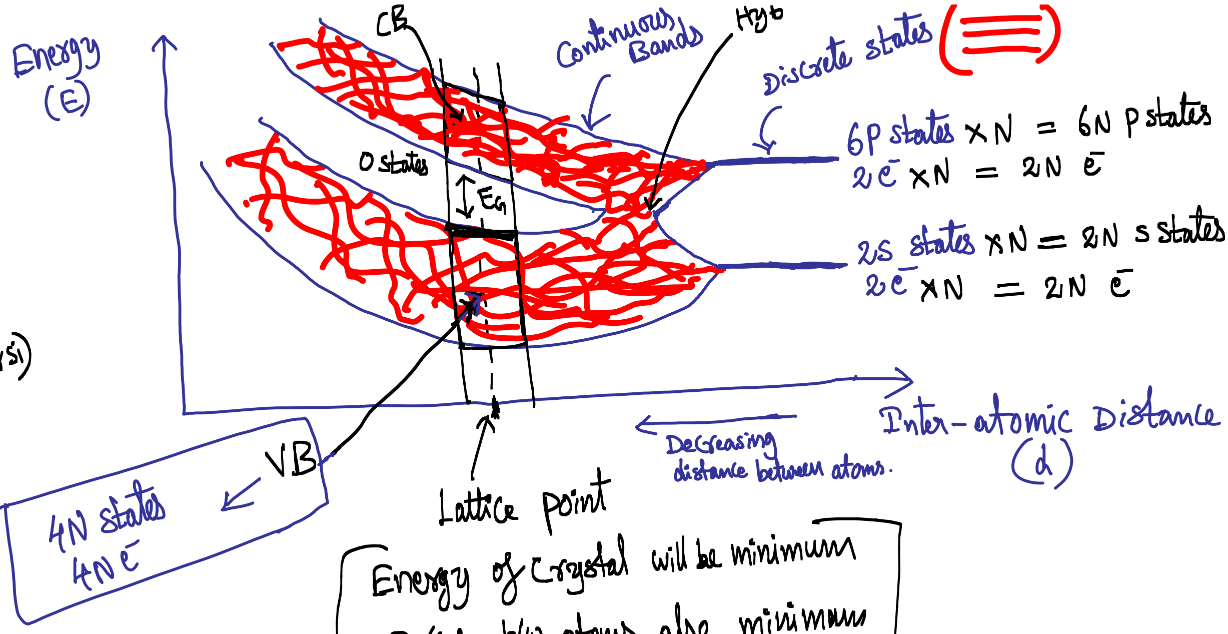
$3p^2$ → $\boxed{1\_ \mid 1\_ \mid \_\,\_}$ → (6p states, 2 $\bar{e}$)

* one Energy state can accommodate only one $\bar{e}$.
* These states they exist in pairs.



$\boxed{\text{4N states } 0\bar{e}}$

...ridization (sp^3)



$E_G = 1.21\ eV$
(0K for Si)

Energy of Crystal will be minimum
Forces b/w atoms also minimum

Extrinsic Semiconductors :-

p-type SC

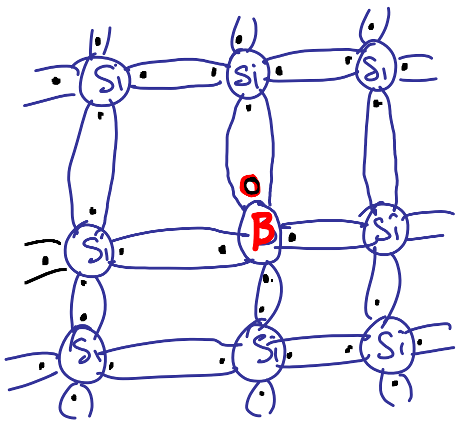
Add Trivalent atoms (valence-3)

Ex: B, Al, Ga, In
Dopants used.

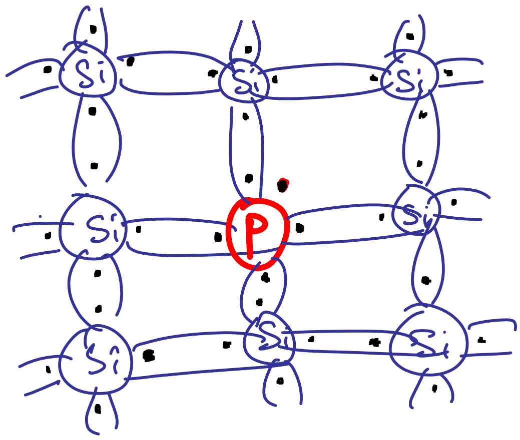
n-type SC

Add pentavalent atoms (valence-5) to pure sc.

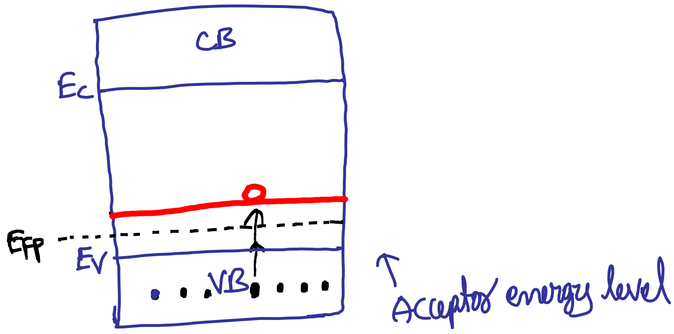
Ex: P, As, Sb, Bi

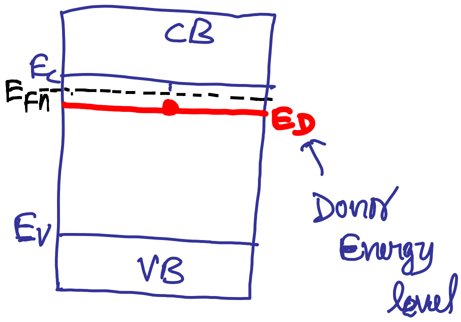


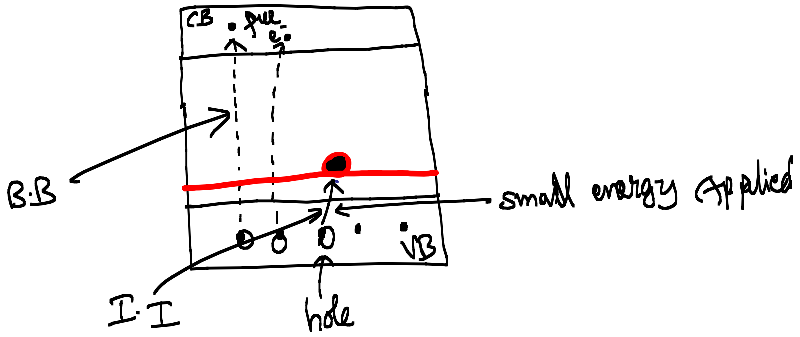
p-type SC

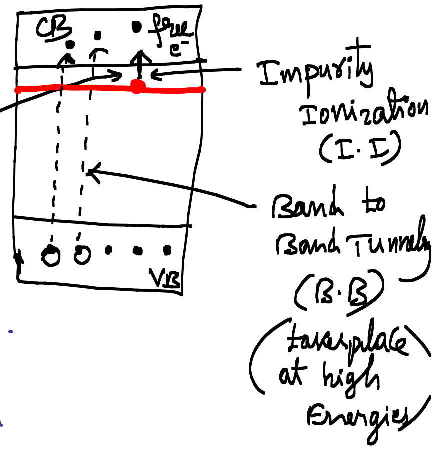


n-type SC



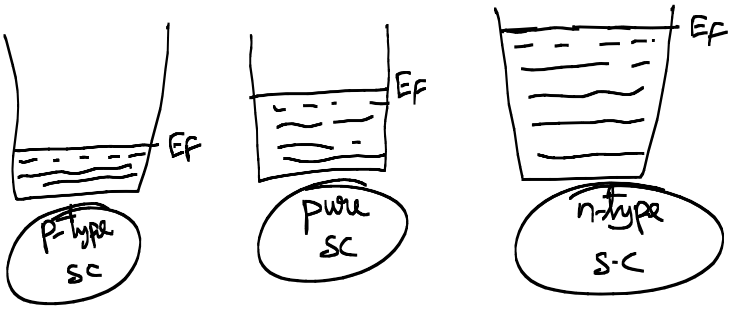


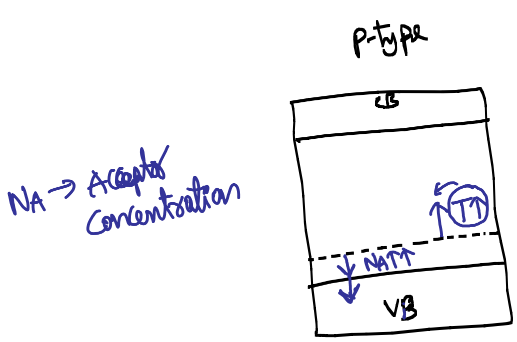


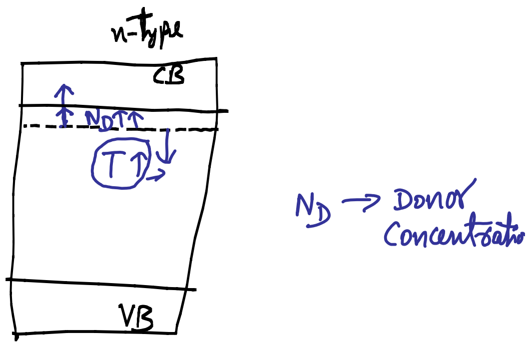


I.I → from VB to E_A (or) from E_D to CB tunneling of $\bar{e}$.

B.B → from VB to CB tunneling of $\bar{e}$.

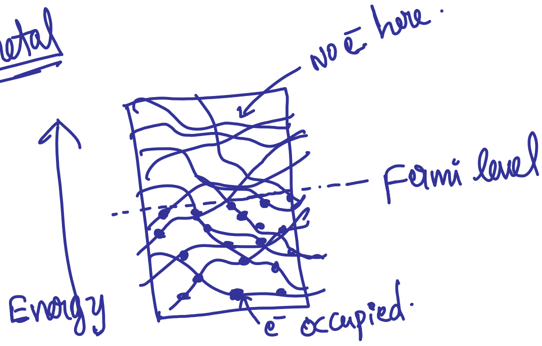






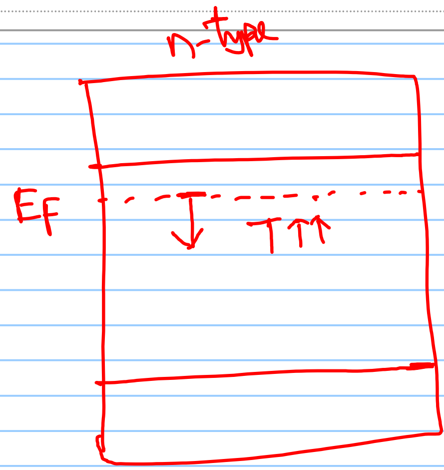
T → Temperature

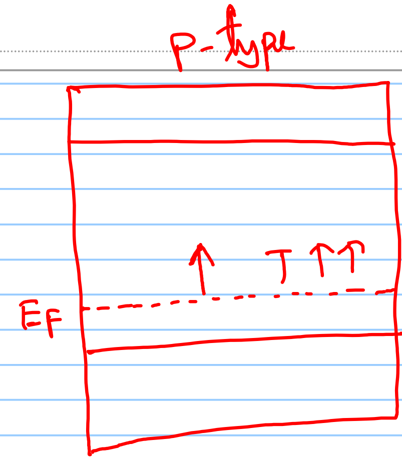
Metal

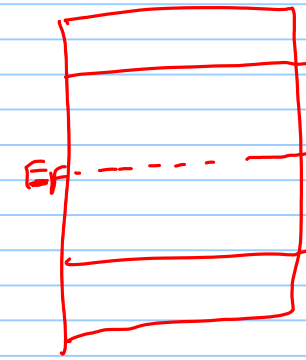


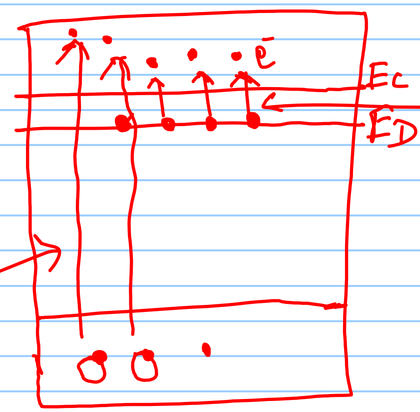
Book Integrate Electronics – Millman & Halkias.

Note Title 2021-01-11









(small amount of energy)
Impurity Ionization
(I.I)
⇓
produces only majority carriers

(for large energy)
Band to Band
Tunneling
(B.B)

⇓ Majority & Minority carriers.

Note:

Intrinsic sc : no. of free electrons = holes ✓

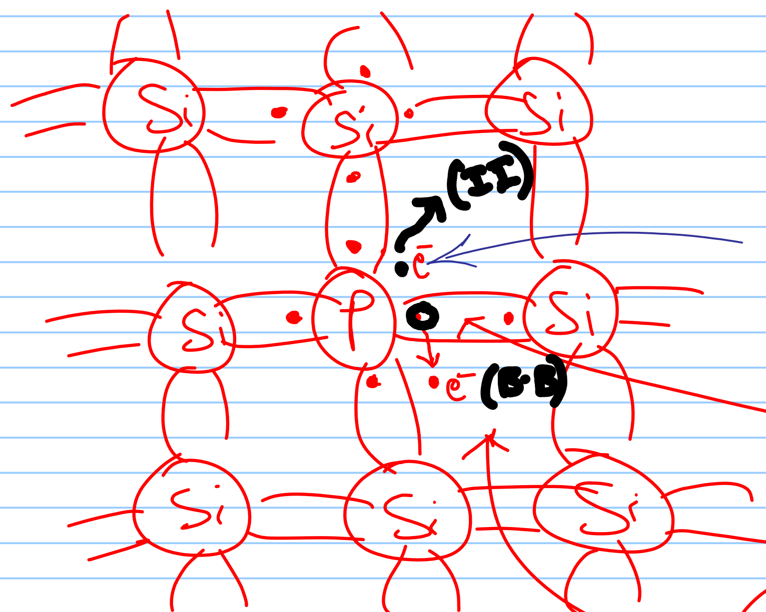
n-type sc : no. of free electrons >> holes

p-type sc : no. of holes >> free electrons.

Temperature | Extrinsic semi-conductor eg: (n-si) |
--- | --- | ---
T (small) → | 100 $\bar{e}$ (I.I) | 0 holes
T ↑ → | 100,000 $\bar{e}$ (B.B) + 100 $\bar{e}$ (I.I) = 100,100 | 100,000 holes (B.B)
T ↑↑ → | 900,000 $\bar{e}$ (B.B) + 100,100 $\bar{e}$ = 10,00,100 $\bar{e}$ $\approx$ | 900,000 holes (B.B) + 100,000 holes = 10,00,000

At High temperatures, In extrinsic S.C

$\boxed{\text{no. of free electrons} \approx \text{no. of holes}}$

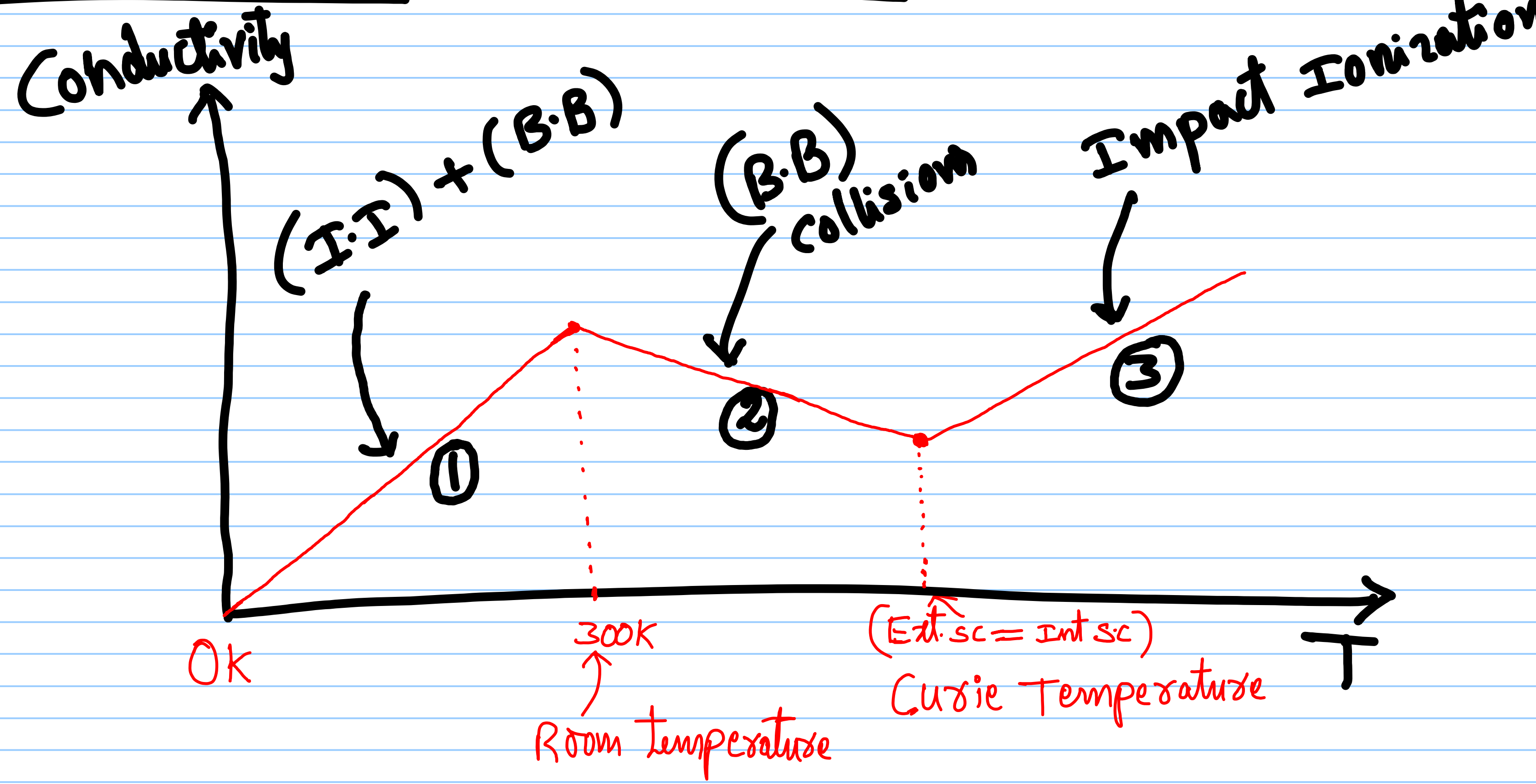


small energy
(extra e will become free)

Bonds
(valance Band)

(Conduction Band)

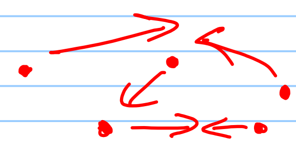
Temperature Impact on Conductivity of Ext. SC :-



(1) mainly Impurity Ionization (I.I) & some Band to Band Tunneling (B.B)

These carriers cause increased conductivity.

(2) After 300K, B.B dominates & the collisions among the carriers will increase.

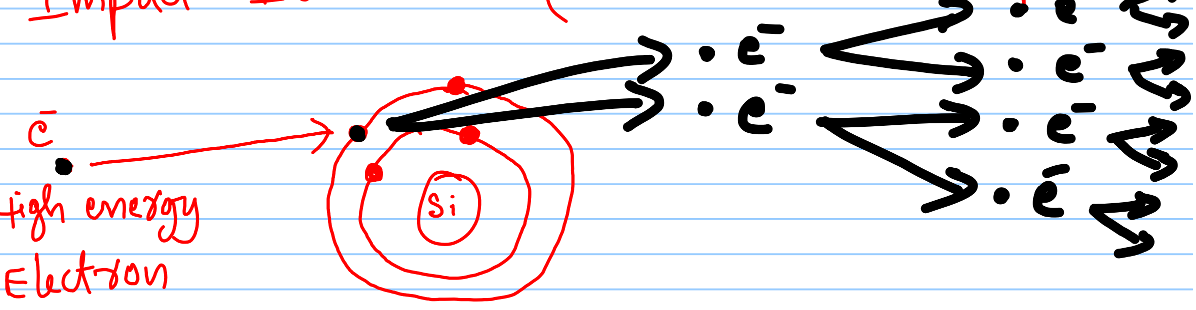


At curie temperature, the minority carriers equal the majority carriers (almost). Thus the

the extrinsic SC behaves like a Intrinsic SC.

③ After Curie temperature,

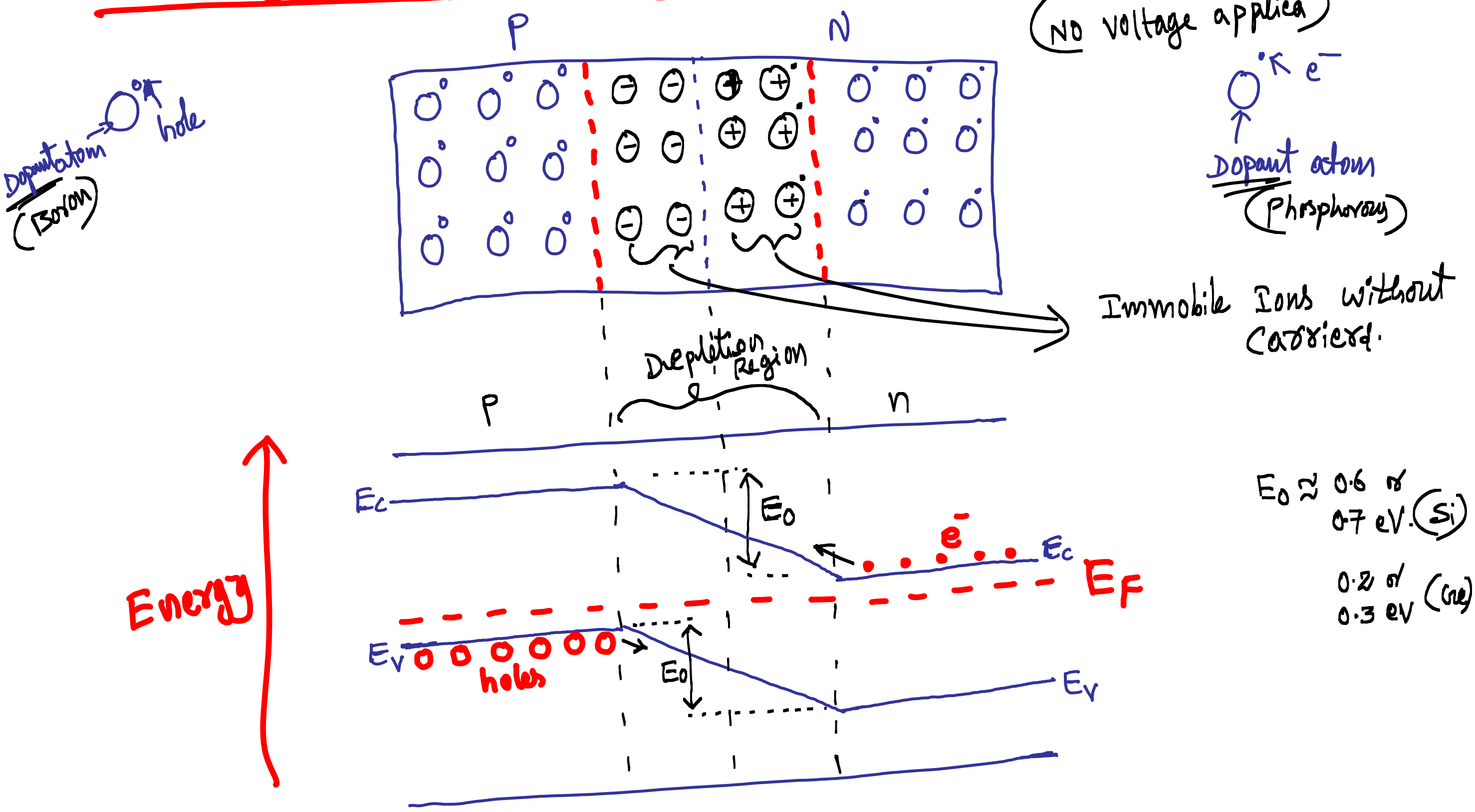
Impact Ionization (or Carrier multiplication)



The free electrons gain very high energy, they Collide with the bounded electrons & frees them. This is called "Carrier multiplication" (or) "Impact Ionization".

Energy Band Diagram of PN-Diode :—

(No voltage applied)

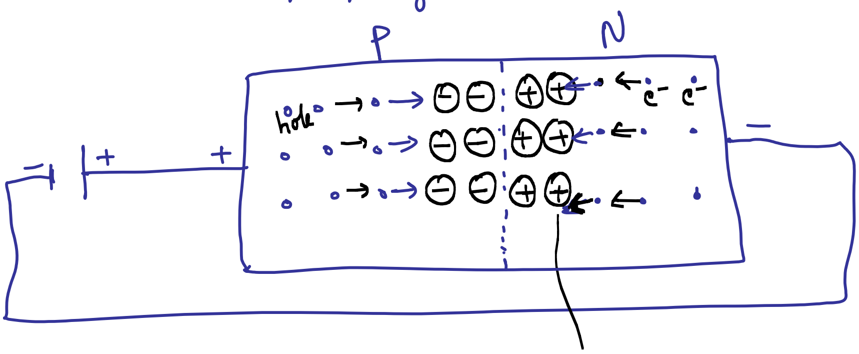


Note: Fermi level in any electronic Device at equilibrium & no applied voltages is always Constant throughout the Device.

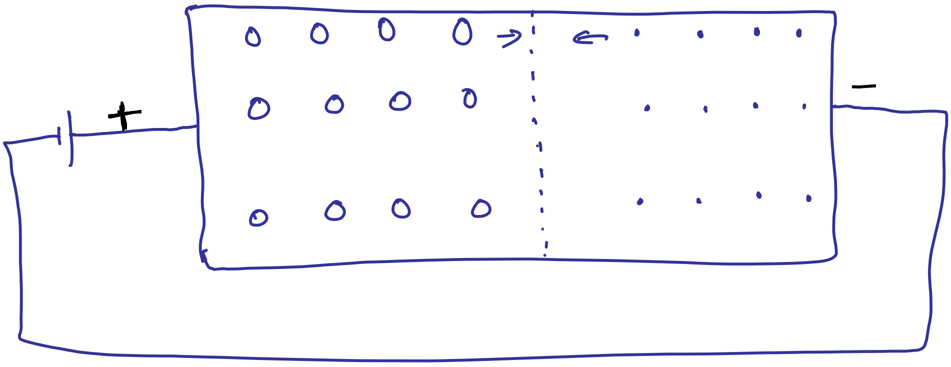
Forward Bias :—

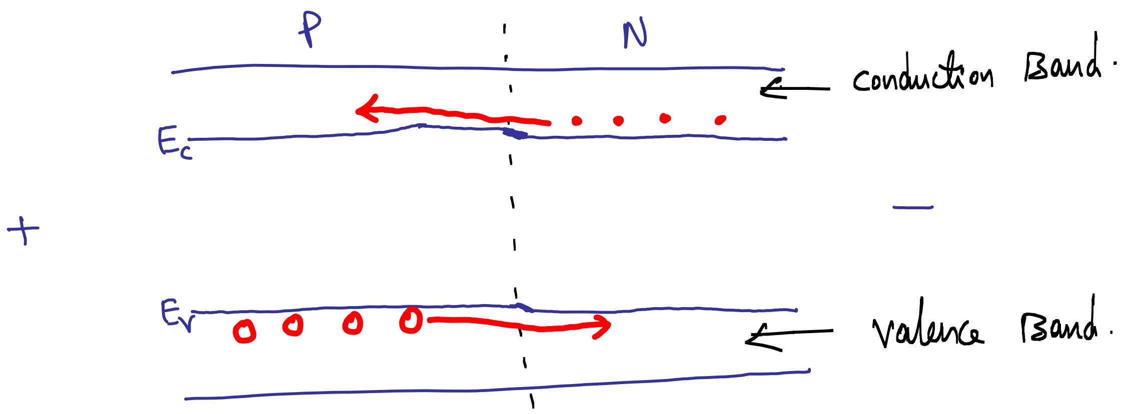
+ve voltage → P-side (Anode)

−ve voltage → N-side (Cathode)



Earlier Lost an electron → Turned into Ion
Now it will an electron → Turns to normal Dopant.





Note:

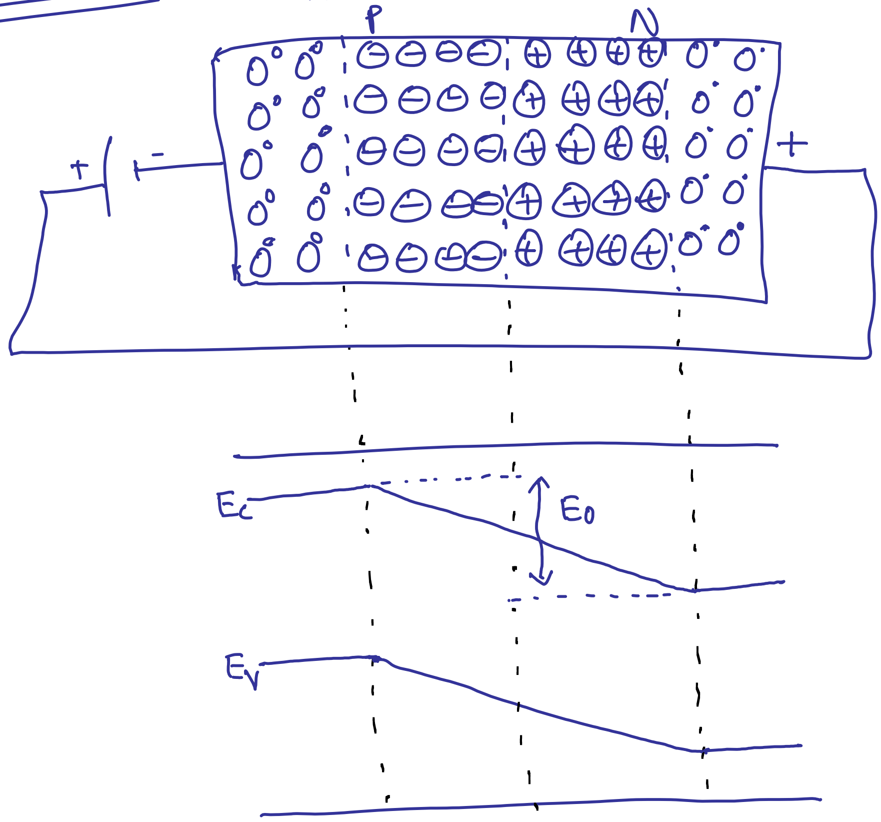
1. electrons conduct in the Conduction Band.
2. Holes will conduct in the valence Band.
3. Current Direction is opposite to e^- Direction.
4. current " equal in direction to hole.

5. Current because of e^- > Current because of hole.

because $\mu_n > \mu_p$.

Reverse Bias :-

$-ve$ voltage $\rightarrow$ P-side
$+ve$ voltage $\rightarrow$ N-side



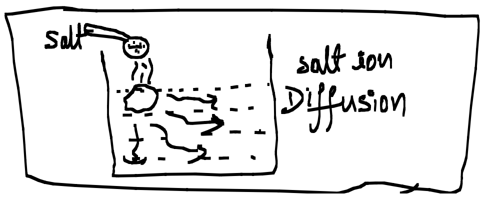
* In FB, E_0 decreases, because shift between the Band edges decreases.

* In RB, E_0 Increases, because shift between the Band edges increases.

Note :-

* Drift $\rightarrow$ pulling of carriers by the applied voltage.

Diffusion $\rightarrow$ movement of carriers from High concentration region to low concentration.



Various Junctions of Diode :—

① Step Junction

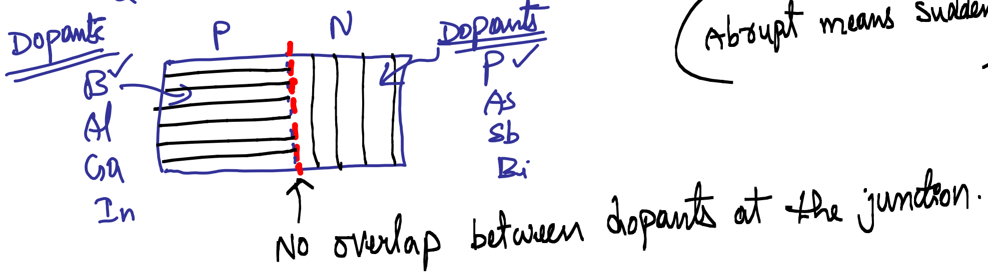
② Graded "

③ Step - Graded "

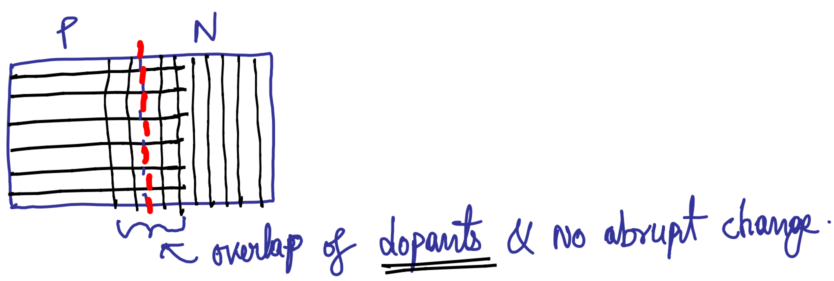
④ Linearly - Graded "

Step Junction : Abrupt change of doping type at the Junction. & No overlap between Dopants.

(Abrupt means sudden.)



Graded Junction: A overlap between the dopants at the Junction.

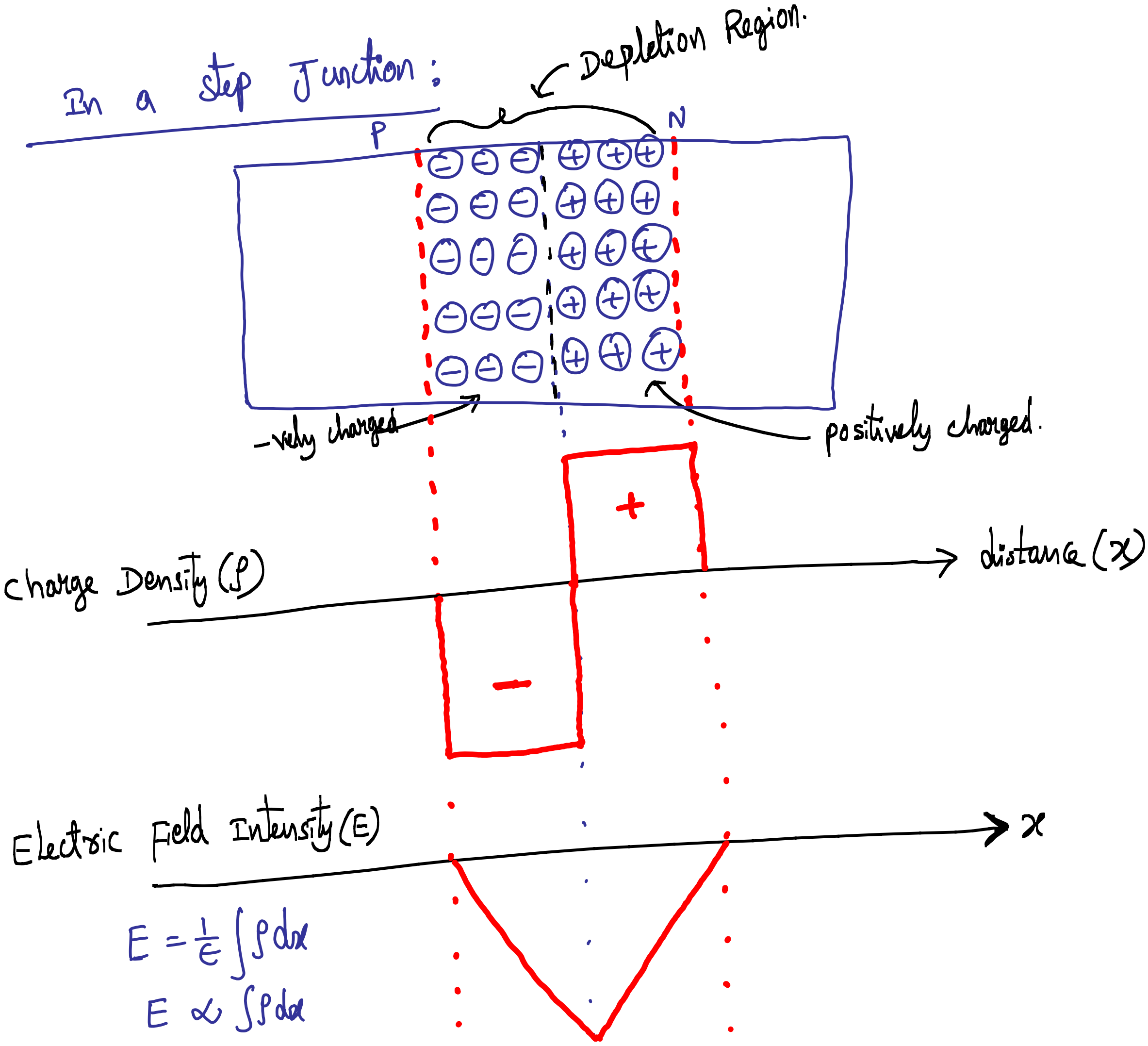


Step-Graded Junction: A step junction where Dopant concentrations on P-side & N-side are not same.

Linearly-Graded Junction: A Graded junction where the charge density profile varies linearly across the Depletion Region.

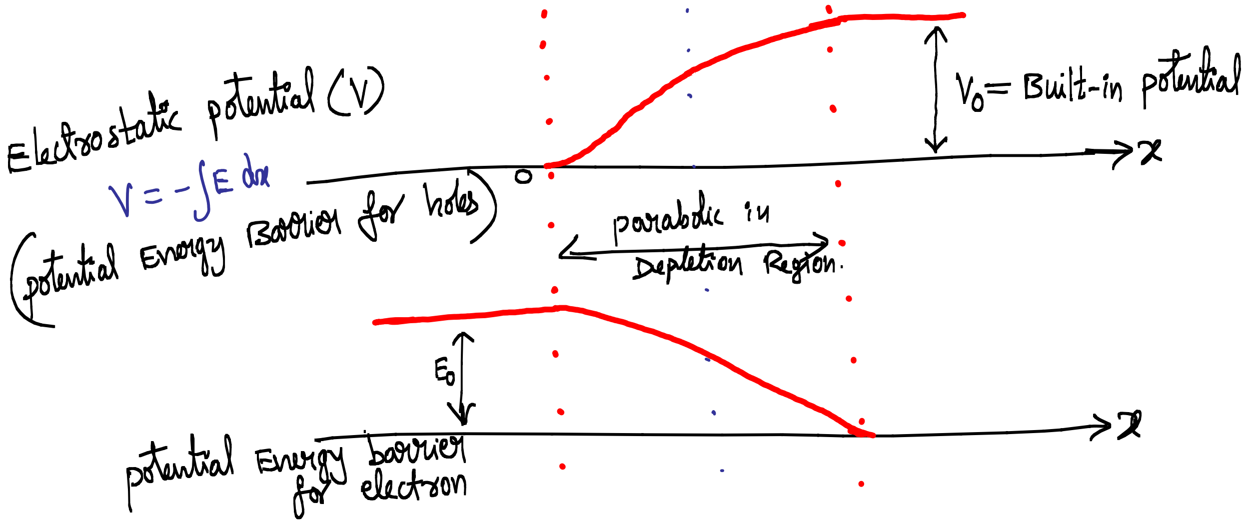
→ Charge Density (ρ), Electric Field Intensity (E) & Electrostatic potential (V) profiles:—

In a step Junction:



$E = \frac{1}{\epsilon}\int \rho\, dx$

$E \propto \int \rho\, dx$



Poisson's equation → applicable in the depletion Region.

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon} \quad \text{——— (1)}$$

$\rho \rightarrow$ charge density
$\epsilon \rightarrow$ permittivity
$V \rightarrow$ potential
$x \rightarrow$ distance (space)

General expression for Electric field Intensity,

$$E = -\frac{dV}{dx} \quad \text{——— (2)}$$

$E \rightarrow$ Electric field Intensity.

Get an expression for E in terms of ρ,

Rewrite eq (1),

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon}$$

$$\frac{d}{dx}\left(\boxed{-\frac{dV}{dx}}\right) = \frac{\rho}{\epsilon}$$

substitute eq (2) in above eq,

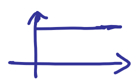
$$\frac{d}{dx}(E) = \frac{\rho}{\epsilon}$$

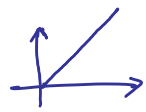
$$E = \int \frac{\rho}{\epsilon}\,dx$$

$$\boxed{E = \frac{1}{\epsilon}\int \rho \, dx}$$

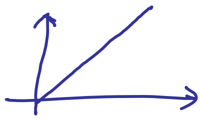
Rewrite eq(2), $E = -\frac{dV}{dx} \Rightarrow \boxed{V = -\int E \, dx}$

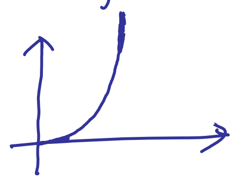
(1) $\int$ step function = Ramp function

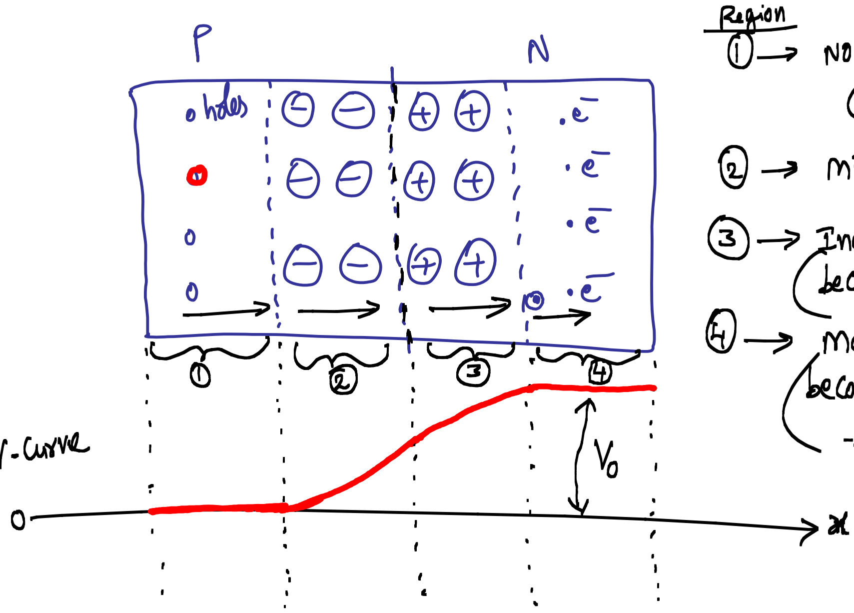




(2) $\int$ Ramp function = parabolic function







(potential Energy - Barrier for hole)

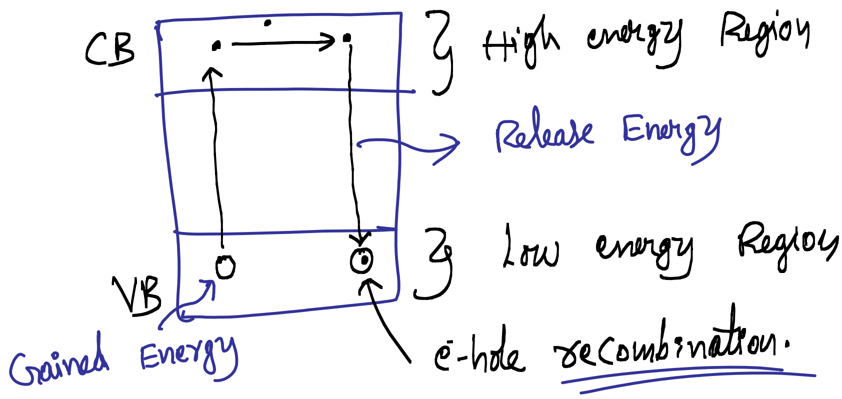
Region

1 → No opposition for hole. (zero barrier)

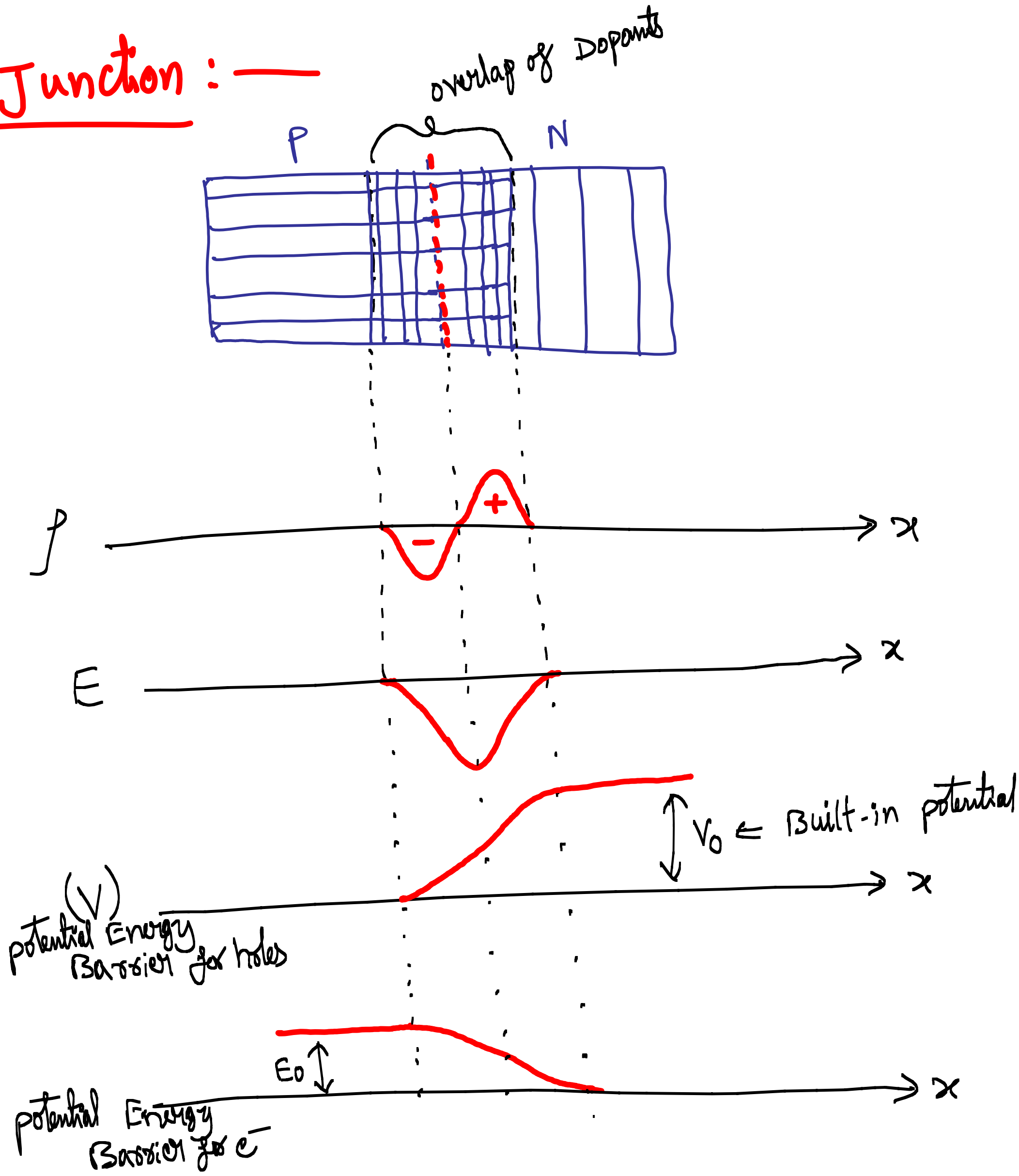
2 → minimum opposition for hole.

3 → Increased opposition for hole. (because of positive Ions)

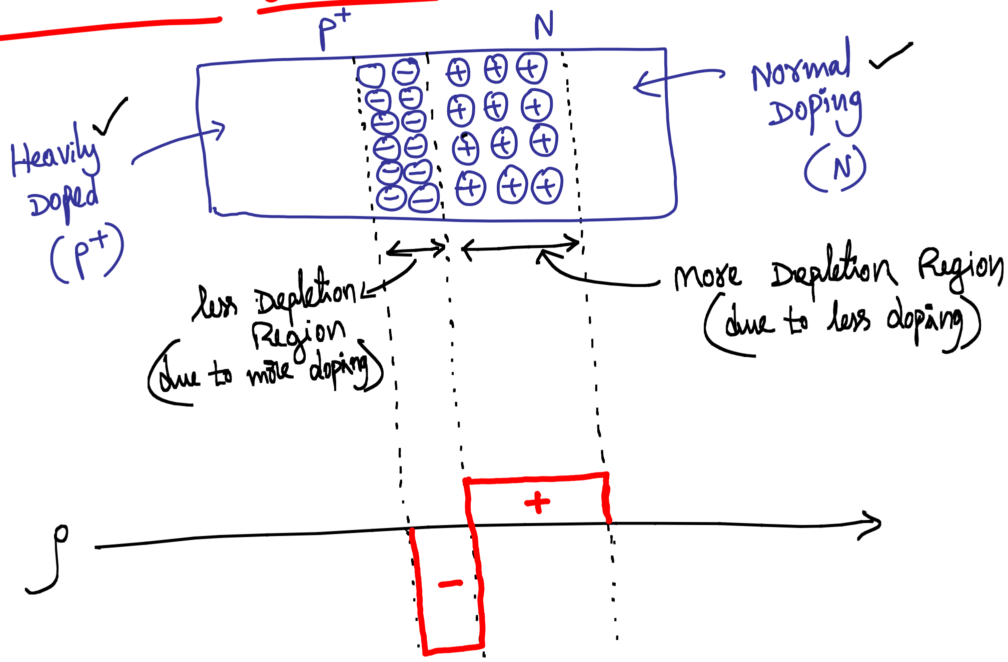
4 → maximum opposition for hole. (because of e-hole recombination in N-side)



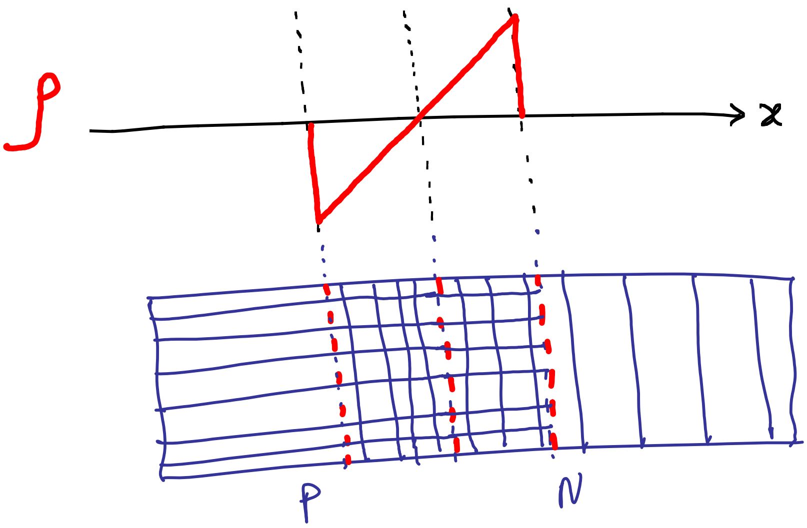
Graded Junction :—



Step-Graded Junction :-



Linearly-Graded Junction :-



Note:

(not 100% preferred)

Step Junction is usually preferred for Zener diodes.
Graded Junction is usually preferred for Normal PN diodes.
Step-Graded Junction is usually preferred for Emitter-Base Junction of Transistor.
Linearly-Graded " " " Collector-Base " .

→ Capacitances in Diode :—

Transition capacitance (C_T)

⇓

* prominent in Reverse Bias
* It is used to design Varicaps (or) Voltage variable capacitors. (or) Voltcaps.
* In ICs, the Varicaps are used for several applications like,
  - LC oscillator circuit
  - Amplifiers, etc.

Integrated circuit

Diffusion Capacitance (C_D)

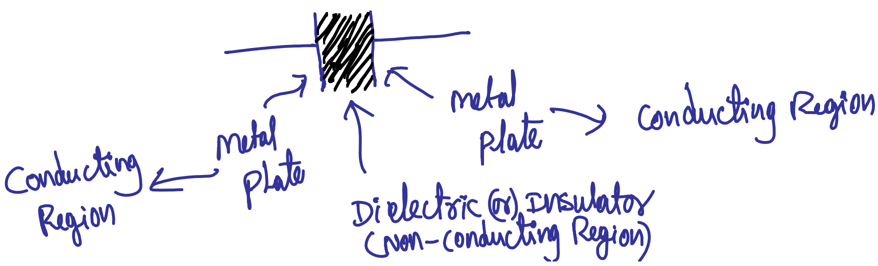
⇓

* prominent in Forward Bias
* So, time constant $(T = rC_D)$ is very low because, in forward bias the resistance(r) is very low.

Transition Capacitance (C_T) :—

It uses depletion Region (or) space-charge Region (or) Transition Region as a Dielectric.

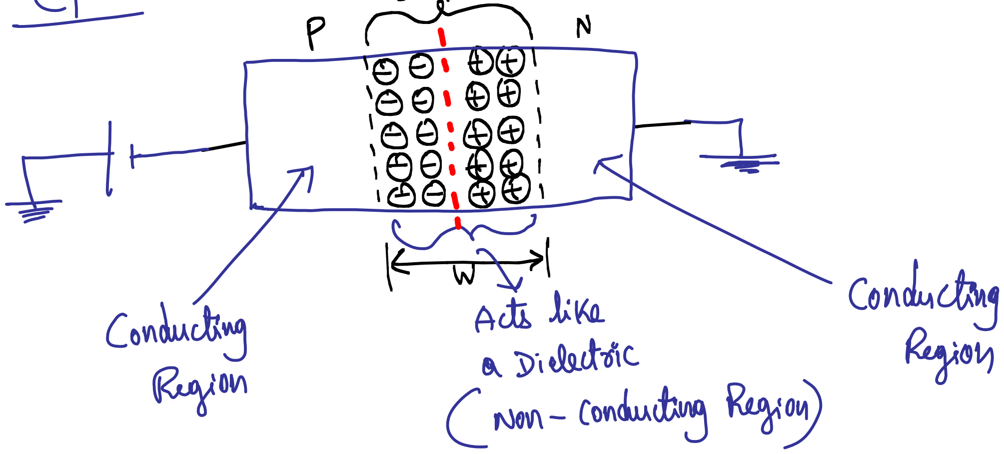
Parallel plate Capacitor—



$C = \frac{\epsilon A}{d}$ ← Area of cross section of metal plate

d ← distance b/w plates

C_T –



Here, between two conducting Regions a Non-conducting Region is Sandwiched so it acts like a capacitor.

$C_T = \frac{\epsilon A}{W}$ ← Area of cross section of diode.

ϵ ← permittivity

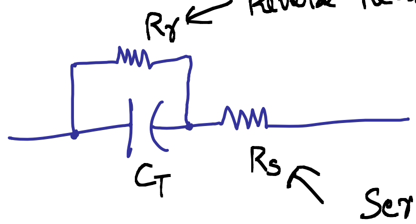
W ← Length of depletion Region.

$RB \uparrow \Rightarrow W \uparrow \Rightarrow C_T \downarrow$

Voltage variable capacitor –

Symbol

R_r ← Reverse Resistance



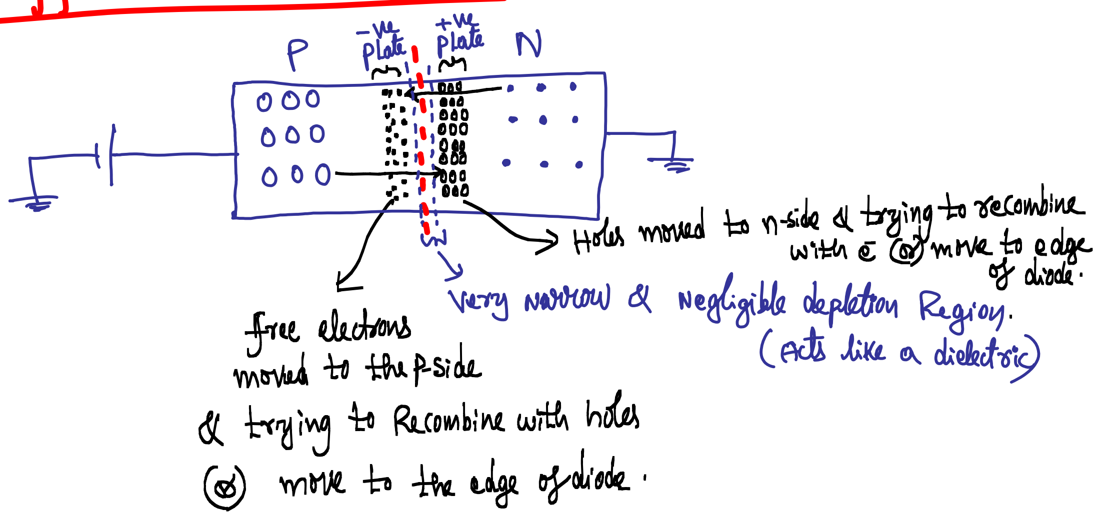
R_s ← Series Resistance

Equivalent Circuit

At $V_R = 4V$, the typical values of

$$C_T \approx 20\,pF$$
$$R_s \approx 8.5\,\Omega$$
$$R_r > 1\,M\Omega$$

Diffusion Capacitance (C_D) -



The capacitance thus formed is called diffusion capacitance.

$$C_D = \frac{\tau I}{\eta V_T}$$

$\tau \rightarrow$ life time of carriers.

$I \rightarrow$ current through diode.

$\eta \rightarrow$ Constant

$V_T \rightarrow$ Thermal voltage.

Here,

$$\tau = \tau_n + \tau_p$$

τ_n: life time of $\bar{e}$

τ_p: life time of holes.

$\eta = 1$, Germanium

$= 2$, silicon

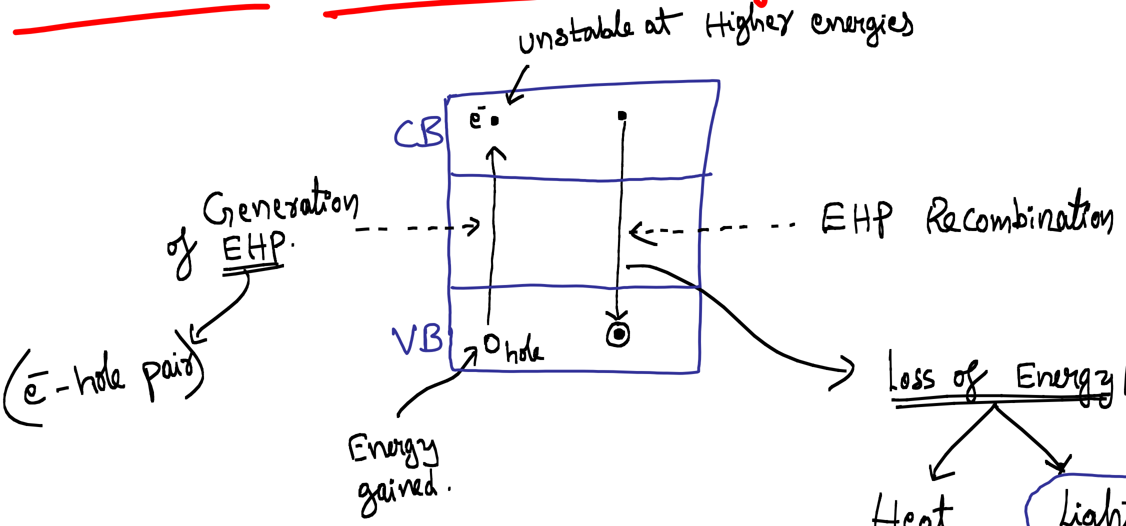
$$I = I_o \left(e^{V/\eta V_T} - 1 \right)$$

$\eta = 1$, Ge
$= 2$, Si

$$V_T = \frac{KT}{q} \simeq 26\,mV \text{ at } 300^\circ K.$$

T → Temperature (in Kelvin)
K → Boltzmann Constant
q → charge of carrier. (1.6×10^{-19} C)

Generation, Recombination & Lifetime :—



Loss of Energy Happens.

Heat | Light

Heat is generated by Indirect band-gap Semiconductors.

Ex: Si, Ge

Light is generated by Direct Bandgap SC.

Ex: GaAs
InGaAs

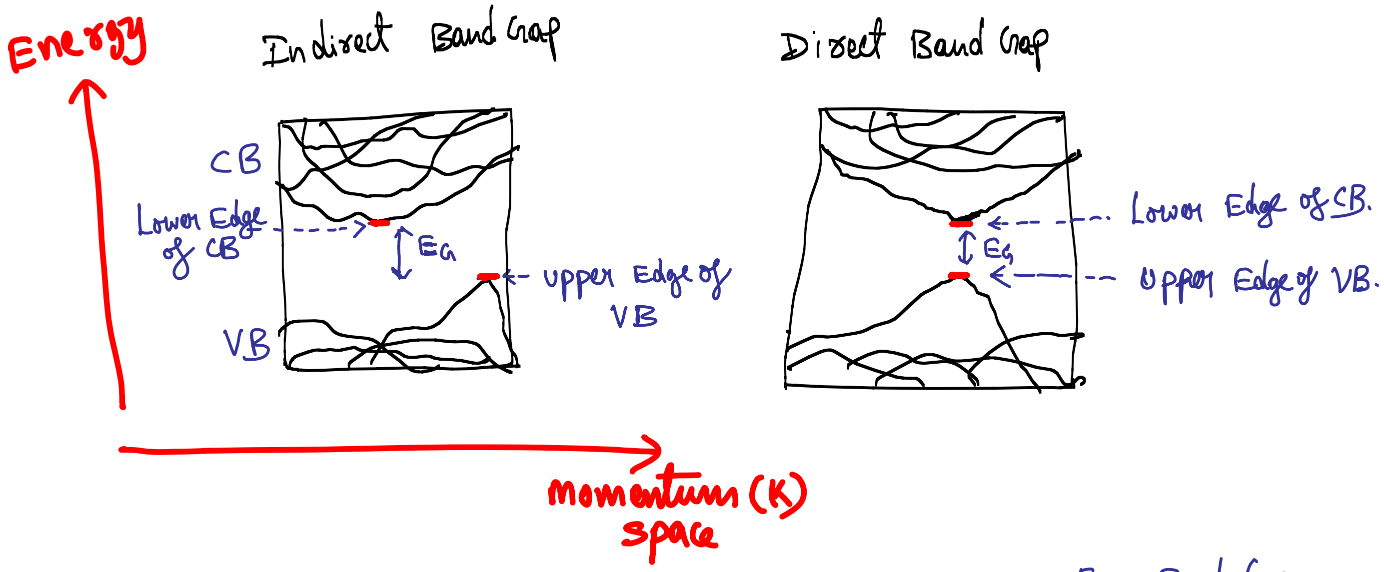
Gallium Arsenide (Compound SC)

Indium GaAs (Compound SC)

Applications:

LED ← Light Emitting Diode.

LASER → Light Amplification by Stimulated Emission of Radiation.



$E_G \rightarrow$ Band Gap.

Lifetime of Carriers → It is the time duration spent by electron in CB & hole in VB to support conduction before undergoing Recombination.

Life time of $\bar{e}$,

$$\tau_n = \frac{l_n^2}{D_n}$$

Lifetime of hole,

$$\tau_p = \frac{l_p^2}{D_p}$$

$l_n \rightarrow$ Diffusion length of $\bar{e}$

$l_p \rightarrow$ " " hole.

D_n & $D_p \rightarrow$ Diffusion Constants of $\bar{e}$ & hole.

→ Temperature effect on Leakage (I_0) :—

* Experimentally, in Si & Ge diodes, the leakage increases with temperature by $7\%/^\circ C$.

$$\boxed{I_{02} = I_{01} \cdot 2^{(T_2 - T_1)/10}}$$ ✓

$$(1.07)^{10} \approx 2$$

Means, leakage current Doubles for every $10^\circ C$ rise in temperature.

Example

$T_1 = 20^\circ C$ (I_{01})

$T_2 = 30^\circ C$ (I_{02})

$$I_{02} = I_{01} \cdot 2^{(30-20)/10}$$

$$= I_{01} \cdot 2^{\cancel{10}/\cancel{10}}$$

$$I_{02} = I_{01} \times 2$$

→ Temperature Impact on V_γ :—

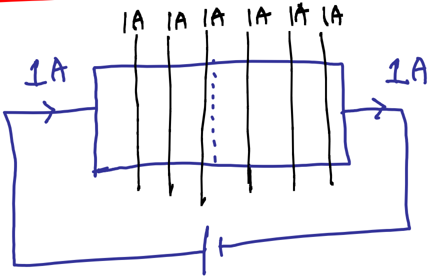
Threshold voltage (V_γ) decrease if temperature Increases.

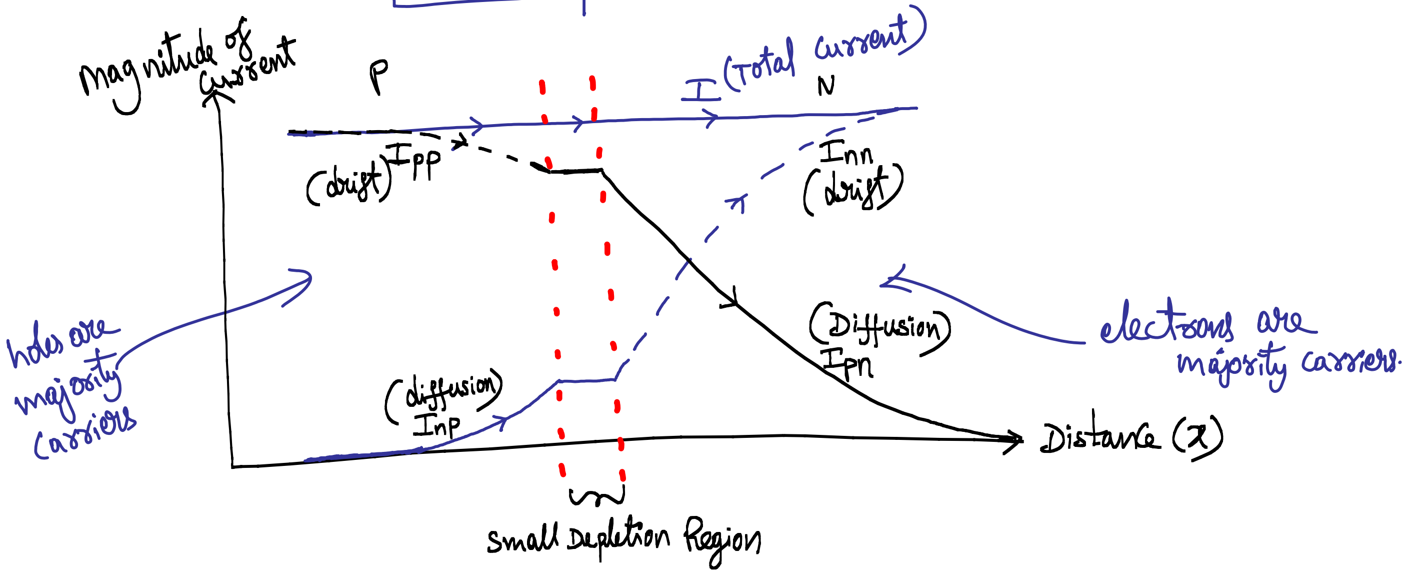
$$V_\gamma = -2.1 \text{ mV}/^\circ C \rightarrow Ge$$

$$= -2.3 \text{ mV}/^\circ C \rightarrow Si$$

Threshold voltage (or) cutin voltage (V_γ) → The minimum required to switch ON the diode.

→ Current Components in PN-diode :—





At any place in diode,

Total current (I) = Current due to $\bar{e}$ + current due to holes

$= I_{np} + I_{pp}$ (p-side)

$= I_{nn} + I_{pn}$ (n-side)

$I_{np} \rightarrow$ Current due to $\bar{e}$ on p-side

$I_{pp} \rightarrow$ " " holes "

$I_{nn} \rightarrow$ Current due to $\bar{e}$ on n-side

$I_{pn} \rightarrow$ " holes "

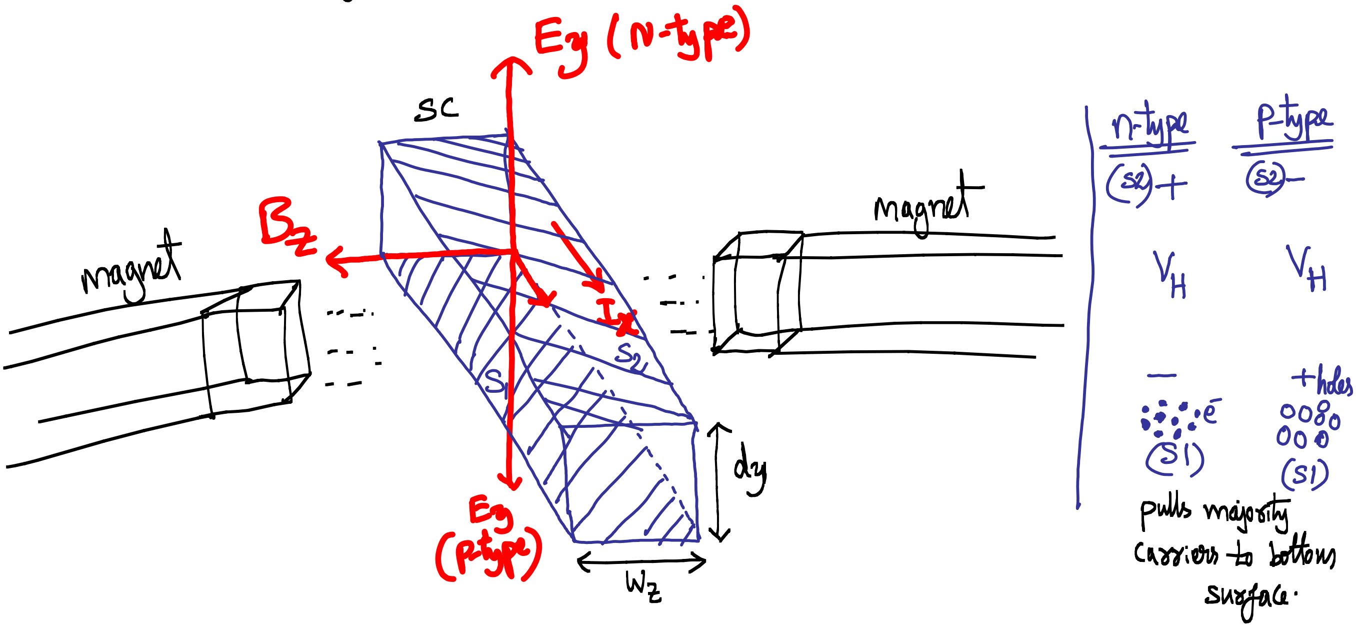
→ HALL Effect :—

Used to identify type of extrinsic SC (i.e n-type or p-type)

Introduced by Scientist Edwin Hall.

" If a current carrying extrinsic SC is placed in Transverse (cross sectional) magnetic field, then an electric field induces in a direction perpendicular to both current & magnetic field".

This electric field pulls the majority carriers of sc to the bottom surface (S_1 surface).



For n-type sc : S_1 surface will be -vely charged.

" p " " : " +vely " .

Hall voltage,

$$V_H = \frac{B_z I_x}{\rho W_z}$$

$W_z \rightarrow$ width of sc.

ρ = charge density

$= nq$ (n-type sc) n - $\bar{e}$ Conc.

$= pq$ (p-type sc) p - hole Conc.

q - elementary charge. (1.6×10^{-19} C)

Electric field Intensity,

$$E_y = \frac{V_H}{d_y}$$

Q1

$$I = I_0 \left(e^{V/\eta V_T} - 1 \right) \simeq \underline{\underline{450 \text{ mA}}}$$

$I_0 = 2nA$

$V = 1V$

$\Rightarrow$ Si, $\eta = 2$

$\Rightarrow T = 300K$, $V_T = 26 mV$ (Thermal voltage)

$$V_T = \frac{KT}{q} \doteq \underline{\underline{26 \text{ mV}}}$$