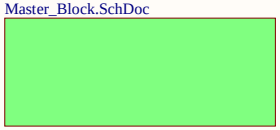
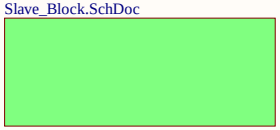
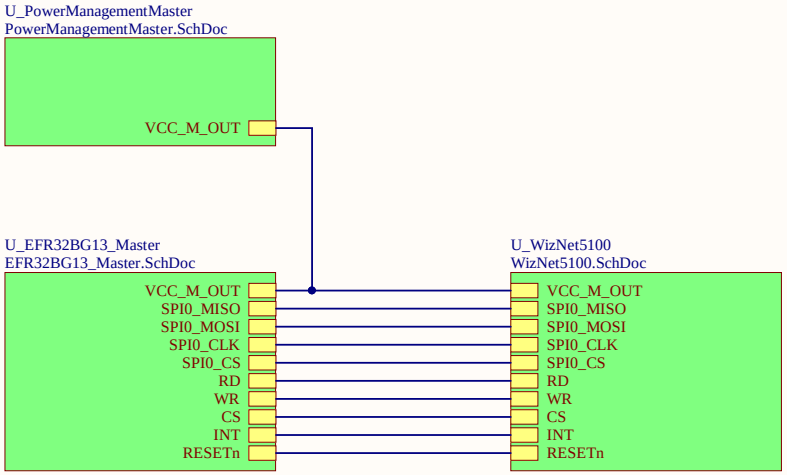
U_Master_Block
Master_Block.SchDoc



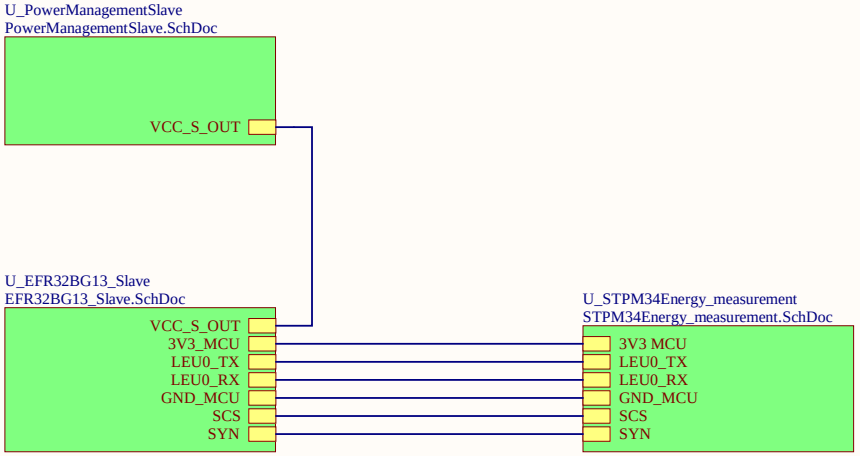
U_Slave_Block
Slave_Block.SchDoc



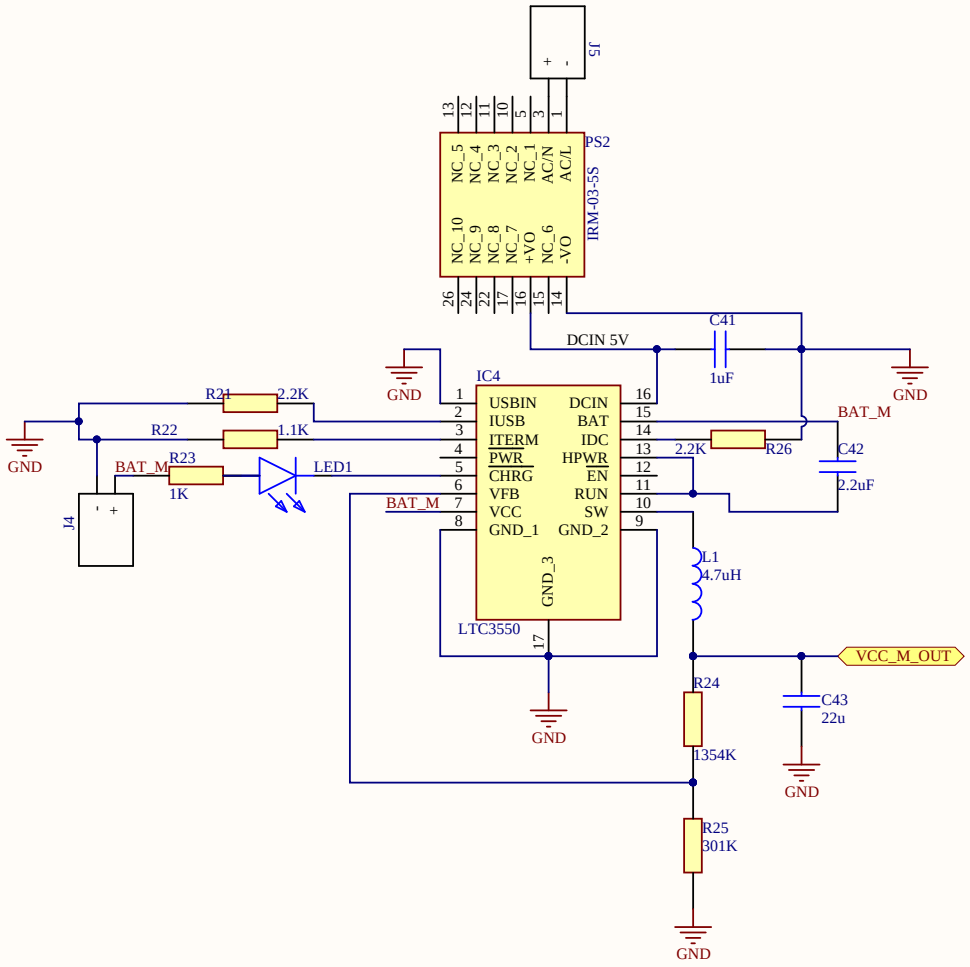
Title	**Block Diagram**		*University of Colorado Boulder*
Size: A4	Number:	Revision:	*Bhishma*
Date: 10/22/2019	Time: 11:13:38 PM	Sheet 1 of 9	*Low Power Embedded Design Techniques*
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\Block Diagram.SchDoc			



Title	***Master Block Diagram***		*University of Colorado Boulder* *Bhishma* *Low Power Embedded Design Techniques*
Size: A4	Number:	Revision:	
Date: 10/22/2019	Time: 11:13:38 PM	Sheet 2 of 9	
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\Master_Block.SchDoc			



Title	***Slave Block Diagram***		*University of Colorado Boulder* *Bhishma* *Low Power Embedded Design Techniques*
Size: A4	Number:	Revision:	
Date: 10/22/2019	Time: 11:13:38 PM	Sheet 3 of 9	
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\Slave_Block.SchDoc			



Relation between input voltage and capacitance required is:
Cin required = Iomax * sqrt(Vout*(Vcc-Vout)) / Vcc

Relation between output voltage and capacitance required is:
Difference in Vout = (Difference in Load current) (ESR + ((1/8)*f*Cout))

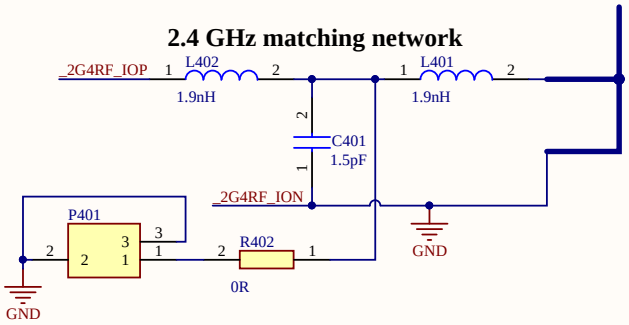
We have considered a voltage swing of 0.2V. Our required output voltage is 3.3V,
and the maximum cutoff voltage for our ICs is given by Wiznet W5100, as 3V.
For safety margin, we have considered 3.1V.
Switching frequency = 1.5MHz
Value of delta load current came as 0.6mA for a pulse current of 300mA.
Factoring all these values in, we get an output capacitance of 20uF and an input capacitance of 1uF. For these parts, ESR = .00456728 ohm.

C43, our bulk capacitor, has a capacitance of 20.79uF at DC bias voltage of 3.3V,
which is exactly the capacitance required by our buck circuit to maintain voltage at 3.3V,
with a dip of 400mV for worst-case current requirement of 300mA, being drawn by the ethernet processor.
This leads to an output voltage of 3.1mV, which is sufficient to drive all our ICs.

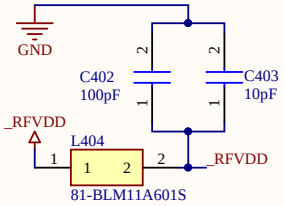
Title	*LTC3550 Power Management - Master*		University of Colorado Boulder Bhishma Low Power Embedded Design Techniques
Size: A4	Number: *	Revision: 0.1	
Date: 10/22/2019	Time: 11:13:38 PM	Sheet 4 of 9	
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\PowerManagementMaster.SchDoc			

Antenna & Radio Interface

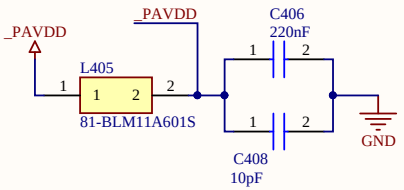
2.4 GHz matching network



RF Analog Power

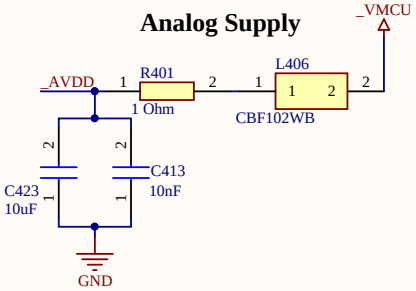


PA Power

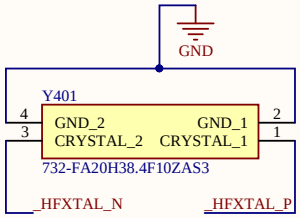


Power & Decoupling

Analog Supply

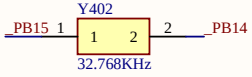


High Frequency Crystal

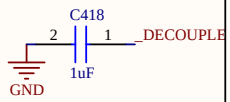


RF Crystal

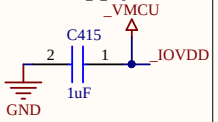
Low Frequency Crystal



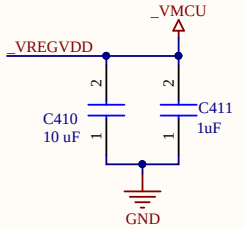
Digital Logic



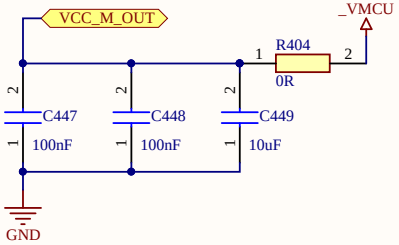
I/O Supply



Digital Supply

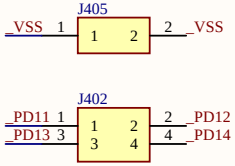


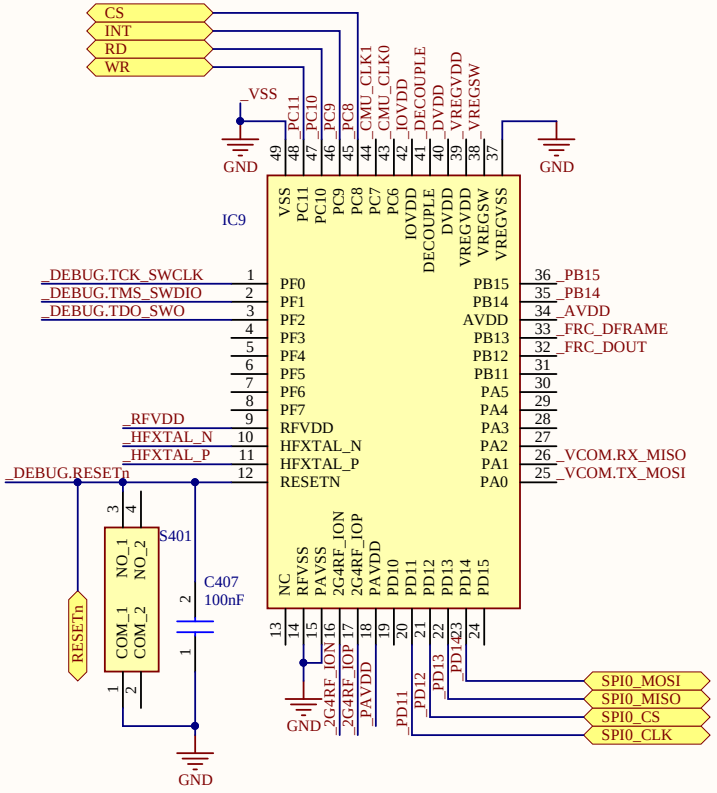
WSTK Power Decoupling



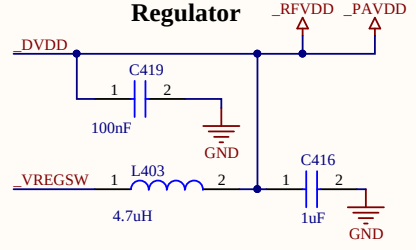
Debug Interface

Pins

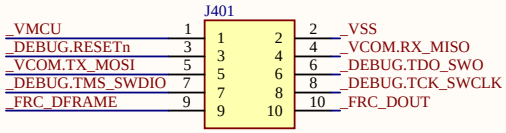


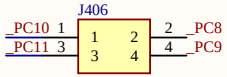


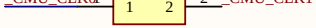
Regulator



Connector



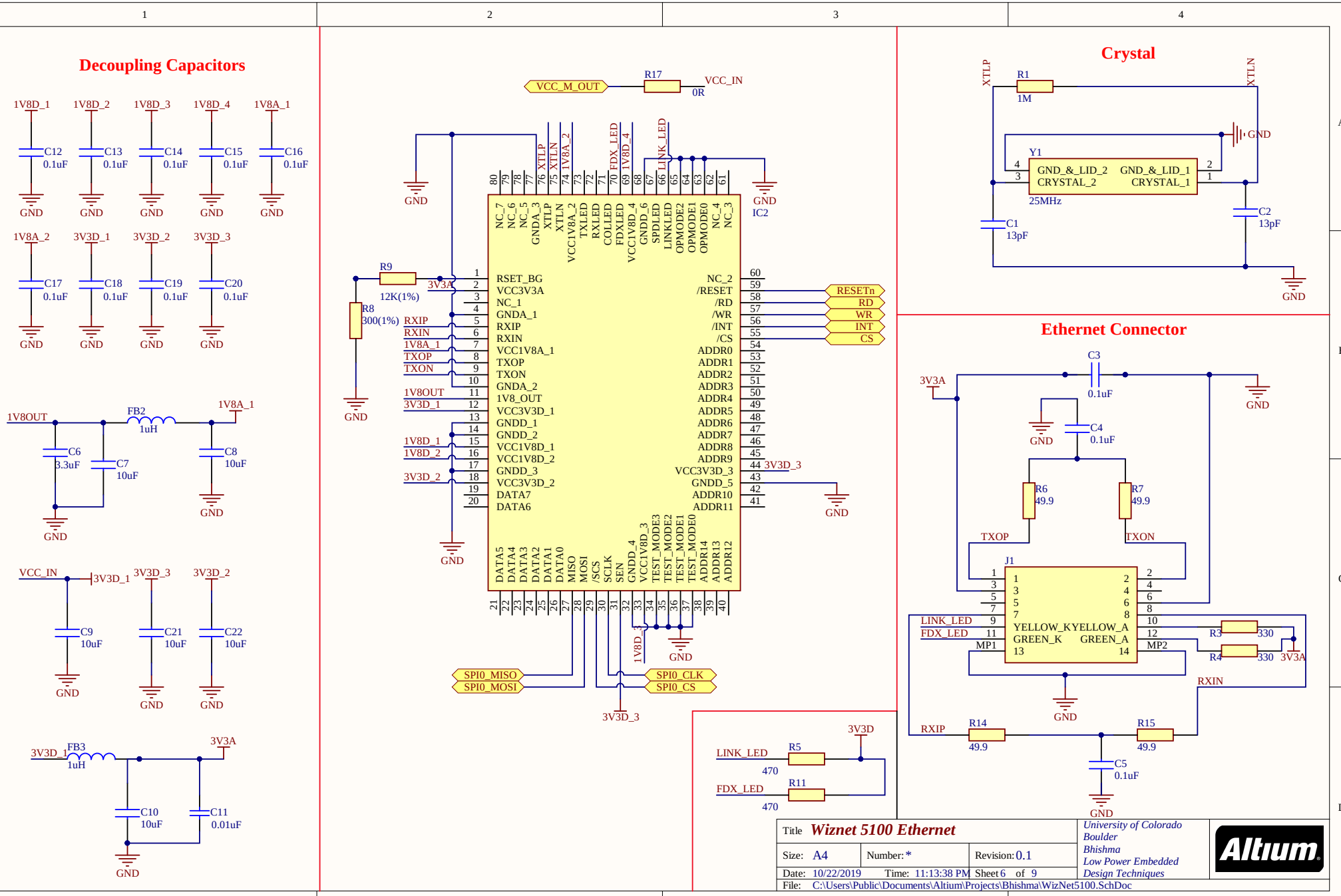


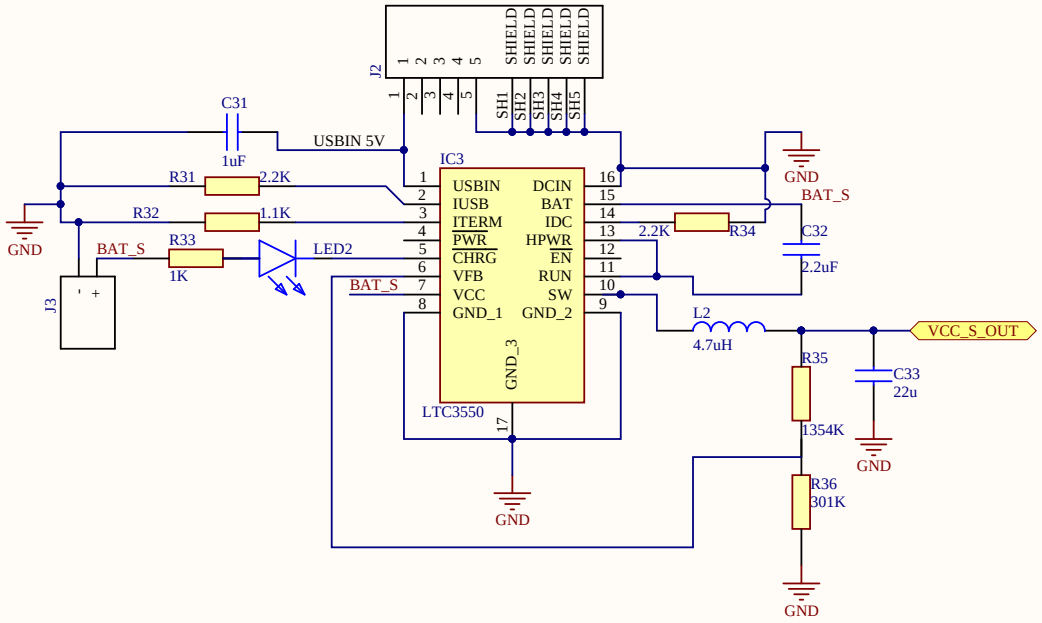


Title: *EFR32BG13 Blue Gecko Master*		
Size: A4	Number:	Revision: 0.1
Date: 10/22/2019	Time: 11:13:38 PM	Sheet 5 of 9
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\EFR32BG13_Master.SchDoc		

University of Colorado Boulder
Bhishma
Low Power Embedded Design Techniques

Altium


Decoupling Capacitors
1V8D_1
1V8D_2
1V8D_3
1V8D_4
1V8A_1
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
GND
1V8A_2
3V3D_1
3V3D_2
3V3D_3
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
1V8OUT
FB2 1uH
C6 3.3uF
C7 10uF
C8 10uF
VCC_IN
C9 10uF
C21 10uF
C22 10uF
3V3D_1
3V3A
FB3 1uH
C10 10uF
C11 0.01uF
VCC_M_OUT
R17 0R
VCC_IN
IC2
R9 12K(1%)
R8 300(1%)
3V3A
RXIP
RXIN
1V8A_1
TXOP
TXON
1V8OUT
3V3D_1
1V8D_1
1V8D_2
3V3D_2
RSET_BG
VCC3V3A
NC_1
GNDA_1
RXIP
RXIN
VCC1V8A_1
TXOP
TXON
GNDA_2
1V8_OUT
VCC3V3D_1
GNDD_1
GNDD_2
VCC1V8D_1
VCC1V8D_2
GNDD_3
VCC3V3D_2
DATA7
DATA6
NC_2
/RESET
/RD
/WR
/INT
/CS
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
ADDR7
ADDR8
ADDR9
VCC3V3D_3
GNDD_5
ADDR10
ADDR11
RESETn
RD
WR
INT
CS
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
MISO
/SCS
SCLK
SEN
GNDD_4
VCC1V8D_3
TEST_MODE3
TEST_MODE2
TEST_MODE1
TEST_MODE0
ADDR14
ADDR13
ADDR12
SPI0_MISO
SPI0_MOSI
SPI0_CLK
SPI0_CS
LINK_LED
FDX_LED
R5 470
R11 470
3V3D
Crystal
XTLP
XTLN
R1 1M
Y1
GND_&_LID_2
GND_&_LID_1
CRYSTAL_2
CRYSTAL_1
25MHz
C1 13pF
C2 13pF
Ethernet Connector
C3 0.1uF
C4 0.1uF
R6 49.9
R7 49.9
TXOP
TXON
J1
YELLOW_K
YELLOW_A
GREEN_K
GREEN_A
MP1
MP2
R3 330
R4 330
R14 49.9
R15 49.9
C5 0.1uF
RXIN
RXIP
Title Wiznet 5100 Ethernet
Size: A4
Number: *
Revision: 0.1
Date: 10/22/2019
Time: 11:13:38 PM
Sheet 6 of 9
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\WizNet5100.SchDoc
University of Colorado Boulder
Bhishma
Low Power Embedded Design Techniques
Altium



Relation between input voltage and capacitance required is:
Cin required = Iomax * sqrt(Vout*(Vcc-Vout)) / Vcc

Relation between output voltage and capacitance required is:
Difference in Vout = (Difference in Load current) (ESR + ((1/8)*f*Cout))

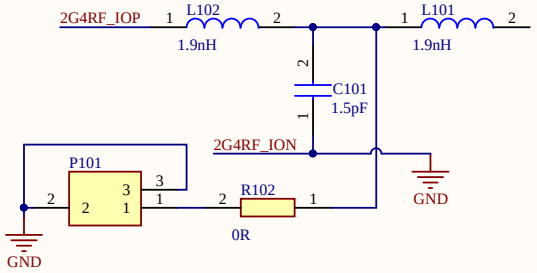
We have considered a voltage swing of 0.2V. Our required output voltage is 3.3V,
and the maximum cutoff voltage for our ICs is given by Wiznet W5100, as 3V.
For safety margin, we have considered 3.1V.
Switching frequency = 1.5MHz
Value of delta load current came as 0.6mA for a pulse current of 300mA.
Factoring all these values in, we get an output capacitance of 20uF and an input capacitance of 1uF. For these parts, ESR = .00456728 ohm.

C33, our bulk capacitor selected, has a capacitance of 20.79uF at DC bias voltage
of 3.3V, which is exactly the capacitance required by our buck circuit to maintain
voltage at 3.3V, with a very slight dip of 12mV for worst-case current requirement
of 80mA, on the slave device, which is sufficient to drive all our ICs.

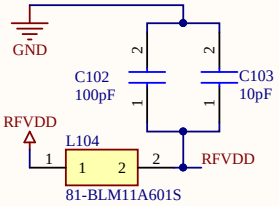
Title	*LTC3550 Power Management - Slave*		University of Colorado Boulder Bhishma Low Power Embedded Design Techniques
Size: A4	Number: *	Revision: 0.1	
Date: 10/22/2019	Time: 11:13:38 PM	Sheet 7 of 9	
File: C:\Users\Public\Documents\Altium\Projects\Bhishma\PowerManagementSlave.SchDoc			

Antenna & Radio Interface

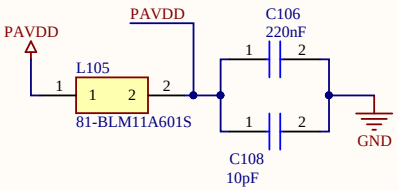
2.4 GHz matching network



RF Analog Power

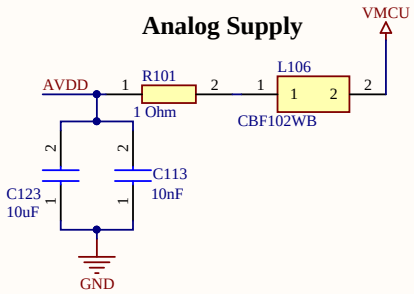


PA Power

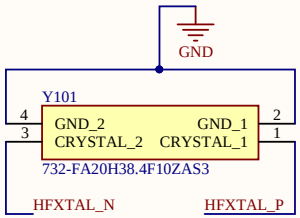


Power & Decoupling

Analog Supply

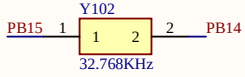


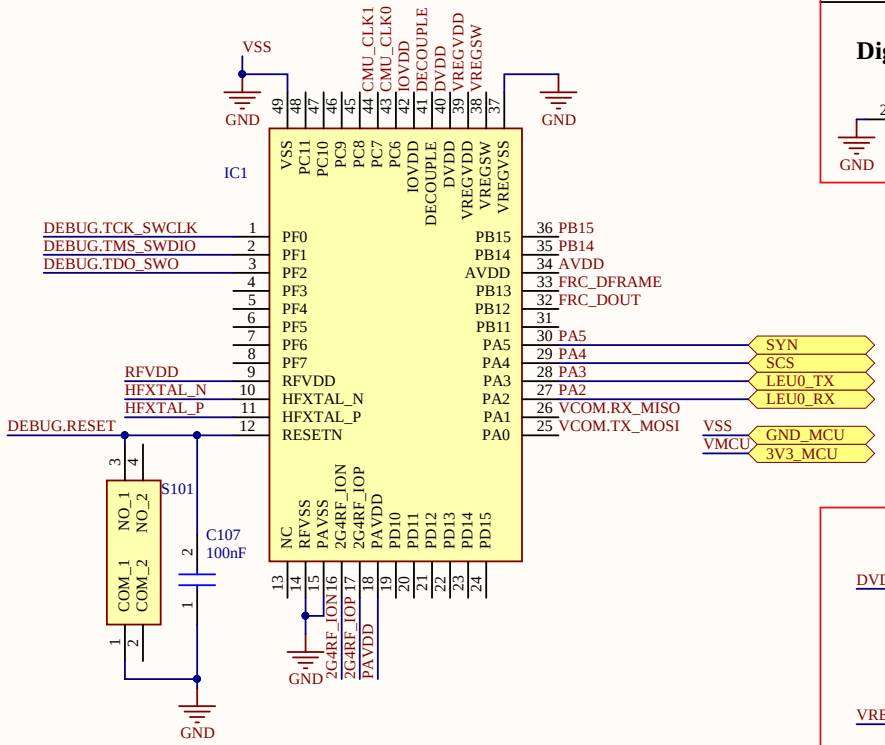
High Frequency Crystal



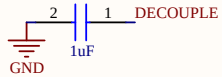
RF Crystal

Low Frequency Crystal

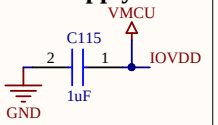




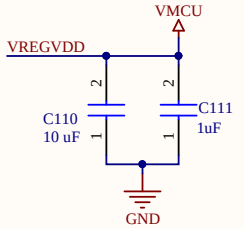
Digital Logic



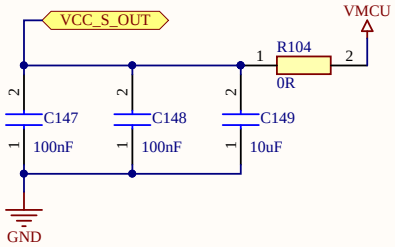
I/O Supply



Digital Supply

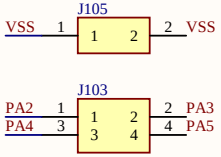


WSTK Power Decoupling

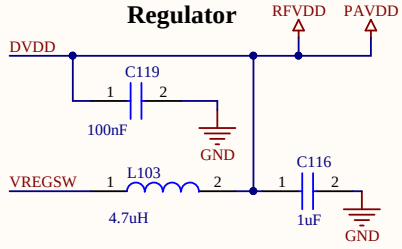


Debug Interface

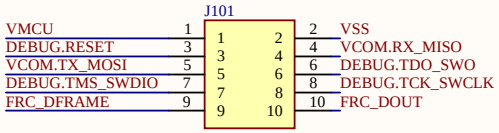
Pins

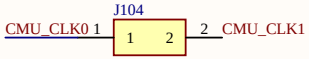


Regulator



Connector





Title	*EFR32BG13 Blue Gecko Slave*		
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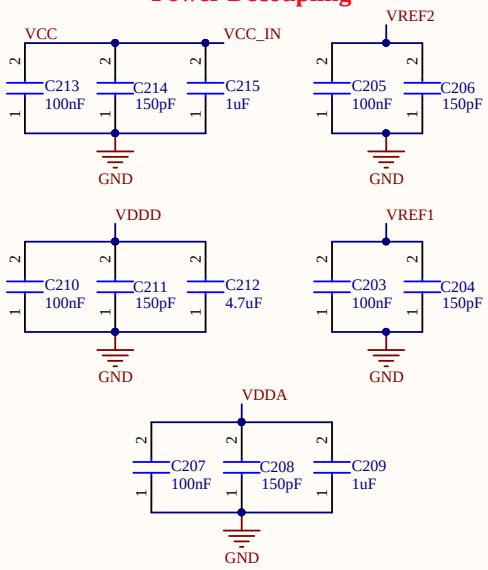
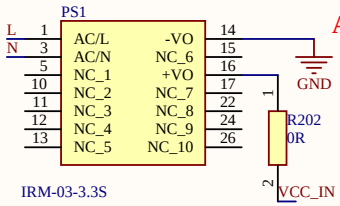
Low Power Embedded Design Techniques

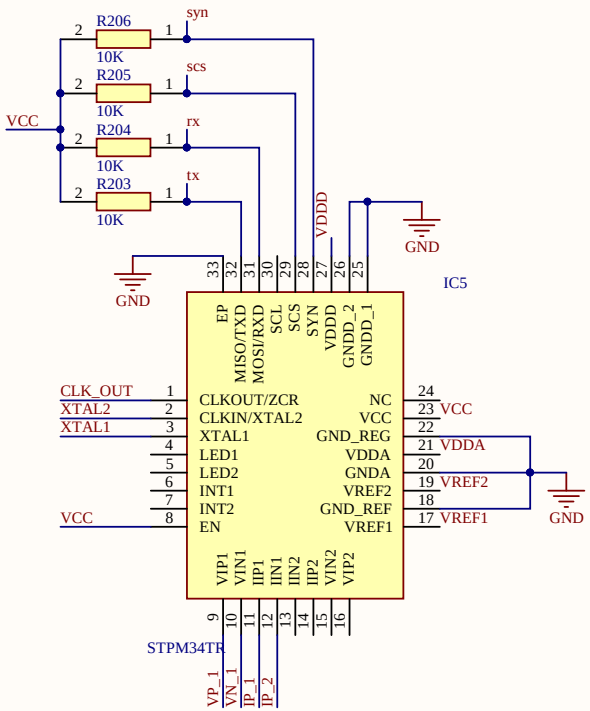
Altium

Power Decoupling

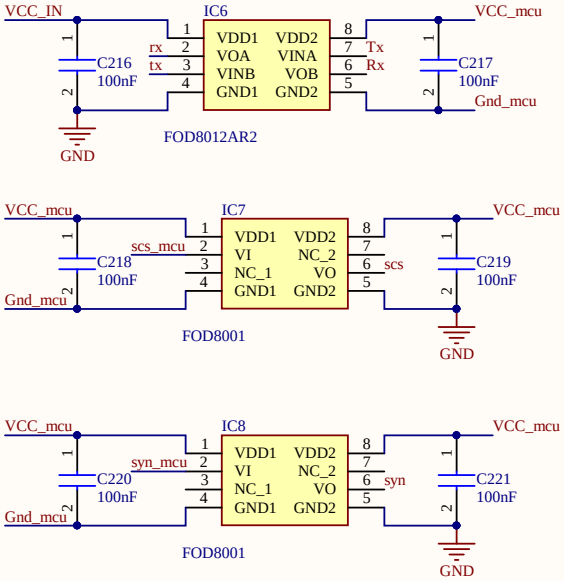


AC/DC converter

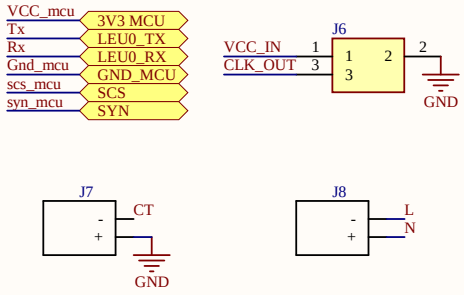




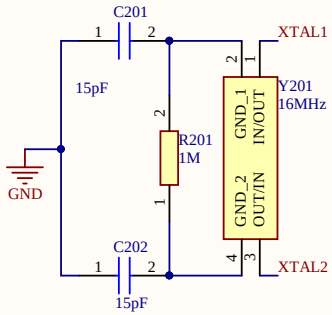
Optoisolator circuit



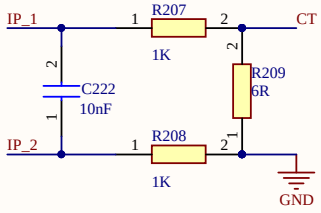
Headers & Connectors



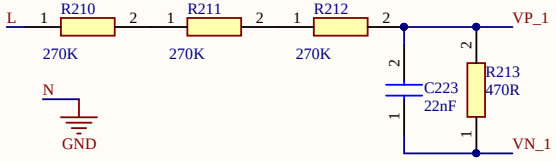
Crystal



Current sensing



Voltage Sensing



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