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Section 1: *Memory subsystem organization*

Question 1.1: Organization of CPU-Cache Bus

1) What type of memory devices should be used for cache data buffering
(Underline the correct variant below):
a) Static RAM; b) Dynamic RAM; c) EDO-RAM; d) SDRAM **(1 mark)**

2) Select the bus type (Underline the correct variant): **(1 mark)**
a) Serial synchronous; b) Parallel synchronous
c) Serial asynchronous; d) Parallel asynchronous

3) Select necessary control and synchronization signals (underline correct) to be included in the bus for CPU-to-Cache interface **(2 marks)**
Address/Data Valid; RAS; CAS; WE; OE; Bus Clock; Byte select

4) Determine number of CPU-to-Cache bus lines: _4B _____= ___32bits **(1 mark)**

5) Calculate maximum CPU Data transaction rate (in MB per second) taking in account shared address/data bus organization: **(2 marks)**
Show calculations: CPU bus data rate =_(400810^6 *4)/(1024*1024)_= 1525.87___MB/s

Question 1.2: Organization of Cache – Main Memory Bus

1) What type of memory devices should be used for Main memory for this system?
(Underline the correct variant below):
a) Static RAM; b) Dynamic RAM; c) EDO-RAM; d) SDRAM **(1 mark)**

2) Select the bus type (Underline the correct variant): **(1 mark)**
a) Serial synchronous; b) Parallel synchronous
c) Serial asynchronous; d) Parallel asynchronous

3) Select necessary control and synchronization signals (underline correct) to be included in the bus for Cache – Main Memory Bus:
Control lines: Address/Data Valid; RAS; CAS; WE; OE; Bus Clock; **(1 mark)**

Synchronization: Address/Data Valid; RAS; CAS; WE; OE; Bus Clock **(1 mark)**

4) Calculate number of Address lines **(1 mark)**
Show calculations: _log(256 M) = log(2^28)/log(2)/2_____ = _14_____ lines

5) Calculate total number of lines in the Main memory bus including address and data lines + control and synchronization lines determined above in Q 1.2.3):

Show calculations: _32+1RAS+1CAS+1clk+1WE_____ = _36__ lines **(2 marks)**

6) Calculate the average Memory bus bandwidth taking in account access time (RAS +CAS latency) and burst length following the steps below:
   a) Determine the latency for SDRAM access (RAS+CAS latency)

Show calculations: __(1/200*10^6)*15_____ = _75_____ nsec **(1 mark)**

a) Calculate the period of time for one burst transfer by formula:
T bt= (RAS+CAS latency) + N t, where N is number of words in burst and t – is word transfer time over the bus* **(2 mark)**
Show calculations: *Tbt* =_7.5E-9+(16*1/200)=155 ns

b) Calculate the average Memory bus bandwidth by formula: *BW mb= Nbytes / Tbt, where N bytes are number of bytes transferred within one burst transfer.* **(2 marks)**

*BWmm = _(4/155E-9)/(1024^3)_____ = _0.024_____*GB/s

Section 2: *Virtual memory and Cache interaction*

Question 2.1

a) As per TLB current content, which page was recently used? Write the Physical page number _02A4_____ **(1 mark)**

b) Was the recent access to the page read or write? (Underline): **Rd** **Wr** **(1 mark)**

c) As per current content of Page Table, list two non-referenced virtual page numbers of the running task segment (e.g. 0000X) below: **(1 mark)**

   1) 0382___ 2) 0188___

Question 2.2: The CPU request is to read data from the Virtual address = 00005010 h,

Determine the following:

- Virtual page # = __00005_____ Page offset = ___010____ **(1 mark)**
- TLB hit or miss = miss_____ **(1 mark)**

If miss, calculate the physical address of the Page Table entry where the physical page number of the requested data should be found
Page table entry address = 28C73205_____ **(1 mark)**

Physical page number = ___02C0_____ **(1 mark)**

- Physical address = __02C0010_____ **(1 mark)**

- Determine the best TLB-entry (in Figure.2) to be modified after reference and fill up the TLB entry after the reference: **(3 marks)**

Entry #	*V-bit*	*TAG*	*Physical page #*	*D-bit*	*R-bit*
02C0	1	00005	02C0	1	1

- Cache hit or miss = miss_____ **(1 mark)**
- Cache index = _01_____ ; Block Offset =____0_____ **(1 mark)**
- Fill up the Cache entry: in Cache bank_____ after the reference: **(3 marks)**

Index	**V-bit**	**D-bit**	**R-bit**	**TAG**
01	1	1	1	02A2

Question 2.3

CPU issues the request to read data from the virtual address VA = 00002030 (Rd), Determine the following:

- Virtual page # = __00002_____ Page offset = __030_____ **(1 mark)**
- TLB hit or miss = hit_____ **(1 mark)**
- Physical page # _02A4_____ Physical address = _02A4030___ **(1 mark)**
- Out of the Physical Address word determine: **(1.5 marks)**
  Block offset = __0_____ ; Index = __03_____ ; TAG = _02A4_____
- Is it hit or miss in Cache? __= hit_____ **(1 mark)**

  If hit, which Cache bank is referenced? _0_____
- Which data-word is sent to CPU according to Figure 5? Word# 2B480921___ **(0.5 mark)**
- Should write back procedure be initiated? **Yes** or **No** (underline correct) **(1 mark)**
- Indicate values of V, D and R bits in **TLB** after the reference: **(1.5 marks)**

  V = __1_____; D = __0_____; R = __1_____
- Indicate values of V, D and R bits in **Cache** after the reference: **(2 marks)**

  Cache bank # ___0____; V = ___1_____; D = __0_____; R = __1_____

Question 2.4

CPU issues the request to write data to the virtual address VA = 0000402F (Wr)
Determine the following:

- Virtual page # = _00004_____ Page offset = __02F_____ **(1 mark)**
- TLB hit or miss __hit_____ **(1 mark)**
- Physical page# = 02A0_____ Physical address =_02A002F_____ **(1 marks)**
- Cache hit or miss _= miss_____ **(1 marks)**

  Show: Block offset = _F_____, Index = __02_____, TAG =_02A0_____ **(1.5 marks)**

- If miss, from which Cache bank the block should be replaced? **(1 marks)**

  Indicate: Cache bank # ___1_____;

- Should write back procedure be initiated? **Yes** or **No** (underline correct) **(1 mark)**

If "Yes", indicate physical start address of the block to be written back to Memory:

Start address =__02CF_____ **(2 mark)**

Indicate physical start address of the block to be loaded into the Cache from the Memory:

Start address = 02A0_____ **(2 mark)**

- Indicate values of V, D and R bits in TLB after the reference: **(1.5 marks)**

  V = __1_____; D = __0_____; R = ___1_____

- Indicate values of V, D and R bits in Cache after the reference: **(2 marks)**

  Cache bank # __1_____; V = ____1____; D = ____1____; R = ___1_____

Section 3: *Video-output subsystem organization*

Question 3.1 ***Synchronous signal generator design:***

Calculate the frequencies of the following:

i) Vertical synchronization signal ***Fvs*** = __120_____Hz **(0.5 mark)**

ii) Horizontal synchronization signal ***F hs*** = (120*1080)_=_129.6____KHz **(1 marks)**

Show calculations_____

iii) Video-clock generator if each pixel generation needs 2 clock cycles.

Video-clock rate (Video-CLK frequency) Fvclk = ___497.664_____ MHz **(2 marks)**

Show
calculations____(1920*1080*120)_____

Question 3.2 ***Video-Frame memory design (for graphic mode):***

1) Calculate the total volume of Video-RAM in Graphic mode, which should provide two pages. One page is used for displaying the current video-frame and another page is needed to accumulate data for the next video-frame.

Determine width of pixel-word (number of bits per RGB pixel) **(1 mark)**
Show calculations: Pixel word=Red =10bits, Green=12bits, Blue=10bits___= 10+12+10=32 bits

Total number of pixels in video-frame = __2,073,600_pixels____ **(2 marks)**
Show calculations: ___1920*1080 = 2,073,600_____

Total volume of the Video-RAM = (2,073,600*4*2)/(1024^2)__=_15.82___ MB **(2 marks)**

2) Calculate required data access (cycle) time for Video-RAM memory chips:
Note: This time must not exceed pixel display time (assuming that R, G and B codes can be accessed in simultaneously as one data-word)

Video-RAM data access time = _4.0187_____ ns **(3 marks)**

Show calculations_1/(120*1920*1080) = 4.0187 * 10^-9_____

3) Determine the maximum bandwidth of the Advanced Graphic Port (AGP 8X) bus to support run-time update of one video-frame in 1080p 120fps video standard:
Note: The AGP 8X bus must be able to transfer video-data of one frame 1920x1080 pixels within the period of one frame display time (1/120 fps)
AGP 8X bus *BW = _949.21_____ MB/sec* **(3 marks)**

Show calculations__(1920*1080*120*4)/(1024^2)_= 949.21875_____
Question 3.3 ***Video-RAM memory design (for Character mode)*****:**

1) Calculate the volume of the Character ROM which contains images of all 4 (four) alphabets with 256 possible symbols in each when each symbol is encoded by 16 x 24 pixel matrix.
   Show calculations____(16*24*256)/(8*1024) = 12 KB_____

   Total Character ROM volume = ___12_____ KB **(2 marks)**

2) Calculate the volume of the Video-text RAM to be reserved for encoding the video-text (80 characters per line x 64 lines), when each symbol can be displayed in one of 256 colors.
   Show calculations_____

   Each symbol should be encoded by= log(256) = 8 Bytes **(1 mark)**

   Total Video-text memory volume = 10,240_____Bytes **(2 marks)**

   Show calculations__(80*64)*(1B+1B) = 10,240_____

Section 4: *Interfacing processor and peripherals: Peripheral Buses*

The above system is equipped with I/O Processor (PPU) to provide access to the Main memory for the Video-output sub-system and secondary data storage based on solid state drive (SSD): Kingston HyperX 120 GB 2.5 in SATA3 SandForce SF-2281 (Figure 1):

Question 4.1

Underline the type of arbitration scheme used in the Peripheral Processing Unit (Bus-bridge based PPU) on the Block diagram shown in Figure 1: **(1 mark)**

a) Centralized serial (Daisy chain) arbitration;
b) Centralized parallel arbitration;
c) Distributed arbitration with self-selection;
d) Distributed arbitration by collision detection.

Question 4.2

For the above SSD with total volume of 120 GB calculate the maximum number of pages which can be stored on SSD if the page size is equal to 4096 Words (1 word = 4Bytes).

Number of pages to be stored in SSD = ___7,864,320_____ **(2 marks)**

Show calculations
._____(120*2^30)/(4096*4) = 7864320_____
Question 4.3

SSD Kingston HyperX 120 GB 2.5in SATA3 SandForce SF-2281 provides the following Rd/Wr characteristics: Rd/Wr transfer rate = 512 MB/sec via serial high speed SATA bus. The PPU provides the "transparent" transfer mode with the block size for each transfer = 64 Byte / transfer. SSD controller's time overhead is negligible. Each Bus request (BR) & Bus grant (BG) process requires (in average) 24 ns. Calculate the following:

1) Number of blocks to be transferred to/from SSD to deliver or return one Page (4096 x 4Bytes) from/to Main memory. **(2 marks)**

   Number of blocks = __(4096*4)/64 = 256_____

2) Period required for one block transfer via SATA with 512 MB/s transfer rate (without BR&BG overhead) **(2 marks)**

   Block transfer time =_(64)/(512*1024^2) = 119.2*10^-9_____=_119.2____ ns

3) Page fault penalty (page replacement time) taking in account that page replacement in worst case scenario requires returning the "dirty" page to the SSD prior to loading the new (requested) page to the Main memory. **(3 marks)**

   Page fault penalty = _(119.2*2)+24 = 262.4ns_____= 0.2624_____ micro sec.