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1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3  USE ieee.std_logic_arith.ALL;
4  USE ieee.std_logic_unsigned.ALL;
5
6  ENTITY reset_circuit IS
7  PORT
8      (
9          Reset : IN STD_LOGIC;
10         Clk : IN STD_LOGIC;
11         Enable_PD : OUT STD_LOGIC;
12         Clr_PC : OUT STD_LOGIC
13     );
14  END reset_circuit;
15
16  ARCHITECTURE description OF reset_circuit IS
17  signal counter: integer range 0 to 5;
18  BEGIN
19      process(clk,Reset)
20          variable counter :integer:=5;
21          BEGIN
22              if (rising_edge(clk) and (clk='1'))
23                  then
24                      if(Reset='1')
25                          then
26                              counter:=0;
27                          end if;
28                      if(counter<4)
29                          then
30                              Enable_PD<='0';
31                              Clr_PC<='1';
32                              counter:=counter+1;
33                          else
34                              Enable_PD<='1';
35                              Clr_PC<='0';
36                          end if;
37                      end if;
38                  end process;
39  END description;
```