Ryerson University
ELE 704 CMOS Analog Integrated Circuits
Mid-Term Examination

Instructor : Dr. Fei Yuan

Date : October 17, 2006

Instructions :

- This is a closed book test. An A-size sheet is allowed to be brought into the examination.
- Check that there is one (1) question in this examination. The marks for each part of the question are indicated in the paper. The maximum marks are 100.
- The duration of the examination is **60 minutes** (10:10 am -11:10 am.).

Question	Marks
1	/100
Total	/100

NAME OF STUDENT :
STUDENT ID :

1 Examination Paper

The schematic of the common-gate amplifier with a current-source load is shown Fig.1. Assume that all transistors are biased in saturation. The $i_{DS} - v_{DS}$ curve of M1 is also shown.

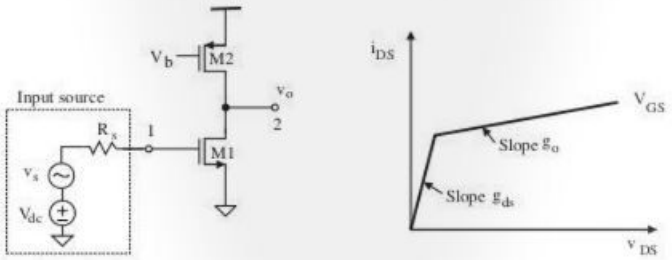

Figure 1: Common-source amplifier and I-V curve of transistor M1.

1) The slope of the two sections of $i_{DS} - v_{DS}$ curve of M1 is denoted by g_{ds} and g_o, respectively. Show that

$$\begin{aligned} g_{ds} &\approx \mu_n C'_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_T), \\ g_o &\approx \lambda I_{DS}, \end{aligned} \tag{1}$$

where V_{GS} and I_{DS} are dc value of v_{GS} and i_{DS}, respectively, and other variables have their usual meaning (10 marks).

2) Show that the transconductance of M1 denoted by g_{m1} is given by $g_{m1} \approx \dfrac{2I_{DS}}{V_{GS} - V_T}$ (10 marks).

3) Identify the gate-source, gate-drain, source-substrate, and drain-substrate capacitances of M1 and M2 by showing them in the schematic. Give the expression of gate-source and gate-drain capacitances of M1 and M2. A linear capacitor is a capacitor whose capacitance is constant. Briefly explain why the source-drain and drain-substrate capacitors are nonlinear (10 marks).

4) Give the expression of the input and output impedances of the amplifier in the dc steady-state (10 marks).

5) Give the expression of the voltage gain $A_v(0) = \dfrac{v_o}{v_{in}}$ in the dc steady-state (10 marks).

6) Find the frequency of the pole at the input ω_{in} and the frequency of the pole at the output ω_{out} (10 marks).

7) Assume the transfer function of the amplifier is given by $A_v(s) = \dfrac{A_v(0)}{(\frac{s}{\omega_{in}}+1)(\frac{s}{\omega_{out}}+1)}$ with $\omega_{out} < \omega_{in}$. Sketch the Bode plots (both magnitude and phase) of $A_v(s)$ (10 marks).

8) Identify the noise sources of the amplifiers by showing them in the schematic (neglect the noise of source resistance, drain, resistance, and gate series resistance). Give the expression of the power of these noise sources (10 marks).

9) Assume the power of the input-referred noise-voltage generator of the amplifier and that of the noise-current generator, denoted by $\overline{v_n^2}$ and i_n^2, respectively, are known. Find the noise figure of the amplifier in the dc steady-state (10 marks).

10) Identify the maximum swing of v_{ds} and i_{ds} (ac components of v_{DS} and i_{DS}) of M1 in Fig.2 when the dc biasing voltage of M1 is $V_{GS1} \sim V_{DS}$ and $V_{GS2} \sim V_{DS}$ such that no distortion in i_{ds} and v_{ds} occurs (10 marks)

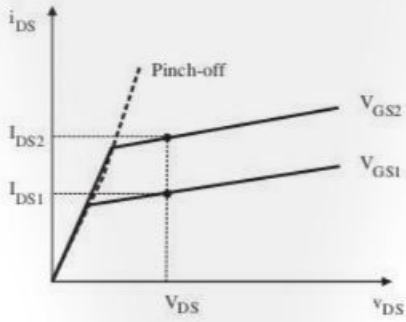

Figure 2: I-V curve of transistor M1.

2 Formula Sheet

- Channel current of MOSFETs :

$$\begin{aligned} i_{DS} &= \tfrac{1}{2}\mu_n C'_{ox}\tfrac{W}{L}(v_{GS}-V_T)^2(1+\lambda v_{DS}) \quad \text{(Saturation)},\\ i_{DS} &= \mu_n C'_{ox}\tfrac{W}{L}[(v_{GS}-V_T)v_{DS}-\tfrac{1}{2}v_{DS}^2] \quad \text{(Triode)}. \end{aligned} \tag{2}$$

- Noise figure :

$$F = 1+\frac{N'_i}{N_i}, \tag{3}$$

where N_i is the noise power at the input port caused by the noise of the input source and N'_i is the noise power at the input port caused by the input-referred noise sources of the circuit.

- Thermal noise of resistors :

$$\begin{aligned} \overline{v_n^2} &= 4kTR\Delta f \quad \text{(Thevenin equivalent)}\\ \overline{i_n^2} &= \tfrac{4kT}{R}\Delta f \quad \text{(Norton equivalent)}, \end{aligned} \tag{4}$$

- Channel thermal noise of MOSFETs :

$$\overline{i_{nD}^2} = 4kT\gamma g_m \Delta f, \tag{5}$$

where $\gamma \approx 2.5$ for short-channel devices g_m is the transconductance.

- Channel flicker noise of MOSFETs :

$$\overline{i_{nf}^2} = \frac{K i_{DS}}{f} \Delta f, \tag{6}$$

where K is a process-dependent constant and i_{DS} is the channel current.

- Junction capacitance of reverse-biased pn-junctions :

$$C_J = \frac{C_{Jo}}{\sqrt{1 + \frac{v_R}{\phi_o}}}, \tag{7}$$

where C_{Jo} is the junction capacitance at zero reverse-biasing voltage, v_R is the reverse biasing voltage of the junction, and ϕ_o is the build-in junction potential.