```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3
 4  ENTITY CPU_TEST_Sim IS
 5     PORT
 6     (
 7        cpuClk            : in  std_logic;
 8        memClk            : in    std_logic;
 9        rst               : in  std_logic;
10
11        -- Debug data.
12        outA, outB     : out std_logic_vector(31 downto 0);
13        outC, outZ        : out std_logic;
14        outIR             : out std_logic_vector(31 downto 0);
15        outPC          : out std_logic_vector(31 downto 0);
16
17        -- Processor-Inst Memory Interface.
18        addrOut           : out std_logic_vector(5 downto 0);
19        wEn               : out std_logic;
20        memDataOut        : out std_logic_vector(31 downto 0);
21        memDataIn         : out std_logic_vector(31 downto 0);
22
23        -- Processor State
24        T_Info            : out std_logic_vector(2 downto 0);
25
26        --data Memory Interface
27        wen_mem, en_mem   : out std_logic
28        );
29
30  END CPU_TEST_Sim;
31
32  ARCHITECTURE behavior OF CPU_TEST_Sim IS
33
34     COMPONENT system_memory
35        PORT
36        (
37           address     : IN STD_LOGIC_VECTOR (5 DOWNTO 0);
38           clock    : IN STD_LOGIC ;
39           data     : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
40           wren     : IN STD_LOGIC ;
41           q        : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
42        );
43     END COMPONENT;
44
45     COMPONENT cpu1
46        PORT
47        (     -- Input ports
48           clk      : in  std_logic;
49           mem_clk  : in  std_logic;
50           rst      : in  std_logic;
51           dataIn   : in  std_logic_vector(31 downto 0);
52           -- Output ports
53           dataOut     : out std_logic_vector(31 downto 0);
54           addrOut     : out std_logic_vector(31 downto 0);
55           wEn         : out std_logic;
56           -- Debug data.
57           dOutA, dOutB   : out std_logic_vector(31 downto 0);
58           dOutC, dOutZ   : out std_logic;
59           dOutIR         : out std_logic_vector(31 downto 0);
60           dOutPC         : out std_logic_vector(31 downto 0);
61           outT           : out std_logic_vector(2 downto 0);
62           wen_mem, en_mem : out std_logic);
```

```
63      END COMPONENT;
64
65      signal cpu_to_mem: std_logic_vector(31 downto 0);
66      signal mem_to_cpu: std_logic_vector(31 downto 0);
67      signal add_from_cpu: std_logic_vector(31 downto 0);
68      signal wen_from_cpu: std_logic;
69
70   BEGIN
71
72      -- Component instantiations.
73      main_memory : system_memory
74      PORT MAP
75      (
76         address => add_from_cpu(5 downto 0),
77         clock => memClk,
78         data => cpu_to_mem,
79         wren => wen_from_cpu,
80         q => mem_to_cpu
81      );
82
83      main_processor : cpu1
84      PORT MAP
85      (
86         clk => cpuClk,
87         mem_clk => memClk,
88         rst => rst,
89         dataIn => mem_to_cpu,
90         dataOut => cpu_to_mem,
91         addrOut => add_from_cpu,
92         wEn => wen_from_cpu,
93         dOutA => outA,
94         dOutB => outB,
95         dOutC => outC,
96         dOutZ => outZ,
97         dOutIR => outIR,
98         dOutPC => outPC,
99         outT => T_Info,
100        wen_mem => wen_mem,
101        en_mem => en_mem
102     );
103
104     addrOut <= add_from_cpu(5 downto 0);
105     wEn <= wen_from_cpu;
106     memDataIn <= mem_to_cpu;
107     memDataOut <= cpu_to_mem;
108
109
110  END behavior;
111
```