Ryerson University
Department of Electrical and Computer Engineering
ELE734: LOW-POWER DIGITAL INTEGRATED CIRCUITS
Mid-Term Examination, October 24th 2019
Duration:1hr 45mins

Student's Name: SOLUTION

Student's Number: ..... **Section:** .....

NOTES:

1. This is a **Closed Book** examination. No aids other than the approved calculators are allowed.

2. Answer all questions.

3. **No questions are to be asked** in the examination hall. If doubt exists as to the interpretation of any question, the student is urged to submit with the answer paper, a clear statement of any assumptions made.

Question No.	*Mark of each question*	*Mark obtained*
Q1	15	
Q2	15	
Q3	15	
Q4	05	
Total (Out of 50):		

Q1:

Design a static CMOS gate that has the following output.

*Out = !((A+B)*C*D)*

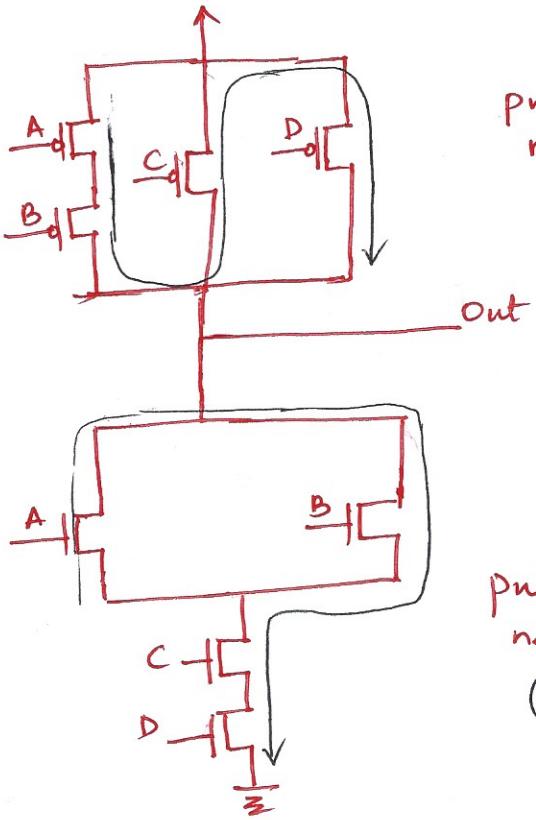
a) Draw the transistor-level schematic of your design. Sizing is not required. (6 marks)

b) Draw stick diagram of the gate that you have designed (***please minimize layout area by maximizing diffusion sharing*** and clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (6 marks)

c) Estimate the area of the gate based on your stick diagram. (3 marks)

$Out = \overline{(A+B)\cdot C\cdot D}$

a)



pull up network (3) marks

pull down network (3) marks

pull down network
(A in parallel with B) in series with C in series with D

pull up network
apply demorgan's law

$\overline{A+B} + \bar{C} + \bar{D} = (\bar{A}\cdot\bar{B}) + \bar{C} + \bar{D}$

(A in series with B) parallel (with C) parallel with D

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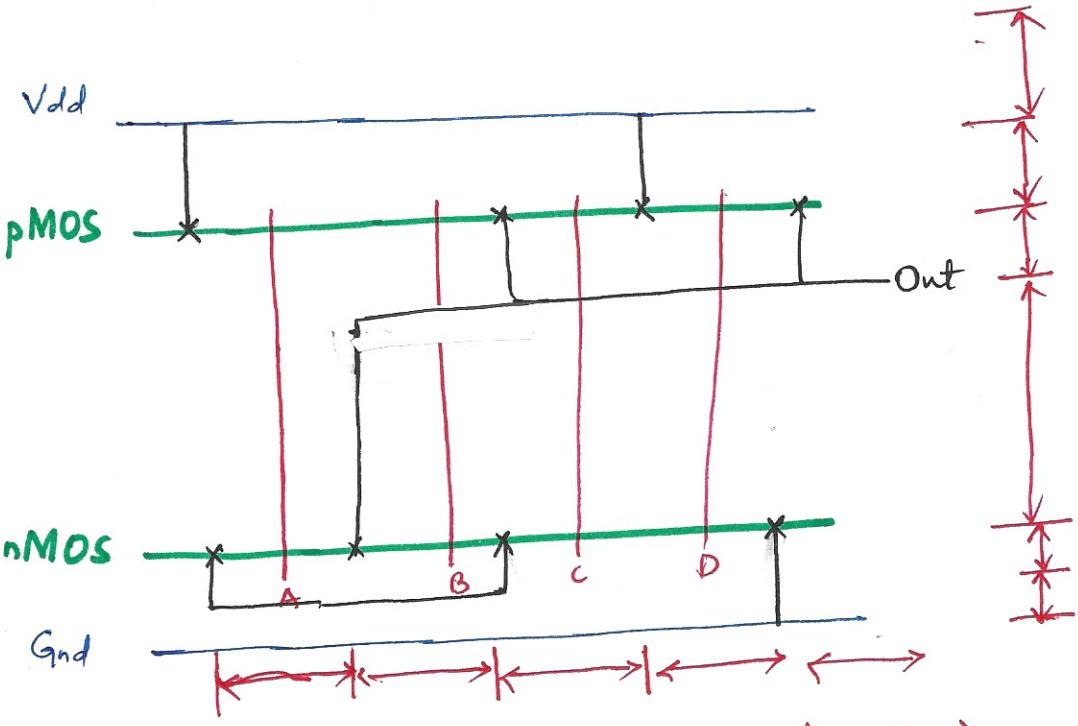
b)



(3 marks)

(3 marks)

c) $5 \times 8\lambda = 40\lambda$ (1 mark)

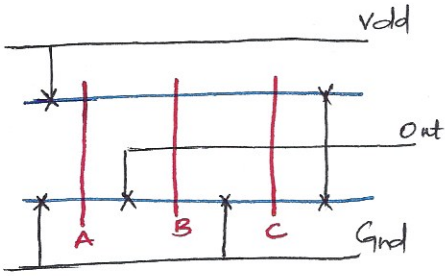
$6 \times 8\lambda = 48\lambda$ (1 mark)

$40\lambda \times 48\lambda = 1920\lambda^2$ (1 mark)

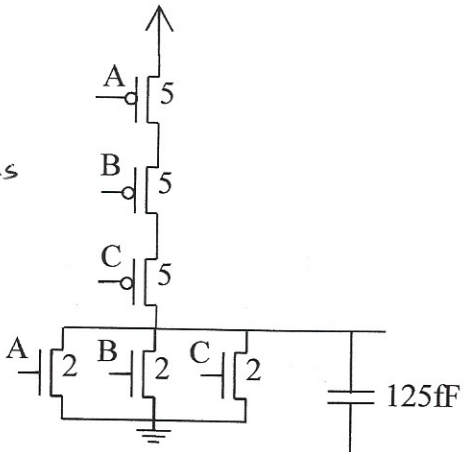
Q2:

Assume the on-resistance of a unit nMOS is 15Kohms and the on-resistance of a unit pMOS is 30Kohms. Also assume the drain, source, and gate capacitances of a unit transistor are all equal to 15fF. Using Elmore delay to calculate the delay of the gate when the input of the gate is transitioned from A=1, B=0, C=0 to A=0, B=0, C=0. ***Please assume diffusion sharing is always used to minimize layout area of the gate.*** (15 marks)

Stick Diagram



② marks



PMOS $\frac{30k\Omega}{5} = 6k\Omega$

$15ff \times 5 = 75ff$

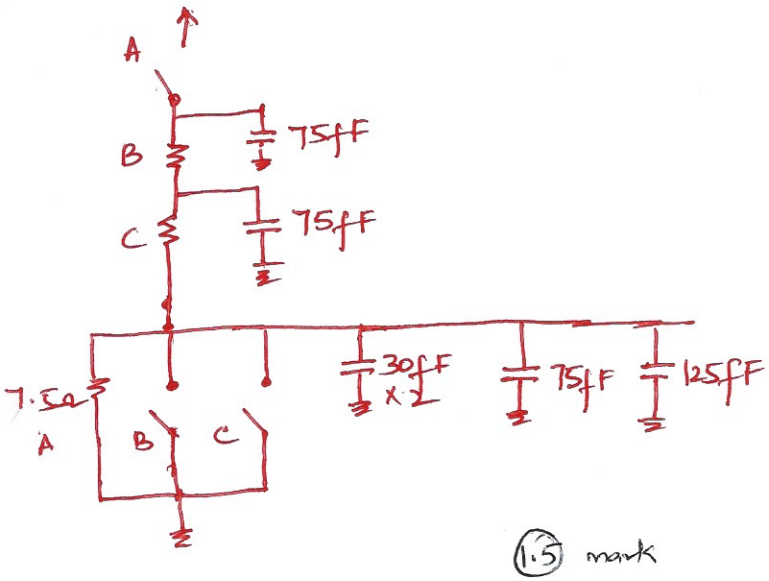
② marks

nMOS $\frac{15k\Omega}{2} = 7.5k\Omega$

$15ff \times 2 = 30ff$

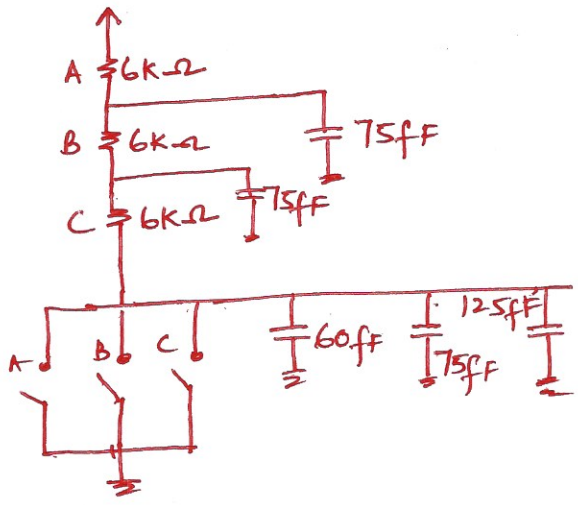
② marks

A=1 B=0 C=0



(1.5) mark

A=0 B=0 C=0



(1.5) mark

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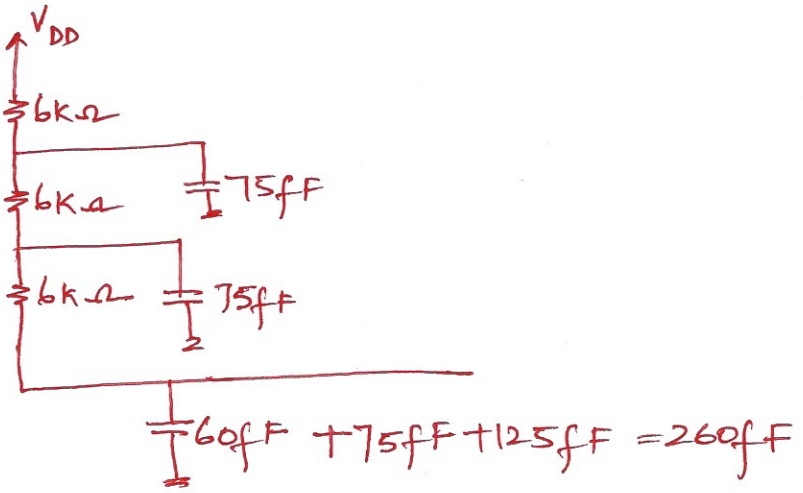


③ marks

Delay =

$= (260fF \cdot 3.6k) + (75fF \cdot 2.6k) + (75fF \cdot 6k)$ → Correct equation ② marks

$= 4680ps + 900ps + 450ps$

$= 6030ps$

$= 6.030ns$ — ① marks

Q3:

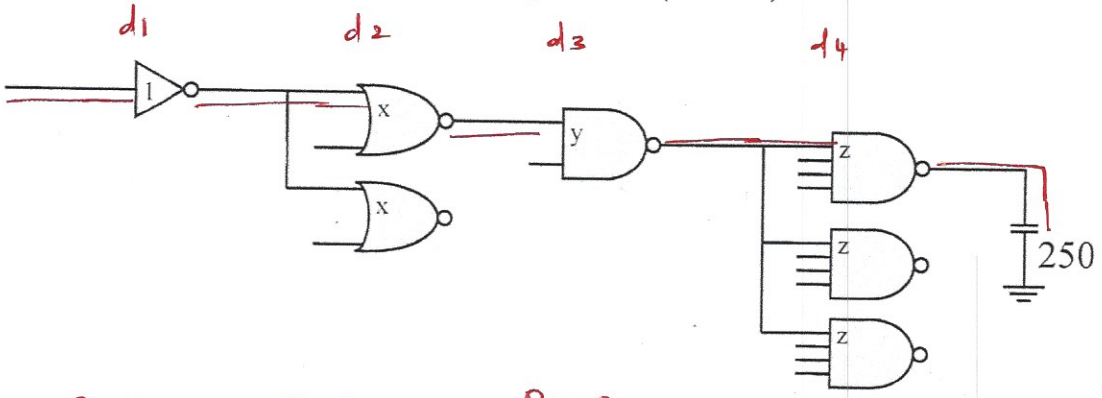
a) Calculate the optimum path delay for the following circuit and the value of x, y, and z in order to achieve the optimum delay. (inverter: g=1, p=1; 2-input nor: g=5/3, p=2; 2-input nand: g=4/3, p=2; 4-input nand: g=6/3, p=4). (7 marks)

b) Draw the transistor level diagram for the 2-input nor gate and clearly label the size of each transistor in the diagram. (2 marks)

c) Draw the transistor level diagram for the 2-input nand gate and clearly label the size of each transistor in the diagram. (2 marks)

d) Draw the transistor level diagram for the 4-input nand gate and clearly label the size of each transistor in the diagram. (2 marks)

e) Calculate the optimum path delay if additional inverter stages can be added between the 4-input nand gate and its load capacitance (2 marks).



$p_1 = 1$ $\quad p_2 = 2$ $\quad p_3 = 2$ $\quad p_4 = 4$

$g_1 = 1$ $\quad g_2 = \frac{5}{3}$ $\quad g_3 = \frac{4}{3}$ $\quad g_4 = \frac{6}{3}$

$h_1 = \frac{2x}{1}$ $\quad h_2 = \frac{y}{x}$ $\quad h_3 = \frac{3z}{y}$ $\quad h_4 = \frac{250}{z}$

a)

$F = \Pi(g_i h_i)$

$= \left(1 \cdot \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{2}{3}\right)\left(\frac{2x}{1} \cdot \frac{y}{x} \cdot \frac{3z}{y} \cdot \frac{250}{z}\right)$

$= \frac{20000}{3} = 6666.67$

$(F)^{1/4} = (6666.67)^{1/4}$

$(F)^{1/4} = 9.036$ (1.5 mark)

$D_{min} = N(F)^{1/N} + \sum_i p_i$

$= 4(9.036) + (1+2+2+4)$

$D_{min} = 45.144$ (1 mark) 6

$(F)^{1/N} = g_i h_i$

$1 \cdot \frac{2x}{1} = 9.036$ $\quad x = 4.518$ (1.5 mark)

$\frac{5}{3} \cdot \frac{y}{x} = 9.036$

$\frac{5}{3} \cdot \frac{y}{4.518} = 9.036$ $\quad y = 24.49$ (1.5 mark)

$\frac{4}{3} \cdot \frac{3z}{y} = 9.036$

$\frac{4}{3} \cdot \frac{3z}{24.49} = 9.036$ $\quad z = 55.32$ (1.5 mark)

$\frac{6}{3} \cdot \frac{250}{z} = 9.036$

$\frac{6}{3} \cdot \frac{250}{55.32} = 9.036$ ✓ checked

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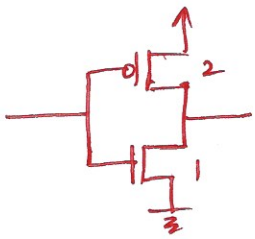
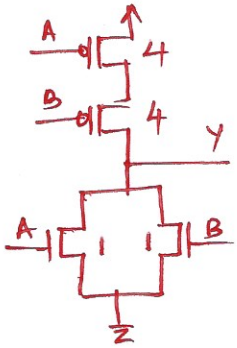


1 Unit = 3C

b.

$x = 4.518$



nmos $4.518 \times \frac{1}{5} = 0.904$

pmos $4.518 \times \frac{4}{5} = 3.614$

① mark

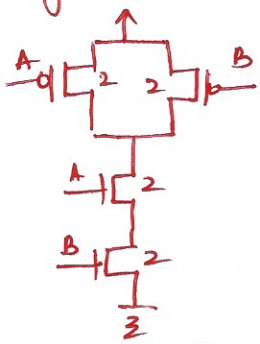
nmos width $= 0.904 \times 3 = 2.712$ C

pmos width $= 3.614 \times 3 = 9.49$ C

① mark

c)

$y = 24.49$



① mark

nmos $24.49 \times \frac{2}{4} = 12.245$

pmos $24.49 \times \frac{2}{4} = 12.245$

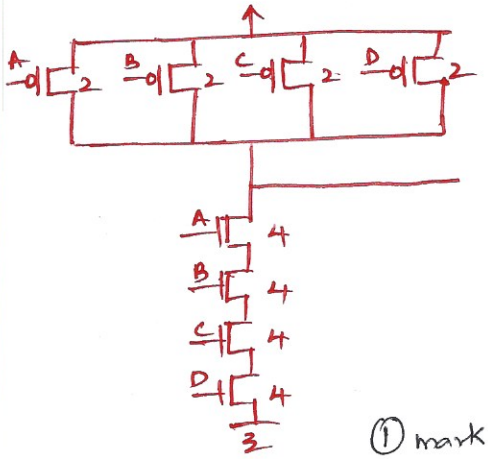
nmos width $= 12.245 \times 3 = 36.735$C

pmos width $= 12.245 \times 3 = 36.735$C

① mark

d)

$Z = 55.32$



① mark

nmos $55.32 \times \frac{4}{6} = 36.88$

pmos $55.32 \times \frac{2}{6} = 18.44$

nmos width $36.88 \times 3 = 110.64$C

pmos width $= 18.44 \times 3 = 55.32$ C

① mark

e. $F = \prod g_i h_i = 6666.67$

$(F)^{1/N} = 3.59$

$(6666.67)^{1/N} = 3.59$

$\frac{1}{N} \log (6666.67) = \log 3.59$

$N = \frac{\log (6666.67)}{\log 3.59}$

$N = 6.89$

$N = 7$ ① mark

$D_{min} = N(F)^{1/N} + \sum P_i$

$= 7(6666.67)^{1/7} + 1+2+2+4+3$

$= 7(3.5178) + 12$

$= 36.63$

Optimal Delay $= 36.63\tau$ ① mark

Q4: Multiple Choice Questions

1. Modern process technologies in which device sizes are reduced require
   - **a)** high VDD
   - **b)** low VDD
   - **c)** zero VDD
   - **d)** infinite VDD

2. Each transistor switch is modeled by a finite ON resistance, which is the
   - **a)** gate-drain resistance
   - **b)** source-drain resistance
   - **c)** source-gate resistance
   - **d)** source -body resistance

3. To reduce power dissipation in a circuit, C must be
   - **a)** maximum
   - **b)** minimum
   - **c)** infinite
   - **d)** 10 F

4. Complementary CMOS of inverters switched by
   - **a)** supply voltage
   - **b)** output voltage
   - **c)** input voltage
   - **d)** load capacitance

5. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____ region
   - **a)** linear
   - **b)** saturation
   - **c)** non saturation
   - **d)** cut-off