Quiz Submissions - Midterm Exam

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Attempt 1

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Submission View

Your quiz has been submitted successfully.

An announcement will be made once grades are ready for viewing.

Question 1 **1 / 1 point**

Page fault handler is a type of _____.

- ✔ Exception
- Program
- Hardware instruction
- Process

Question 2 **0 / 1 point**

Assume that the value stored in the r1 register is 10. After the following ARM instruction is executed, what is the value in register r0?

```
ADD r0, r1, r1, LSL #2
```

- ➡ ◯ 90
- ✖ ◯ 50
- ◯ 40
- ◯ 20

Question 3 **1 / 1 point**

What does indirect memory addressing mean in ARM instruction set?

- ◯ memory location addresses must be referred to by physical addresses
- ◯ memory location addressess are virtual and not physical addresses
- ✔ ◯ memory location addresses must be referred to through registers
- ◯ memory location addresses must be referred to by the program counter (PC)

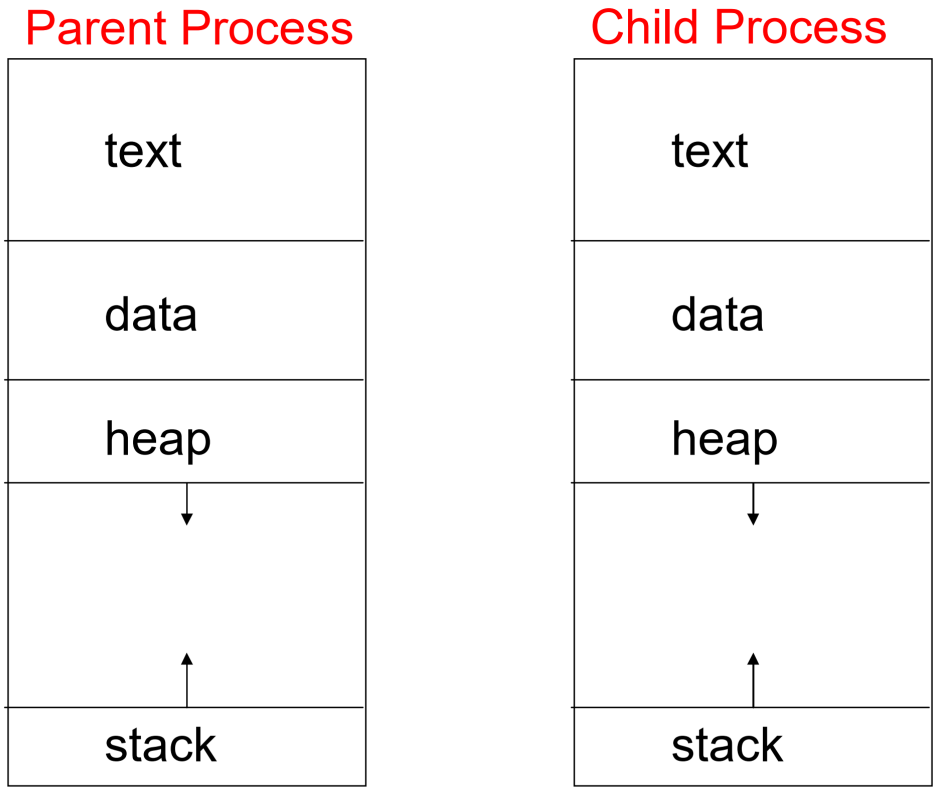
Question 4 **1 / 1 point**

In microcontrollers, None recurring cost (NRE) means

- Cost of maintaining technical documentation
- Cost of maintaining software for the microcontroller
- ✔ Cost of designing of the architecture
- Cost of parts and material

Question 5 **1 / 1 point**

A system call results in the following process being created



Which system call was likely executed?

- ✔ fork()
- exec()
- read()
- write()

Question 6

0 / 1 point

What is the final instruction in any subroutine called in an ARM based code?

- MOV pc, SUBROUTINE
- ➡ MOV pc, r14
- MOV pc, CLPR
- ✖ MOV pc, r13

Question 7

1 / 1 point

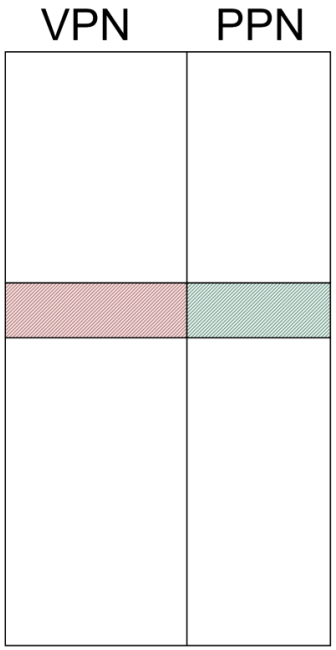
Assume that we have a 16 bit virtual address space mapping to a 16 bit physical address space. If there is an entry for every 32 bits (4 Bytes) of physical memory, how large will the address translation table be?

- ✔ 32 KB
- 128 KB
- 256 KB
- 64 KB

Question 8

0 / 1 point

A simplified page translation table is shown below.



Translation table
PAGE TABLE

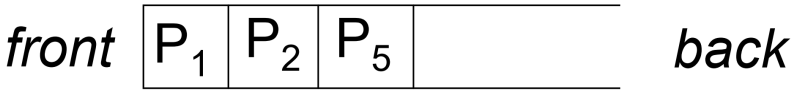
Assume that the physical address space and virtual address space are the same. How much savings space saving can be achieved if the virtual page numbers (VPN) are made to be the indices to the table rather than a separate column as shown above?

- ✗ ○ 100%
- ➡ ○ 50%
- ○ 12.5%

25%

Question 9 **1 / 1 point**

Assume that we are implementing a non-preemtive scheduling policy using FCFS (first come, first serve). A new process P4 comes in, where does this process go in the ReadyQ shown below?



- Between P1 and P2
- In front of P1 (at the front)
- ✔ After P5 (in the back)
- Between P2 and P5

Question 10 **1 / 1 point**

There is one page translation table for _____.

- ✔ each process that is running
- each hardware instruction executed

- ○ The number of processes executed by the operating system
- ○ each program that is running

Question 11 **1 / 1 point**

What of the following is NOT true about an LRU (least recently used) policy implemetned using a stack for replacing pages in main memory?

- ✔ ○ The LRU page is at the top of the stack
- ○ LRU requires a large number of comparisons
- ○ The stack must be updated after every memory stack
- ○ LRU may be too expensive

Question 12 **1 / 1 point**

What is the main advantage of using conditional execution in ARM?

- ○ Avoids many small branch jumps
- ○ Improves code efficiency
- ○ Improves code density

✔ All the above

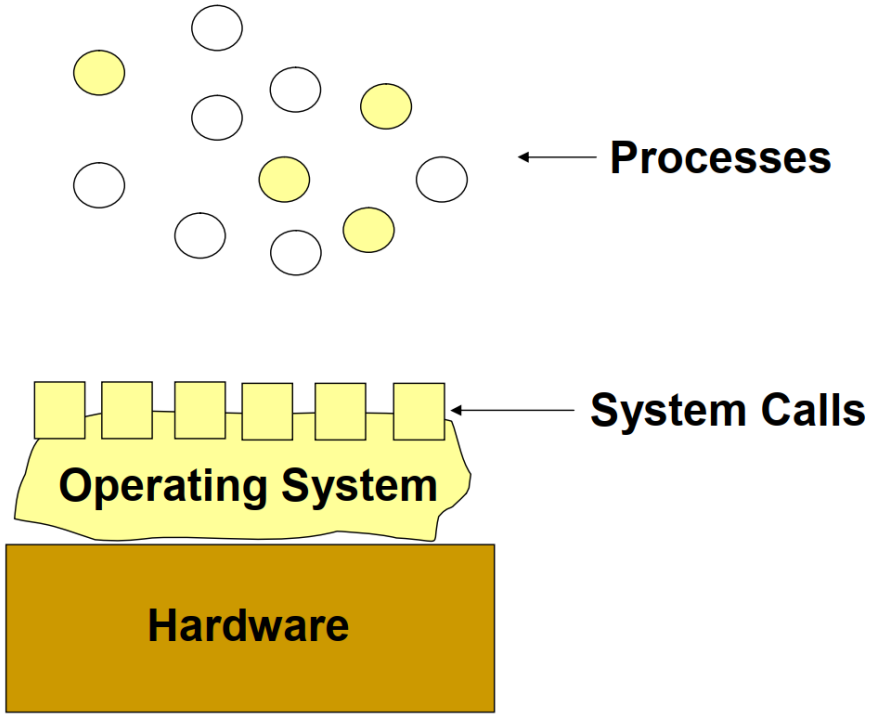
Question 13 **1 / 1 point**

Which of the following statements is false?

- In Von Neumann architecture, both instructions and data are stored in the same memory
- ✔ In Von Neumann architecture, instructions and data are stored in separate memory
- In Harvard architecture, instructions and data are stored in separate memory
- All are false

Question 14 **1 / 1 point**

We described the operating system interaction with the hardware as shown below:



What do the white circles above the diagram represent?

- Process that interact with the hardware
- Any process
- ✔ Process that the user runs
- Processes that run code for the Operating System

Question 15 **1 / 1 point**

What can be said about stacks in ARM based microcontrollers?

- ○ Both software and hardware stacks are available
- ✔ ○ Only software stack is available
- ○ Only hardware stack is available
- ○ Neither hardware or software stacks are available

Question 16 **1 / 1 point**

A modern processor's speed compared to a main memory speed is in the order of

- ○ 3 (1ns vs 1 ms)
- ✔ ○ 2 (1ns vs 100 ns)
- ○ 5 (1ns vs 100 ms)
- ○ 4 (1ns vs 10 ms)

Question 17 **1 / 1 point**

What best describe a context switch?

- A situation that occurs anytime a program is started
- A program that calls a subroutine
- ✔ The process by which the operating system changes the running process
- The process where an operating system creates a new process

Question 18 **1 / 1 point**

How many times is the following piece of code executed?

```
        MOV r2, #0
LOOP    ADD r2, r2, #1
        CMP r2,#20
        BNE LOOP
```

- 19
- ✔ 20
- 21
- 1
- Never executes as condition is false

Question 19

0 / 1 point

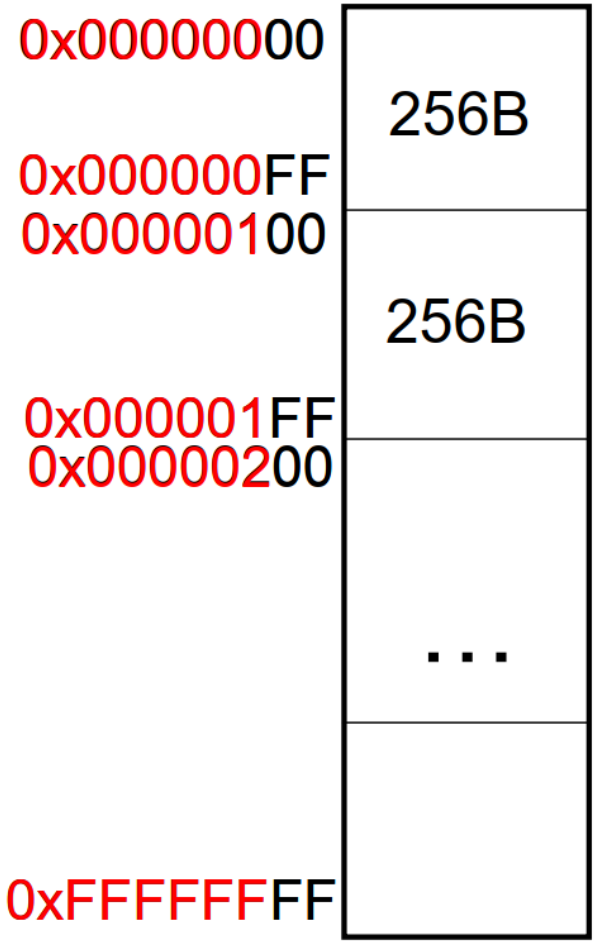
Which one of the following scheduling policies is exclusively for preemptive scheduling?

- Shortest Process Next
- ✗ Round Robin
- First Come First Serve
- ➡ Priority based

Question 20

1 / 1 point

Assume that a computer system has the following virtual address space. How many virtual pages exist on this system?



- 4095
- 65535
- ✔ 16777215
- 1048575

Question 21

1 / 1 point

When is it likely for a page fault to occur?

- There a virtual address without a page table entry
- ✔ There is a virtual address whose page table entry is empty
- There is a virtual address whose page table entry has a nonsensical value
- There is virtual address that is out of bounds

Question 22

0 / 1 point

System calls can be best described as:

- Hardware instructions executed by the operating system
- ✖ Process running on the operating system
- ➡ Functions that access operating system code
- Operating system programs running independently of other programs

Question 23

1 / 1 point

Which of the following page replacement policies used in memory management is the least computationally expensive?

- LRU (least recently used)
- ✔ Random
- FIFO (first come, first serve)
- Approximate LRU

Question 24 **0 / 1 point**

What is true about designing of microcontrollers?

- Time to market is flexible, microcontrollers are needed regardless
- ✖ Designers must have both software and hardware skills
- None recurring cost is very important for large scale manufacturing
- ➡ Cost and complexity can be improved at the same time

Question 25 **1 / 1 point**

A modern processor's speed compared to a Hard disk access speed is in the order of

- ✔ 4 (1ns vs 10 ms)
- 5 (1ns vs 100 ms)
- 3 (1ns vs 1 ms)
- 2 (1ns vs 100 ns)

Question 26 **1 / 1 point**

Assume that we initialize register r9 to the value 1000. What will be stored in register r2 when the following piece of ARM based instructions are executed?

Assume that memory locations 1000 has data 10, memory location 1004 has value 20 and memory location 1008 has value 30 stored in it.

```
LDR     r8, [r9]
LDR     r6, [r9, #4]
LDR     r7, [r9, #8]
ADD     r3, r8, r6
SUB     r3, r3, r7
```

- 10
- 30
- ✔ 0

40

Question 27 **0 / 1 point**

Assume that most programs executing on an embedded system show very good locality of reference. If there is a page fault, which replacement policy would BEST suit this system?

➡ MRU - most recently used

✖ MFU - most frequenty used

LRU - least recently used

LFU - least frequently used

Question 28 **1 / 1 point**

What is an instruction that is specail to ARM instruction set compared to other microcontrollers?

None of these answer

Branching and linking

✔ Conditional execution

Autoincrementing registers by defined literal

Question 29

0 / 1 point

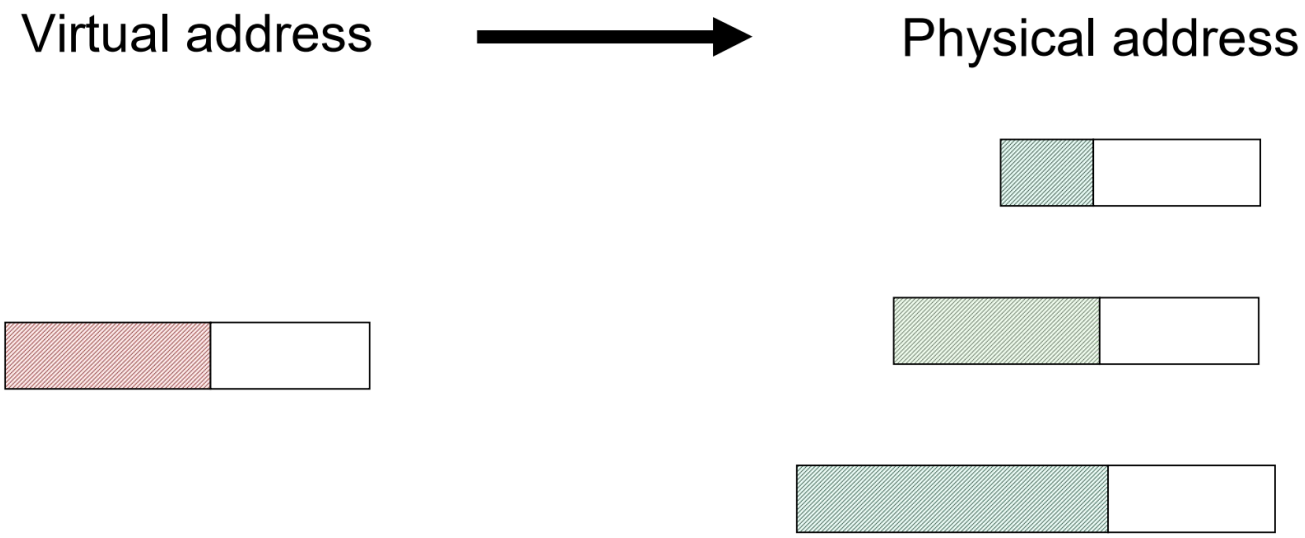
What is a typical CPU slice time in modern operating systems?

- Order of 100's of millisecond
- Order of milliseconds
- ✗ Order of microseconds
- Orders of 100's of microseconds

Question 30

0 / 1 point

Virtual address size can be the same, less or more than the physical address size as shown below. In modern operating systems with a modern processor, which case is the most common?



- ✗ ○ Virtual address is larger than physical address
- ➡ ○ Virtual address is same as physical address
- ○ Virtual address is smaller than physical address

Question 31 **1 / 1 point**

How is a process preempted?

- ○ Hardware handles it periodically
- ○ None of these answers

- ◯ Through a system call
- ✔◯ Through a software exception

Question 32 **1 / 1 point**

Assume that the following page tables exist on a computer system

Page Tables

P1

0	0
1	-
2	-
3	-

P2

0	-
1	-
2	3
3	-

If we try to access P1 at address 3, this will result in a _____.

- ✔◯ Page fault
- ◯ fork
- ◯ Main memory access
- ◯ Memory violation

Question 33

0 / 1 point

What must generally be true about CPU slice time compared to Context Switch time?

- CPU slice time must be comparable to Context Switch time
- ✗ CPU slice time must be much smaller than Context Switch time
- ➡ CPU slice time must be much larger than Context Switch time
- There is no relevance between the two

Question 34

0 / 1 point

What is the ARM instruction mneumonic to jump to a branch label?

- ➡ B
- ✗ Branch
- Jump
- BNE

Question 35

1 / 1 point

What is the purpose of doing concurrent programming?

- Write programs that are more efficient
- Write programs that run faster
- Write programs that make use of inner working of hardware/software interaction
- ✔ All of the above

Question 36 **0 / 1 point**

Assume that we only want to load a single Byte into a register. Which ARM instruction is most efficient to use for this?

- LDR
- LDRBYTE
- ✖ LDRSH
- ➡ LDRB

Question 37 **1 / 1 point**

In a traditional computer system, why can't two process run at the same time?

- Operating system cannot handle more than one process

✔ There is only one processor to run on

Main memory can only handle one memory unit at a time

Disk access can only occur one at a time

Question 38 **0 / 1 point**

Where are virtual pages stored?

✖ In main memory

In hard disk

➡ In main memory and hard disk

They are not stored, they are "virtual"

Question 39 **1 / 1 point**

The major problem with a FIFO (first in first out) page replacement policy is:

Has many computations

None of these answers

- Must be updated after every in-memory page access
- ✔ FIFO does not guarantee that the number of page faults will decrease with increasing memory size

Question 40 **1 / 1 point**

By default, the LDR comand in ARM loads values of which size?

- 8 bits
- ✔ 32 bits
- Can be set by a literal
- 16 bits

Question 41 **1 / 1 point**

Which of the following statements are true?

- ✔ Improving performance increases the power consumption
- None of these
- Power consumption and performance can be simultaneously improved

- ◯ NRE cost and performance can be simultaneously improved

Question 42 **1 / 1 point**

Which of the following is not an example of an exception?

- ◯ Page fault
- ◯ System call
- ◯ Timer interrupt
- ✔ ◯ Cache optimization miss

Question 43 **1 / 1 point**

Which of the following is the most LIKELY page size in a modern operating system.

- ◯ 24 KBytes
- ◯ 256 Bytes
- ◯ 32 Bytes
- ✔ ◯ 8 KBytes

Question 44

1 / 1 point

Why can't a program be thought of as a process?

- ○ A program does not deal with functions
- ○ A program does not deal with data
- ○ A program executes only on a kernel
- ✔ ○ A program can cause multiple processes to execute

Question 45

1 / 1 point

Assume that we have a 16 bit virtual address space mapping to a 16 bit physical address space. If there is an entry for every 16 bits (2 Byte) of physical memory, how large will the address translation table be?

- ✔ ○ 64 KB
- ○ 256 KB
- ○ 128 KB
- ○ 32 KB

Question 46

0 / 1 point

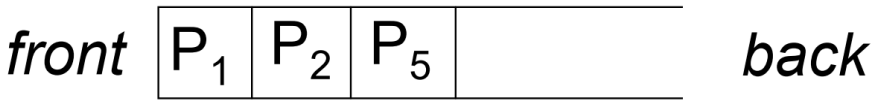
Assume that we have a register r4 that contains the value 1000. What will this register hold once the following peice of instruction is exectued?

```
LDR      r8, [r4, #24]!
```

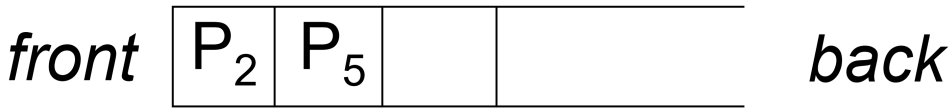
- ➡ ◯ 1004
- ◯ 1076
- ✖ ◯ 1024
- ◯ 1000

Question 47 **0 / 1 point**

A ReadyQ is shown below for a scheduling policy.



After a while, the ReadyQ is changed to the following



What kind of policy is shown?

- ✖ ◯ Preemptive FCFS (First Come First Serve)

- Non-preemptive FCFS (First Come First Serve)
- Shortest Process Next
- ➡ Either Preemptive or non-preemptive FCFS (First Come First Serve)

Question 48 **1 / 1 point**

How many times is the following piece of code executed?

```
        MOV r2, #1
LOOP    ADD r2, r2, #1
        CMP r2,#20
        BNE LOOP
```

- 21
- Never executes as condition is false
- 1
- ✔ 19
- 20

Question 49 **1 / 1 point**

Assume that we have a register r5. We set this register value to the decimal number 2857740885. What will be the equivalent Hexadecimal number in register r6 after the following code executes?

```
MVN r6,r5
```

- 00AA00AA
- FFFFFFFF
- ✔ 55AA55AA
- AA55AA55

Question 50 **1 / 1 point**

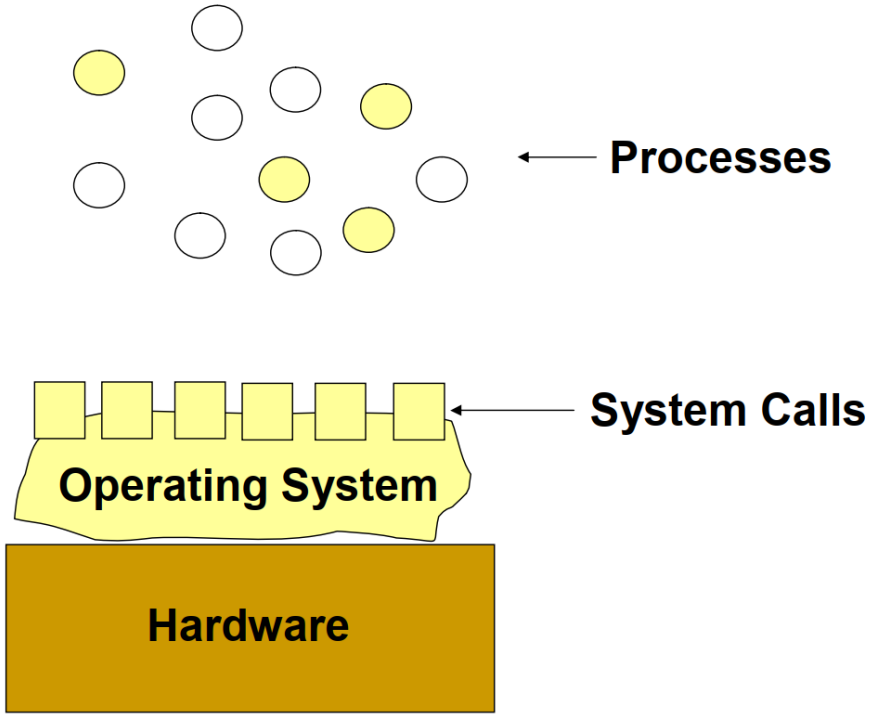
What is a typical Context Switch time in modern operating systems?

- Order of 100's of millisecond
- ✔ Order of microseconds
- Order of milliseconds
- Orders of 100's of microseconds

Question 51

1 / 1 point

We described the operating system interaction with the hardware as shown below:



What do the yellow circles above the diagram represent?

- ✔ Processes that run code for the Operating System
- Process that interact with the hardware
- Process that the user runs

- Any process

Question 52 **1 / 1 point**

What is Thumb mode in ARM?

- Allows you to perform 8 bit operations
- Allows you to perform 32 bit operations.
- Allows you to perform 4 bit operations
- ✔ Allows you to perform 16 bit operations

Question 53 **0 / 1 point**

Assume that we have a register r4 that contains the value 5000. What will this register hold once the following peice of instruction is exectued?

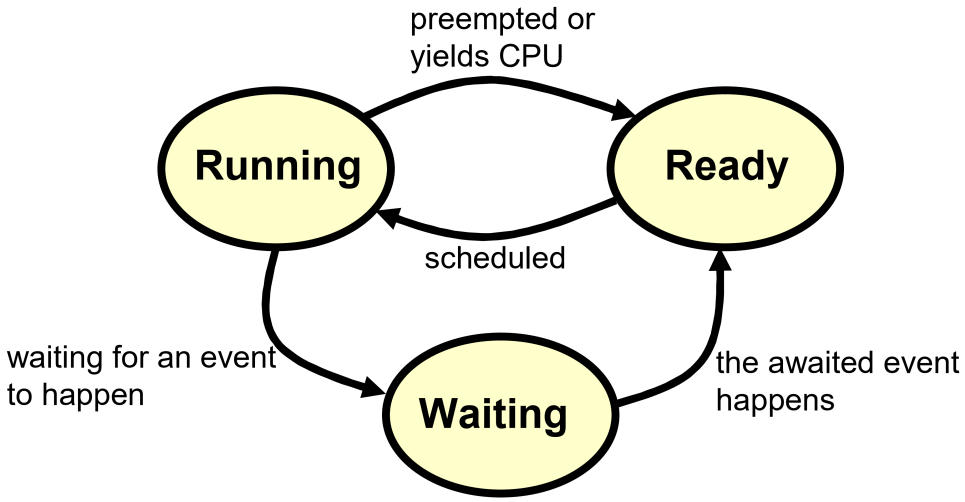
```
LDR      r8, [r4, #24]!
```

- 5000
- 4076
- ➡ 5004

✖ ◯ 5024

Question 54 **1 / 1 point**

The following is a Process state transition program



How many running events are there at any given time?

◯ Depends on the OS

◯ Depends how many ready processes there are

◯ at least one

✔ ◯ only one

Question 55

1 / 1 point

The amount of time that a process within your program uses a CPU is called

- process real time
- ✔ process virtual time
- process wallclock time
- process elapsed time

Question 56

1 / 1 point

Consider a 5-state pipeline with stage delays of 45, 30, 28, 42, and 30 nanonseconds including the delay. It is required to process 1000 data items in the pipeline. What will be the minimum time required to process the data items?

- 28.11 microseconds
- ✔ 45.18 microseconds
- 42.17 microseconds
- 42.17 microseconds

Question 57 **1 / 1 point**

Conditional executions are something specific to ARM family of microcontrollers, you generally do not see it in other microcontroller families.

- ✔ ◯ True
- ◯ False

Question 58 **1 / 1 point**

ARM microcontroller are normally work on 32 bit registers. If you want to work on 8 bit registers, in general, the instructions are the same except that you add the following to the end of the regular 32 bit instructions

- ◯ BIT
- ◯ WORD
- ◯ BYTE
- ✔ ◯ B

Question 59 **1 / 1 point**

Which of the following statements is false?

- ✔ ◯ In Von Neumann architecture, instructions and data are stored in separate memory

- In Von Neumann architecture, both instructions and data are stored in the same memory
- In Harvard architecture, instructions and data are stored in separate memory
- All are false

Question 60 **1 / 1 point**

Assume that an ARM Cortex M3 microcontroller has register values r1=10, r2=20 and r3=30. Assume we execute the following Assemly code

ADD r4, r1, r3

SUB r4, r4, r2

RSB r4, r1, r4

What will be the value stored in register r4?

- 20
- ✔ 10
- 30
- 25

Attempt Score:73.33 %

Overall Grade (highest attempt)**:**73.33 %

Done