QUESTIONNAIRE

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1. Section: *Memory and Cache*

Question 1.1: Determine the cache controller's interface to Cache SRAM.

a) Number of FPGA pins reserved for SRAM Address Bus = _____20_____ [1 mark]

b) Number of FPGA pins reserved for Cache SRAM Data Bus = ___32_____ [1 mark]

c) Select from the list below and print two control lines to be used for Cache SRAM interface:

1. __WE_____ and 2. _OE__ [2 marks]

Question 1.2: Determine the cache controller's interface to Main Memory (DDR-SDRAM)

a) Number of FPGA pins reserved for the SDRAM Address bus = ___16_____ [2 marks]

Show calculations on the line below:

Log(4G)/Log(2)

b) Number of FPGA pins reserved for the SDRAM Data bus = _____32__ [1 mark]

c) Select from the list below and print two control lines to be utilized for Main memory DDR-SDRAM interface:

1. _WE_ and 2. _OE____ [2 marks]

d) Select three synchronization lines to be utilized for DDR-SDRAM interface:

1. _RAS___ ; 2. _CAS__ and 3. _Clock_ [3 marks]

Determination of the Cache controller organization

Question 1.3: Determine the "Block offset" field associated with the block size (Number of 32-bit words in the block) performing the following steps of design:

Step 1: Determine the bus clock period – $\boldsymbol{t}_{bus}$ = ___5_____ nS [1 mark]

Step 2: Determine the 32-bit data word transfer time – $\boldsymbol{T}_{wt}$ = _____2.5_____ ns [2 marks]

Show calculations on the line below:

Twt = Tbus / 2 = 2.5 ns

Step 3: Determine miss penalty *T miss* = *138.33* *nsec* [2 marks]
Show calculations on the line below:

Thit =2.5+2.5=5ns; Tmiss = (7-(0.985*5))/0.015=138.33ns

Step 4: Determine the optimal block size (Number of words in block - *N*)

Thus, number of words in block - *N* = 16 words [2 marks]
Show calculations on the line below:

T miss = 1.3*((13*5)+N*Twt)+Thit; Thit=5; N =16

Step 5: Therefore, Block offset = 4 bits [1 mark]

Question 1.4: Determine the "Index" field associated with the number of Cache entries.

Number of Cache entries = 65536 [2 marks]
Show calculations

Cache volume/Block Size = 4*1024*1024/(32*4) = 32768

Index field (number of bits for "Index") = 15 bits [1 mark]

Question 1.5: Determine the "TAG" field (number of bits for tag associated with the volume of Main memory address area)

Number of TAG bits = 15 [1 marks]
Show calculations

Word length – Index length – Block offset

Question 1.6: Calculate the volume of service cache controller's BRAM

Volume of BRAM = 64 KB [2 marks]

Show calculations
*2B*32768/1024 = 64 KB*

Cache performance verification

Question 1.7: 027C124A Rd; 027C124C Wr; 02AC124C Wr; 027C1242 Rd [5 marks]

Reference Address (hex) *	TAG (hex)	Cache entry # = Index (hex)	Word # (Decimal)	Hit? Y/N	D-bit 0 or 1
027C124A Rd	027	C124	10	N	0
027C124C Wr	027	C124	12	Y	1
02AC124C Wr	02A	C124	12	N	1
027C1242 Rd	027	C124	2	N	0

Question 1.8: List all references which will initiate the "Write back" procedure [3 marks]

Reference Address which caused "write back" (hex)	Initial block address to be returned to memory (hex)	Initial block address to be loaded from memory (hex)
02A C124 C	027 C124 0	02A C124 0
027 C124 2	02A C124 0	027 C124 0

Question 1.9: For the above test sequence list references that caused ping-pong effect.

a) ___**02AC124C** _____ and b)_____ **027C1242** _____ [2 marks]

2. Section: *Virtual memory*

Question 2.1:
a) Calculate the maximum number of page table entries for Task 1, Task 2.and Task 3:

Maximum number of Page Table entries:

For Task 1 = ____16 GB /16 KB = 1048576 entries_____ = _1 M [1 mark]

For Task 2 = ____4 GB /16KB = __262144 entries_____ =__250 K [1 mark]

For Task 3 = ____5632 MB / 16KB = 360448 entries _____ =__352 K [1 mark]

b) Calculate the volume of Main memory (SDRAM) used for all page tables

Physical page number field = __20_____ bits [1 mark]

Show calculations
Log(Memory Volume/Page Size) = log(16GB/16KB)/log(2) = 20

Page entry length = ____1_____ Bytes [1 mark]

Show calculations

20+3 = 23 bits; 23/(4*8) = 0.71 bytes = 1 Byte; this is because minimum accessible data is 4 Bytes

Main memory volume to be reserved for Page Tables = __2_____ MB [1 mark]

Show calculations

(1671168 entries)*1Byte/1024 =1632 KB = 2MB

Question 2.2: Determine the following:

a) Page offset (hex) = ___03F0_____ [1 mark]

b) Virtual page number of the addressed data = ____00D9_____ [1 mark]

c) Calculate the physical address of the Page Table entry where Physical page number of the requested data should be found:

Page Table Entry address = ___2C2AB0D9_____ [2 marks]

Show calculations ___2C2AB000 + 00D9_____

d) If the physical page number retrieved from the addressed Page Table entry was valid (exist in the Page Table) and was equal to 01CB7 (hex), calculate the physical address of the requested data.

Physical address = _____1CB703F0__ [1.5 marks]

Show calculations ___01CB7 concatenated with page offset 03F0_____

e) Fill the entry of this TLB [2.5 marks]

TLB –entry

V-bit	TAG	Physical Page #	Dirty-bit	Reference bit
1	00D9	01CB7	1	1