

Ryerson University
Department of Electrical and Computer Engineering
ELE734 and EE8506: LOW-POWER DIGITAL INTEGRATED CIRCUITS
Final Examination, December 13, 2017
Duration: 3 hours

Student's Name: *Solution*.....

Student's Number: Section:

NOTES:

1. This is a **Closed Book** examination. No aids other than the approved calculators and **1 aid-sheet (both sides)** is allowed.
2. Answer all questions.
3. **No questions are to be asked** in the examination hall. If doubt exists as to the interpretation of any question, the student is urged to submit with the answer paper, a clear statement of any assumptions made.

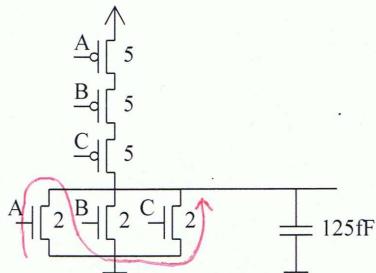
<i>Question No.</i>	<i>Mark of each question</i>	<i>Mark obtained</i>
Q1	20	
Q2	20	
Q3	20	
Q4	20	
Q5	20	
Q6	20	

Total (Out of 120):

Q1:

Assume the on-resistance of a unit nMOS is 15Kohms and the on-resistance of a unit pMOS is 30Kohms. Also assume the drain, source, and gate capacitances of a unit transistor are all equal to 15fF. Use Elmore delay to calculate the delay of the following gate when the input of the gate is transitioned from A=1, B=0, C=0 to A=0, B=0, C=0.

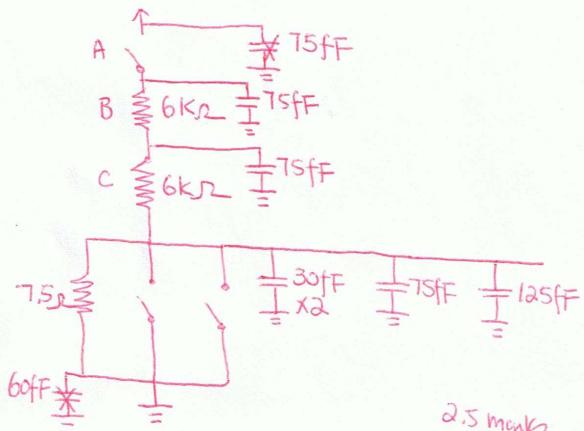
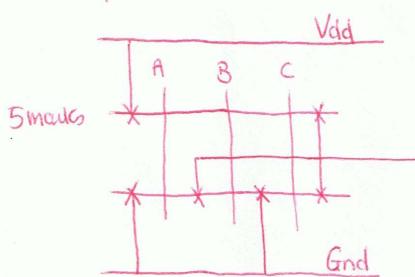
Please assume diffusion sharing is always used to minimize the layout area of the gate.
 (20 marks)



$$\rightarrow \frac{30k\Omega}{5} = 6k\Omega \quad 15fF \cdot 5 = 75fF$$

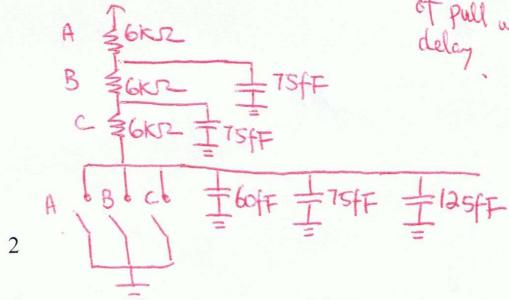
A=1 B=0 C=0

$$\rightarrow \frac{15k\Omega}{2} = 7.5k\Omega \quad 15fF \cdot 2 = 30fF$$



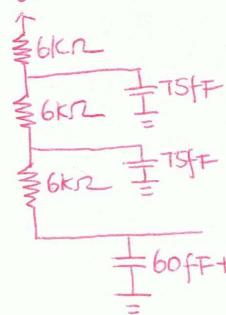
A=0 B=0 C=0

2.5 marks
 correct prediction
 of pull up
 delay.



2

V_{DD}



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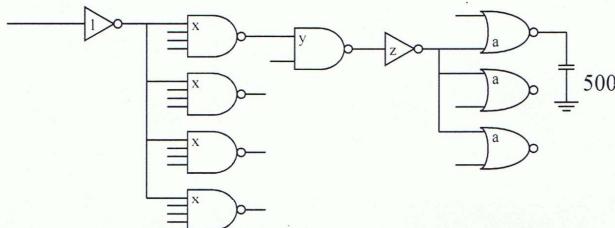
5 marks correct pull up network
R + C values

$$\frac{1}{2} 60ff + 75ff + 125ff = 260ff$$

$$\begin{aligned}
 & (260ff \cdot 3 \cdot 6K) + 75ff \cdot 2 \cdot 6K + 75ff \cdot 6K & \text{5 marks} \\
 & = 4680ps + 900ps + 450ps & \text{correct equation} \\
 & = 6030ps & \\
 & = 6.030 \text{ ns} & \text{Q.5 marks correct answer}
 \end{aligned}$$

Q2:

- Calculate the optimum path delay for the following circuit and the value of x, y, z, and a in order to achieve optimum delay. (inverter: $g=1$, $p=1$; 4-input nand: $g=6/3$; $p=4$; 2-input nand: $g=4/3$, $p=2$; 2-input nor: $g=5/3$, $p=2$). (8 marks)
- Draw the transistor level diagram for the 2-input nand gate and clearly label the size of each transistor on your drawing. (3 marks)
- Draw the transistor level diagram for the inverter that is between the 2-input nand gate and the 2-input nor gate and clearly label the size of each transistor on your drawing. (3 marks)
- Calculate the optimum path delay if additional inverter stages can be added between the 2-input nor gate and the load capacitance. (2 marks)
- How many additional stages should be added in part d) in order to achieve the optimum delay and what should be the size of each stage? (4 marks)



a) $F = GBH$

$$G = 1 \cdot \frac{6}{3} \cdot \frac{4}{3} \cdot 1 \cdot \frac{5}{3}$$

$$B = 4 \cdot 1 \cdot 1 \cdot 3 \cdot 1$$

$$H = \frac{500}{1}$$

$$F = 1 \cdot \frac{6}{3} \cdot \frac{4}{3} \cdot 1 \cdot \frac{5}{3} \cdot 4 \cdot 1 \cdot 1 \cdot 3 \cdot 1 \cdot \frac{500}{1}$$

$$= \frac{720000}{27}$$

$$= 26666.67$$

$$(F)^{\frac{1}{5}} = (26666.67)^{\frac{1}{5}}$$

$$= 7.677 \quad (1.5 \text{ marks})$$

$$(7.677 \cdot 5) + 1 + 4 + 2 + 1 + 2$$

$$= 48.385 \quad (1.5 \text{ marks})$$

$$1 \cdot \frac{4 \cdot x}{1} = 7.677$$

$$x = 1.919$$

(1 mark)

$$\frac{6}{3} \frac{y}{x} = 7.677$$

$$y = 7.366$$

(1 mark)

$$\frac{4}{3} \frac{z}{y} = 7.677$$

$$z = 42.412$$

(1 mark)

$$1 \cdot \frac{3 \cdot a}{z} = 7.677$$

$$a = 108.532$$

(1 mark)

$$\frac{5}{3} \frac{500}{a} = 7.678$$

(1 mark for effort)

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b)

$$y = 7.366$$

$$7.366 \cdot 3c = 22.098 \text{ C}$$

c)

$$z = 42.412$$

$$\frac{42.412 \cdot 3c}{3} \cdot 2 = 84.824$$

$$\frac{42.412 \cdot 3c}{3} \cdot 1 = 42.412$$

d) $F = GBA$

$$= 26666.67$$

$$(F)^{1/8} = 3.59$$

$$N = 7.97 \approx 8 \text{ stages}$$

$$(26666.67)^{1/8} = 3.575$$

$$(26666.67)^{1/8} \cdot j + 1 + 4 + 2 + 1 + 2 + 1 + 1 + 1 = 41.598 \quad (2 \text{ marks})$$

e) 3 stages

$$1 \text{ mark}$$



$$1 \cdot \frac{500}{d} = 3.575$$

$$d = 139.860 \quad 1 \text{ mark}$$

$$\frac{4 \cdot 4.281}{3} = 3.575$$

$$1 \cdot \frac{139.860}{c} = 3.575$$

$$y = 1.5967$$

$$c = 39.122 \quad 1 \text{ mark}$$

$$\frac{6}{3} \cdot \frac{1.5967}{x} = 3.575$$

$$1 \cdot \frac{39.122}{b} = 3.575$$

$$x = 0.893$$

$$b = 10.943 \quad 1 \text{ mark}$$

$$1 \cdot \frac{4 \cdot 0.893}{1} = 3.573 \checkmark$$

$$\frac{2}{3} \cdot \frac{10.943}{a} = 3.575$$

$$a = 5.102$$

$$1 \cdot \frac{3 \cdot 5.102}{z} = 3.575$$

$$z = 4.281$$

Q3:

- Consider an 8mm-long, 4λ wide metal wire in a 0.6 um process. The sheet resistance of the metal is 0.08 ohm per square and the capacitance of the wire is 0.2 fF per um. Construct a 4-segment π -model for the wire. (7 marks)
- Assume one end of the wire is attached to the input of a 2x unit-sized inverter and a 5x unit-sized inverter drives the other end of the wire. Also assume both the gate and diffusion capacitance of a minimum width transistor is 2fF, the diffusion resistance of a minimum width nmos transistor is 2.5k ohms and the diffusion resistance of a minimum width pmos transistor is 5k ohms, and a unit-sized inverter consists of a 1x nmos transistor and a 2x pmos transistor. Use the π -model constructed in part a) to calculate the propagation delay from the 5x inverter to the 2x inverter. (7 marks)
- If a unit-sized inverter is inserted to the middle of the wire, what will be the new propagation delay from the 5x inverter to 2x inverter. (6 marks)

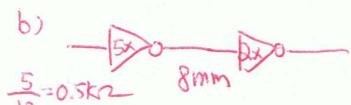
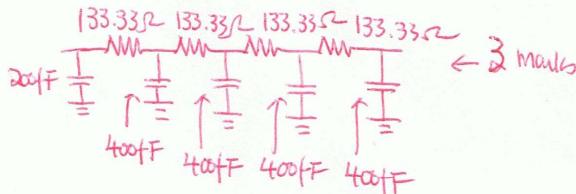
$$(a) \lambda = \frac{0.6 \mu m}{2} \\ = 0.3 \mu m$$

$$4\lambda = 4 \cdot 0.3 = 1.2 \mu m$$

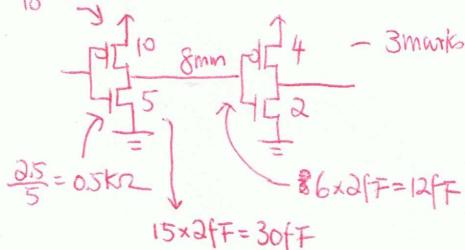
$$\frac{8mm}{1.2 \mu m} = \frac{8 \times 10^{-3}}{1.2 \times 10^{-6}} = 6,666.7 k\Omega \quad \leftarrow 1 \text{ mark}$$

$$6,666.7 k\Omega \cdot \frac{0.08 \Omega}{\square} = 533.33 \Omega \quad \leftarrow 1 \text{ mark}$$

$$\frac{8mm}{1 \mu m} \cdot 0.2 fF/\mu m = 1600 fF \quad \leftarrow 1 \text{ mark}$$



b)

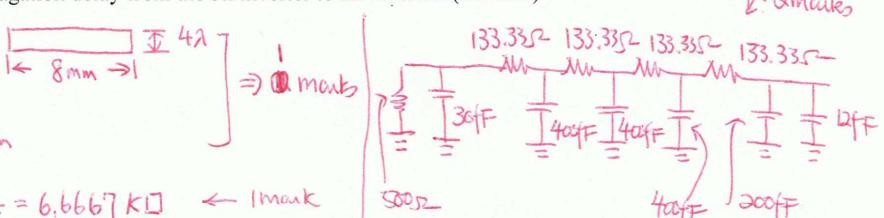


$$\frac{0.25}{5} = 0.05 k\Omega$$

$$15 \times 2 fF = 30 fF$$

$$8.6 \times 2 fF = 12 fF$$

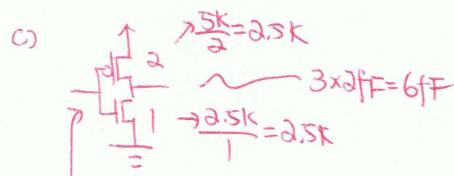
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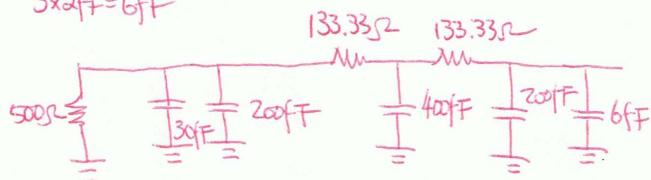
$$212 fF (133.33 \times 4 + 500) + 400 fF (133.33 \times 3 + 500) \\ + 400 fF (133.33 \times 2 + 500) + 400 fF (133.33 + 500) \\ + 230 fF \cdot 500$$

$$= (0.219 + 0.360 + 0.307 + 0.253 + 0.115) \text{ ns} \\ = 1.254 \text{ ns} - 2 \text{ marks.}$$

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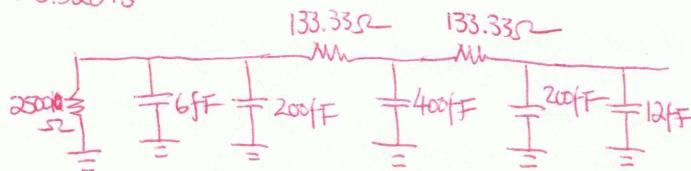
$$3 \times 2fF = 6fF$$



$$206fF(133.33 \times 2 + 500) + 400fF(133.33 + 500) + 230fF \cdot 500$$

$$= 0.158ns + 0.253ns + 0.115ns$$

$$= 0.526 ns$$



$$212fF(133.33 \times 2 + 2500) + 400fF(133.33 + 2500) + 206fF(2500)$$

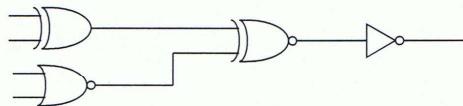
$$= 0.587ns + 1.053ns + 0.515 ns$$

$$= 2.155ns$$

$$0.526 + 2.155 = 2.681 ns$$

Q4:

- a) Assume each primary input to the circuit has 50% probability of being 1. Calculate the activity factor for all internal and output nodes of the following circuit. (5 marks)



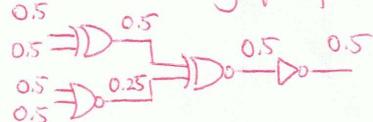
- b) Draw the circuit diagram of a d-type static flip-flop. (5 marks)
 c) Draw the circuit diagram of a circuit that allows a signal to safely cross clock domains. (5 marks)
 d) What is stack effect? (5 marks)

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

$$0.5 \times 0.5 + 0.5 \times 0.5 = 0.5$$

A	B	XOR
0	0	1
0	1	0
1	0	0
1	1	0

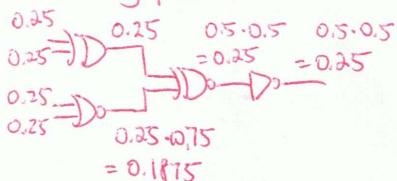
Probability of being 1.



A	B	XOR
0	0	1
0	1	0
1	0	0
1	1	1

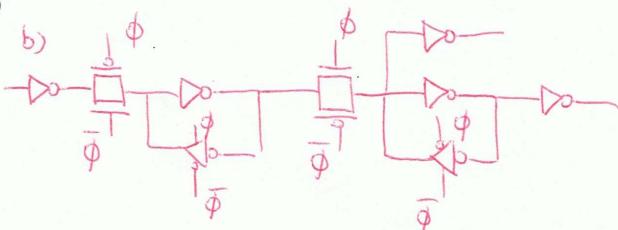
$$0.5 \times 0.5 = 0.25$$

Activity factor



1 mark for each activity factor

1 mark for effort

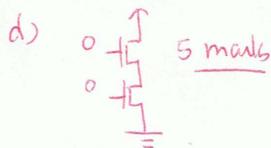


Topology 2.5 marks

clocking 2.5 marks



5 marks

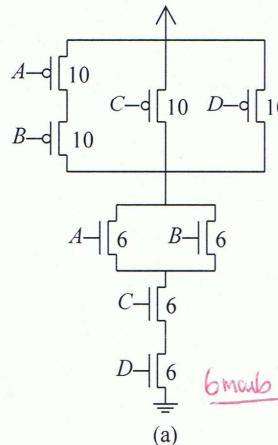


5 marks

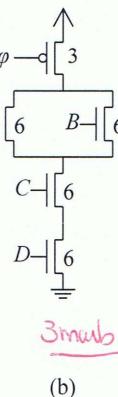
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Q5:

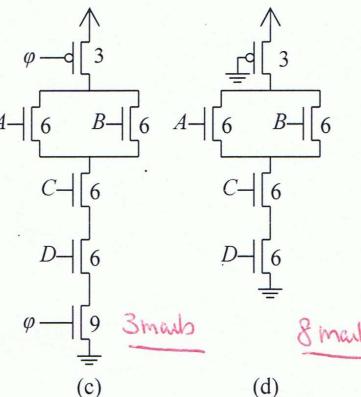
Estimate the worst case pull-down and pull-up (if applicable) logic efforts and parasitic delays for input A of the following 4 gates. (20 marks)



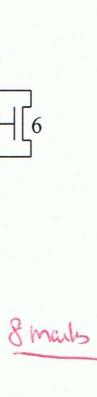
(a)



(b)



(c)



(d)

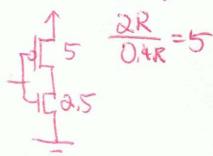
a) Pull up

$$\frac{2R}{10} \cdot 2 = \frac{4R}{10} = 0.4R$$

Pull down

$$\frac{R}{6} \cdot 3 = \frac{R}{2} = 0.5R$$

Pull up logic effort + Parasitic delay



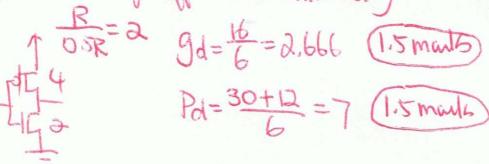
$$g_u = \frac{16}{7.5} = 2.133$$

1.5 mauls

$$P_d = \frac{30+12}{7.5} = 5.6$$

1.5 mauls

Pull down logic effort + Parasitic delay



$$g_d = \frac{16}{6} = 2.666$$

$$P_d = \frac{30+12}{6} = 7$$

1.5 mauls

b) Pull up logic effort + Parasitic delay N/A.

Pull down logic effort + Parasitic delay.

$$g_u = \frac{6}{2} = 3$$

$$g_d = \frac{6}{6} = 1$$

-1.5 mauls

$$P_d = \frac{6+6+3}{6} = 2.5$$

-1.5 mauls

c) Pull up logic effort + Parasitic delay N/A.

$$\frac{R}{6} \times 3 + \frac{R}{9} = 0.6111R$$

$$\frac{R}{0.6111R} = 1.636$$

$$g_u = \frac{6}{3.273+1.636} = 1.222$$

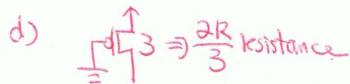
$$g_d = \frac{6}{3.273+1.636} = 1.222$$

-1.5 mauls

$$P_d = \frac{6+6+3}{3.273+1.636} = 3.056$$

-1.5 mauls

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d)  $\Rightarrow \frac{2R}{3}$ resistance

$$I_{DD} = \frac{V_{DD}}{\frac{3+2R}{3}} = \frac{3V_{DD}}{2R}$$

pull up logic effort + parasitic delay



$$g_u = \frac{6}{4.5} = 1.333 \text{ - } 2 \text{ mauls}$$

$$P_u = \frac{6+6+3}{4.5} = 3.333 \text{, } 2 \text{ mauls}$$

pull down logic effort + parasitic delay

$$\frac{R}{6} \cdot 3 = \frac{R}{2}$$

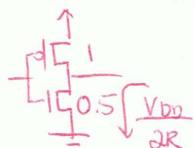
$$I_{GND} = \frac{V_{DD}}{\frac{R}{2}} = \frac{2V_{DD}}{R}$$

Net flow down current

$$I_{GND} - I_{DD} = \frac{2V_{DD}}{R} - \frac{3V_{DD}}{2R}$$

$$= \frac{4V_{DD} - 3V_{DD}}{2R}$$

$$= \frac{V_{DD}}{2R}$$

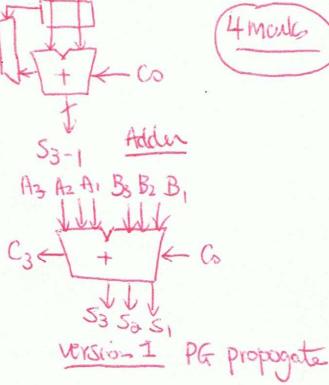
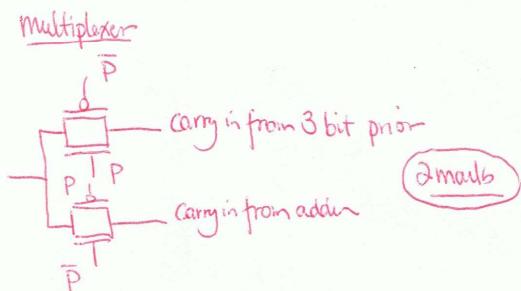
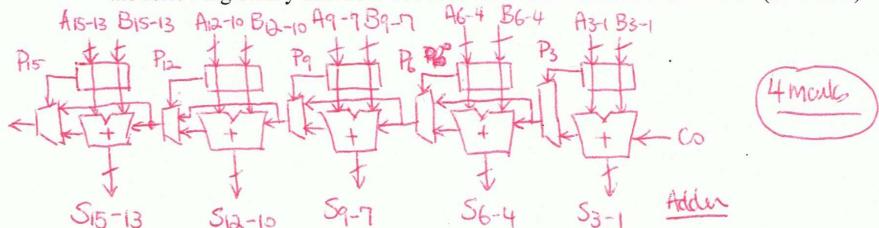


$g_d = \frac{6}{1.5} = 4 \text{ - } 2 \text{ mauls}$

$P_d = \frac{6+6+3}{1.5} = 10 \text{ - } 2 \text{ mauls}$

Q6:

- a) Design a 15-bit carry-skip adder based on 3-bit group propagate signals. Please describe your design in detail all the way down to the logic gates. (10 marks)
- b) Let t_{pg} be the propagation delay of generating a 3-bit group propagate signal, t_{AO} be the delay of an AND-OR gate, t_{mux} be the delay of a two-input multiplexer, t_{xor} be the delay of a 2-input xor gate. What will be the delay for the adder to perform the following binary addition: 101110110110111 + 101101101010111? (10 marks)



$$P_x = A_x \oplus B_x$$

$$G_x = A_x \cdot B_x$$

$$S_x = P_x \oplus C_{x-1}$$

$$S_1 = P_1 \oplus C_0$$

$$S_2 = P_2 \oplus C_1$$

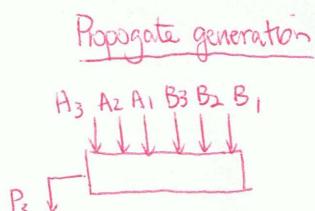
$$S_3 = P_3 \oplus C_2$$

$$C_x = G_x + P_x \cdot \cancel{C_{x-1}}$$

$$C_1 = G_1 + P_1 \cdot C_0$$

$$C_2 = G_2 + P_2 \cdot C_1$$

$$C_3 = G_3 + P_3 \cdot C_2$$



Ax	Bx	
0	0	K
0	1	P
1	0	P
1	1	G

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version 2 carry propagate (also 0, k.)

~~version 1 carry propagate~~

Ans:

$$S_x = A_x \oplus B_x \oplus C_{x-1}$$

↓

$$S_1 = A_1 \oplus B_1 \oplus C_0$$

$$S_2 = A_2 \oplus B_2 \oplus C_1$$

$$S_3 = A_3 \oplus B_3 \oplus C_2$$

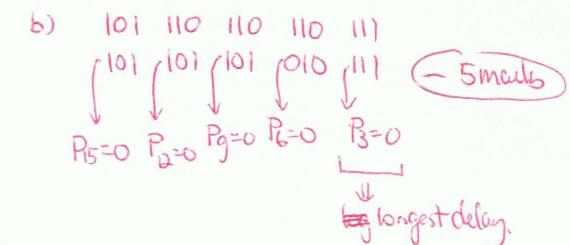
$$C_x = A_x \cdot B_x + A_x \cdot C_{x-1} + B_x \cdot C_{x-1}$$

↓

$$C_1 = A_1 \cdot B_1 + A_1 \cdot C_0 + B_1 \cdot C_0$$

$$C_2 = A_2 \cdot B_2 + A_2 \cdot C_1 + B_2 \cdot C_1$$

$$C_3 = A_3 \cdot B_3 + A_3 \cdot C_2 + B_3 \cdot C_2$$



$$\begin{aligned} \text{delay} &= t_{pg} + (3-1)t_{ao} \\ &= t_{pg} + 2t_{ao} \end{aligned}$$