
# Faculty of Engineering and Architectural Science

## Department of Electrical and Computer Engineering

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| **Course Number** | ELE 734 |
| **Course Title** | Low-Power Digital Integrated Circuits |
| **Semester/Year** | F2020 |
| **Lab No** | 04 |
| **Instructor Name** | Dr. Andy Ye |
| **Section No** | 06 |

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|---|---|
| **Submission Date** | 12/07/2020 |
| **Due Date** | 12/07/2020 |

| Name | Student ID | Signature* |
|---|---|---|
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# Contents

# 1. Pre-Lab

## 1.1.

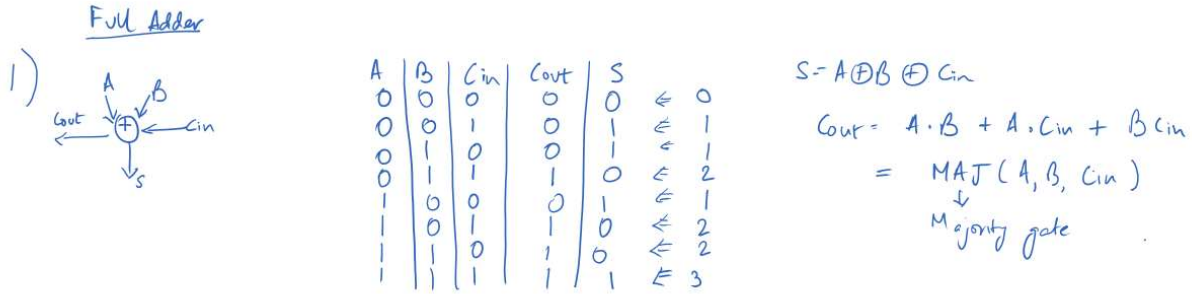


*Figure 1: Truth table of a 1-bit full adder, and the Boolean logic derivation describing the S and $C_{out}$ bits.*

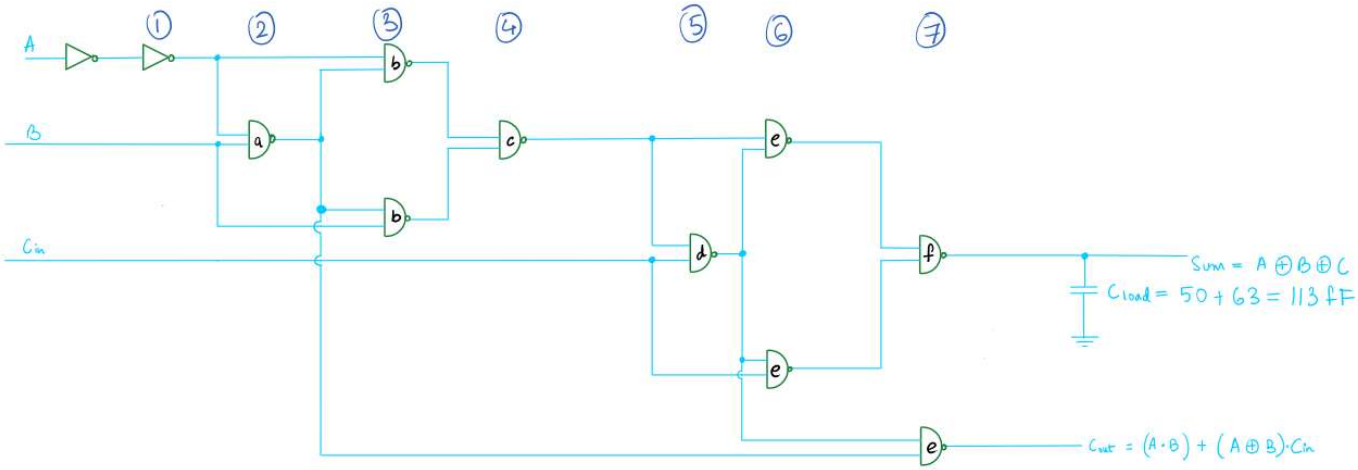


*Figure 2: Full Adder gate level schematic.*

## 1.2

$g_1 = 1$ ; $p_1 = 1$ ; $h_1 = a/1$ ; $b_1 = 2$
$g_2 = 4/3$ ; $p_2 = 2$ ; $h_2 = b/a$ ; $b_2 = 3$
$g_3 = 4/3$ ; $p_3 = 2$ ; $h_3 = c/b$ ; $b_3 = 1$
$g_4 = 4/3$ ; $p_4 = 2$ ; $h_4 = d/c$ ; $b_4 = 2$
$g_5 = 4/3$ ; $p_5 = 2$ ; $h_5 = e/d$ ; $b_5 = 3$
$g_6 = 4/3$ ; $p_6 = 2$ ; $h_6 = f/e$ ; $b_6 = 1$
$g_7 = 4/3$ ; $p_7 = 2$ ; $h_7 = 113/f$ ; $b_7 = 1$

$F = G \times B \times H$
$G = 1 \times 1 \times 4/3 \times 4/3 \times 4/3 \times 4/3 \times 4/3 \times 4/3 = 5.686$
$B = 2 \times 3 \times 1 \times 2 \times 3 \times 1 \times 1 = 36$
$H = 18.25\,fF$

$F = 3691.42$
$(F)^{1/8} = 2.791$

$g_7 b_7 h_7 = 2.791 = \frac{4}{3} \times \frac{113}{f}$ ; $53.98 = f$

$g_6 b_6 h_6 = 2.791 = \frac{4}{3} \times \frac{f}{e}$ ; $25.78 = e$

$g_5 b_5 h_5 = 2.791 = \frac{4}{3} \times \frac{e}{d} \times 3$ ; $36.96 = d$

$g_4 b_4 h_4 = 2.791 = \frac{4}{3} \times \frac{d}{c} \times 2$ ; $35.31 = c$

$g_3 b_3 h_4 = 2.791 = \frac{4}{3} \times \frac{c}{b} \times 1$ ; $16.87 = b$

$g_2 b_2 h_2 = 2.791 = \frac{4}{3} \times \frac{b}{a} \times 3$ ; $24.17 = a$

NAND:-
width of 'a' ≈ 24/2 = 12
width of 'b' ≈ 17/2 = 8.5
width of 'c' ≈ 35/2 = 17.5
width of 'd' ≈ 37/2 = 18.5
width of 'e' ≈ 26/2 = 13
width of 'f' ≈ 54/2 = 27

$C_{load} = 50f + 63f = 113\,fF$

$F = G \times B \times H$

$H = \frac{C_{out}}{C_{in}}$ → Complete path

$= \frac{C_{out}}{2 \times C_{g,p} \times C_{g,n}}$

To get $C_{g,n}$, $C_{g,p}$:

ADE → DC Analysis → Results
DC operating points

$C_{gg}$ = total gate capacitance of MOS

$C_{g,n} = 1.8\,fF$

$C_{g,p} = 1.72\,fF$

$H = \frac{C_{out}}{C_{in}} = \frac{113}{2 \times 1.72 \times 8} = 18.25$

*Figure 3: Full Adder sizing to drive a load capacitance of 113fF at the its sum output.*

# 2. Post-Lab

## 2.1 Schematic of Full Adder using NAND2 gates

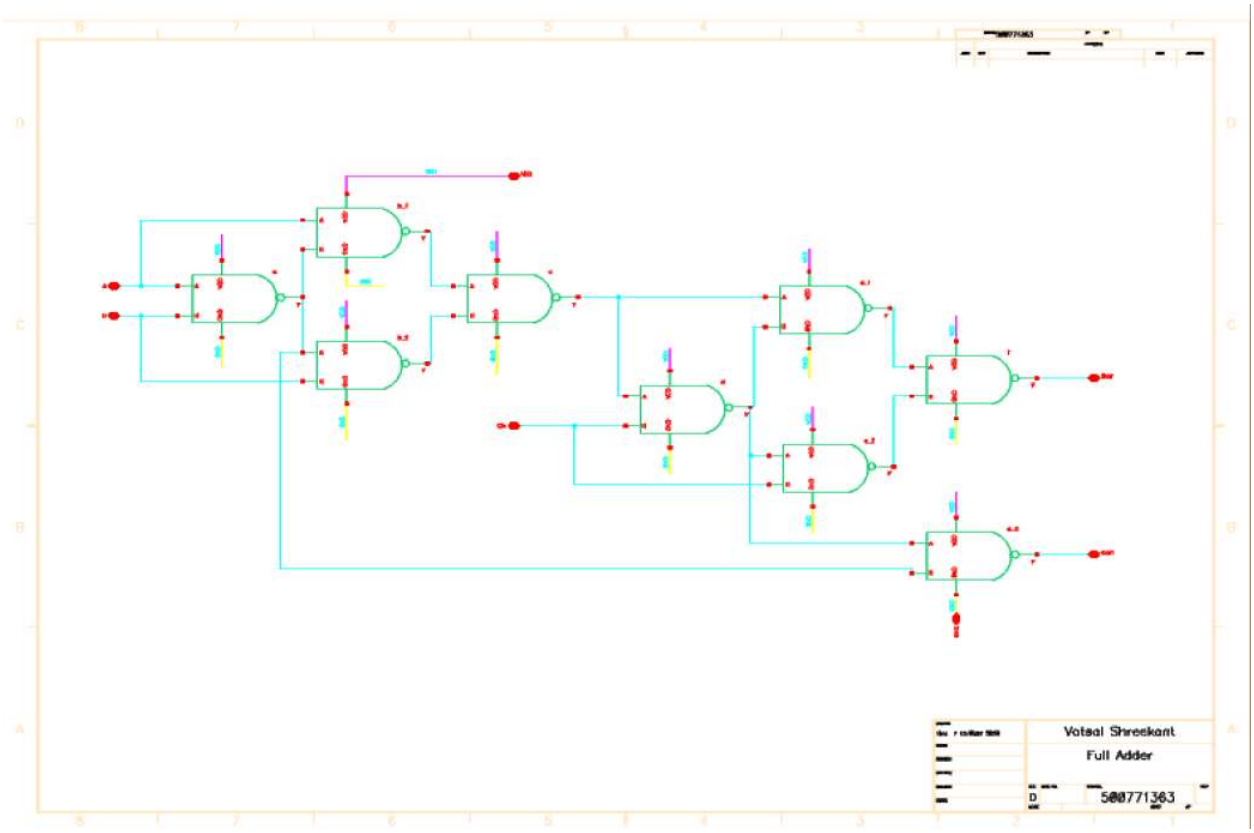


*Figure 4: Schematic of 1-bit Full Adder*

## 2.2 Schematic of Testbench of Full Adder

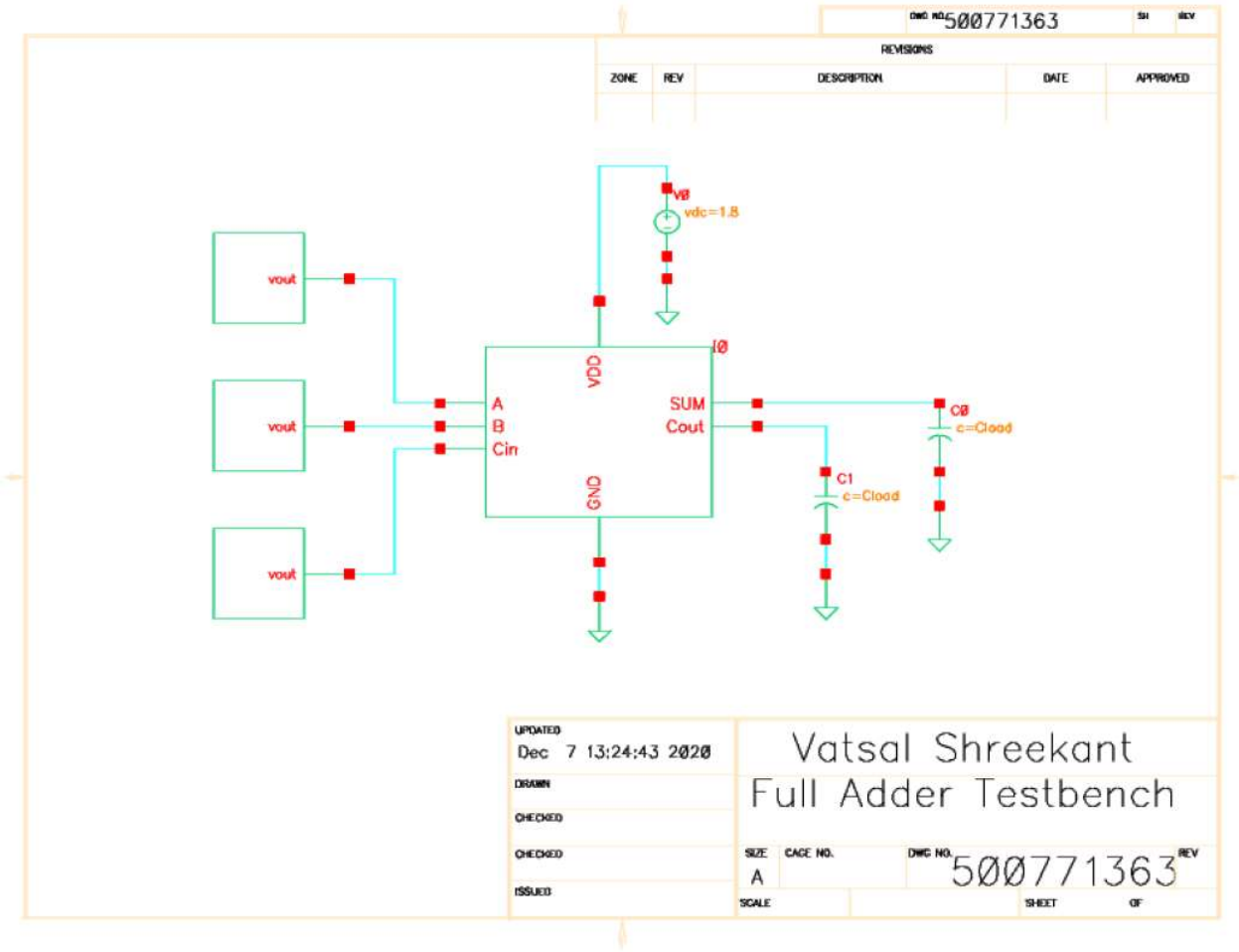


*Figure 5: Schematic of Full Adder Testbench*

## 2.3 Simulation of full adder for 20ns to verify the functionality.

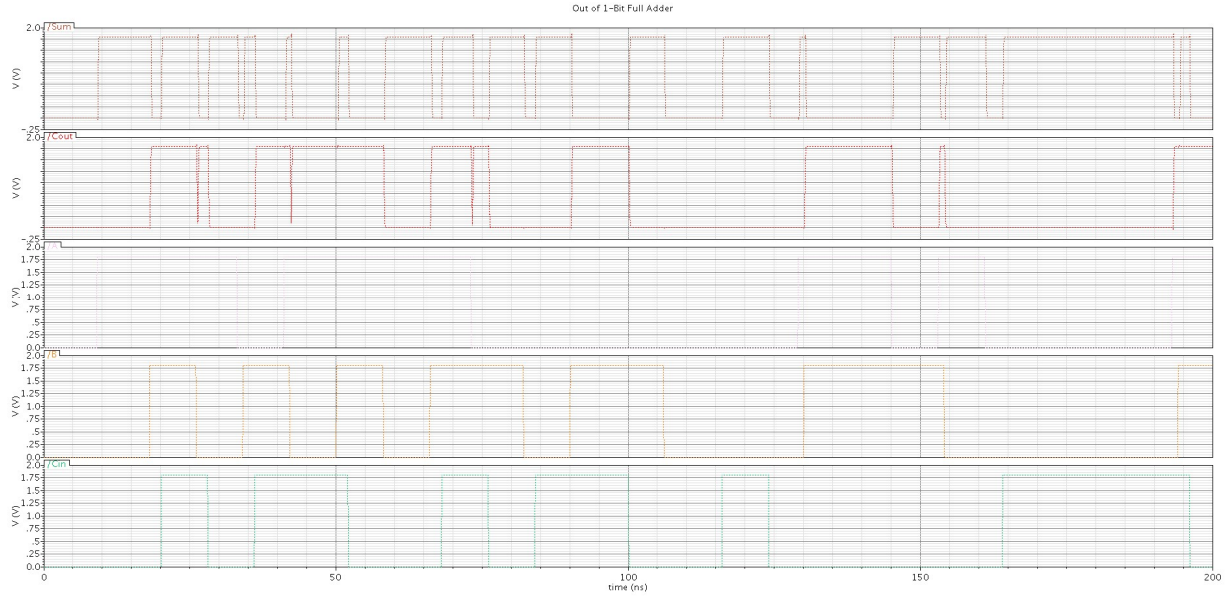


*Figure 6: Simulation of full adder for 20ns*

## 2.4 Layout and Extracted Views of the Full Adder

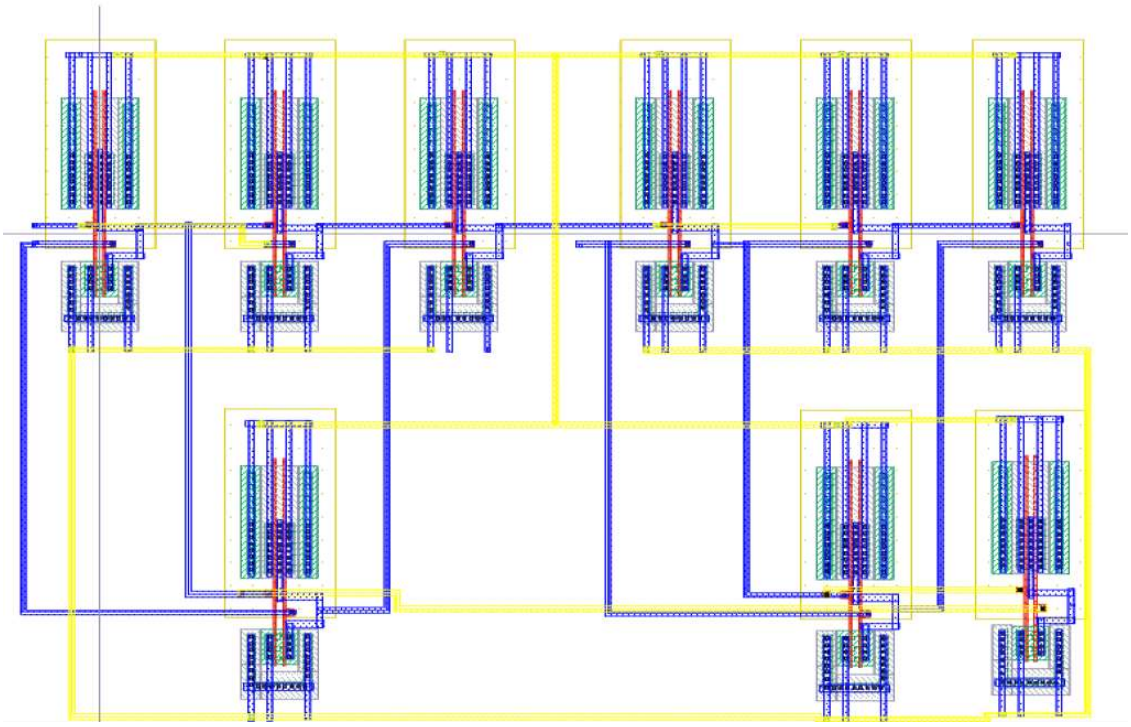

*Figure 7: Layout View of Full Adder*

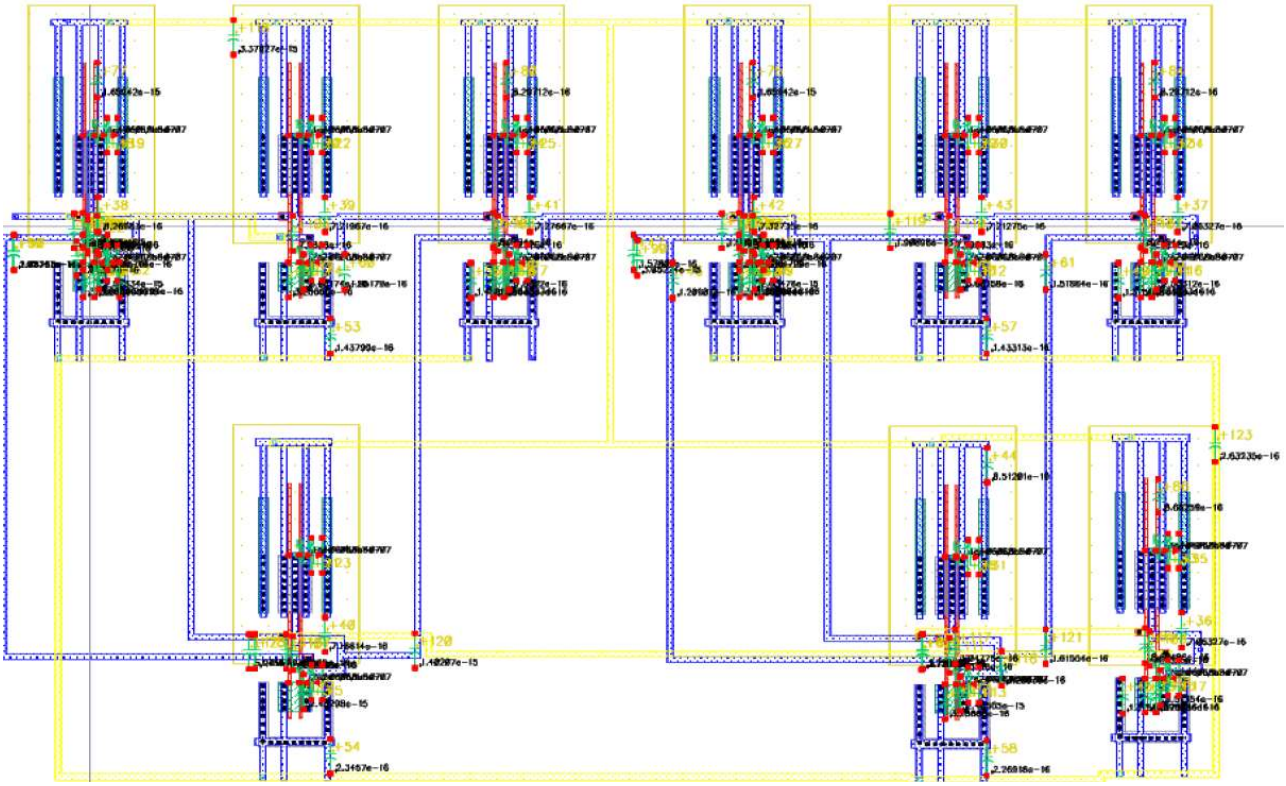

*Figure 8: Extracted View of Full Adder*

## 2.5 Post-layout simulation.

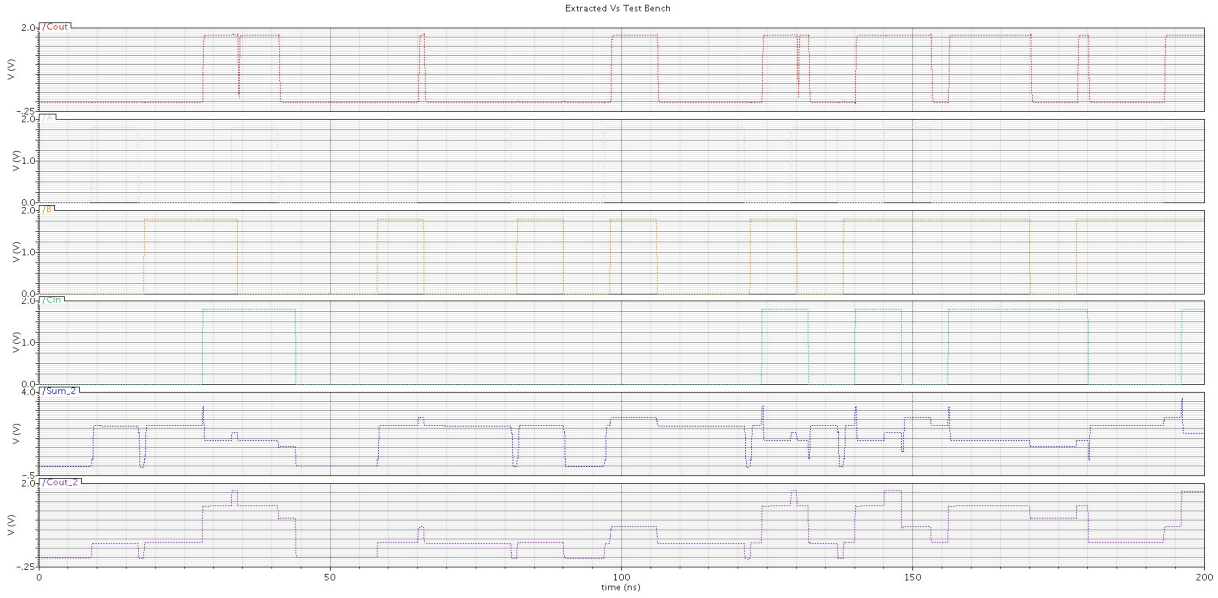


*Figure 9: Results comparison of the extracted and testbench view.*

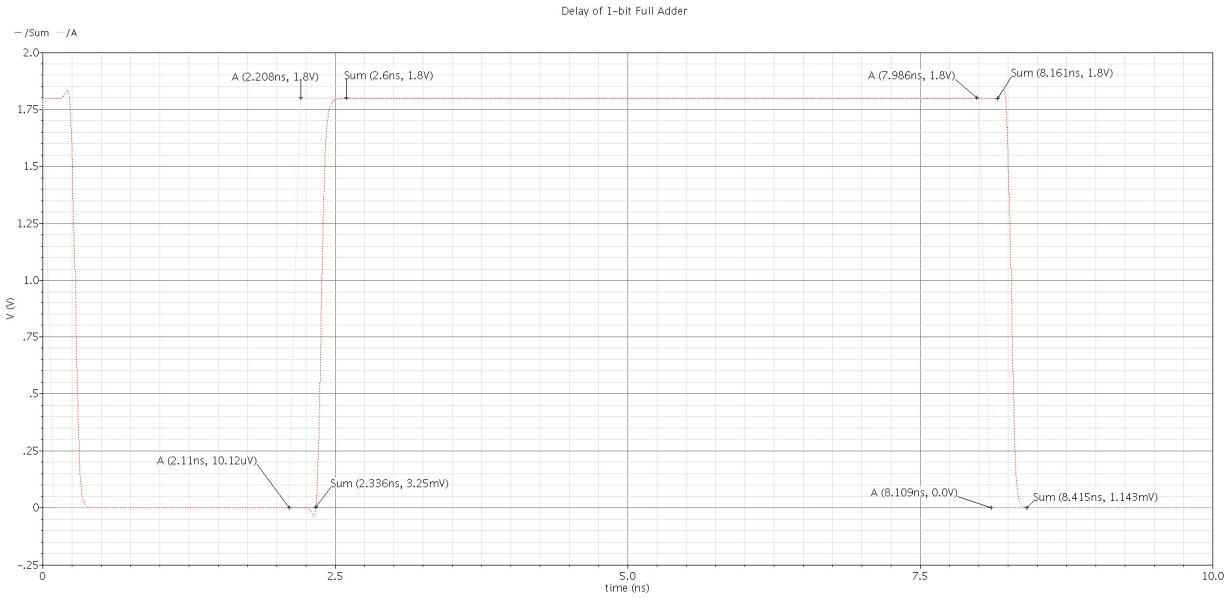


*Figure 10: Simulation for vpulse inputs to measure the worst-case delay.*

## 3 Conclusion

This lab explored functionality of the Full Adder and its role as the building block for circuits meant for arithmetic operations. The simulations were performed through Transient and Parametric analysis. It was observed that the results obtained in the net list window were not perfect and had some discrepancies from the ideal simulation. The deviations between extracted and testbench view was very low for the worst-case delay. The delay was simulated with inputs of the full adder as '$v_{pulse}$'. Moreover, in an instance when the worst case-delay for an 'n-bit ripple carry adder' arises, this can be then be attributed to the carry-in of the LSB propagates through to the MSB. The worst-case delay can be expressed as, $t_{delay}$ as a function of the delay from $t_{carry}$ (from $C_{in}$ to $C_{out}$) and $t_{sum}$ (from $C_{in}$ to $C_{sum}$). Thus, it can be assumed that this lab was successful in execution.

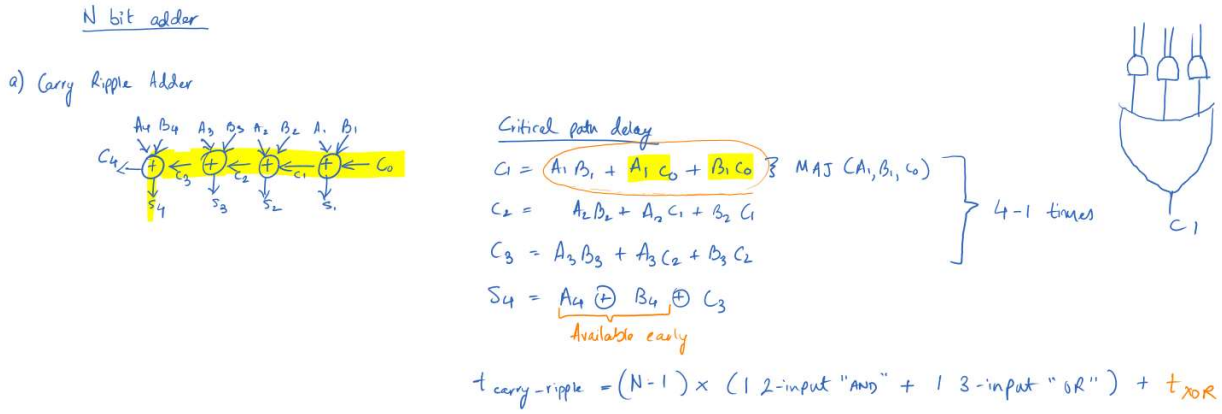


*Figure 11: $t_{delay}$ expressed as a function of the delay from $t_{carry}$ and $t_{sum}$ .*