Faculty of Engineering and Architectural Science

Department of Electrical and Computer Engineering

Course Number	ELE 734
Course Title	Low-Power Digital Integrated Circuits
Semester/Year	F2020
Lab No	04
Instructor Name	Dr. Andy Ye
Section No	06

Submission Date	12/07/2020
Due Date	12/07/2020

Name	Student ID	Signature*
Vatsal Shreekant	500771363	

Contents

1. Pre-Lab

1.1.

Figure 1: Truth table of a 1-bit full adder, and the Boolean logic derivation describing the S and C_{out} bits.

Figure 2: Full Adder gate level schematic.

1.2

$g_1 = 1 \; ; \; P_1 = 1 \; ; \; h_1 = a/1 \; ; \; b_1 = 2$

$g_2 = 4/3 \; ; \; P_2 = 2 \; ; \; h_2 = b/a \; ; \; b_2 = 3$

$g_3 = 4/3 \; ; \; P_3 = 2 \; ; \; h_3 = c/b \; ; \; b_3 = 1$

$g_4 = 4/3 \; ; \; P_4 = 2 \; ; \; h_4 = d/c \; ; \; b_4 = 2$

$g_5 = 4/3 \; ; \; P_5 = 2 \; ; \; h_5 = e/d \; ; \; b_5 = 3$

$g_6 = 4/3 \; ; \; P_6 = 2 \; ; \; h_6 = f/e \; ; \; b_6 = 1$

$g_7 = 4/3 \; ; \; P_7 = 2 \; ; \; h_7 = 113/f \; ; \; b_7 = 1$

$F = G \times B \times H$

$G = 1 \times 1 \times 4/3 \times 4/3 \times 4/3 \times 4/3 \times 4/3 \times 4/3 = 5.606$

$B = 2 \times 3 \times 1 \times 2 \times 3 \times 1 \times 1 = 36$

$H = 18.25 \, fF$

$F = 3691.42$

$(F)^{1/8} = 2.791$

$g_7 \, b_7 \, h_7 = 2.791 = \frac{4}{3} \times \frac{113}{f} \; ; \; 53.98 = f$

$g_6 \, b_6 \, h_6 = 2.791 = \frac{4}{3} \times \frac{f}{e} \; ; \; 25.78 = e$

$g_5 \, b_5 \, h_5 = 2.791 = \frac{4}{3} \times \frac{e}{d} \times 3 \; ; \; 36.96 = d$

$g_4 \, b_4 \, h_4 = 2.791 = \frac{4}{3} \times \frac{d}{c} \times 2 \; ; \; 35.31 = c$

$g_3 \, b_3 \, h_4 = 2.791 = \frac{4}{3} \times \frac{c}{b} \times 1 \; ; \; 16.87 = b$

$g_2 \, b_2 \, h_2 = 2.791 = \frac{4}{3} \times \frac{b}{a} \times 3 \; ; \; 24.17 = a$

NAND :-

width of 'a' $\approx 24/2 = 12$

width of 'b' $\approx 17/2 = 8.5$

width of 'c' $\approx 35/2 = 17.5$

width of 'd' $\approx 37/2 = 18.5$

width of 'e' $\approx 26/2 = 13$

width of 'f' $\approx 54/2 = 27$

$C_{load} = 50f + 63f = 113 \, fF$

$F = G \times B \times H$

$H = \dfrac{C_{out}}{C_{in}} \rightarrow$ Complete path

$= \dfrac{C_{out}}{2 \times C_{g,p} \times C_{g,n}}$

To get $C_{g,n}$, $C_{g,p}$:

ADE $\rightarrow$ DC Analysis $\rightarrow$ Results
DC operating points

C_{gg} = total gate capacitance of MOS

$C_{g,n} = 1.8 \, fF$

$C_{g,p} = 1.72 \, fF$

$H = \dfrac{C_{out}}{C_{in}} = \dfrac{113}{2 \times 1.72 \times 8} = 18.25$

Figure 3: Full Adder sizing to drive a load capacitance of 113fF at the its sum output.

2. Post-Lab
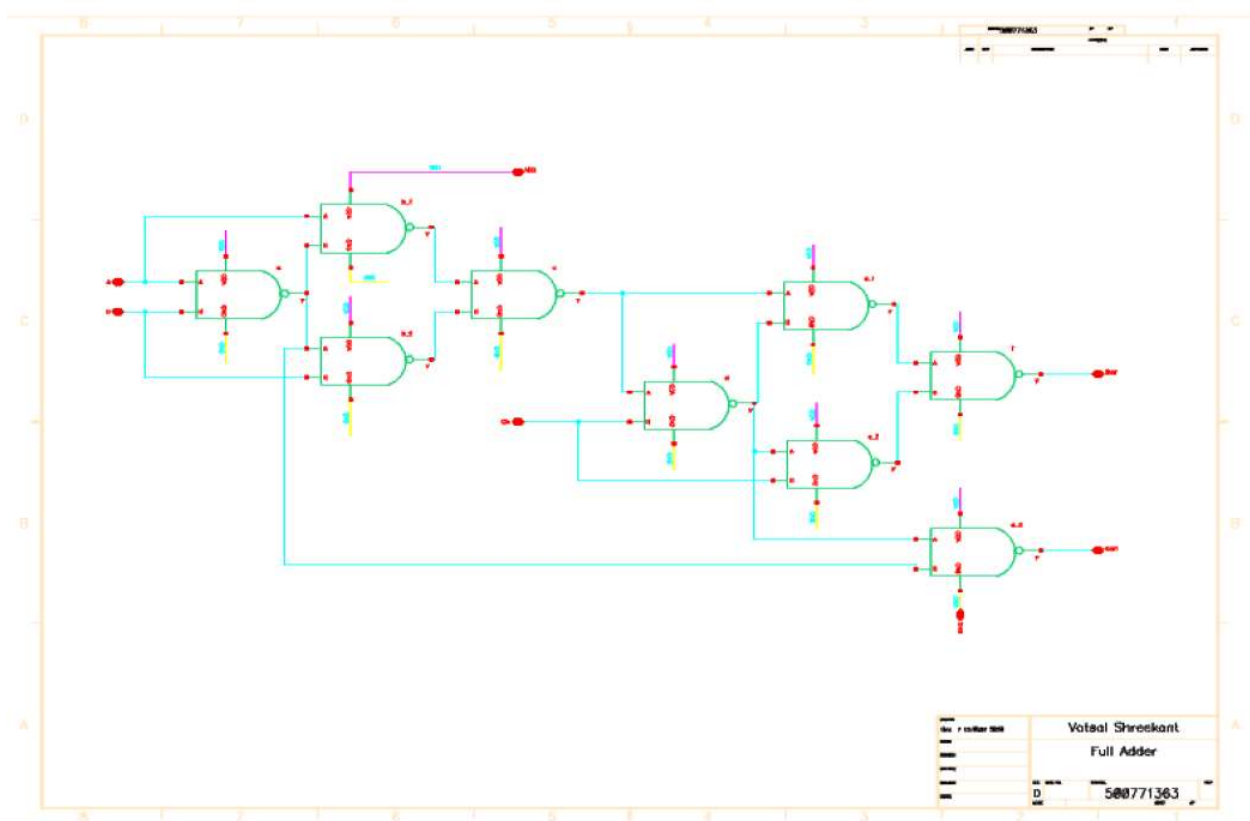
2.1 Schematic of Full Adder using NAND2 gates

Figure 4: Schematic of 1-bit Full Adder

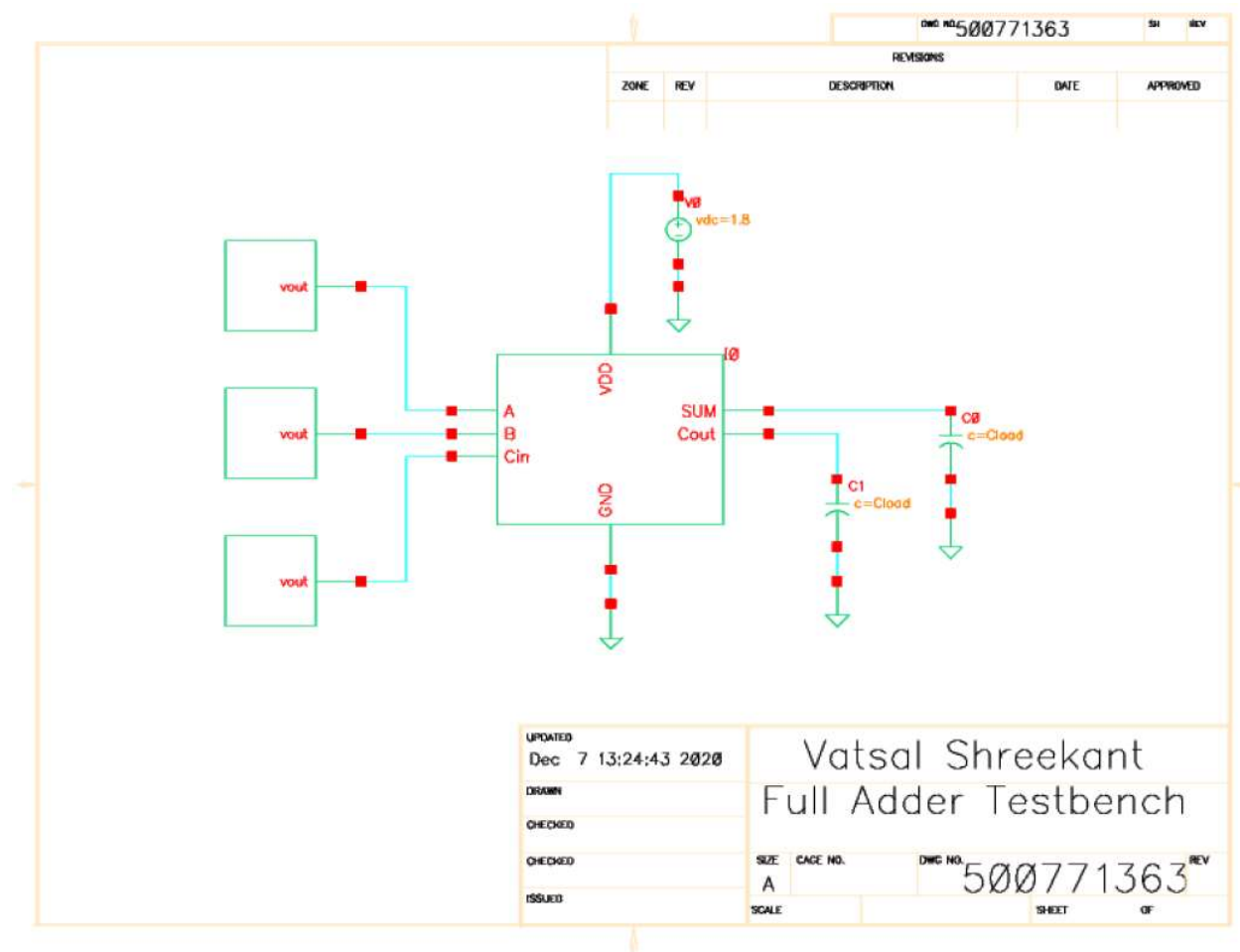## 2.2 Schematic of Testbench of Full Adder

Figure 5: Schematic of Full Adder Testbench

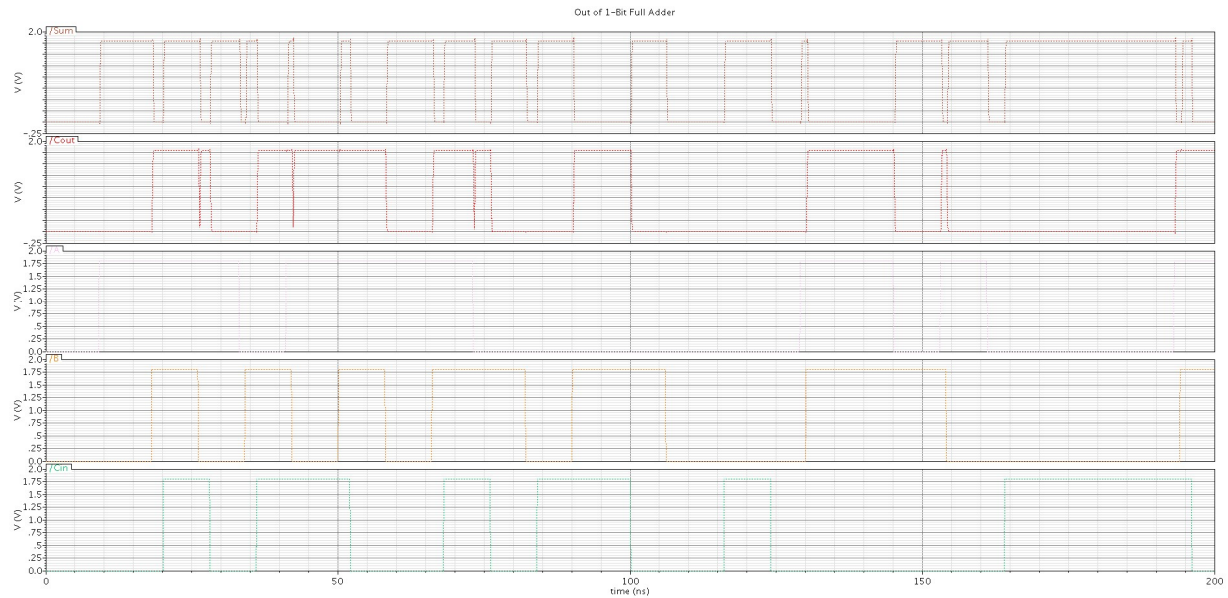## 2.3 Simulation of full adder for 20ns to verify the functionality.

Figure 6: Simulation of full adder for 20ns
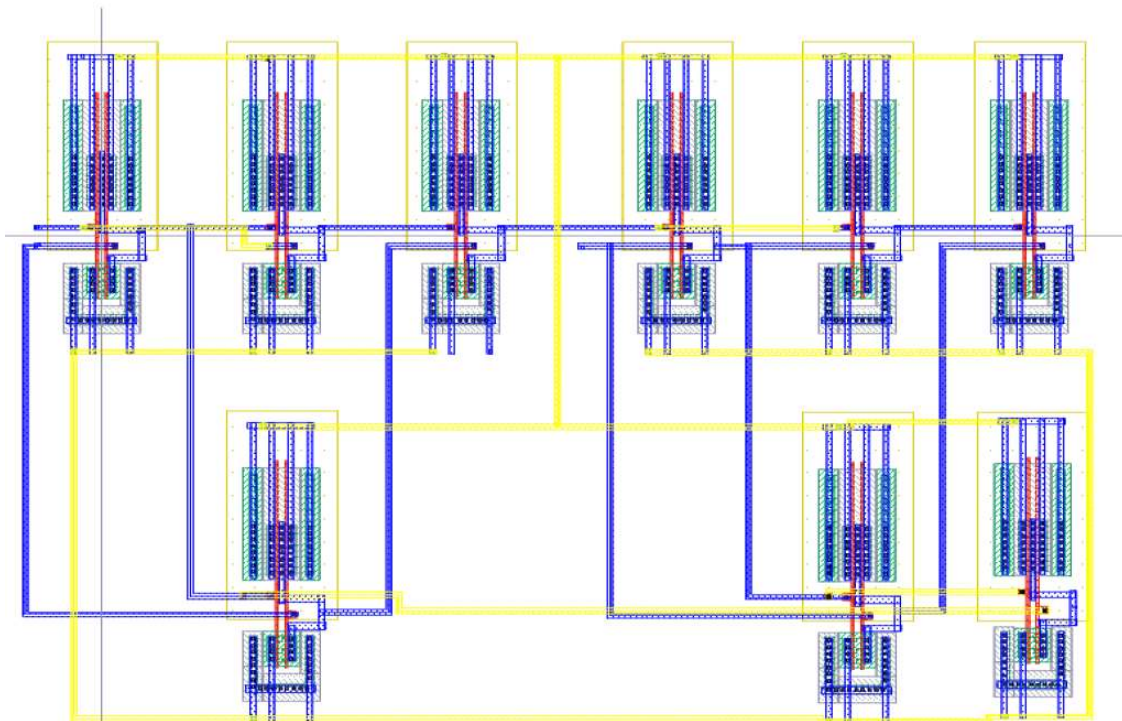
2.4 Layout and Extracted Views of the Full Adder

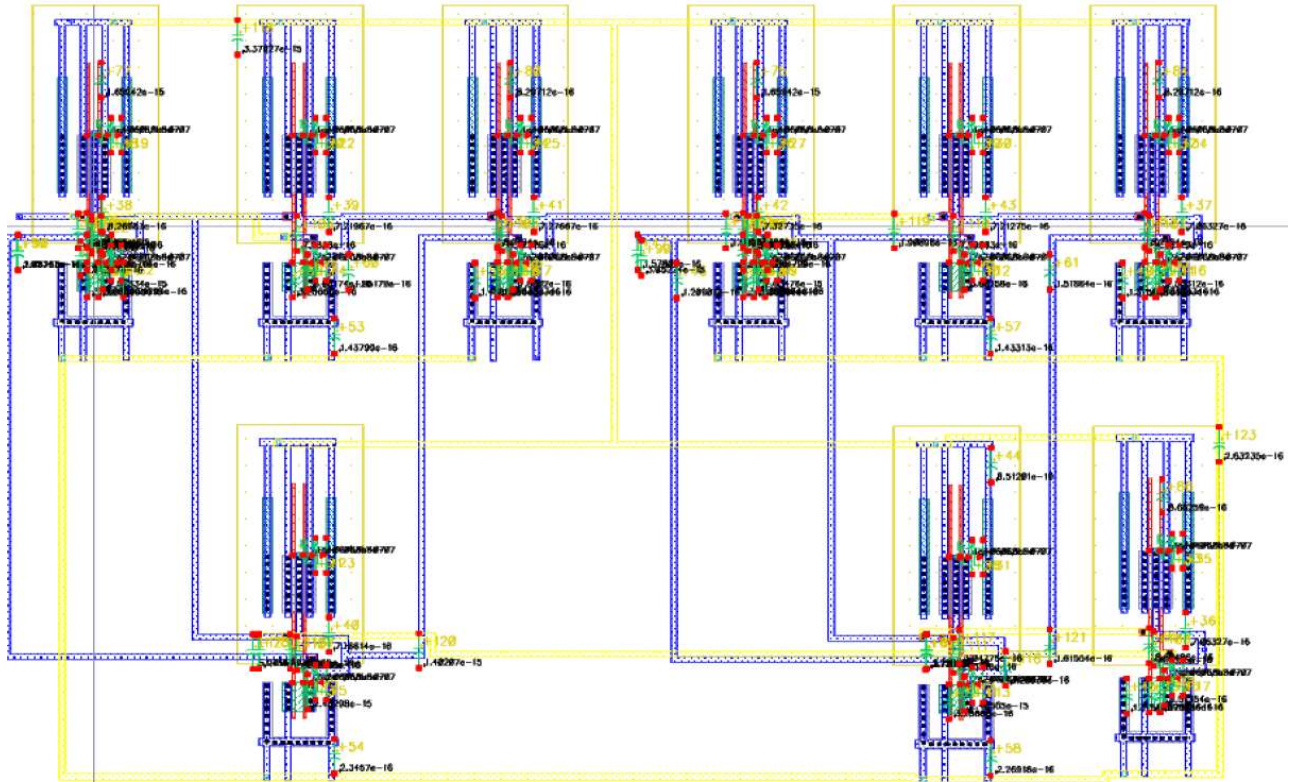*Figure 7: Layout View of Full Adder*

Figure 8: Extracted View of Full Adder

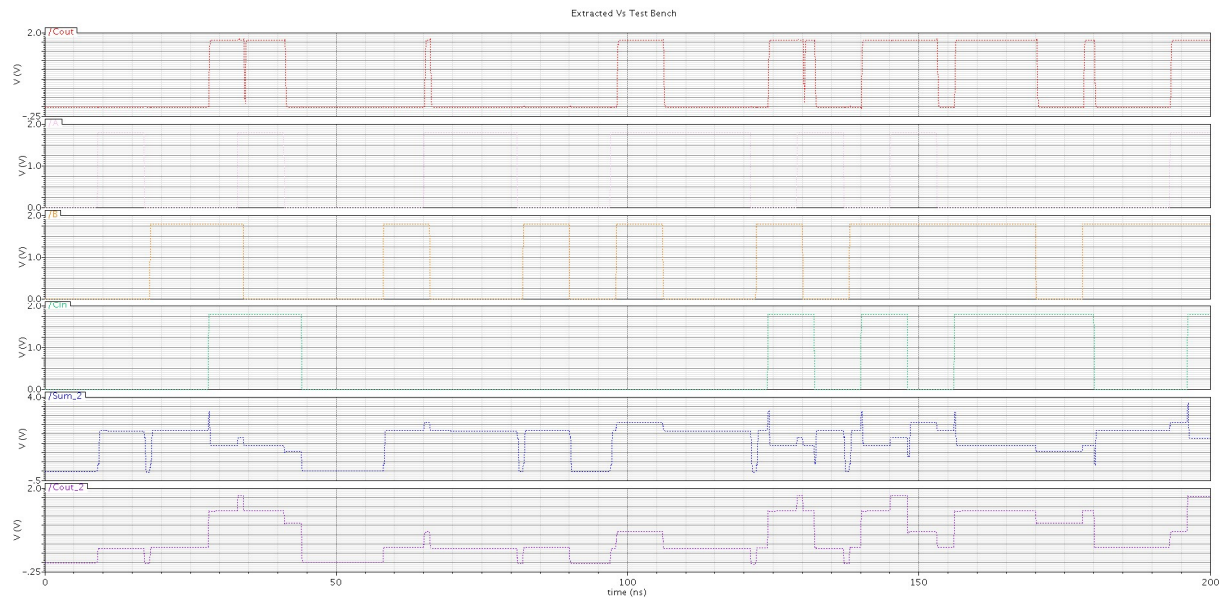## 2.5 Post-layout simulation.

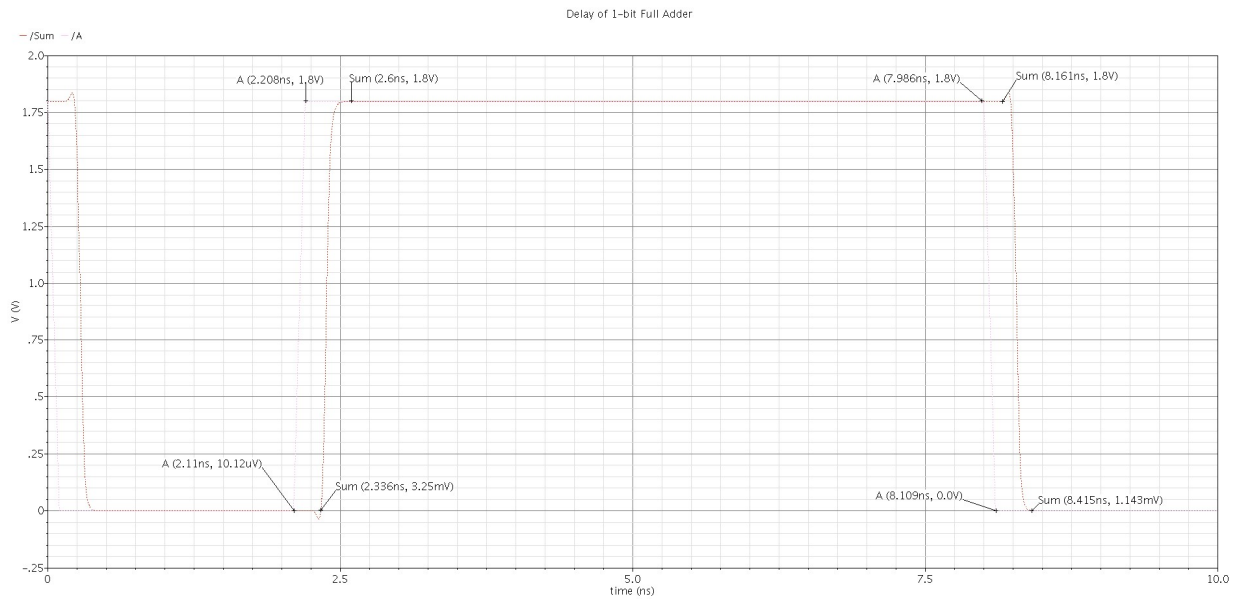*Figure 9: Results comparison of the extracted and testbench view.*

Figure 10: Simulation for vpulse inputs to measure the worst-case delay.

3 Conclusion

This lab explored functionality of the Full Adder and its role as the building block for circuits meant for arithmetic operations. The simulations were performed through Transient and Parametric analysis. It was observed that the results obtained in the net list window were not perfect and had some discrepancies from the ideal simulation. The deviations between extracted and testbench view was very low for the worst-case delay. The delay was simulated with inputs of the full adder as 'v$_{pulse}$'. Moreover, in an instance when the worst case-delay for an 'n-bit ripple carry adder' arises, this can be then be attributed to the carry-in of the LSB propagates through to the MSB. The worst-case delay can be expressed as, t$_{delay}$ as a function of the delay from t$_{carry}$ (from C$_{in}$ to C$_{out}$) and t$_{sum}$ (from C$_{in}$ to C$_{sum}$). Thus, it can be assumed that this lab was successful in execution.