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Faculty of Engineering and Architectural Science

Department of Electrical and Computer Engineering

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Instructor Name	Dr. Andy Ye
Section No	06

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Contents

1 Pre-Lab

1.2 Drain current equations for an ideal NMOS and PMOS Transistor & Ids-Vds Curves

NMOS Transistor:

$$I_{ds} = \begin{cases} 0\,, & V_{gs} < V_t (Cutoff) \\ \beta\left(V_{gt} - \frac{V_{ds}}{2}\right) * V_{ds}, \quad V_{ds} < V_{gs} - V_t, & V_{gs} > V_t (Linear) \\ \frac{\beta}{2} * {V_{gt}}^2, \quad V_{ds} \geq V_{gs} - V_t, & V_{gs} > V_t (Saturation) \end{cases}$$

Equation 1: Drain Current for ideal NMOS Transistor

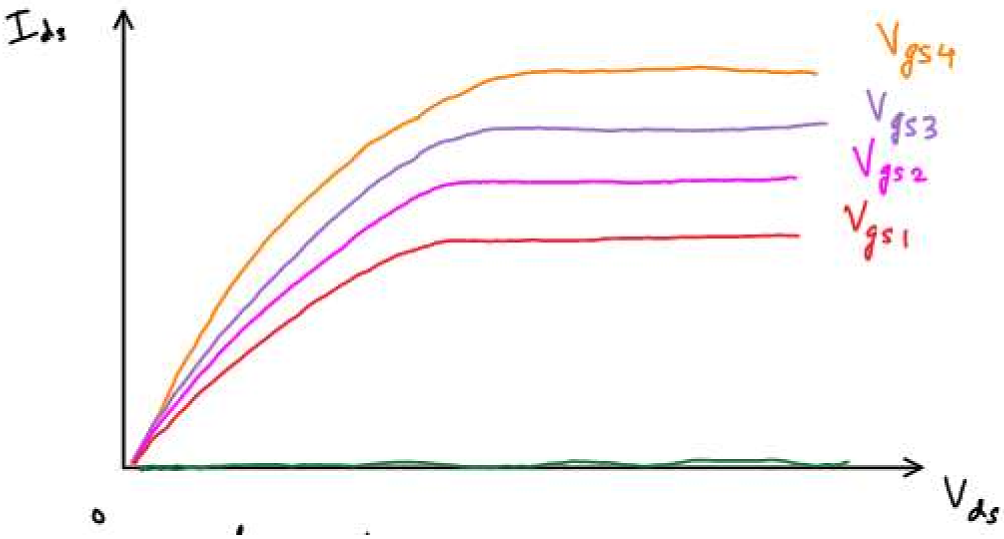

Figure 1: I-V Characteristics of Waveforms for ideal NMOS Transistor

PMOS Transistor:

$$Isd = \begin{cases} 0\,, & V_{sg} \leq |V_{tp}|\ (Cutoff) \\ \beta_p\left(V_{sg} - |V_{tp}| - \frac{V_{sd}}{2}\right) * V_{sd}, & V_{sd} < V_{sg} - |V_{tp}|\ (Triode\ Region) \\ \frac{\beta_p}{2}\left(V_{sg} - |V_{tp}|\right)^2, & V_{sd} > V_{sg} - |V_{tp}| \quad (Saturation) \end{cases}$$

Equation 2: Drain Current for ideal PMOS Transistor

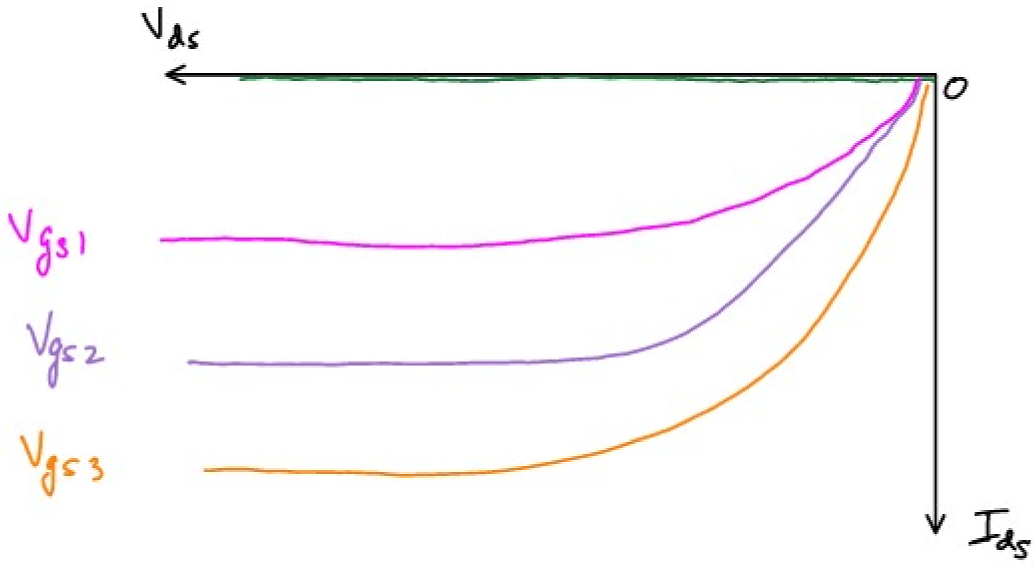

Figure 2: I-V Characteristics of Waveforms for ideal PMOS Transistor

1.3 Equation for the Threshold Voltage of a MOS Transistor

$$V_t = V_{to} + \gamma(\sqrt{\varphi_s + V_{sb}} - \sqrt{\varphi_s})$$

Equation 3: Threshold Voltage for a MOS Transistor

When a voltage V_{sb} is applied, the threshold voltage increases. It is evident from the equation that when V_{sb} decreases, V_t decreases as well.

1.4 Channel Length Modulation (CLM)

Assuming that the surface voltage is approximately the body voltage, that is, $V_{db} = V_{ds}$; the effective channel length $L_{eff} = L-L_{dt}$(depletion region).

L_d increases as V_{db} increases.

A shorter channel length equals to a higher current.

Hence, Ids increases with V_{ds} in saturation.

The drain current is modified to account for CLM as follows:

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 * (1 + \frac{V_{ds}}{V_A})$$

Equation 4: Drain Current Equation Modified to Account for CLM

1.5 Subthreshold Current

In an ideal transistor, the current doesn't get cut-off when V_{gs}<V_t. It rather drops exponentially. The subthreshold leakage current increases significantly with Vds due to drain induced barrier lowering.

There is a lower limit on Ids set by drain junction leakage.

$$I_{ds} = I_{ds0} * e^{\frac{V_{gs}-V_{to}+nV_{ds}-K_\gamma V_{sb}}{nV_t}}(1 - e^{-\frac{V_{ds}}{V_t}})$$

Equation 5: Drain Current when the Transistor Operates in the Subthreshold Region

1.6 Symbol for NMOS Transistor and it's Intrinsic Capacitances

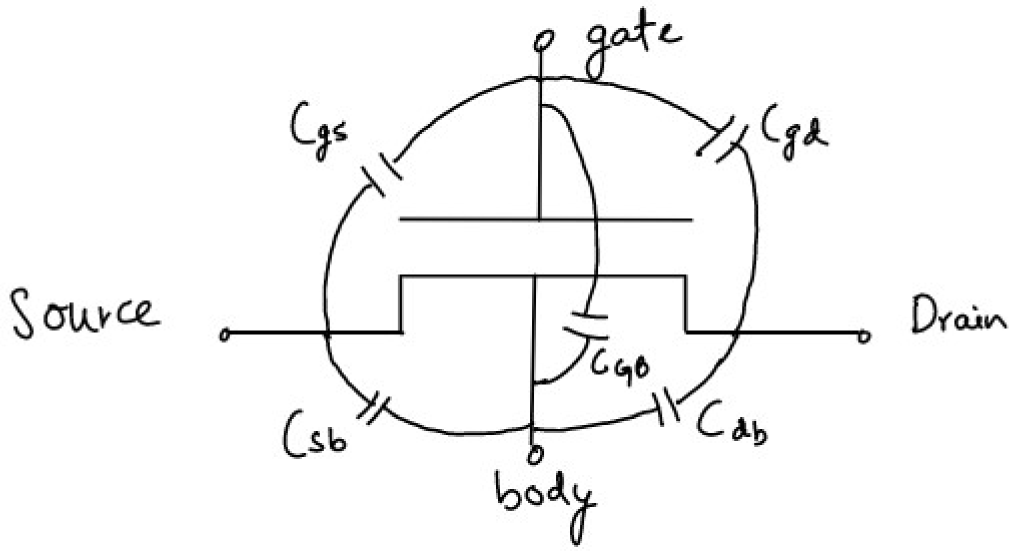

Figure 3: Symbol for NMOS with Intrinsic Capacitances

2 Post-Lab

2.1 Schematic for NMOS and PMOS Transistors

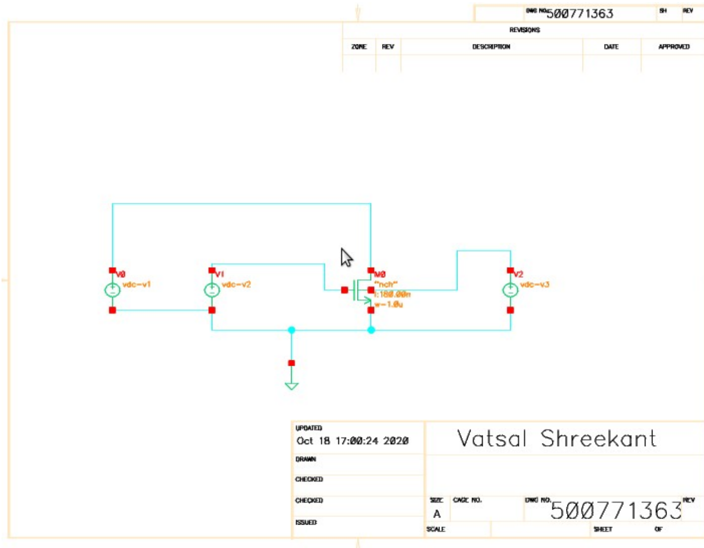

Figure 4: Schematic for NMOS Transistor

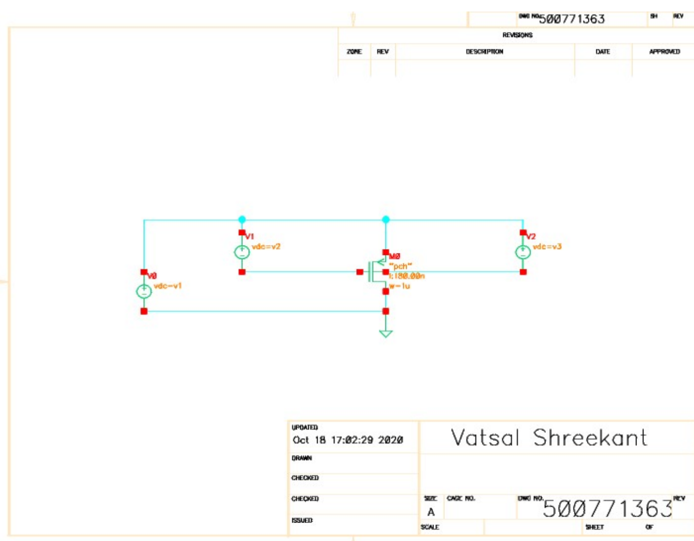

Figure 5: Schematic for PMOS Transistor

2.2 Family of I-V Characteristic Waveforms for NMOS and PMOS Transistors

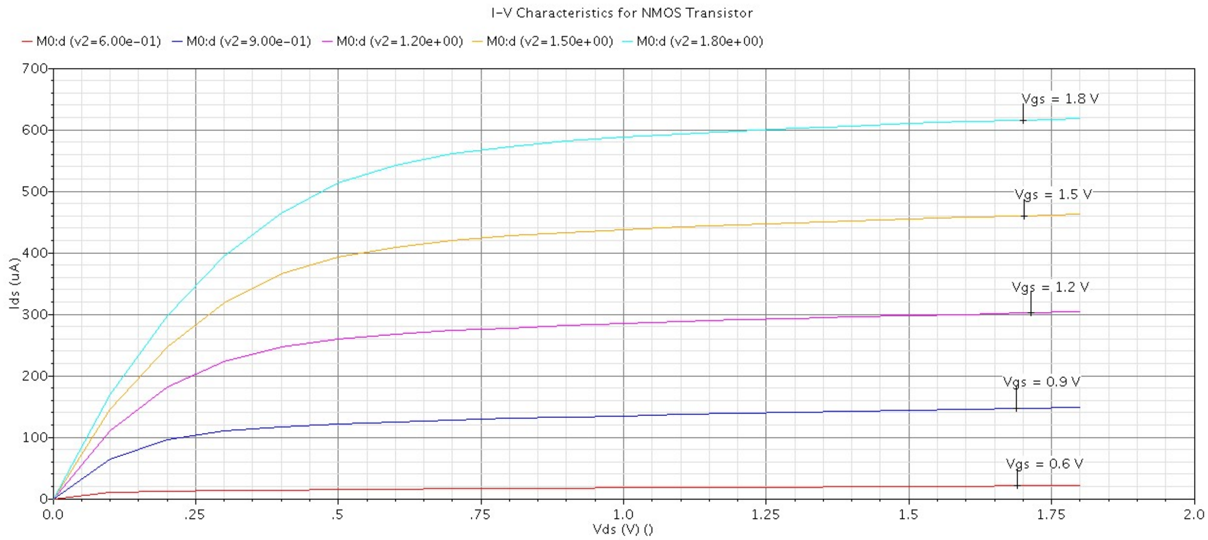

Figure 6: I-V Characteristics of Waveforms for NMOS Transistor

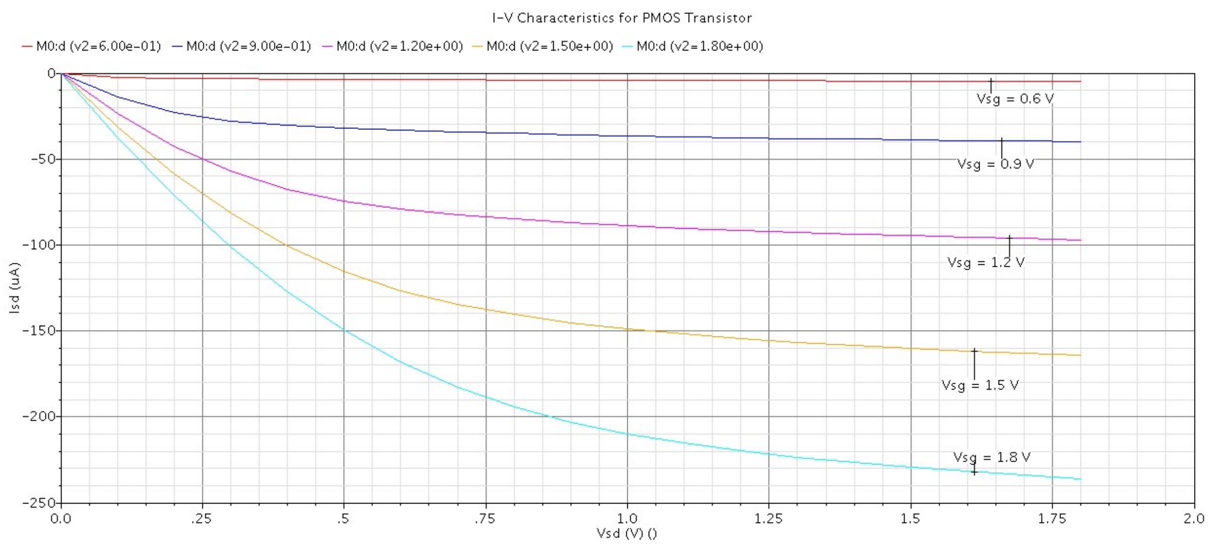

Figure 7: I-V Characteristics of Waveforms for PMOS Transistor

2.3 Subthreshold Conduction for NMOS and PMOS Transistors

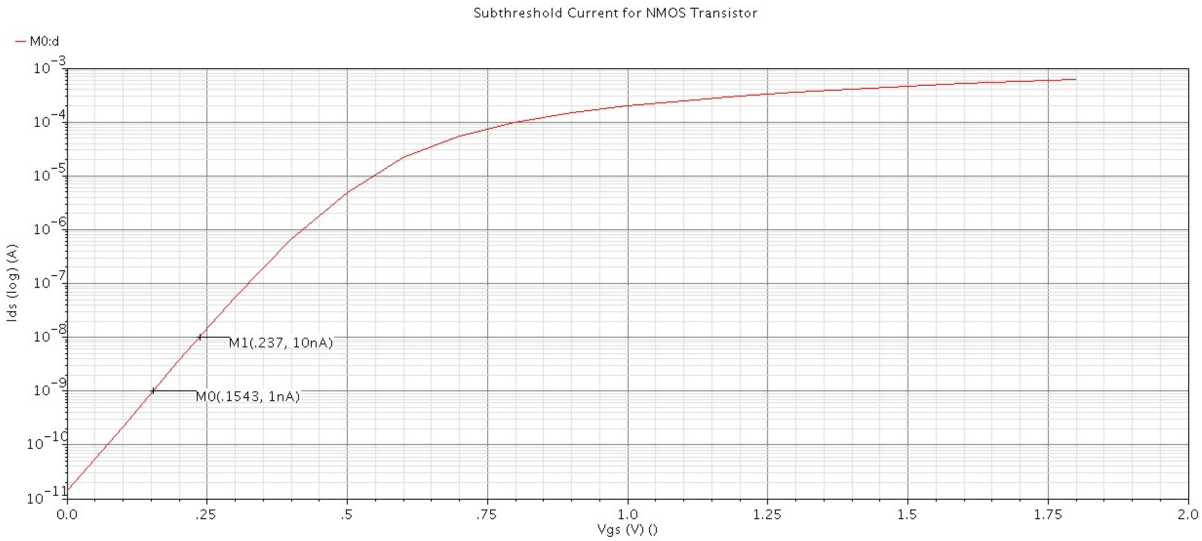

Figure 8: Subthreshold Current for NMOS Transistor

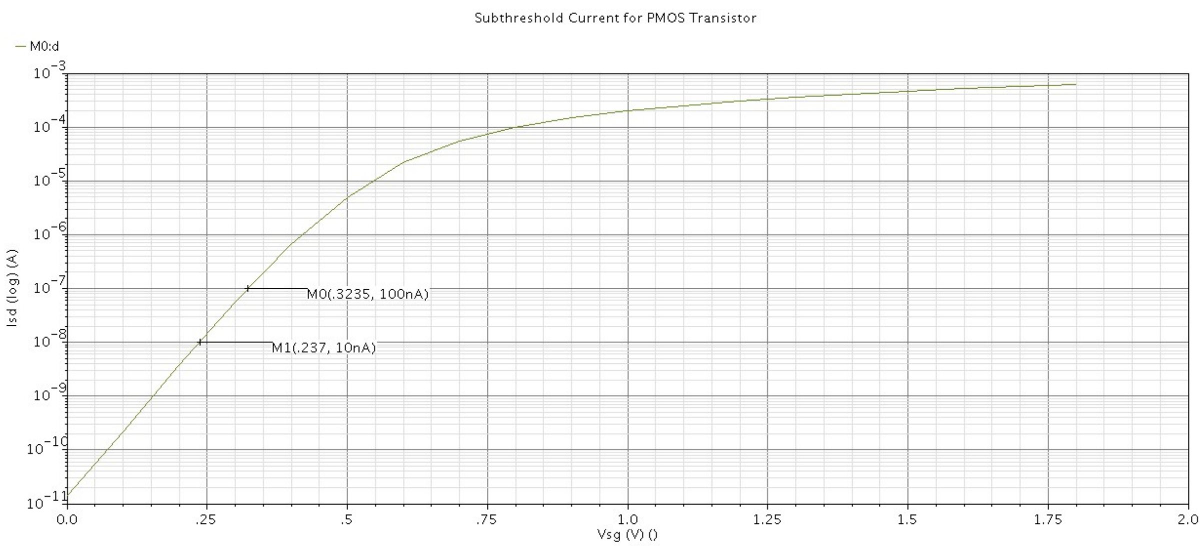

Figure 9: Subthreshold Current for PMOS Transistor

2.4 Body Effect Analysis for NMOS and PMOS Transistors

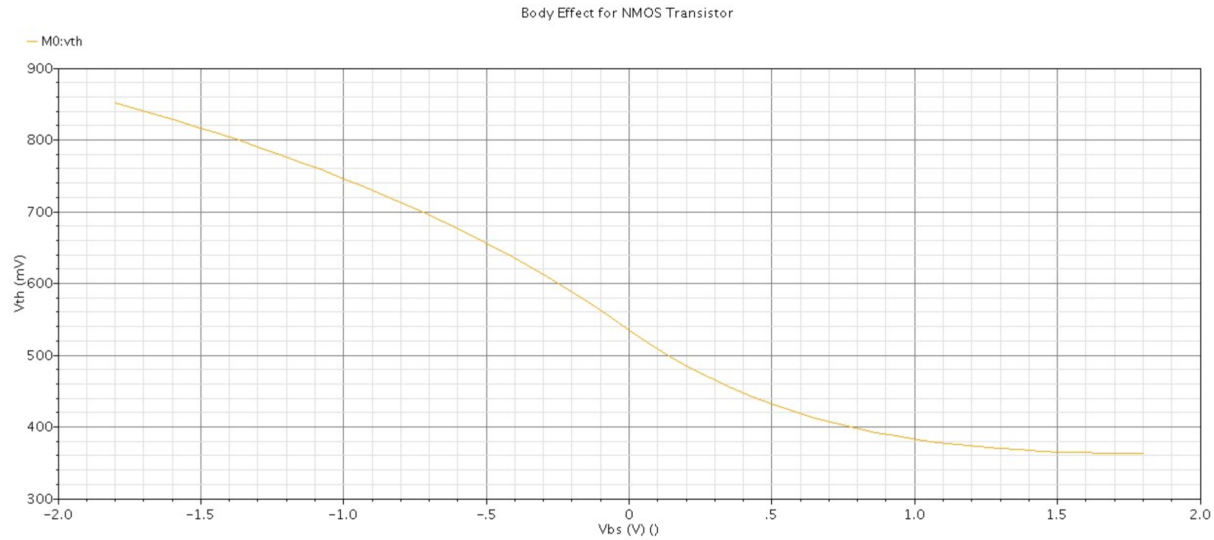

Figure 10: Body Effect Analysis for NMOS Transistor

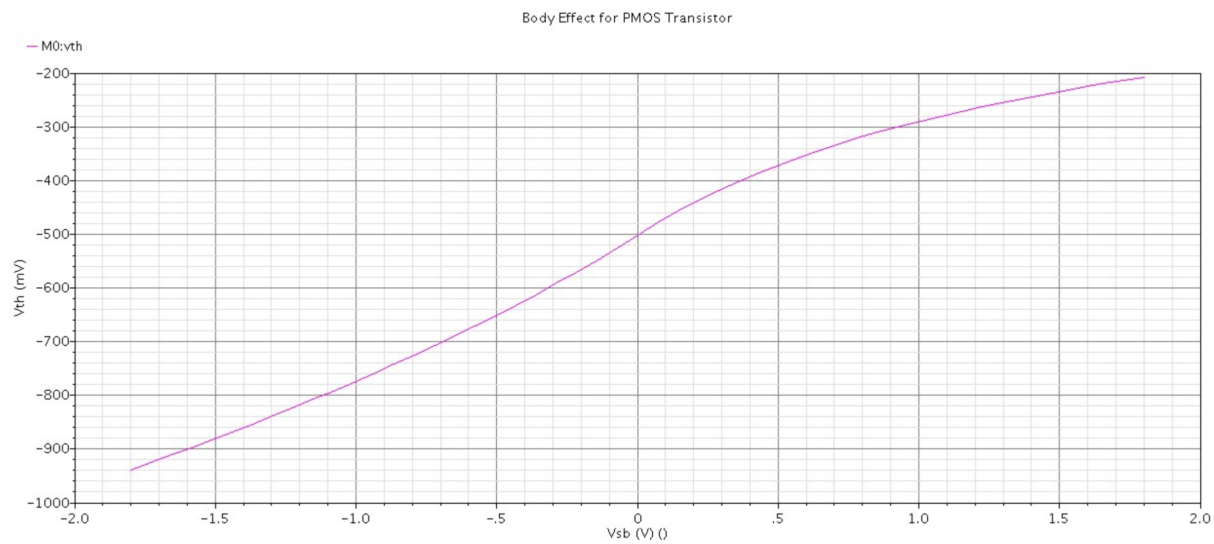

Figure 11: Body Effect Analysis for PMOS Transistor

2.5 Layout and Extracted View of NMOS Transistor

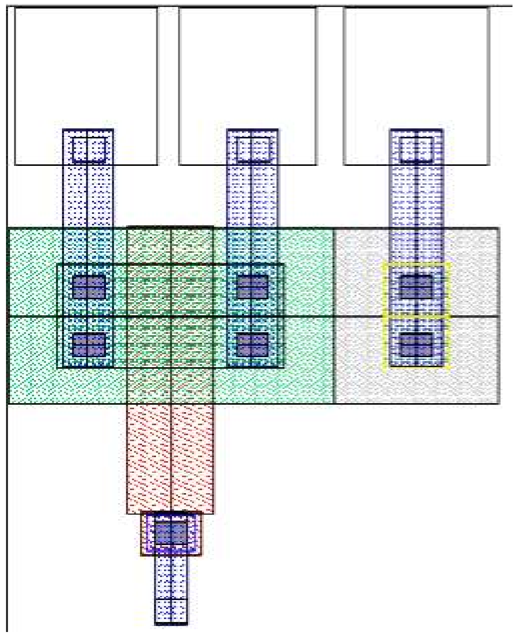

Figure 12: Layout View of NMOS Transistor

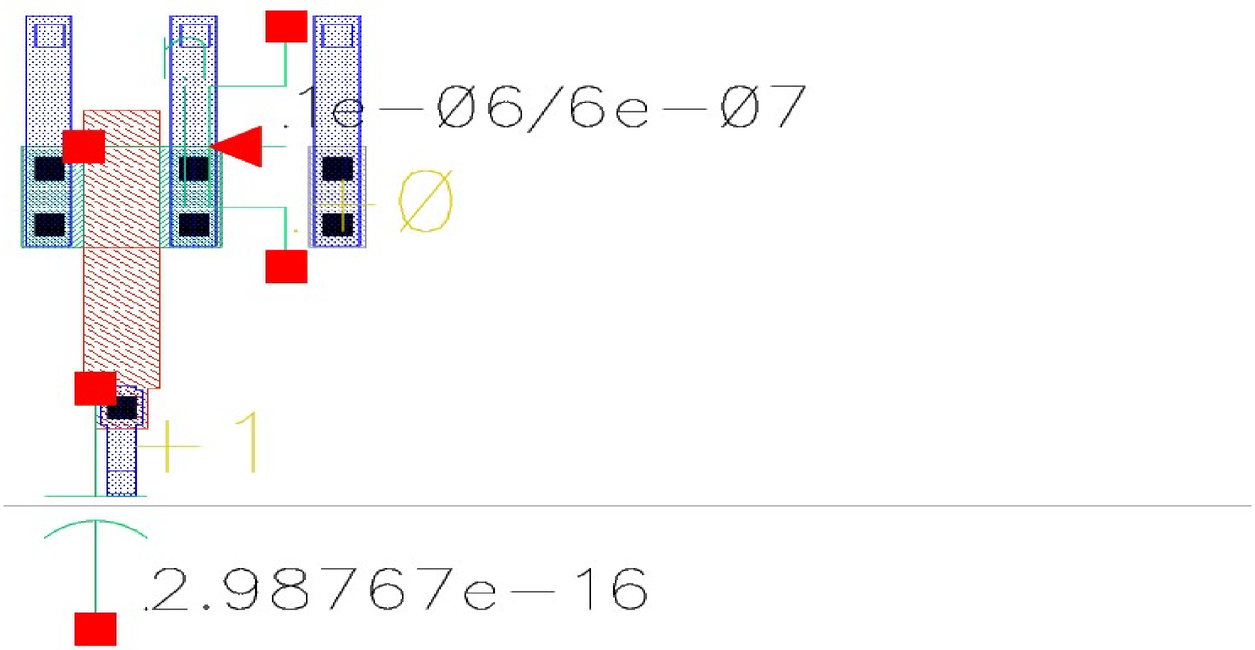

Figure 13: Extracted View of NMOS Transistor

2.6 Family of I-V Characteristics of Waveforms for the Schematic and Extracted NMOS Transistor

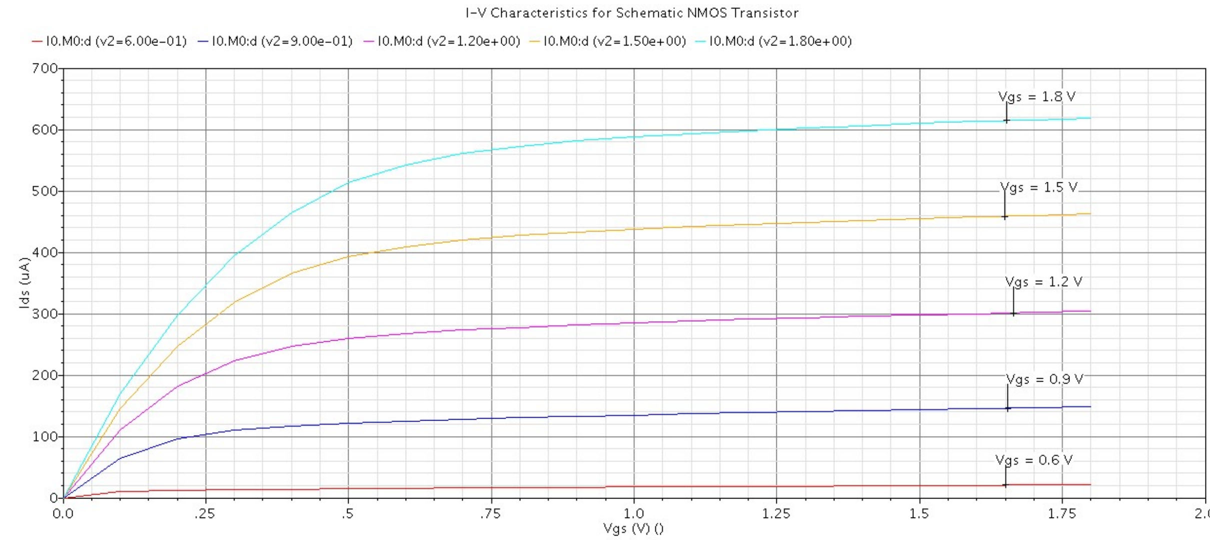

Figure 14: I-V Characteristics for Schematic NMOS Transistor

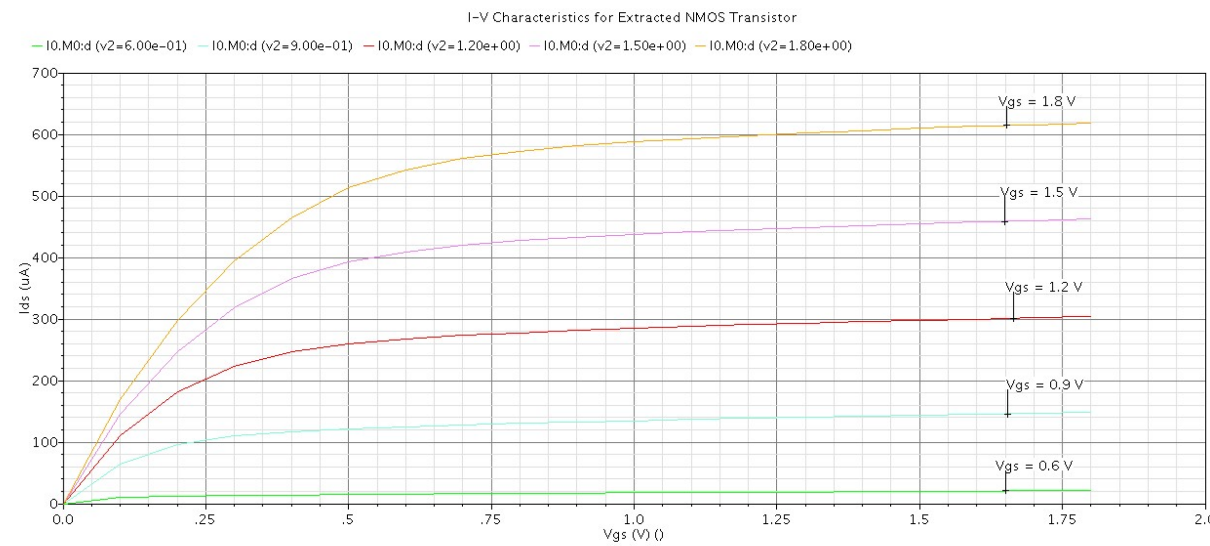

Figure 15: I-V Characteristics for Extracted NMOS Transistor

3 Conclusion

The results recorded during the execution of the Lab for both the PMOS and NMOS transistors were very much identical to the results recorded in the prelab. After running the simulation in the Cadence software, technical difficulties did arise when the 'dc-dc' file and its sub-files were not displayed in the 'Results Browser'. This was rectified by clearing the cache in the Results Browser by hovering over to 'File->Clear' and then running the simulation. Since the results in the prelab and post-lab were free of any discrepancies, it is safe to assume that the lab was executed successfully.