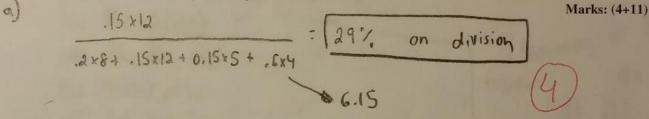
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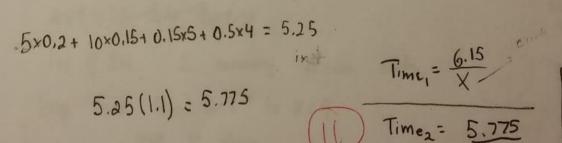
- i) The midterm exam consists of four questions and it has four pages. Answer all questions.
- ii) An instruction set sheet for the MIPS processor is allowed for your reference.
- iii) Estimated time for each question is equivalent to the marks assigned to it.
- Your answer should be concise, to the point and in the space provided.
- Q-1. Consider an application program with the following types of instructions and their frequency. A specific CPU executes the above program.

Instruction Type	Instruction Frequence	cy CPI
Multiply	20% F	8
Divide	15%	0 12
Load Store	15%	. 5
Rest of the Instructions	50%	4

- (a) What percentage of time does the CPU spend doing division operations?
- (b) The hardware engineering team is suggesting an option of modifying the CPU hardware to reduce the number of cycles required for multiplication and division. The modified CPU reduces the number of cycles required for multiplication to 5 and division to 10 but it will require a 10% increase in the overall clock cycle time.

Nothing else affected, does this modification will reduce the overall execution time? Justify your answer by showing all the calculations, etc.





b) Time will reduce

by a fador of 1.064

Times = 1.

COE608

Q-2. Consider the following for loop code sequence in a C-like language:

for 
$$(k = 1; k < 10; k++)$$
 {

 $pix[k+1] = pix[k] + i;$ 
 $i = i + 2;$ 
 $pix[k+1] = pix[k] + i;$ 

Assume that i and k are integers stored in registers \$s3 and \$s6, base address of the pix array (i.e. pix[0]) is in register \$s5 and the, pix array is also of integer type.

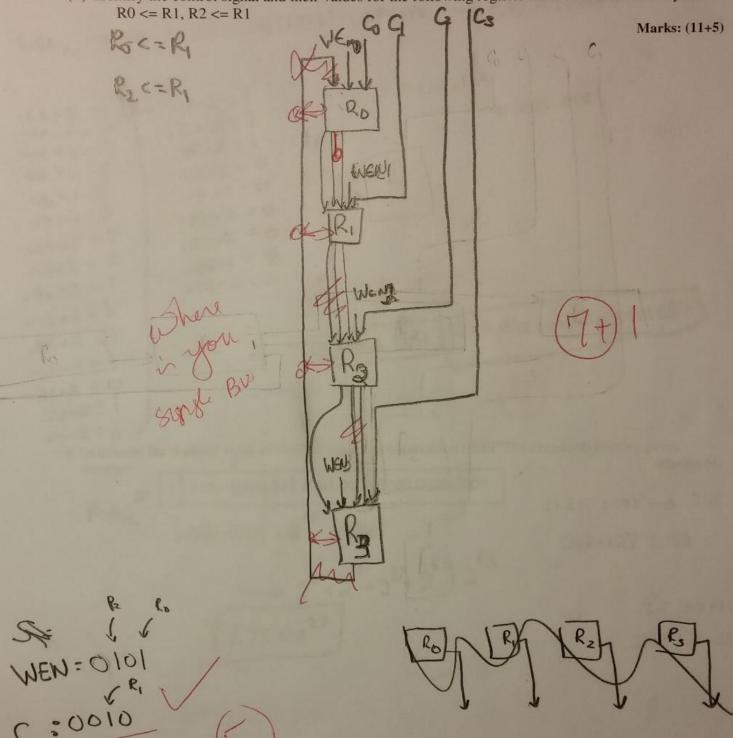
(a) Write MIPS CPU assembly code for the above for loop with minimum number of instructions. 11 K = 0+1; Since Value & K is Marks: (12) olddi \$30, \$70001 1/40 = 1, H K<10 31ti Sto, 356, 10 10000 11 if \$ to = 0 , lexit beg Sto, Bzero, exit add \$to,\$st,\$sb sll 4xk sll \$10, \$56,2 add \$to, \$to, \$to add \$60, \$to, \$55 (Assuming all tempony In \$t2,0(\$t0) add Sta, Sta, 833 += " ... registari SW 4(1to) (1t2) addi \$53,\$53,2 otherwise addi \$56, \$56, ! addi \$56, \$zero, i loop How many memory accesses take place while executing the assembly code of part (a)? nesseccary befor Justify your answer. 4x40 44 bytes

IN & SW 1 memory

runs from K=1 to K=9 loops 9 times

2×9=18 memory acc

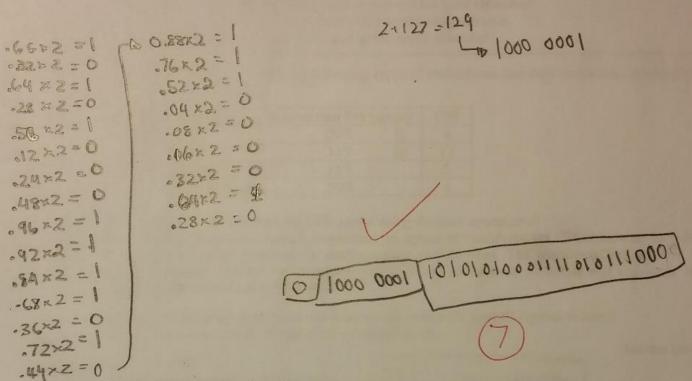
- Q-3. Design a tri-state buffer based single-bus datapath containing four 1-bit registers (R0, R1, R2 and R3) that facilitates all the register transfers in one or more clock cycles.
  - (a) Draw the datapath circuit and show all the control signals at the control points of your datapath.
  - (b) Identify the control signal and their values for the following register transfers in one clock cycle.



Q-4. (a) Determine a single precision, IEEE 754 floating-point standard representation of  $20/3 = (6.66666)_{10}$ 

$$G_{10} \rightarrow 110$$

$$G_{1$$



(b) Determine the decimal value of the following single precision (IEEE 754 Standard) floating point number.

Marks: (4)

$$217-127 = 90$$
  
 $E = exp+127 2$   
 $217-127 = exp$ 

1101 1001 -> 217