Faculty of Engineering and Architectural Science

Department of Electrical and Computer Engineering

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Section No	06

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1. Pre-Lab

1.1. Transfer Function of a CMOS Inverter

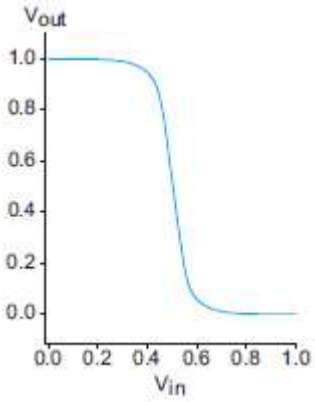

Figure 1: CMOS Inverter DC Characteristic [1]

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$

Table 1: Summary of CMOS Inverter Operation [1]

The inverter is Figure 1 is an un-skewed inverter with beta ration r=1. The input threshold voltage for the inverter in Figure 1 is $V_{DD}/2$.

The formula for skewed inverters with varying beta ratios is $r = \frac{\beta_p}{\beta_n}$.

A HI-skew inverter (r>1) has a stronger pMOS transistor. Therefore, if the input is $V_{DD}/2$, we would expect the output will be greater than $V_{DD}/2$. Thus, the input threshold for a HI-skew inverter must be higher than that of an unskewed inverter.

A LO-skew inverter (r<1) has a weaker pMOS transistor and thus a lower switching threshold.

A HI-skew inverter shifts the DC Characteristic graph to the right for an un-skewed inverter. Similarly, a LO-skew inverter shifts the DC Characteristic to the left for an un-skewed inverter.

1.2 Expression Derivation for an Ideal Static CMOS Inverter V_M

$$I_{dn} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2$$

$$I_{dp} = \frac{\beta_p}{2}(V_{inv} - V_{DD} - V_{tp})^2$$

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$

$$I_{dn} = W_n C_{ox} \vartheta_{sat-n}(V_{inv} - V_{tn})$$

$$I_{dp} = W_p C_{ox} \vartheta_{sat-p}(V_{inv} - V_{DD} - V_{tp})$$

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}}$$

Equation 1: Threshold Voltage for a MOS Transistor

where V_{inv} is the input threshold.

1.3 Noise Margin

Noise margin is a parameter that allows us to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted. The noise margin decreases as the supply voltage decreases.

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{IH} - V_{OH}$$

Equation 2: Expression for Low Noise Margin (NM_L) and High Noise Margin (NM_H)

1.4 Expression Derivation for Propagation Delay

$$\tau_{pdr} = ln2 * R_{eqp} * C_L$$

$$\tau_{pdf} = ln2 * R_{eqn} * C_L$$

$$R_{eq} = \frac{V_{DD}}{2 * ln2 * I_{Dsat\ n,p}}$$

$$\tau_p = \frac{\tau_{pdr} + \tau_{pdf}}{2}$$

$$R_{eqn} = \frac{V_{DD}}{2 * ln2 * I_{Dsat\,n}} = \frac{V_{DD}}{2 * ln2 * \frac{\beta_n}{2}\left(V_{gs} - V_{th,n}\right)^2} = \frac{V_{DD}}{ln2 * \mu_n * C_{ox,n} * \frac{W_n}{L}\left(V_{gs} - V_{th,n}\right)^2}$$

$$R_{eqp} = \frac{V_{DD}}{2 * ln2 * I_{Dsat\,p}} = \frac{V_{DD}}{2 * ln2 * \frac{\beta_p}{2}\left(V_{sg} - |V_{th,p}|\right)^2} = \frac{V_{DD}}{ln2 * \mu_p * C_{ox,p} * \frac{W_p}{L}\left(V_{sg} - |V_{th,p}|\right)^2}$$

$$\tau_{pdf} = ln2 * R_{eqn} * C_L = ln2 * \frac{V_{DD}}{ln2 * \mu_n * C_{ox,n} * \frac{W_n}{L}\left(V_{gs} - V_{th,n}\right)^2} * C_L$$

$$\tau_{pdf} = \frac{V_{DD} * C_L}{\mu_n * C_{ox,n} * \frac{W_n}{L}\left(V_{gs} - V_{th,n}\right)^2}$$

$$\tau_{pdr} = ln2 * R_{eqp} * C_L = ln2 * \frac{V_{DD}}{ln2 * \mu_p * C_{ox,p} * \frac{W_p}{L}\left(V_{sg} - |V_{th,p}|\right)^2} * C_L$$

$$\tau_{pdr} \frac{V_{DD} * C_L}{\mu_p * C_{ox,p} * \frac{W_p}{L}\left(V_{sg} - |V_{th,p}|\right)^2}$$

$$\tau_p = \frac{\tau_{pdr} + \tau_{pdf}}{2} = \frac{V_{DD} * C_L}{2}\left(\frac{1}{\mu_n * C_{ox,n} * \frac{W_n}{L}\left(V_{gs} - V_{th,n}\right)^2} + \frac{1}{\mu_p * C_{ox,p} * \frac{W_p}{L}\left(V_{sg} - |V_{th,p}|\right)^2}\right)$$

Equation 3: Expression for the Propagation Delay (τ_p)

1.5 CMOS Inverter Design

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{(3.9)\left(8.854 \times 10^{-12}\frac{F}{m}\right)}{4.09 \times 10^{-9} m} = 8.463 \times 10^{-3} F$$

$$V_{th} = 0.445\,V$$

$$r = \frac{\beta_p}{\beta_n} = \frac{\mu_p}{\mu_n} * \frac{W_p}{W_n}$$

$$t_p = \frac{1}{2}(t_{pHL} + t_{pLH})$$

$$t_{pHL} = t_{pLH} = 100\,ps$$

$$t_{pHL} = \frac{C_L * V_{DD}}{\frac{W_n}{L_n}\mu_n * C_{ox}(V_{DD} - V_{tn})^2}$$

$$C_L = 50fF, l_{min} = 180nm, \therefore V_{DD} = 1.8\,V$$

$$t_{pHL} = \frac{50 \times 10^{-15} * 1.8 * 180 \times 10^{-9}}{W_n * 459 \times 10^{-4} * 8.463 \times 10^{-3} * 1.355^2}$$

$$W_n = \frac{16200 \times 10^{-24}}{7132 \times 10^{-7} * 100 \times 10^{-12}} = 0.0227 \times 10^{-5} = 227.14\, nm$$

$$t_{pLH} = \frac{C_L * V_{DD}}{\frac{W_p}{L_p}\mu_p * C_{ox}\left(V_{DD} + V_{tp}\right)^2}$$

$$t_{pLH} = \frac{50 \times 10^{-15} * 1.8 * 180 \times 10^{-9}}{W_p * 109 \times 10^{-4} * 8.463 \times 10^{-3} * 1.362^2}$$

$$W_p = \frac{162 \times 10^{-5}}{1710.6} = 947.03\, nm$$

The following is the schematic for the CMOS inverter:

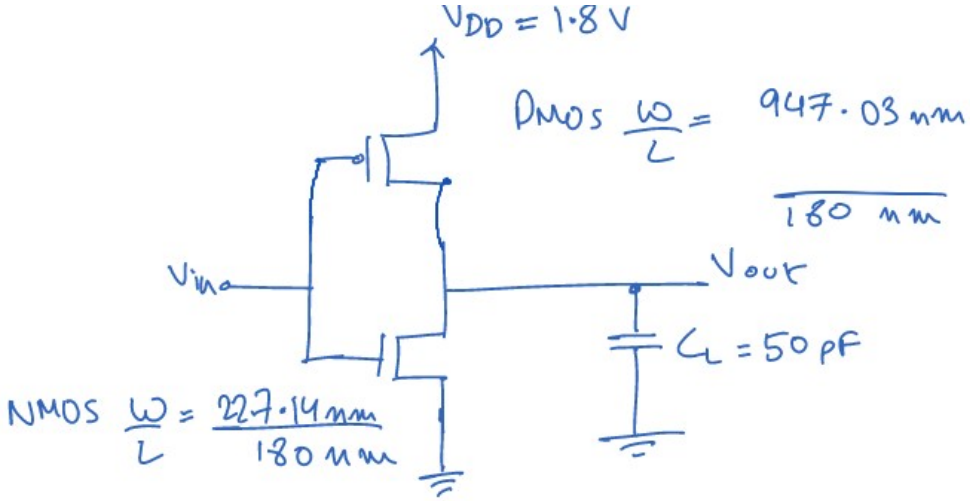

Figure 2: Schematic of CMOS Inverter

2. Post-Lab

2.1 Schematic of CMOS Inverter

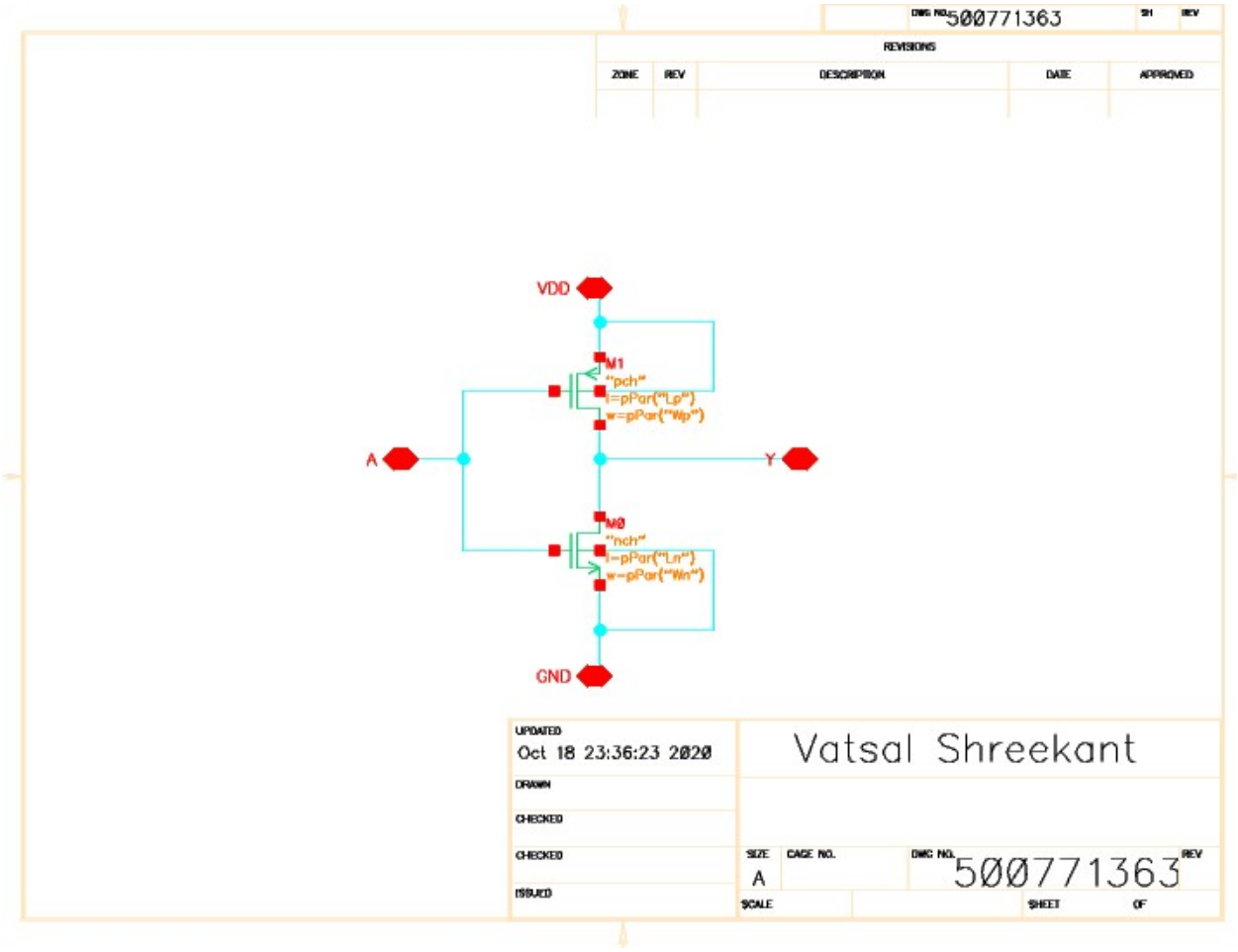

Figure 3: Schematic of CMOS Inverter

2.2 Schematic of Testbench

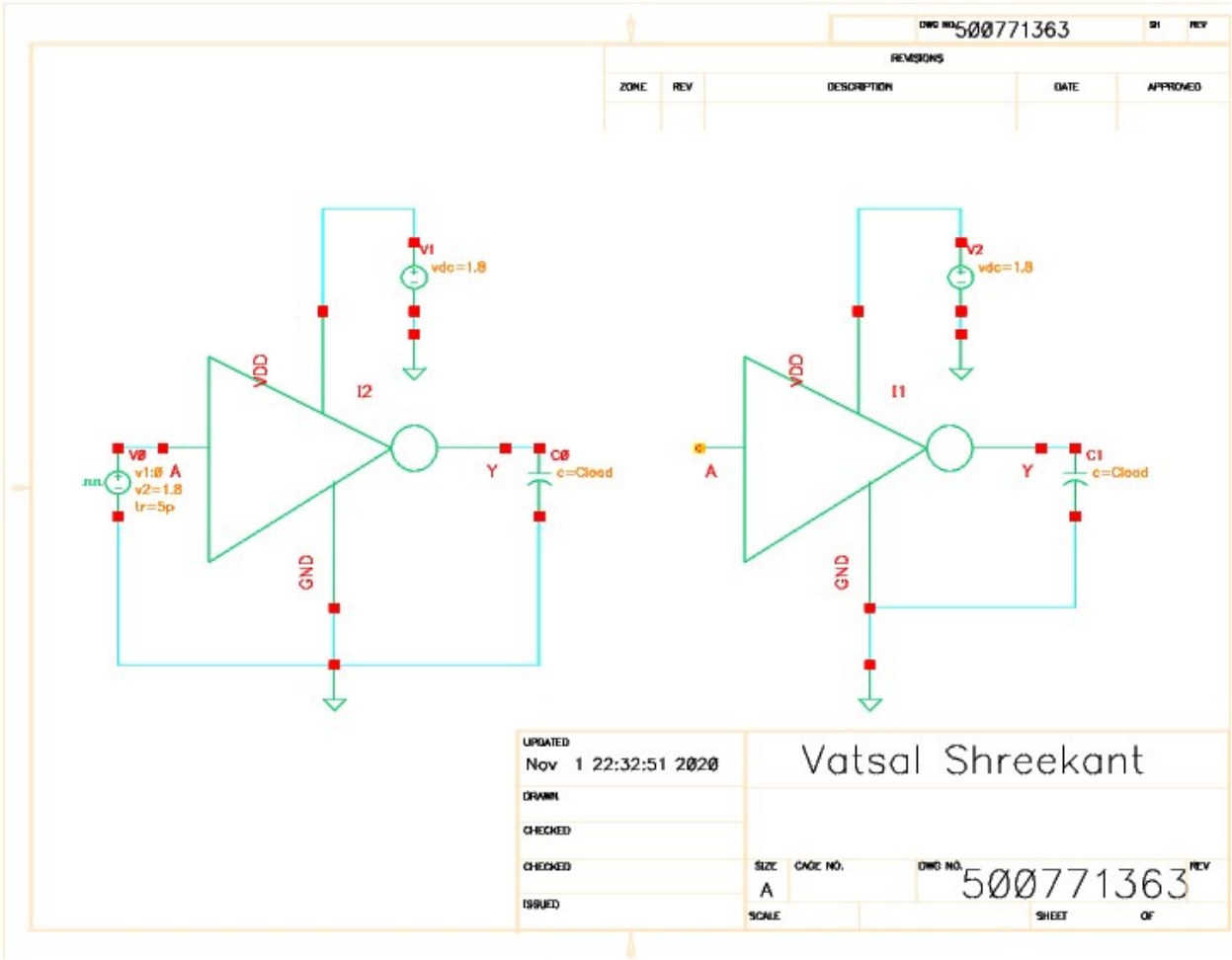

Figure 4: Schematic of Testbench

2.3 Results of Static and Dynamic CMOS Inverter Simulations

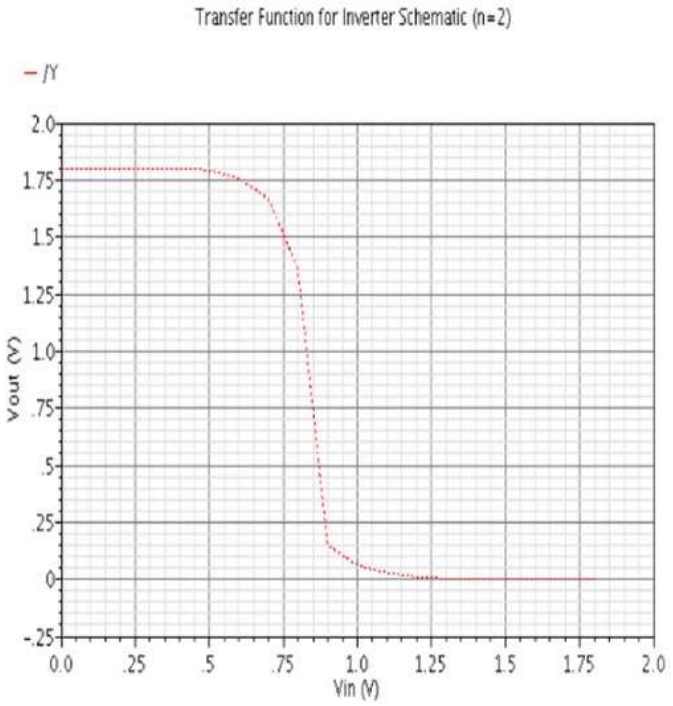

Figure 5: CMOS Inverter DC Characteristic (n=2) (Schematic)

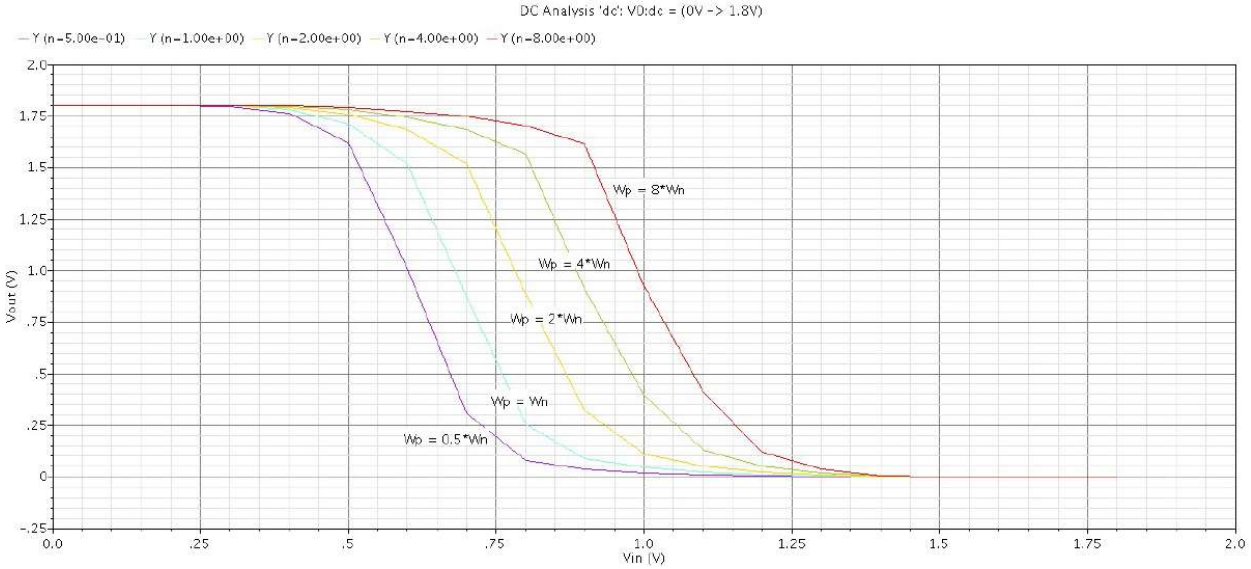

Figure 6: CMOS Inverter DC Characteristic (n=sweep) (Schematic)

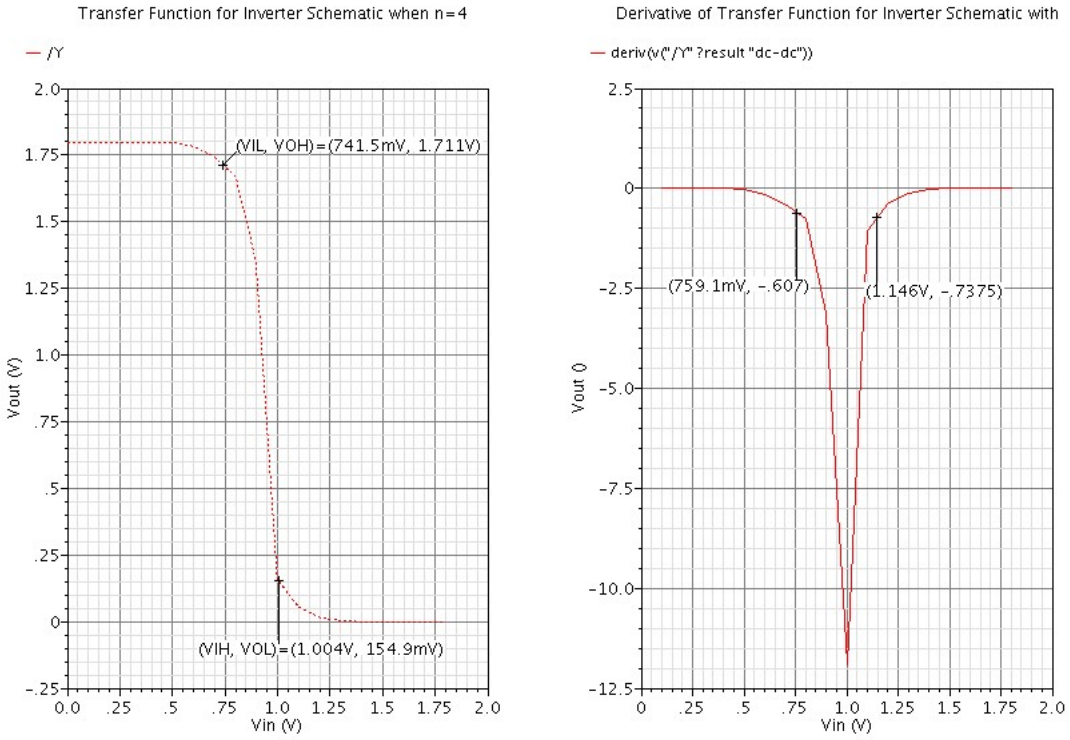

Figure 7: Derivative of CMOS Inverter DC Characteristic to determine V_{IL} and V_{OH} (Schematic)

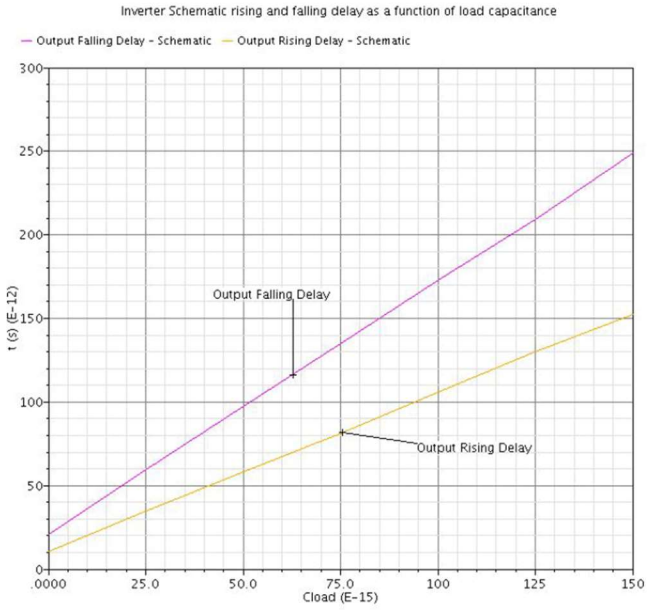

Figure 8: CMOS Inverter Rising and Falling Delay as Function of Load Capacitance (Schematic)

Output Delay Measurements	
Rising Delay (s)	59.25p
Falling Delay (s)	97.49p

Table 2: Output Y Delay Measurement (Schematic)

2.4 Layout and Extracted Views of CMOS Inverter

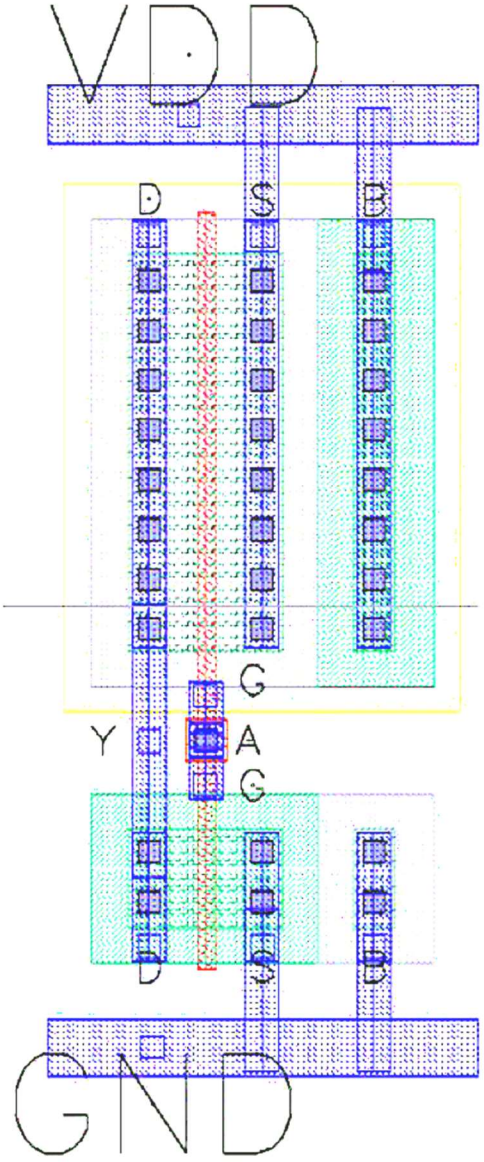

Figure 9: Layout View of CMOS Inverter

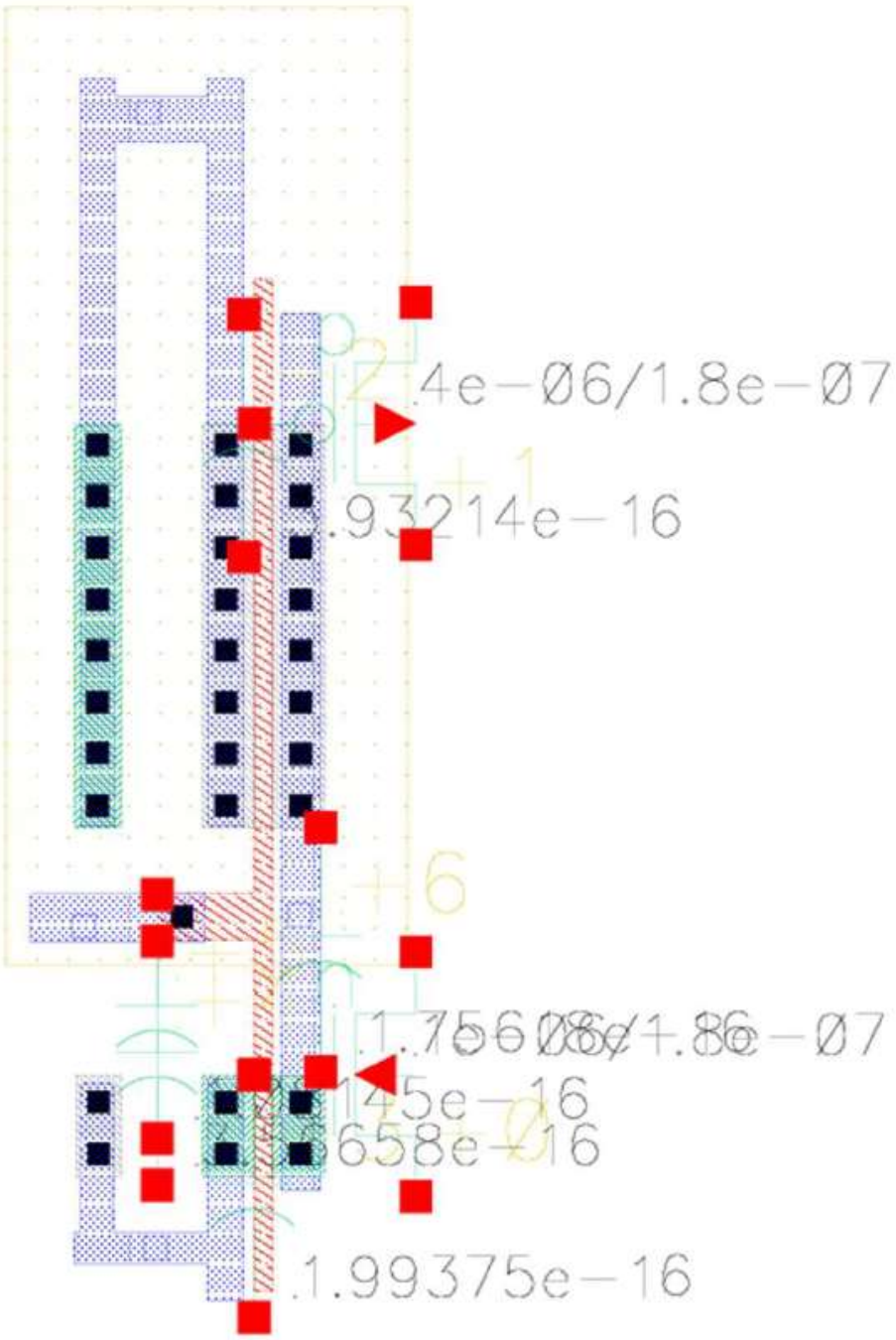

Figure 10: Extracted View of CMOS Inverter

2.5 Post Layout Simulation Results

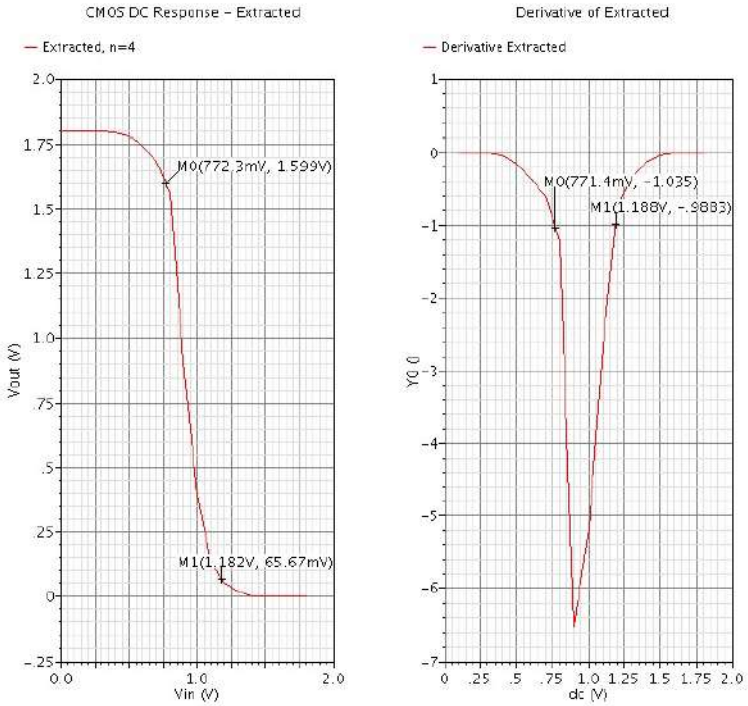

Figure 11: Derivative of CMOS Inverter DC Characteristic to Determine V_{IL} and V_{OH} (Extracted)

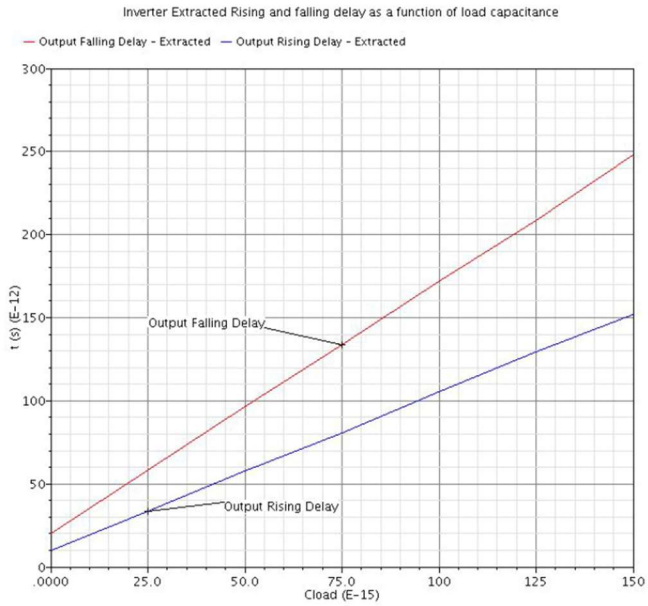

Figure 12: CMOS Inverter Rising and Falling Delay as Function of Load Capacitance (Extracted)

Output Delay Measurements	
Rising Delay (s)	58.16p
Falling Delay (s)	97.20p

Table 3: Output Y Delay Measurement (Extracted)

3 Conclusion

This lab explored different types of characteristics and the layout of a CMOS inverter. The static and dynamic simulations were performed through Transient, DC, and Parametric analysis. From these analyses, a family of curves were created to find an ideal value for n. The ideal value for n was found to be 4 and this value was used for all the simulations. The static analysis was used on this ideal value to create its DC response and find the V_{IL}, V_{OH}, V_{IH}, and VOL by calculating the derivative of the graph. The dynamic simulation was performed using transient analysis for a capacitance from 0f to 150f. The physical view for the CMOS inverter was created and used to create the extracted view. The extracted view had the same analyses applied from before with and had its static compared to the same CMOS schematic. Sizing the PMOS twice as wide as the NMOS did not lead to $V_M = V_{DD}/2$. Increasing the PMOS size relative to NMOS will both increase VM and reduce the rise delay.