Ryerson University
Department of Electrical and Computer Engineering
ELE734: LOW-POWER DIGITAL INTEGRATED CIRCUITS
Mid-Term Examination, October, 2012
Duration:1.5 hours

Student's Name: Solution

Student's Number: ..... **Section:** .....

NOTES:

1. This is a **Closed Book** examination. No aids other than the approved calculators and **1 sheet (2 pages) of aid sheet** are allowed.
2. Answer all questions.
3. **No questions are to be asked** in the examination hall. If doubt exists as to the interpretation of any question, the student is urged to submit with the answer paper, a clear statement of any assumptions made.

Question No.	*Mark of each question*	*Mark obtained*
Q1	20	
Q2	20	
Q3	20	
Q4	20	
Total (Out of 80):		

Q1:

Design a static CMOS gate that has the following output.

$Out = !(A(B+C)+DE)$

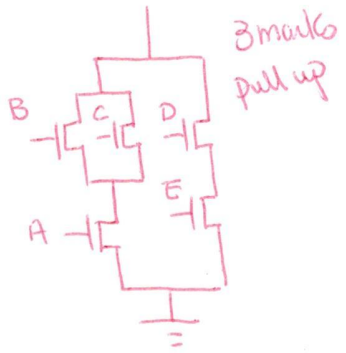
a) Draw the transistor-level schematic of your design. Size the transistors to provide a worst case pull-up and pull-down resistance of R (assuming a unit nmos transistor has the resistance of R and a unit pmos transistor has the resistance of 2R). (10 marks)

b) Draw stick diagram of the gate you designed in Q1 (please clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (5 marks)

c) Estimate the area of the gate based on your stick diagram. (5 marks)

$Z = \overline{A\cdot(B+C)+D\cdot E}$

nmos network.



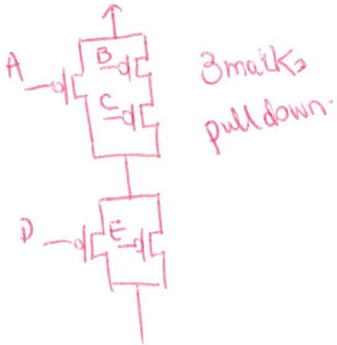
3marks pull up

$Z = \overline{A\cdot(B+C)+D\cdot E}$

$= \overline{A\cdot(B+C)}\cdot\overline{D\cdot E}$

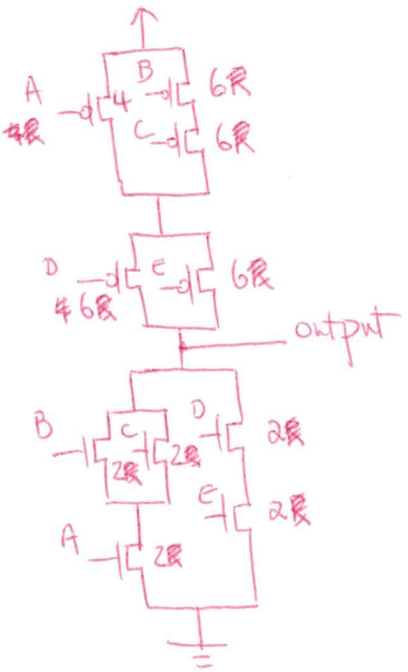
$= (\bar{A}+\overline{B+C})\cdot(\bar{D}+\bar{E})$

$= (\bar{A}+\bar{B}\cdot\bar{C})\cdot(\bar{D}+\bar{E})$



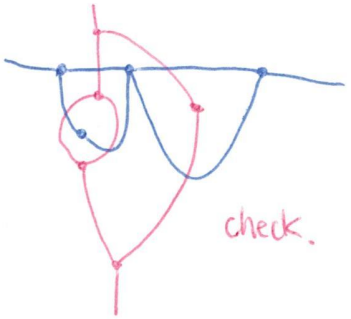
3marks pulldown.

All together



Sizing pull up 2marks

pull down 2marks.



check.

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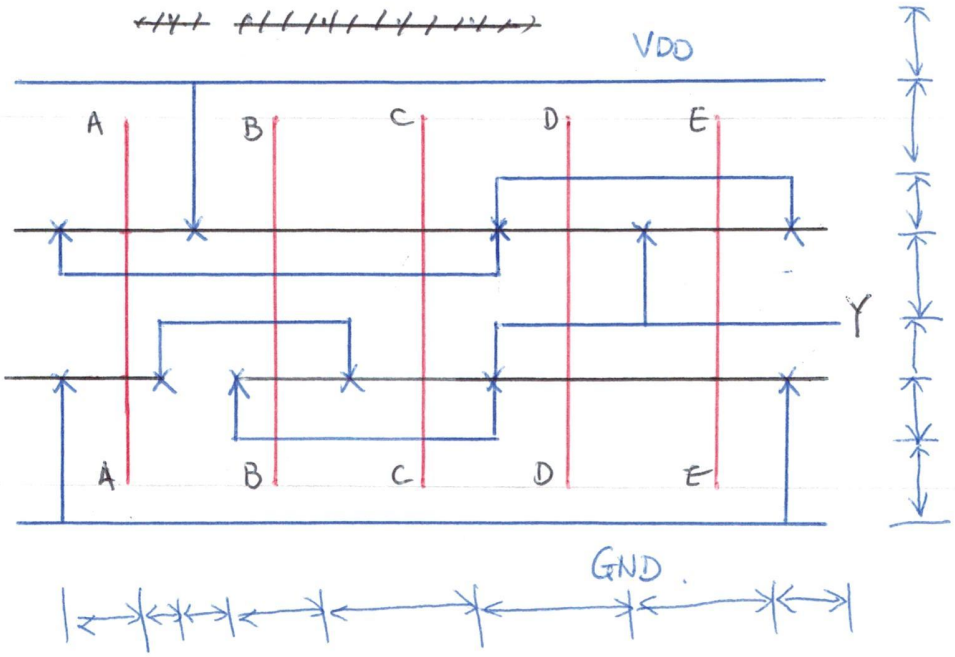

$7 \times 8 = 56\lambda$

$8 \times 8 = 64\lambda$

$56 \times 64\,\lambda^2 = 3584\,\lambda^2$.

+2 basic poly on diffusion layout.
+2 no wire crossing
+2 basic connections are correct.
+2 horizontal dimension
+2 vertical dimension

Q2:

a) List the three I-V equations that govern the cutoff, linear, and saturation regions of operation of an ideal nMOS (long-channel/Shockley model) (10 marks).

b) If one want to increase the threshold voltage through body effect, should the body voltage be increased or decreased? Why? (10 marks).

a)

$$I_{ds} = \begin{cases} 0 & (+1) \\ \beta(V_{GT} - V_{ds}/2)V_{ds} & (+2) \\ \frac{\beta}{2}V_{GT}^2 & (+2) \end{cases}$$

$V_{gs} < V_t$ (+1) cutoff

$V_{ds} < V_{GT}$ (+1) Linear

$V_{ds} > V_{GT}$ (+1) Saturation

$V_{GT} = V_{gs} - V_t$

(+2) $\beta = \mu C_{ox} \frac{W}{L}$ ← transistor width, ← transistor length

mobility ↑, gate oxide capacitance ↑

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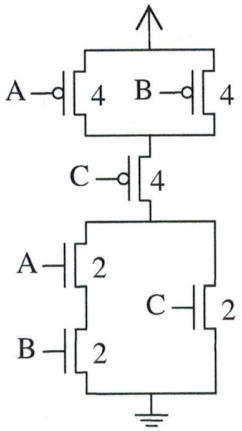
b) $V_t = V_{to} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$ (+4) or $V_t = V_{to} + K_r V_{sb}$.

body voltage should be decreased (+3)

because dec body voltage increases V_{sb} (+3)
increases V_t

Q3:

Calculate the worst case pull-up and pull-down logic effort and the parasitic delay of the following gate (please account for all internal diffusion capacitances in your calculations). (20 marks)

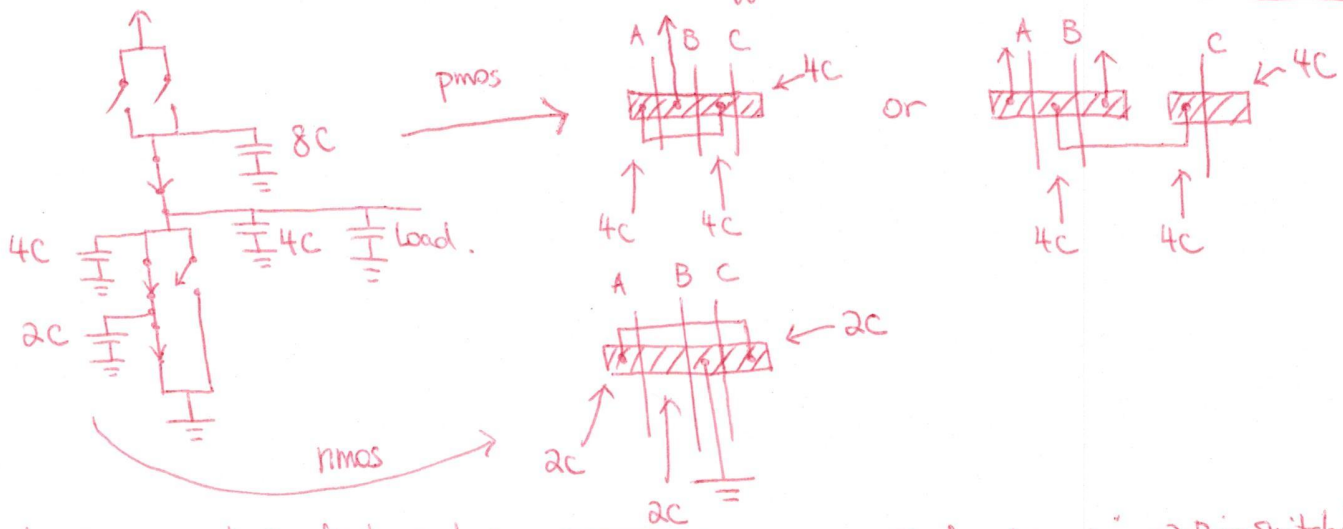


Worst case pull up

① discharge most caps [2 marks]

Initial Configuration

* pmos C must be on ⇒ nmos C must be off ⇒ nmos A+B must be on ⇒ A=1 B=1 C=0 ⇒

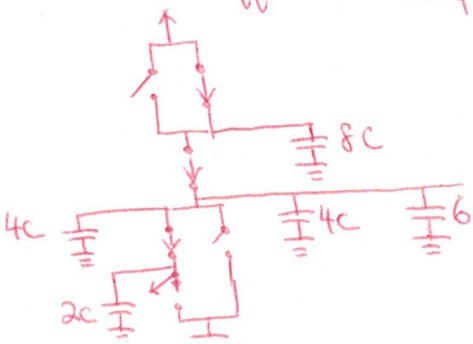


② charge up most of discharged caps [2 marks]

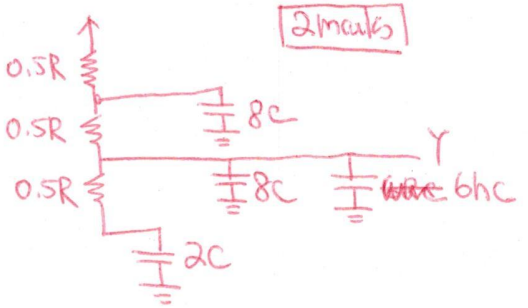
Final configuration ⇒ B is switching

load = 6hc.

* Turn B nmos off ⇒ turn B pmos on ⇒ A=1 B=0 C=0



[2 marks]



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1 mark

parasitic delay

$t_{pdr}/3RC = \frac{14}{3} + 2h$ ← logic effort — 1 mark

$t_{pdr} =$

$2C(0.5+0.5)R + 8C(0.5+0.5)R + 6hC(0.5+0.5)R + 8C \cdot 0.5R$

$= 2RC + 8RC + 6hRC + 4RC$ — 2 marks

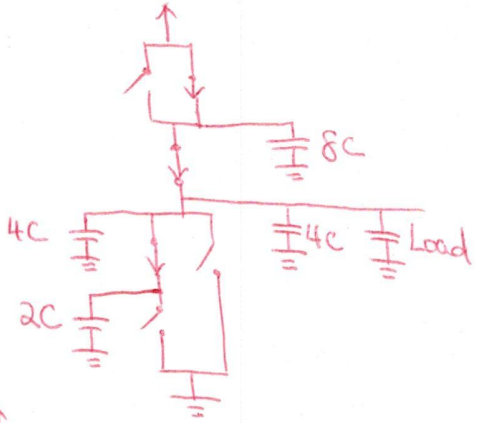
$= 14RC + 6hRC$.

Worst case Pull down

① charge most caps — 2 marks

* pmos C must be on ⇒ nmos C must be off C=0
* A nmos must be on ⇒ pmos A must be off A=1
* B pmos must be on ⇒ B nmos must be off B=0.

A=1, B=0, C=0 ⇒ initial configuration

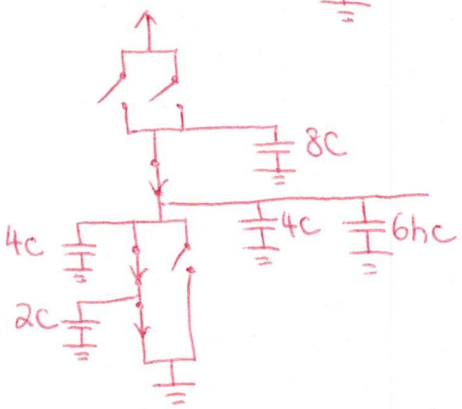


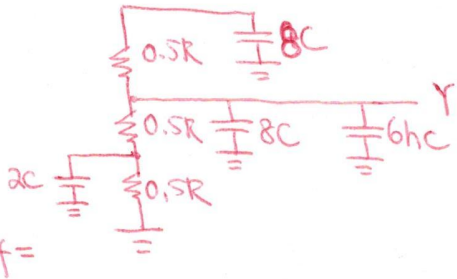
② discharge most of charged caps — 2 marks

* turn B pmos off ⇒ turn B nmos on

A=1, B=1, C=0 ⇒ final configuration

B is switching load = 6hC





2 marks

$t_{pdf} =$

$8C(0.5+0.5)R + 8C(0.5+0.5)R + 6hC(0.5+0.5)R + 2C(0.5)R$ — 2 marks

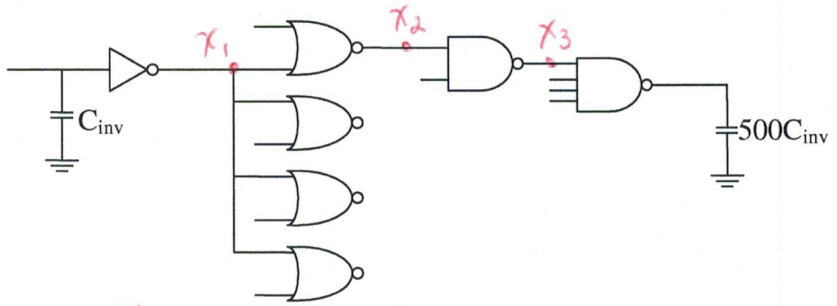
$= 8RC + 8RC + 6hRC + RC$

$= 17RC + 6hRC$ — 1 mark

$t_{pdf}/3RC = \frac{17}{3} + 2h$ — 1 mark

Q4:

Calculate the optimum path delay and the transistor size for the following circuit, where C_{inv} is the input capacitance of the inverter. (inverter: g=1, p=1; 2-input nand: g=4/3, p=2; 2-input nor: g=5/3, p=2; 4-input nand: g=6/3; p=4) (20 marks)



$h_1 = \frac{x_1}{C_{inv}}$ $h_2 = \frac{x_2}{x_1}$ $h_3 = \frac{x_3}{x_2}$ $h_4 = \frac{500C_{inv}}{x_3}$

$b_1 = 1$ $b_2 = 4$ $b_3 = 1$ $b_4 = 1$

$g_1 = 1$ $g_2 = \frac{5}{3}$ $g_3 = \frac{4}{3}$ $g_4 = \frac{6}{3}$

$F = GBH$

$= (g_1 g_2 g_3 g_4)(b_1 b_2 b_3 b_4)(h_1 h_2 h_3 h_4)$ 4 marks

$= (1 \cdot \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{6}{3})(1 \cdot 4 \cdot 1 \cdot 1)(\frac{500C_{inv}}{C_{inv}})$

$= 8888.89$.

$(F)^{1/4} = 9.71$ 2 marks

Optimal path delay $= 9.71 \times 4 + 1 + 2 + 2 + 4 = 47.84$. 2 marks

$g_1 h_1 b_1 = 9.71$

$1 \cdot \frac{x_1}{C_{inv}} \cdot 4 = 9.71$

$x_1 = 2.43 C_{inv}$

2 marks

$g_2 h_2 b_2 = 9.71$

$\frac{5}{3} \cdot \frac{x_2}{x_1} \cdot 1 = 9.71$

$x_2 = 14.16 C_{inv}$

2 marks

$g_3 h_3 b_3 = 9.71$

$\frac{4}{3} \cdot \frac{x_3}{x_2} \cdot 1 = 9.71$

$x_3 = 103.12 C_{inv}$

2 marks

$g_4 h_4 b_4 = 9.71$

$\frac{6}{3} \cdot \frac{500C_{inv}}{x_3} \cdot 1 = 9.71$

$500C_{inv} = 500.65 C_{inv}$

↑ Check.

2 marks

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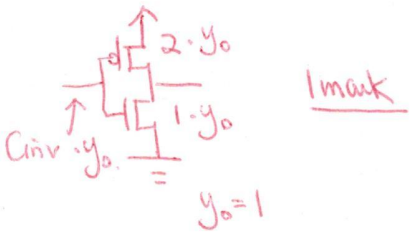
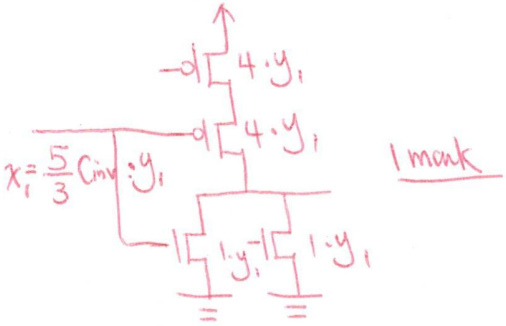


1 mark

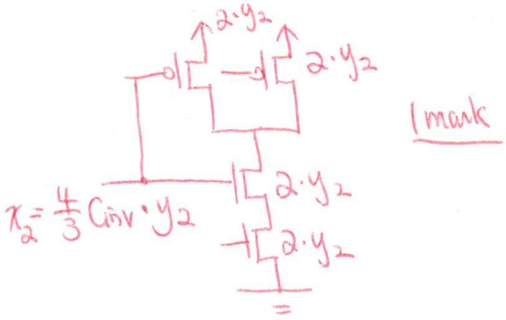
$y_0 = 1$



1 mark

$\frac{5}{3} C_{inv} \cdot y_1 = 2.43 C_{inv}$

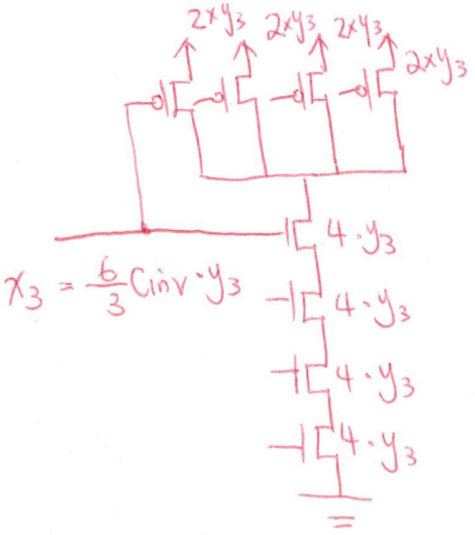
$y_1 = 1.458$



1 mark

$\frac{4}{3} C_{inv} \cdot y_2 = 14.16 C_{inv}$

$y_2 = 10.62$



1 mark

$103.12 C_{inv} = \frac{6}{3} C_{inv} \cdot y_3$

$y_3 = 51.56$