Midterm

Time Limit: 1:30:00 Time Left:Time Exceeded Vatsal Shreekant: Attempt 1

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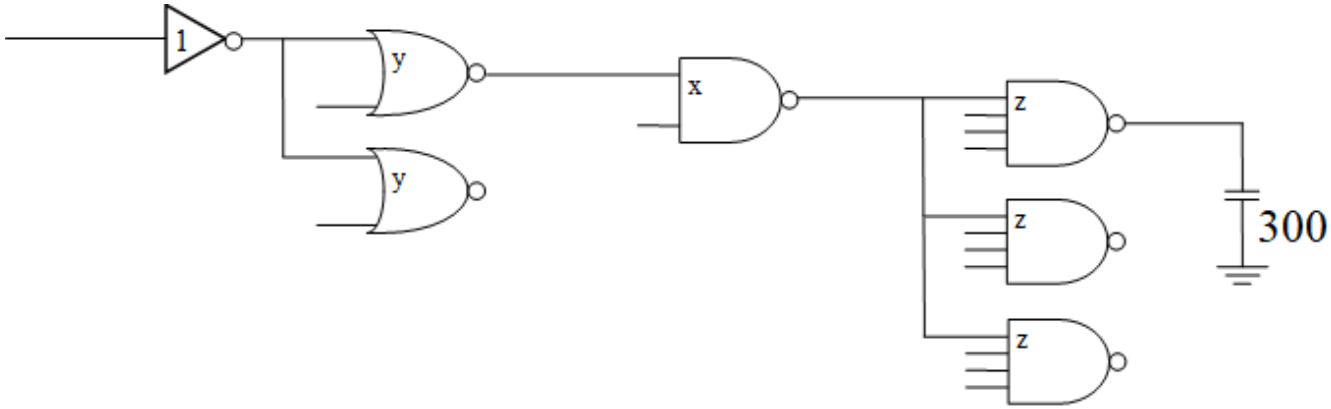
1 ✓ 2 ✓ 3 ✓

b. Draw the transistor level diagram for the 2-input nand gate and clearly label the size of each transistor in the diagram. (4 marks)
c. Calculate the optimum path delay if additional inverter stages can be added between the 4-input nand gate and its load capacitance. (4 marks)
d. How many additional stages should be added in part c) in order to achieve the optimum delay. (4 marks)



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