30/30

Ryerson University
Department of Electrical and Computer Engineering
COE 608–Computer Organization and Architecture

March 8, 2016

Midterm Test

Name: [redacted] **Student Number:** [redacted]

Examiners: N. Mekhiel

Time limit: 1 hour 40 min

Notes:
a) Closed book.
b) No calculators.
c) Answer all questions **in the space provided.**

Total Marks=30

Q1- Assume the following C code :-

```
for(i=0; i<=1000; i++) {
        A[i] =B[i]+ A[i];
    }
```

i = $s3
B[0] = $s1
A[0] = $s0

Assume that $S0 has the address of A[0] and $S1 has the address of B[0] and i is in $S3.

1.1-(5 Marks) Write the above code using MIPS instructions.

```
Initialize : addi $s3, $zero, 0 ; setting i=0
             addi $t5, $zero, 1000 ; setting $t5 to contain the value 1000 so we can check
Loop :  sll $t0, $s3, 2 ; 4xi = $t0
        add $t1, $s0, $t0 ; A[i] = $t1
        add $t2, $s1, $t0 ; B[i] = $t2
        lw $t3, 0($t1) , $t3 = content of (A[i])
        lw $t4, 0($t2) ; $t4 = content of (B[i])
        add $t4 $t3, $t4 ; $t4 = A[i] + B[i]
        sw $t4, 0($t1) ; A[i] = A[i] + B[i] = $t4
        beq $s3 $t5, EXIT ; check if i = $t5 or 1000, then exit
        addi $s3, $s3, 1 ; i++
        J Loop : repeat loop
EXIT, RTS
```

5

Name: _____ Section: _____

1.2 (2 Marks) How many instructions are executed during running this code.

whole program: 2 + (10 × 1001) = 10,003

Constant instruction only runs once

The loop runs for 1001, so there are 10 instructions happening at every loop

without the loop there are 12 instructions in total

(2)

1.3 (2 Marks) How many memory data references will be made during the execution.

Memory data references will be made at lw and sw operations so this code has 2 lw and 1 sw = 3 times memory data referenced and the program runs for 1001 times so 3 × 1001 = 3003 times will the memory data references be made throughout the whole execution of the loop

(2)

1.4 (3 Marks) Find the performance of above code in MIPS 1 GHz processor assuming that arithmetic instruction takes 1 cycle, data transfer instruction takes 6 cycles, conditional branch takes 2 cycles and jump takes 1.2 cycle.

Performance = $\frac{1}{\text{Execution Time}}$ ⇒ CPU Time = CPI × Instruction count × Clock Cycle Time

Clock cycle time = $\frac{1}{\text{Clock rate}}$

$= \frac{1\times7 + 6\times3 + 2\times1 + 1\cdot2\times1}{1\times10^9}$

$= \frac{7 + 18 + 2 + 1\cdot2}{1\times10^9} = \frac{28.2}{10^9}$

Performance = $\frac{1}{28.2\times10^{-9}}$ s

$= 28.2\times10^{-9}$ s

(3)

1.5 (3 Marks) Find the speed up if system uses a cache to speed the data transfer by 2 times.

New = $\frac{1\times7 + 8\times3 + 2\times1 + 1\cdot2\times1}{1\times10^9} = \frac{19.2}{10^9} = 19.2\times10^{-9}$ s for the new Execution time

(3)

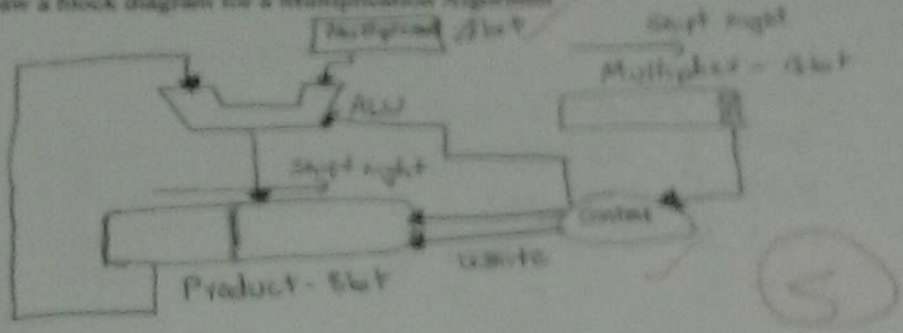
So the speed up = $\frac{28.2\times10^{-9}}{19.2\times10^{-9}} \approx 1.41$

$$
\begin{array}{r}
1.41 \\
19.2\overline{)28.2} \\
19 \\
\hline
90 \\
76 \\
\hline
140 \\
96 \\
\hline
44
\end{array}
$$

∴ By cutting down data transfer by 2 times, the program will run 1.4 times faster

Name _____ - 1 - Section _____

Q2.1 (5 Marks) Draw a block diagram for a Multiplication Algorithm



5

Q2.2 (5 Marks) Apply the above algorithm for the following: 4 3

Operation ADD OR SHIFT	Product 0 0 0 0 0 0 0 0	Multiplicand 0 1 0 0	Multiplier 0 0 1 1
Add	0100	0100	0011
SRR Multiplier SRR Product	01000000 00100000	0100	0001
Add	01100000	0100	0001
SRR Multiplier SRR Product	00110000	0100	0000
SRR Multiplier	00011000	0100	0000
SRR Product	00001100	0100	0000
SRR Multiplier	00000110	0100	0000
SRR Product	00000011	0100	0000
FINAL	00000011	0100	0000

12 = 4 × 3

5

Name:_____ Section:_____

Q2.3- (5 Marks) Determine IEEE754 Floating point representation for -7.875

(-) ⟹ Sign bit is 1

1	7
1	3
1	1
0	0

0111

$0.875 \times 2 = 1.750$
$0.750 \times 2 = 1.500$
$0.500 \times 2 = 1.000$
$0.00 \times 2 = 0.00$
$0 \times 2 = 0.00$

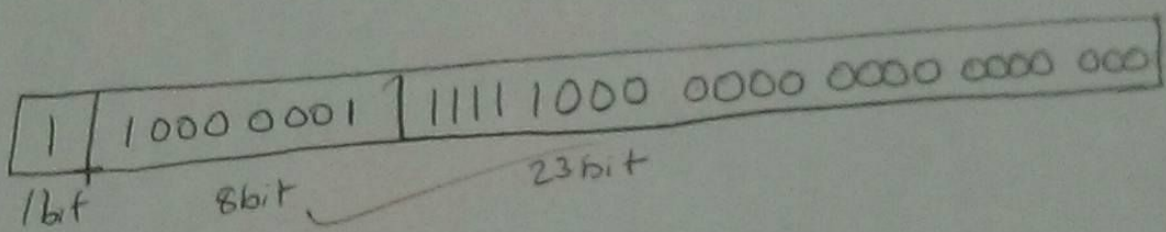
$111\overline{000}$

$= 111.\overline{111000}$

$= 1.\underbrace{11111\overline{000}}_{\text{Mandisa}} \times 2^{2}$ – Exp

$Exp = 2 + 127 = 129$

$Mandissa = 11111\overline{000}$



5