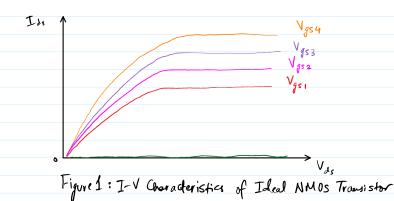
Lab 1 - Prelab September 23, 2020 3:05 PM

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Am -2) NMOs:-



PMOS :-

$$I_{5D} = 0 , V_{5G} < |V_{t}| \quad (\text{cutoff})$$

$$\mu_{P} \cdot (o_{X} \left(\frac{\omega}{L}\right) \cdot \left[\left(V_{g_{5}} - |V_{t}|\right) - \frac{V_{5D}}{2}\right] \cdot V_{5D} , V_{5D} < V_{5G} - |V_{t}| , V_{5G} > |V_{t}| \quad (\text{inver})$$

$$V_{2} \cdot \mu_{P} \cdot (o_{X} \left(\frac{\omega}{L}\right) \cdot \left(V_{5G} - |V_{t}|\right)^{2} , V_{5D} > V_{5G} - |V_{t}| , V_{5G} > |V_{t}| \quad (\text{saturation})$$

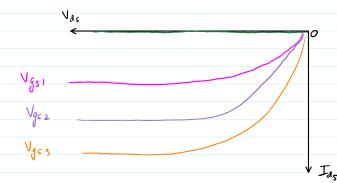


Figure 2: I-V Characteristics of Ideal PMOS Transistor

Ans-3)
$$V_t = V_{to} + \gamma \left(\sqrt{\beta_s} + V_{so} - \sqrt{\phi_s} \right)$$

Applying $V_{so} = \gamma threshold voltage increases as V_{so} increases$

Ans-4) Assuming that the surface voltage is approximately the body voltage, that is, Van = Vas

The effective channel leggth Leff = L- Lat depletion region

· La increases as Von increases

Hunce, increasing Vs will decrease effective channel length.

· A shorter channel length leads to higher current.

Hence, It's increases with Vos in soluration.

Saturation :-

$$I_{ds} = \frac{B}{2} \cdot V_{qT}^2 \cdot \left(1 + \frac{V_{ds}}{V_A}\right)$$

- This equation accounts for (LM for drain-correct equation. - VA is proportional to the channel legate.

Therefore, the effects of CLM are more important in short channel devices.

Ans-5) In an ideal transistor, the correct doesn't get cutoff when Vgs < Vt, rather drops exponentially.

The subthershold leskage current increases significantly with Vas due to drain induced barrier lowering.

There is a lower limit on Ids set by drain junction leakage. $I_{ds} = I_{dso} \cdot e^{\frac{V_{gs} - V_{to} + n \cdot V_{ds} - K_{s} \cdot V_{ss}}{NV_{t}}} \cdot \left(| - e^{\frac{-V_{ds}}{V_{c}}} \right)$

