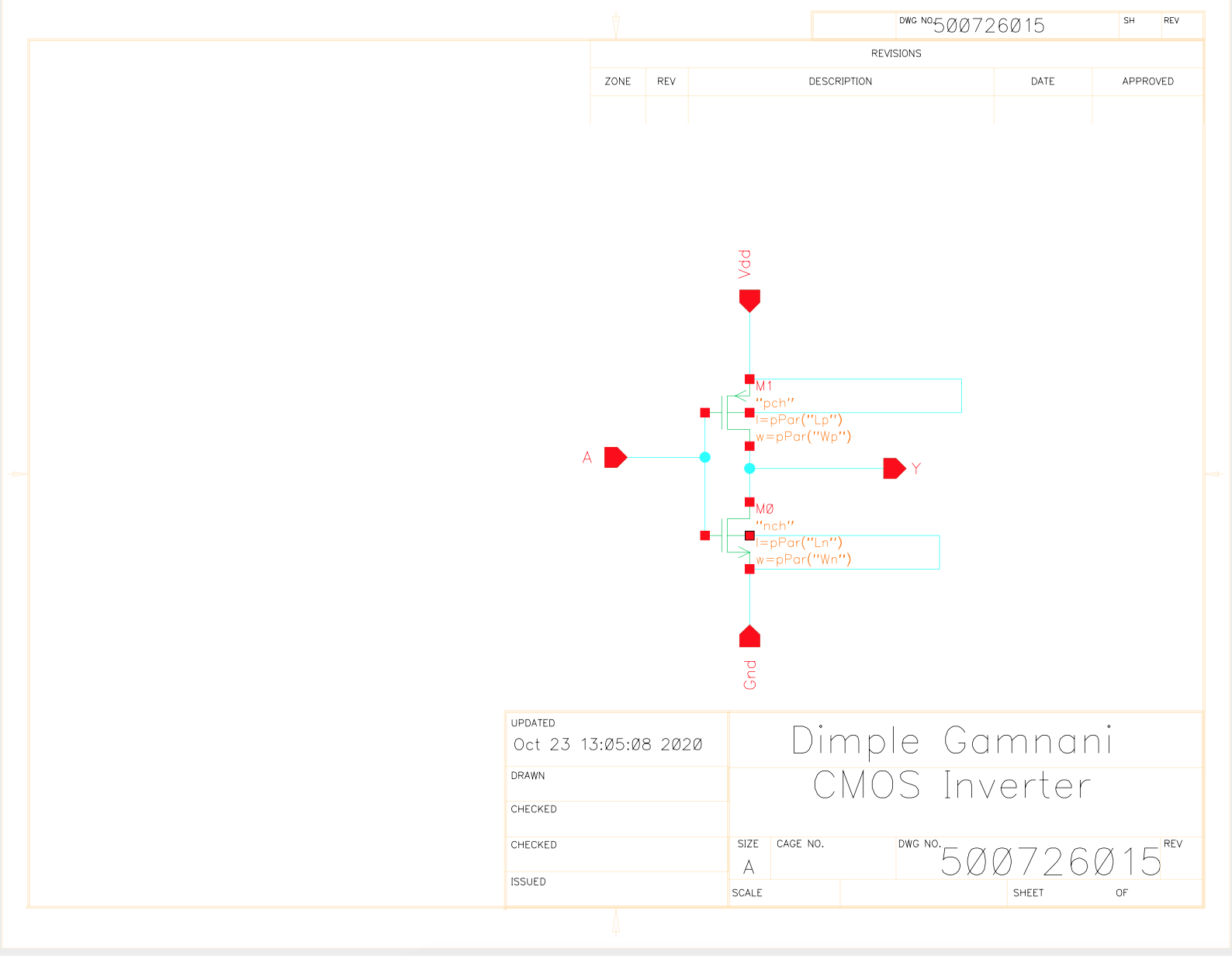
# Post Lab

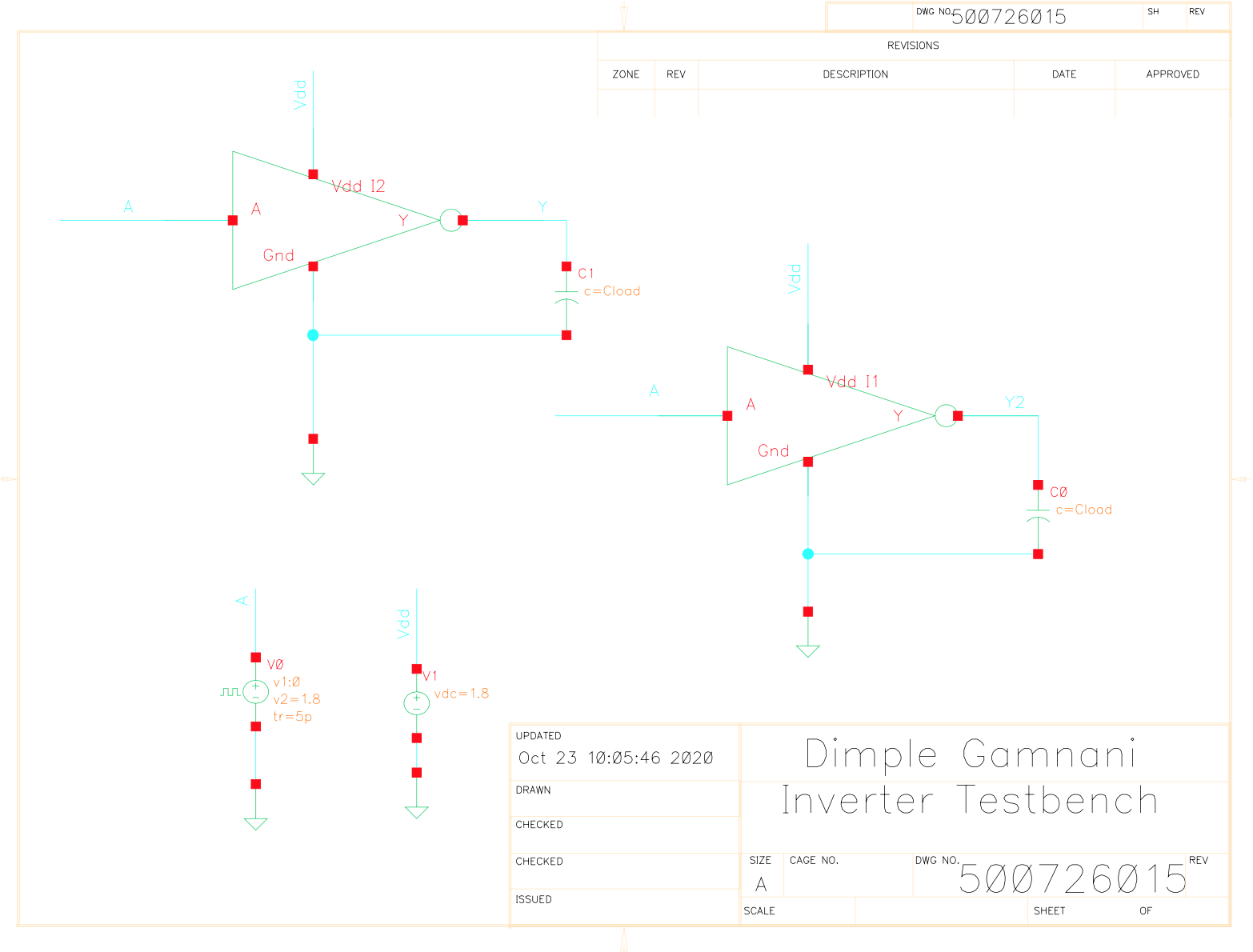
## Schematic of the CMOS Inverter

Figure 1 – Schematic of the CMOS Inverter



## Schematic of the testbench

Figure 2 – Schematic of the Inverter Testbench

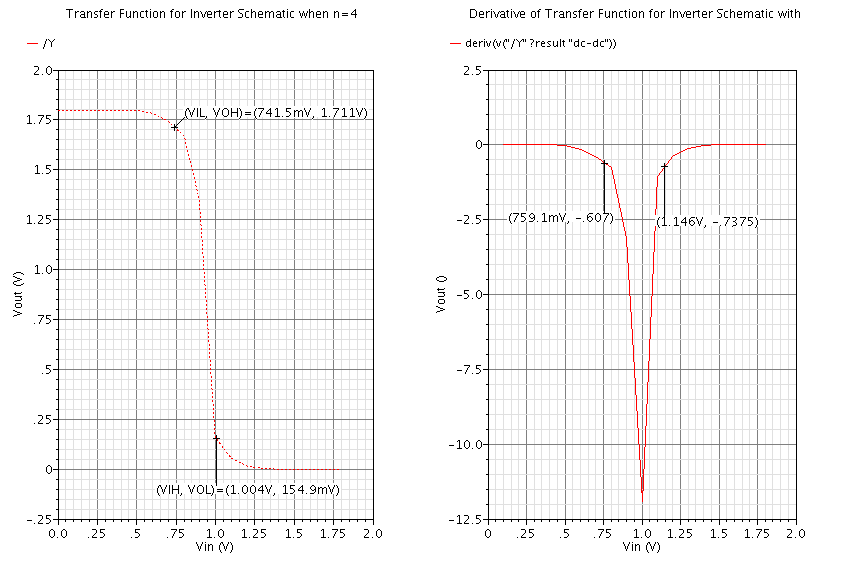


## Static and Dynamic CMOS Inverter Simulations

Figure 3 – Transfer Characteristics of Skewed Inverters



Figure 4 – Transfer Function for Inverter Schematic and its derivative



## Layout and Extracted view of the CMOS Inverter

Figure 7 – Layout view of the CMOS Inverter

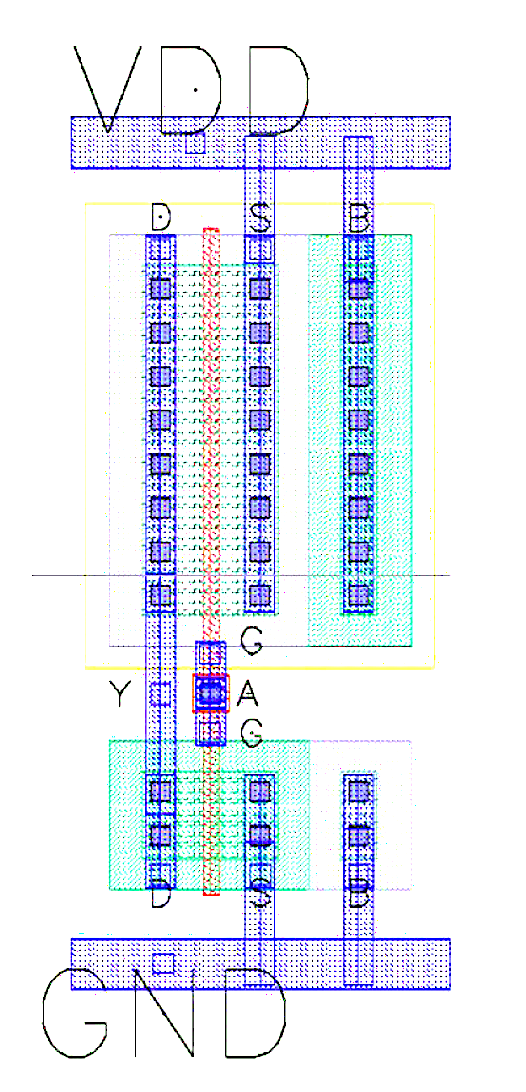
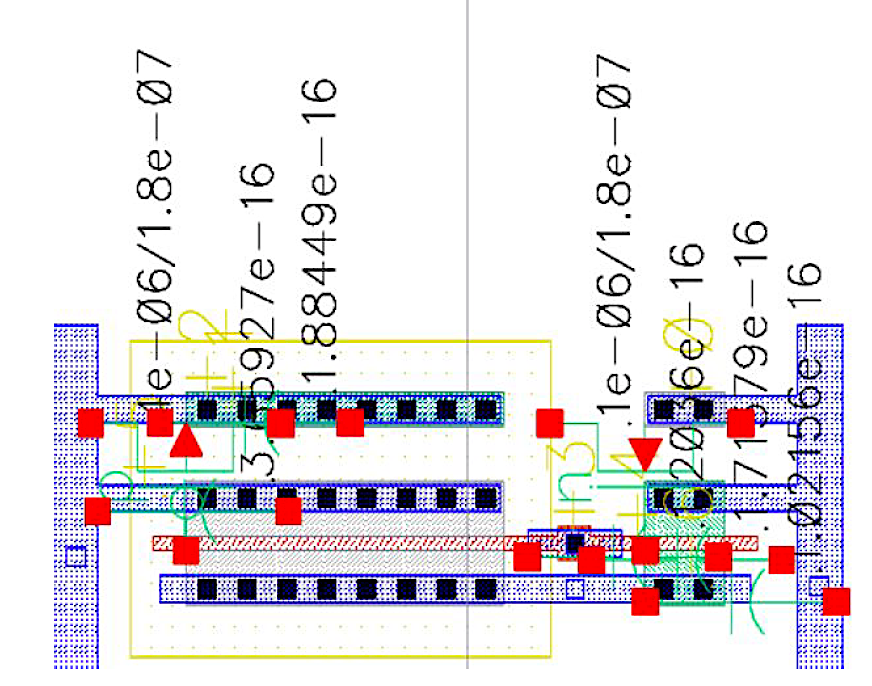


Figure 8 – Extracted view of the CMOS Inverter



## Post-Layout Simulation Results

Figure 9 – Rising and Falling delay as a function of load capacitance (Extracted results)

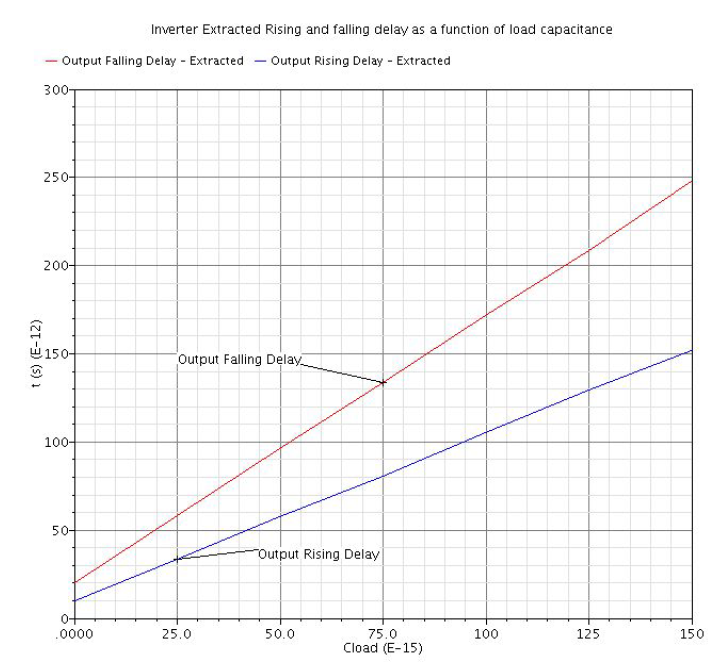


Figure 10 – Rising and Falling delay as a function of load capacitance (Schematic results)

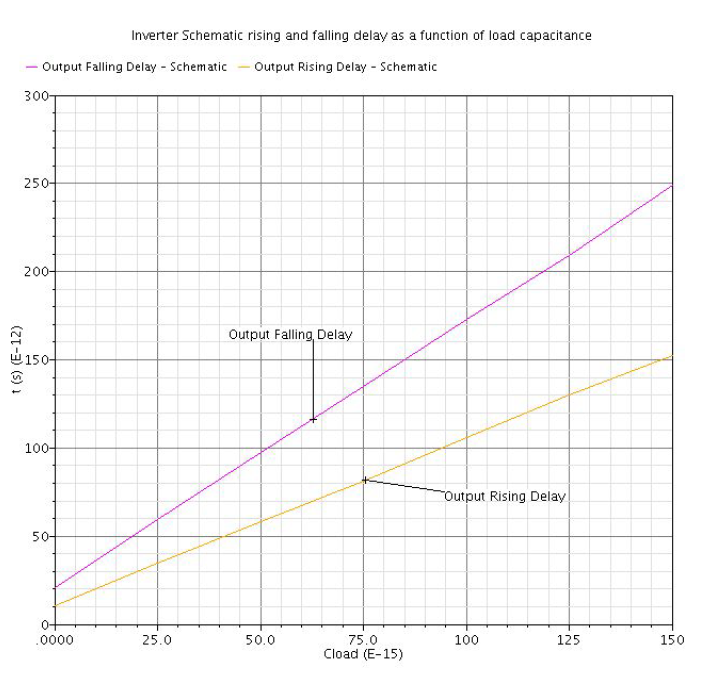


Figure 11 – Transfer Function when n =4 (Extracted results)

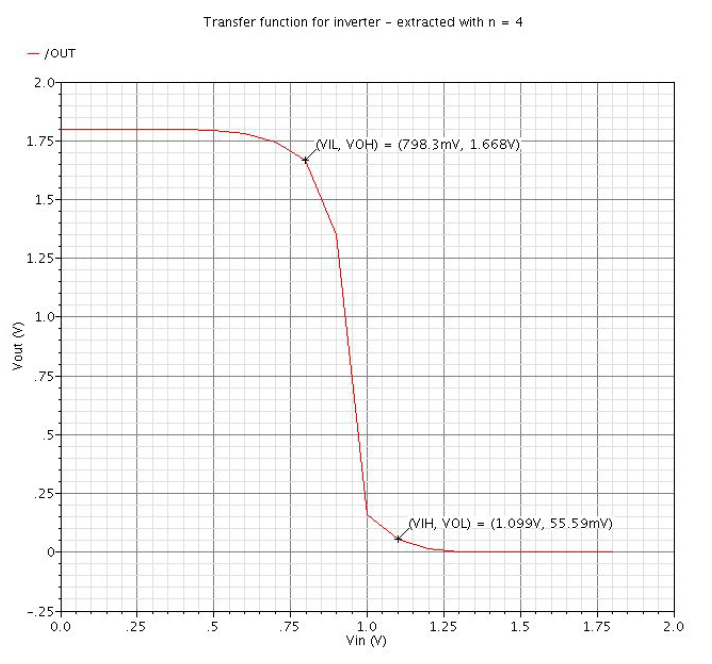


Figure 12 – Transfer Function when n =4 (Schematic results)

