COE718: Embedded Systems Design
Sample Final Exam- Fall 2015

Name and Student ID: _____

Total Time Allowed: **150 Minutes** Maximum Marks: 100

i. The examination has 8 pages and 6 questions. Answer all the questions. State any **assumptions**.
ii. To earn maximum credit, your answer must be concise, to the point and in the given space
iii. All questions are not of the same difficulty and value. Consider this when allocating time for their solutions.

1. Draw a diagram of the Triple Modular Redundancy (TMR) architecture. Describe how it functions. Also list any possible issues that may arise using the TMR approach.

MARKS: 10

2. If an application is 20% serial, and 80% parallelizable, assuming four processors are used, what is the speedup of the application according to Amdahl's Law?

MARKS: 5

3. Table I presents an RMS schedule for a real-time military tracking system. The system consists of 3 tasks to be scheduled, each with their corresponding computation time and period.

Table I: Task Scheduling Requirements

Task	Description	Computation Time (C)	Period (T)	Priority
UTL	Update Track Log	10	20	
UTr	Object Tracking	3	10	
GPST	GPS Triangulation	1	5	

(a) Determine if the military tracking device is schedulable according to the RMS schedulability test.

MARKS: 5

(b) Verify if the schedulability test in (a) was correct by calculating the response times of all three tasks in Table I. Fill the "Priority" column as necessary. State your findings and compare to the schedulability test.

MARKS: 10

(c) Consider that the RMS schedule in Table I needs to be converted into an EDF schedule, with arrival times 1, 3, and 0 for tasks UTL, UTr, and GPST, respectively. Determine if this revised task set is schedulable using (1) the EDF schedulability test and (2) the timing diagram method.

MARKS: 8

(d) Briefly explain the differences between:

- Rate Monotonic Scheduling (RMS) and Deadline Monotonic Scheduling (DMS)
- Rate Monotonic Scheduling (RMS) and Earliest Deadline First (EDF)

MARKS: 6

(e) List and briefly explain two factors that are not considered during the response time calculations and real-time system scheduling you have calculated in (b).

MARKS: 4

4. A fault-tolerant system architecture consisting of seven components is shown in Fig 1. Determine the overall reliability of the system, assuming that the component reliabilities are defined as follows:
R1 = 0.95, R2 = 0.9, R3 = 0.9, R4 = 0.99, R5 = 0.87, R6 = 0.88 and R7 = R8 = 0.85.

MARKS: 10

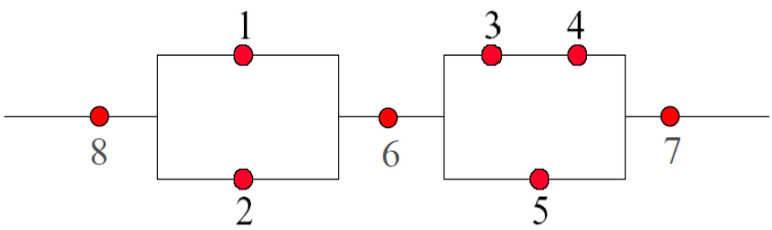

Fig. 1: Fault-Tolerant System Architecture

5. A client has approached you specifying that you are to design a hardware/software embedded system for a parabolic motion estimator. After assessing the requirements, you develop the DFG provided in Fig. 2. Your embedded system may consist of a CPU, and optional multiplier, add, and/or squaring hardware unit. The requirements specified by the client are as follows:

Execution Time $\leq$ *16 msec*
Gates $\leq$ *2000*

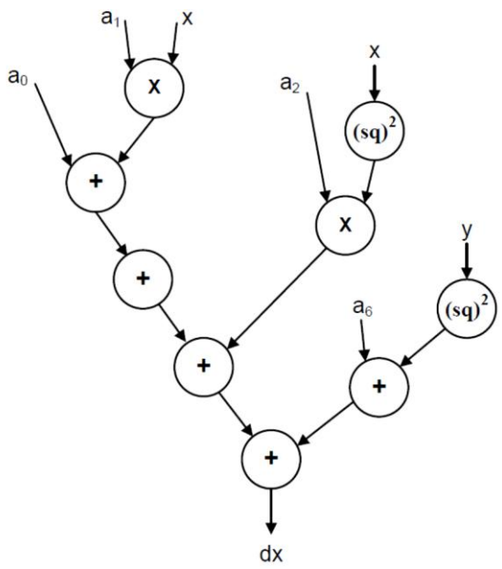

Fig. 2: DFG for Parabolic Motion Estimator Design

Find an ES design which meets the requirements specified above, assuming you have discovered the following specifications listed in Table II. Clearly specify your final results which meet the requirements Show all your work.

MARKS: 10

Table II: HW/SW System Specifications

Operation	**SW Exe (ms)**	**HW Exe (ms)**	**Gates**
Multiply	10.2	2.4	1200
Add	2.54	0.3	300
Square	8.35	1.2	600

6. Consider a system which must read data blocks incoming from a Serial Peripheral Interface (SPI) port. Our system is running on an ARM Cortex-A9 @ 800MHz.

   Specifications of SPI: 32bits per transfer, Max rate = 25Mb/sec

   The Cortex CPU's instruction clock cycles are presented in Table II.

Table II: Cortex-A Instruction Clock Cycles

Instructions		Clock Cycles
PUSH, POP, LDM, STM		1 + #regs
SDIV, UDIV		2–12
SMLAL, UMLAL		4–7
SMULL, UMULL		3–5
Unconditional branch (B, BL, BX)		2–4
Conditional branch	Successful	2–4
	Failed	1
LDRD, STRD		3
ADR, MLA, MLS, & all LDR's and STR's		2
All other instructions		1

   (a) *Assume all branches are taken with the best outcome*. What is the maximum transfer rate (bandwidth) we can achieve if we are using polling, considering that we have derived the following function:

   MARKS: 8

```
spi_block_transfer:

transfer_more:      CBZ    R1, return_main
spi_wait:           LDR    R0, [R2, #0x18]  ; Read status register
                    TST    R0, #0x80        ;Test to see if SPI transfer complete
                    BNE    spi_wait
                    MOV    R3, SPI_DAT      ; move the SPI data to R3
                    STR    R3, [R2]         ; send the data to the device
                    SUB    R1, R1, #1       ; Decrement counter
                    B      transfer_more    ;
return_main:        BX     LR               ; return to main
```

Show all your work.

(b) Assume BX has the best outcome. What is the maximum transfer rate (bandwidth) we can achieve if we are using an IO interrupt method in the system, considering that we have derived the following function for receiving data:

MARKS: 10

```
spi_ISR:

        ADR     R0, SPI_PORT        ; obtain the SPI device address
        MOV     R3, R0              ; move the SPI data to R3
        LDR     R2, SPI_NINDEX      ; update the queue's index
        ADD     R2, R2, #1
        STR     R2, SPI_NINDEX

        LDR     R0, SPI_B_ADDR        ; Get the SPI buffer's address
        STR     R3, [SPI_BUFFER, R0]  ; To place the data we read into the buffer

        LDR     R2, SPI_B_COUNT       ; Update the buffer's num of entries
        ADD     R2, R2, #1
        STR     R2, SPI_B_COUNT

        BX      LR                    ; return
```

Assume tail chaining costs are an additional 6 clock cycles. Show all your work.

(c) The system may also use a DMA unit to transfer the data from the SPI input port to memory without CPU intervention. Assume the DMA may transfer 64b/c.c, and that since it is external to the CPU, it may operate at approximately 20ns/c.c. What is the maximum transfer rate that the DMA method may support?

MARKS: 4

(d) Which methods can support the SPI protocol using the Cortex-A9? Why?

MARKS: 4

(e) List the advantages and disadvantages of implementing each approach from (a) through (c).

MARKS: 6