Ryerson University
Department of Electrical and Computer Engineering
ELE734: LOW-POWER DIGITAL INTEGRATED CIRCUITS
Mid-Term Examination, October 2018
Duration:1.5 hours

Student's Name: ..... Solution .....

Student's Number: ..... **Section:** .....

NOTES:

1.This is a **Closed Book** examination. No aids other than the approved calculators are allowed.

2.Answer all questions.

3.**No questions are to be asked** in the examination hall. If doubt exists as to the interpretation of any question, the student is urged to submit with the answer paper, a clear statement of any assumptions made.

Question No.	*Mark of each question*	*Mark obtained*
Q1	20	
Q2	20	
Q3	20	
Total (Out of 60):		

Q1:

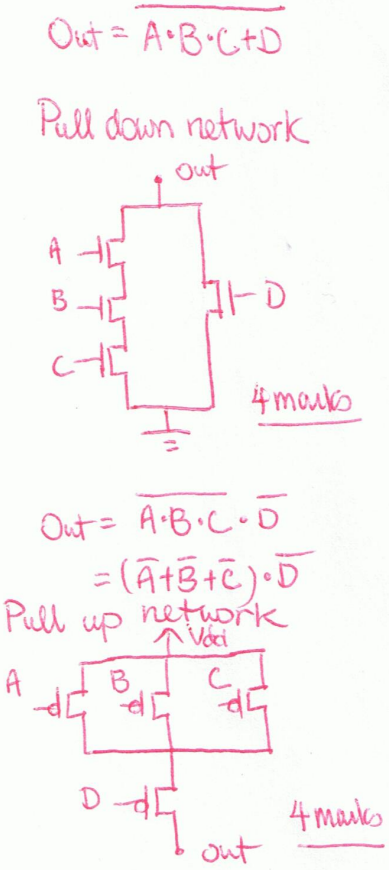
Design a static CMOS gate that has the following output.

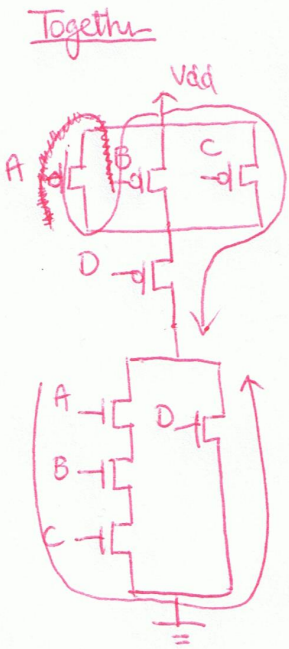
*Out = !(A*B*C+D)*

a) Draw the transistor-level schematic of your design. Sizing is not required. (8 marks)

b) Draw stick diagram of the gate that you have designed (***please minimize layout area by maximizing diffusion sharing*** and clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (8 marks)

c) Estimate the area of the gate based on your stick diagram. (4 marks)





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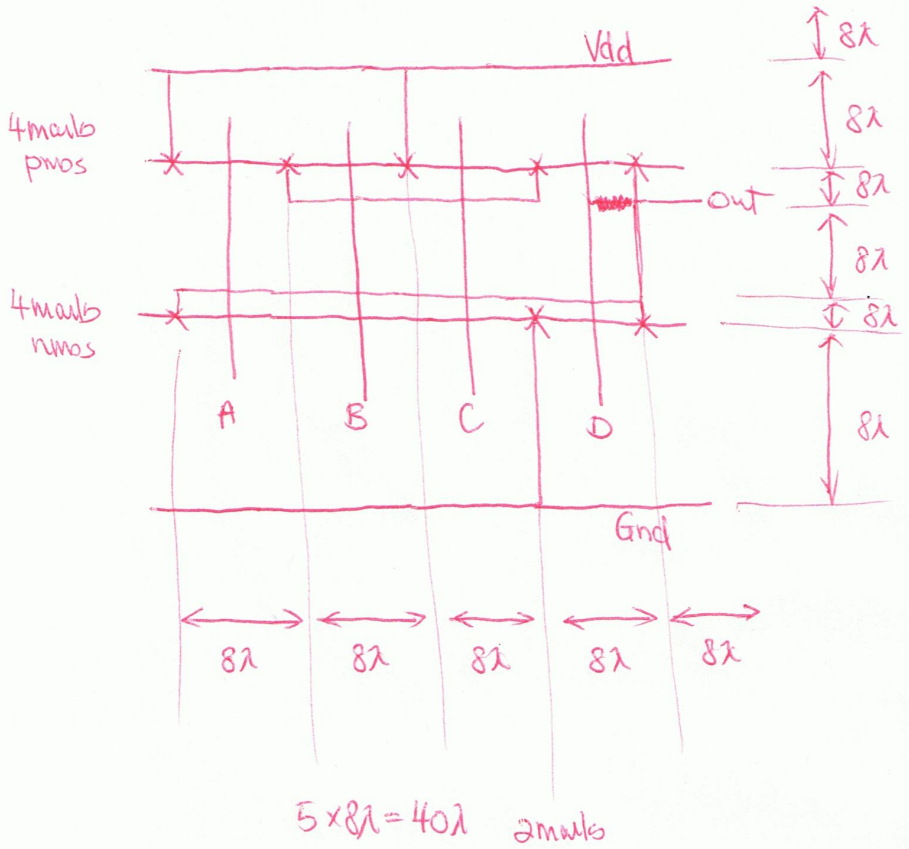
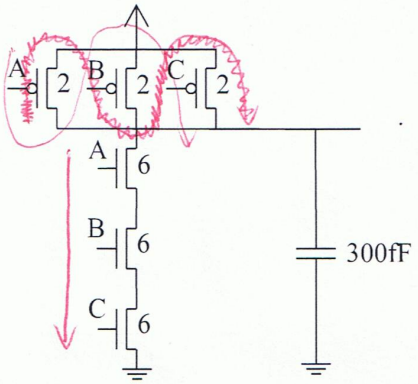
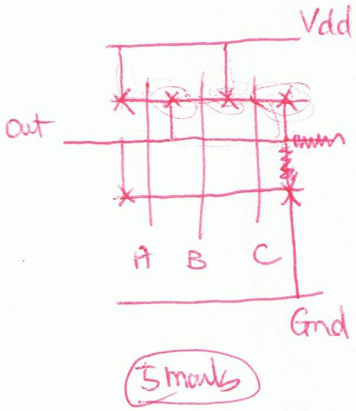


$40\lambda \times 48\lambda = 1920\lambda^2$

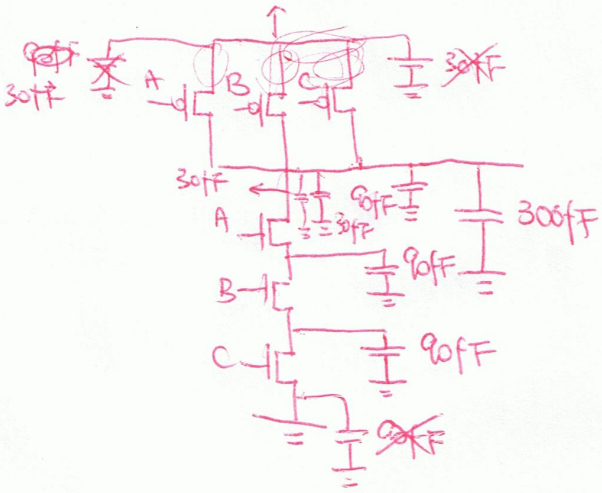
Q2:

Assume the on-resistance of a unit nMOS is 15Kohms and the on-resistance of a unit pMOS is 30Kohms. Also assume the drain, source, and gate capacitances of a unit transistor are all equal to 15fF. Using Elmore delay to calculate the delay of the gate when the input of the gate is transitioned from A=1, B=1, C=1 to A=1, B=1, C=0. ***Please assume diffusion sharing is always used to minimize layout area of the gate.*** (20 marks)
3





5 marks



caps right.

2.5 marks

Out of 7.5 marks
2.5 some sort of RC tree
5 wrong diffusion sharing
7.5 everything right

$\frac{15}{6} = \frac{5}{2} = 2.5$

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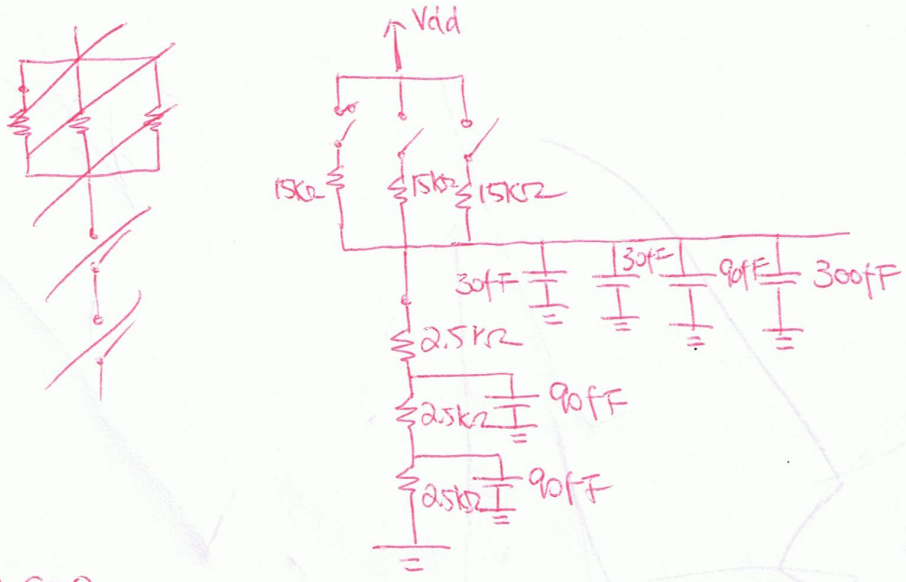
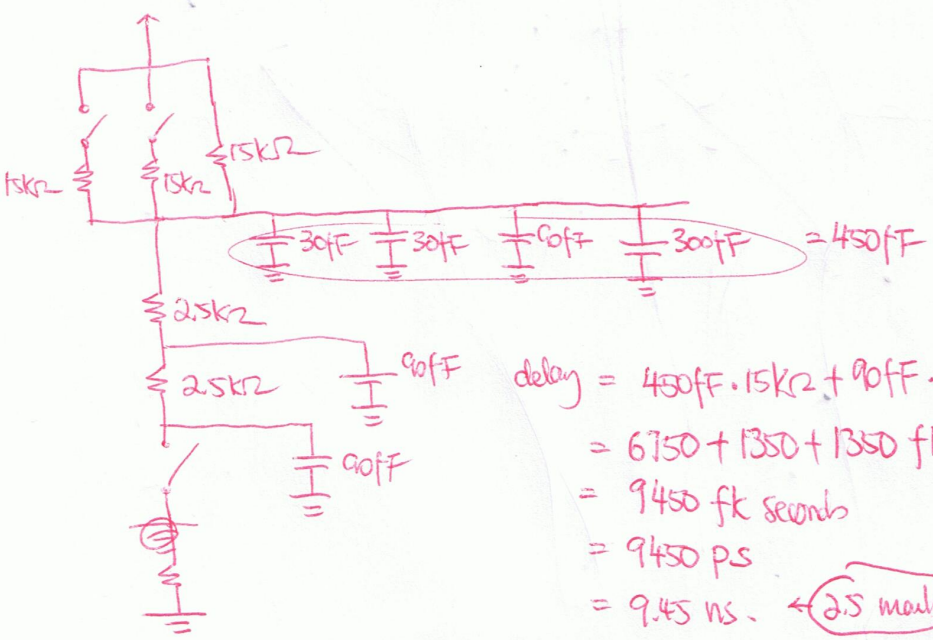
A=1 B=1 C=1



A=1 B=1 C=0



everything else right.

5 marks

delay = 450fF · 15kΩ + 90fF · 15kΩ + 90fF · 15kΩ (5 marks)

= 6750 + 1350 + 1350 fk seconds

= 9450 fk seconds

= 9450 ps

= 9.45 ns. ← 2.5 marks

5 marks RC tree

10 marks equation + RC tree

12.5 marks everything is right

8 marks equation + RC tree with mistakes

Q3:

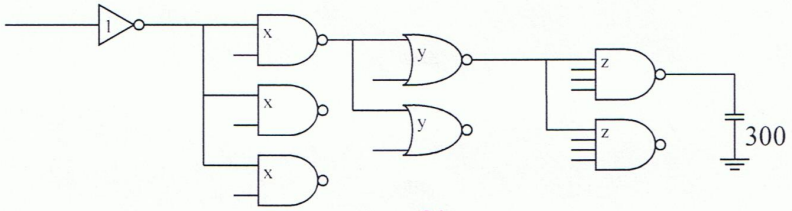
a) Calculate the optimum path delay for the following circuit and the value of x, y, and z in order to achieve the optimum delay. (inverter: g=1, p=1; 2-input nand: g=4/3, p=2; 2-input nor: g=5/3, p=2; 4-input nand: g=6/3, p=4). (8 marks)

b) Draw the transistor level diagram for the 2-input nor gate and clearly label the size of each transistor in the diagram. (3 marks)

c) Draw the transistor level diagram for the 4-input nand gate and clearly label the size of each transistor in the diagram. (3 marks)

d) Calculate the optimum path delay if additional inverter stages can be added between the 4-input nand gate and its load capacitance (2 marks).

e) How many additional stages should be added in part d) in order to achieve the optimum delay and what should be the size of each stage (4 marks).



a) F=GBH

G=logic effort

B=branch effort

H=electrical effort

$G = 1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot \frac{6}{3}$

$B = 3 \cdot 2 \cdot 2 \cdot 1$

$H = \frac{300}{1}$

$F = GBH$

$= 1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot \frac{6^2}{3^2} \cdot 3 \cdot 2 \cdot 2 \cdot 1 \cdot \frac{300}{1}$

$= 20 \cdot 4^3 \cdot 100$

$= 160 \cdot 100$

$= 16000$

$(F)^{1/4} = 11.247$ (1.5 marks)

$4 \cdot 11.247 + 1 + 2 + 2 + 4 = 53.988$ (1.5 marks)

11.247

$1 \cdot \frac{3x}{1} = 11.247$ (1.5 marks)

$x = 3.749$

$\frac{4}{3} \cdot \frac{2y}{3.749} = 11.247$ (1.5 marks)

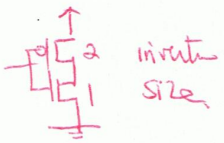
$y = 15.812$

$\frac{5}{3} \cdot \frac{2z}{15.812} = 11.247$ (1.5 marks)

$z = 53.351$

$\frac{6}{3} \cdot \frac{300}{53.351} = 11.246$ ✓ check

0.5 marks for effort



inverter size

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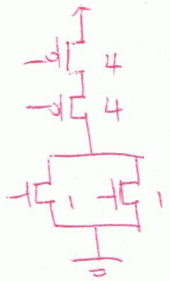
b) 15.812 units of unit inverter gate capacitance



$3C \Rightarrow 1$

$5C \Rightarrow \frac{5C}{3C} = 1.6$

$\frac{15.812 \times 3C}{5} = 9.4872C$

$9.4872 \times 4 = 37.9488C$ ok nmos

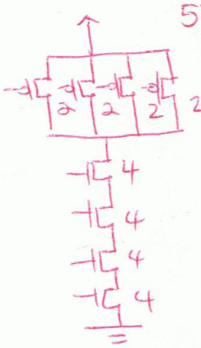
$\frac{9.4872C}{3C} = 3.1624$ ok pmos

$\frac{37.9488C}{3C} = 12.6496$

1.5 for pmos network

1.5 for nmos network.

c) 53.351 units of unit inverter gate capacitance.



1.5 for pmos network

1.5 for nmos network

$\frac{53.351 \times 3C}{6} = 26.6755C$

$26.6755C \cdot 4 = 106.702C$ ok nmos

$26.6755C \cdot 2 = 53.351C$ ok pmos

$\frac{106.702C}{3C} = 35.567$

$\frac{53.351C}{3C} = 17.784$ ~~17.837~~

d) $F = 16000$

$(F)^{1/N} = 3.59$

$(16000)^{1/N} = 3.59$

$N = \frac{\log(16000)}{\log(3.59)}$

$N = 7.57$ stages

$7 \cdot (16000)^{1/7} + 1 + 2 + 2 + 4 + 3 =$ ~~39.936~~ 39.905

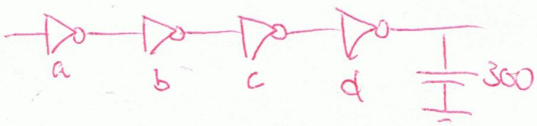
$8 \cdot (16000)^{1/8} + 1 + 2 + 2 + 4 + 4 =$ ~~40.354~~ 39.829 ✓

$N = 8$

optimal delay = 39.829 3RC delay.

(2 marks)

e) (4 stages) 1 mark $(16000)^{1/8} = 3.354$



$1 \cdot \frac{300}{d} = 3.354$

$d = 89.445$ (1 mark)

$1 \cdot \frac{89.445}{c} = 3.354$

$c = 26.669$ (1 mark)

$1 \cdot \frac{26.669}{b} = 3.354$

$b = 7.951$ (1 mark)

$1 \cdot \frac{7.951}{a} = 3.354$

$a = 2.371$

$\frac{6}{3} \cdot \frac{2.371}{z} = 3.354$

$z =$ ~~0.707~~ 1.4136

$\frac{5}{3} \cdot \frac{2 \cdot 1.4136}{y} = 3.354$ ~~0.707~~

$y =$ ~~0.703~~ 1.405

$\frac{4}{3} \cdot \frac{2 \cdot 1.405}{x} = 3.354$ ~~0.703~~

$x =$ ~~0.559~~ 1.117

$1 \cdot \frac{3 \cdot 1.117}{1} = 3.35$ ~~0.559~~ ✓