Faculty of Engineering and Architectural Science

Department of Electrical and Computer Engineering

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Course Title	Low Power Digital Integrated Circuits
Semester/Year	7th Semester, 4th Year
Lab No	2
Instructor Name	Andy Ye
Section No	3

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Due Date	10/25/2020

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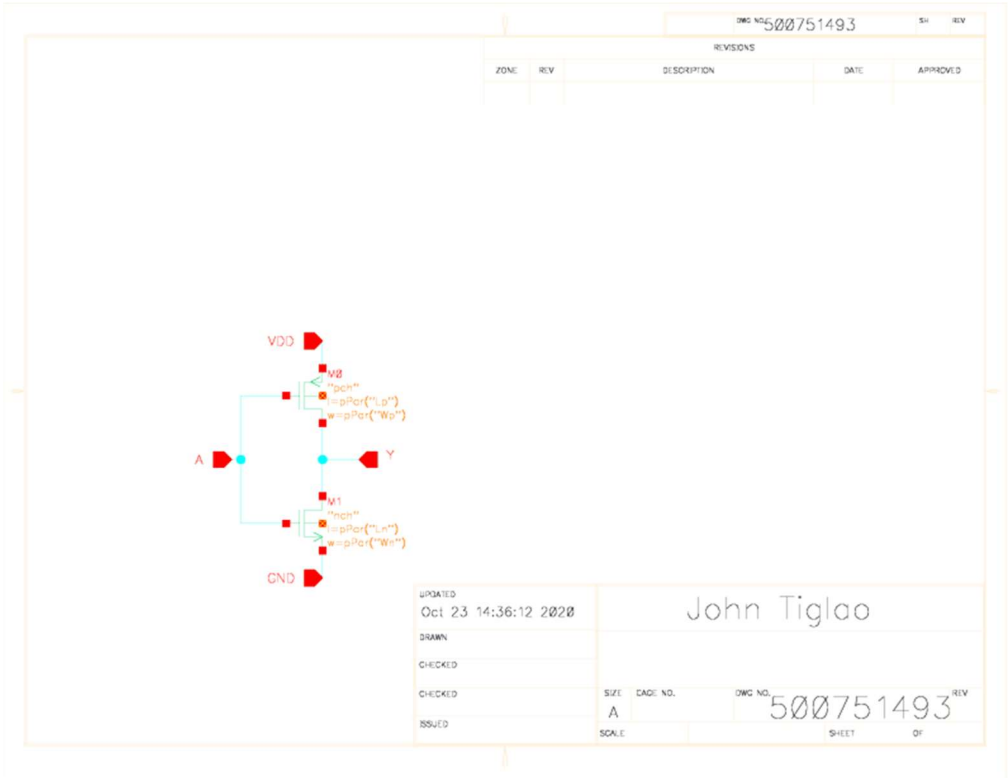
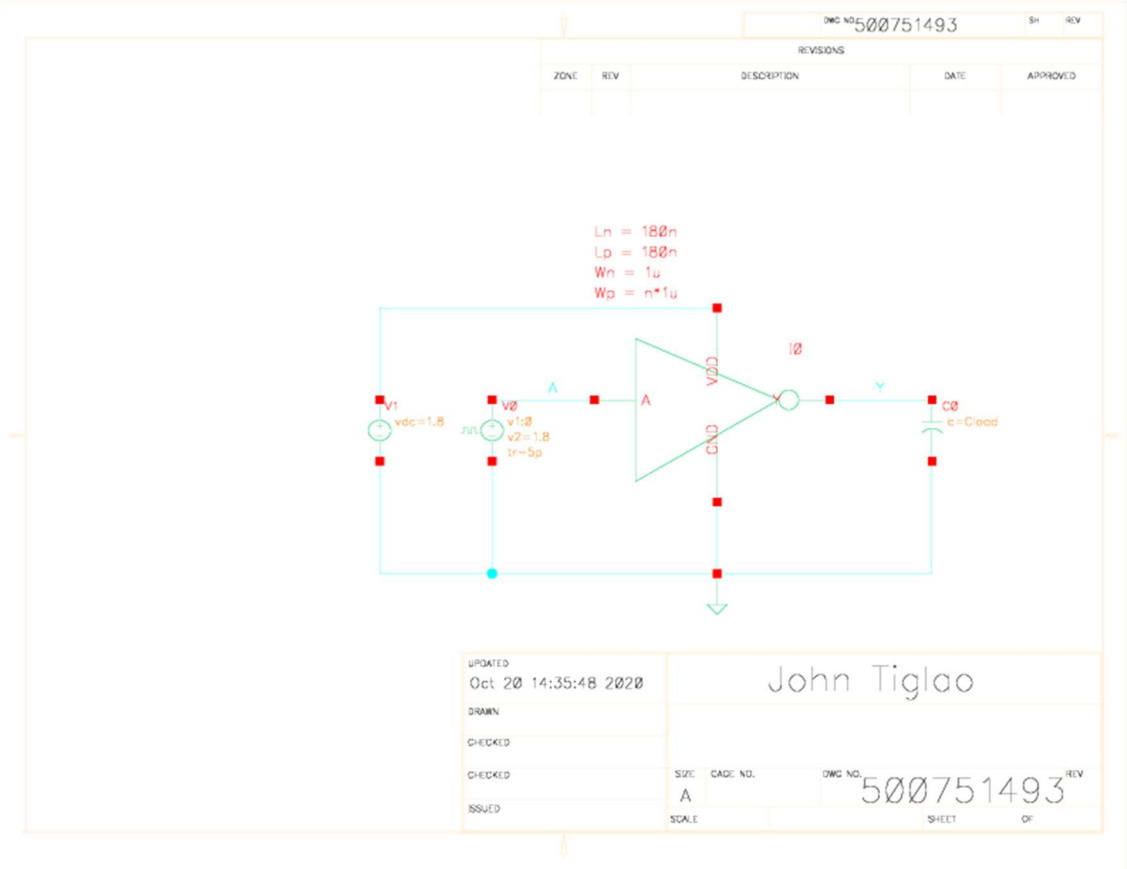
Introduction

The objective of this lab is to investigate the characteristics of the CMOS inverter. The static and dynamic behavior of the gate were looked into, and can be used to further explore logic gates, such as NAND, NOR, and XOR, or subsystems, such as adders and multipliers. DC analysis was first used to understand the static behavior and from it was able to obtain the transfer function, switching threshold, and the noise margin. Using transient analysis, the delay and load driving capability were also investigated. The layout of a CMOS inverter was also created and compared to the equal schematic-level through its static and dynamic results.

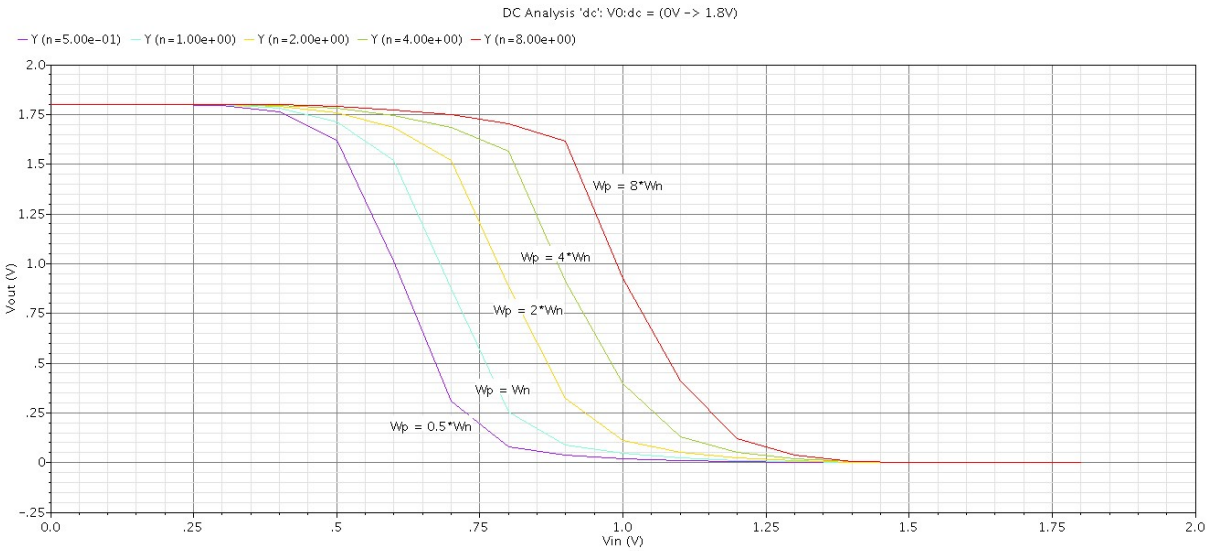
Schematic of CMOS Inverter



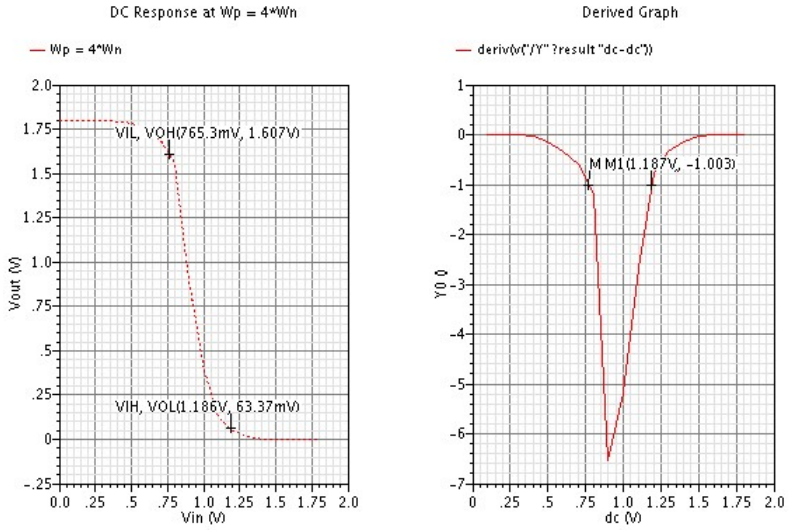
Schematic of Testbench



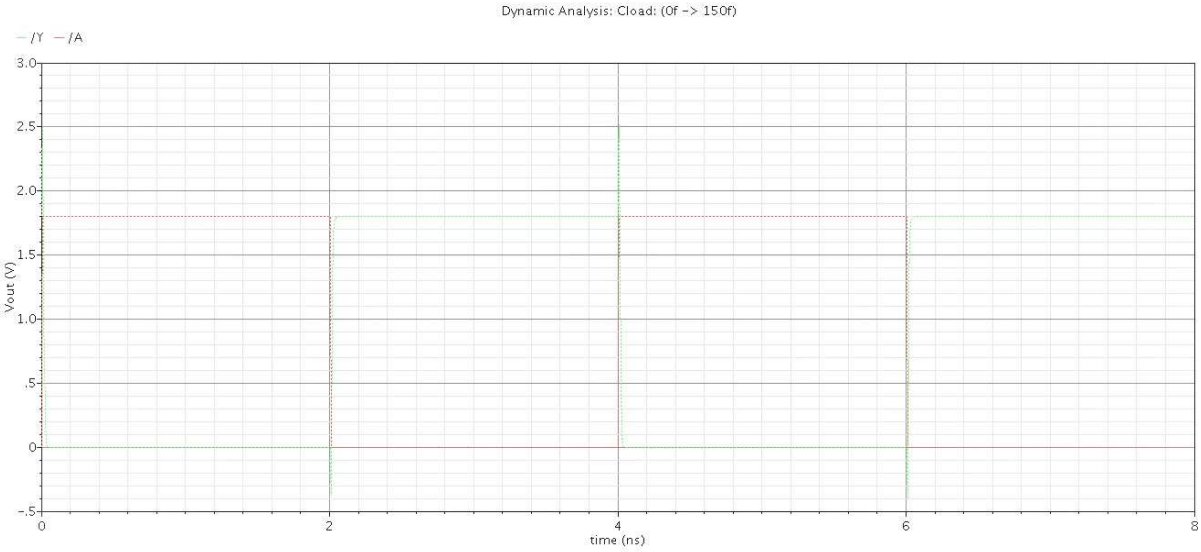
Static Analysis of CMOS Inverter, 0V -> 1.8V



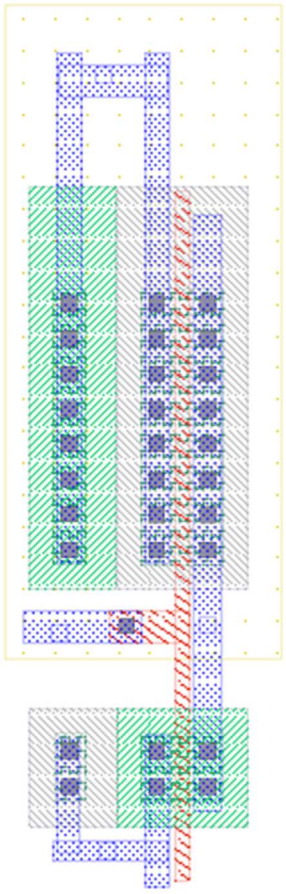
Static Analysis of CMOS Inverter, n = 4



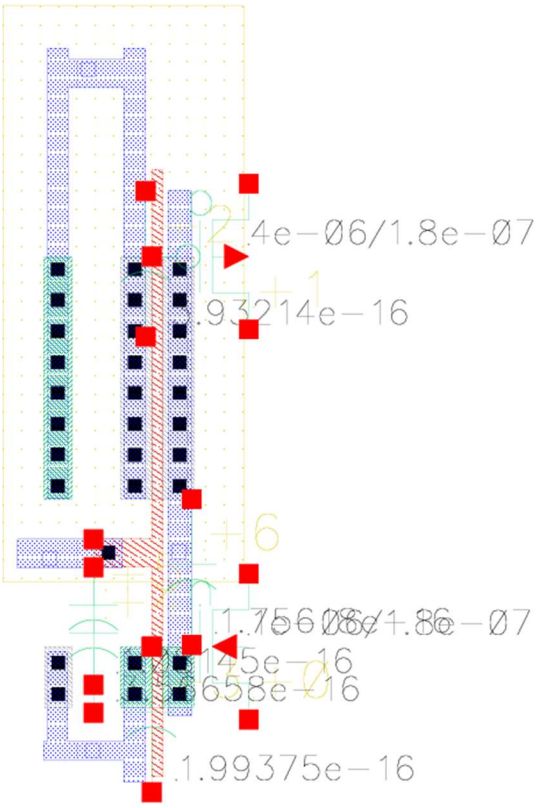
Dynamic Analysis of CMOS Inverter



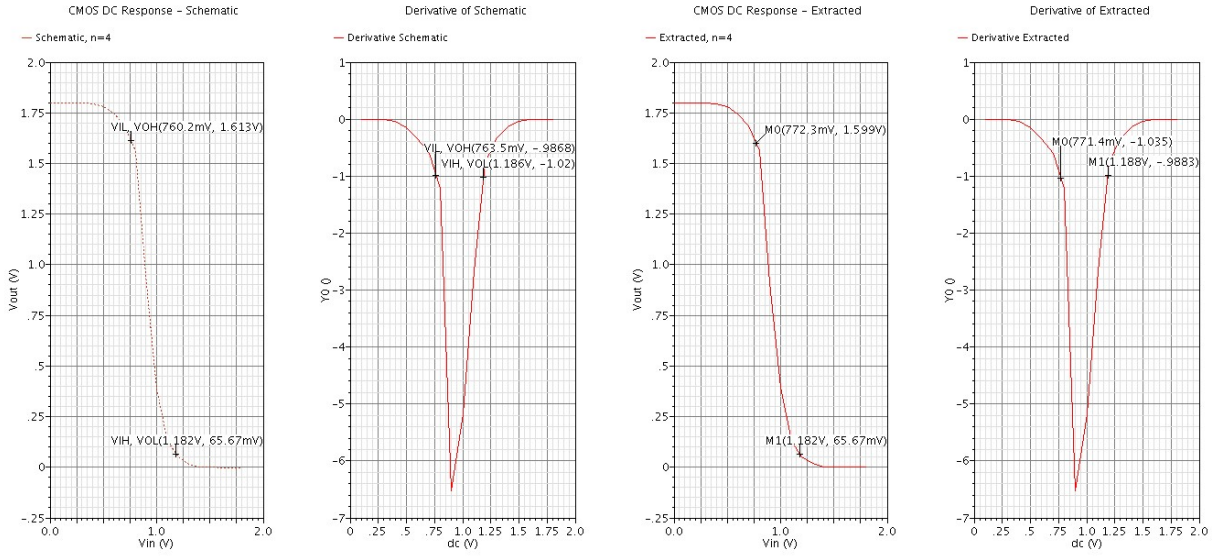
Physical View of CMOS Inverter Layout



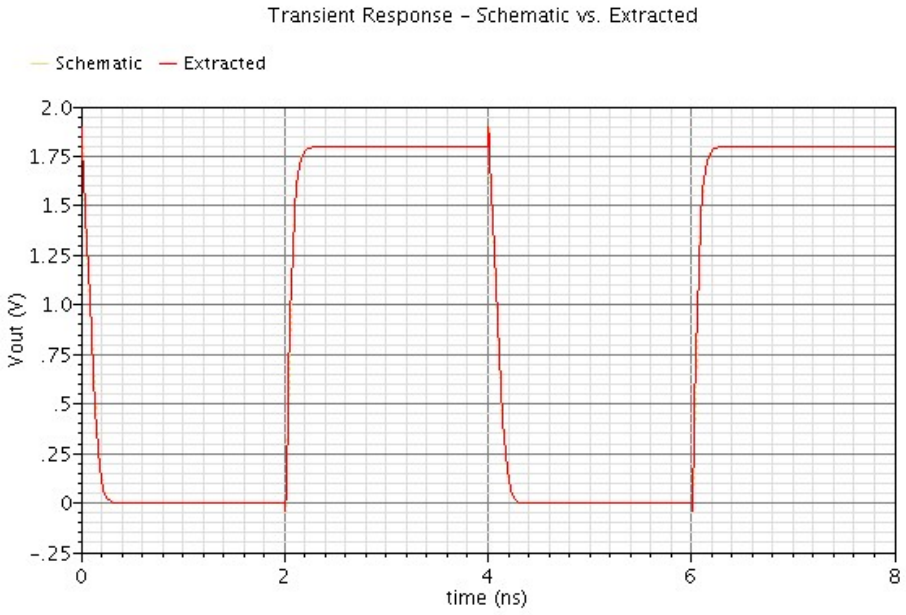
Extracted View of CMOS Inverter Layout



Static Analysis of Schematic vs. Extracted



Dynamic Analysis of Schematic vs. Extracted



Conclusion

In conclusion, this lab experiment studied different types of characteristics of a CMOS inverter, then further studied the layout of a CMOS inverter. The static and dynamic simulations were analyzed through different types of tools and analysis, Transient, DC, and Parametric analysis. From these analyses, a family of curves were created to find an ideal value for n (multiplier for the width of the PMOS). The ideal value for n was found to be 4 and used throughout the lab. The static analysis was used on this ideal value to create its DC response and find the VIL, VOH, VIH, and VOL of the graph by first obtaining the derivative of the graph. The dynamic simulation was investigated using transient analysis for a capacitance from 0f to 150f. The physical view for the CMOS inverter was created and used to create the extracted view. The extracted view had the same analyses applied from before with and had its static compared to the same CMOS schematic. The graph shows the two types of ways to obtain the static simulations, schematic and extracted, and had returned the same graphs. This was further proved through the dynamic simulation which also appeared completely identical. Sizing PMOS twice as wide as the NMOS did not result in VM = VDD/2 because of the delay. Increasing the PMOS size relative to NMOS will both increase VM and reduce the rise delay.