Ryerson University
Department of Electrical and Computer Engineering
ELE734: LOW-POWER DIGITAL INTEGRATED CIRCUITS
Mid-Term Examination, November 2015
Duration:1.5 hours

Student's Name: .....Solution.....

Student's Number: ..... **Section:** .....

NOTES:

1. This is a **Closed Book** examination. No aids other than the approved calculators and **1 page of aid-sheet** is allowed.
2. Answer all questions.
3. **No questions are to be asked** in the examination hall. If doubt exists as to the interpretation of any question, the student is urged to submit with the answer paper, a clear statement of any assumptions made.

Question No.	*Mark of each question*	*Mark obtained*
Q1	20	
Q2	20	
Q3	20	
Q4	20	
Total (Out of 80):		

15min

Q1:

Design a static CMOS gate that has the following output.

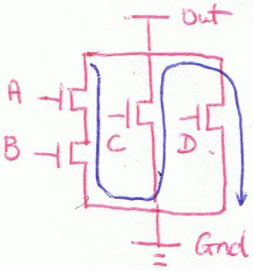
Out = !(AB+C+D)

a) Draw the transistor-level schematic of your design. Sizing is not required. (8 marks)

b) Draw stick diagram of the gate you designed (please clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (8 marks)

c) Estimate the area of the gate based on your stick diagram. (4 marks)

a) Pull down network



$\overline{Out} = \overline{AB+C+D}$

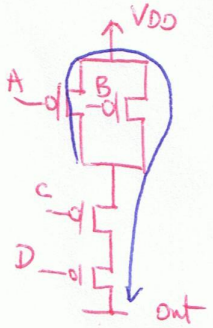
4marks

Pull up network

$\overline{Out} = \overline{AB+C+D}$

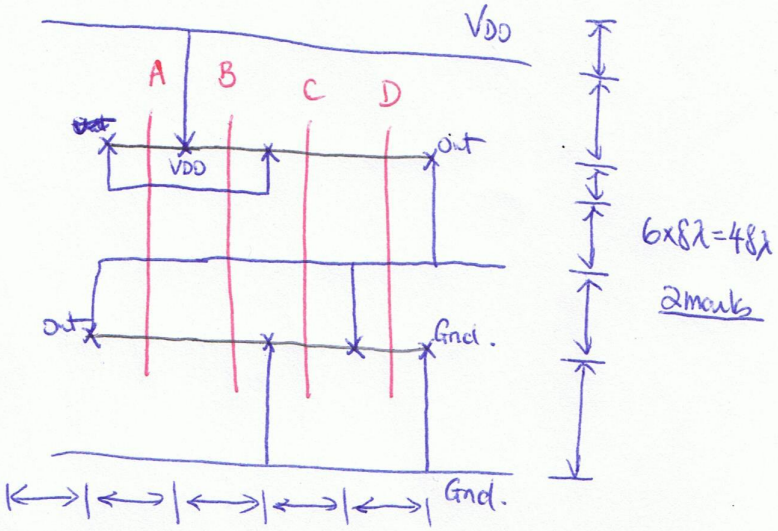
$= \overline{AB} \cdot \overline{C} \cdot \overline{D}$

$= (\overline{A}+\overline{B}) \cdot \overline{C} \cdot \overline{D}$



4marks

b) 4marks nmos network
4marks pmos network



2marks

$5 \times 8\lambda = 40\lambda$

2marks

c) Area = $48\lambda \times 40\lambda$

$= 1920\lambda^2$

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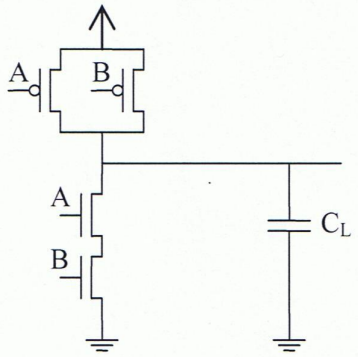
15min

Q2:

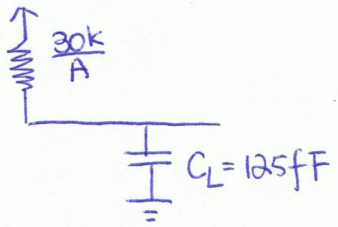
The on resistance of a unit nMOS is 15Kohms and the on resistance of a unit pMOS is 30Kohms. The following CMOS gate is driving a load (C_L) of 125fF.

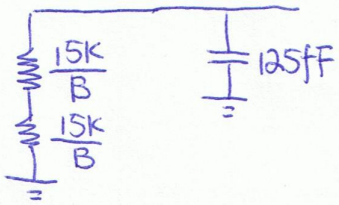
a) Assume the drain and source capacitance of each transistor is 0F. Size the gate to have a $t_{pdr} < 1900$ps and $t_{pdf} < 1600$ps. (10 marks)

b) Assume the drain, source, and gate capacitances of a unit transistor are all equal to 10fF, calculate the worst case pull-up and pull-down logic effort and the parasitic delay of the gate that you have just designed. (10 marks)



a)





$\frac{30k}{A} * 125fF < 1900ps$ 2.5 marks

$\frac{3750ps}{A} < 1900ps$

$\frac{3750ps}{1900ps} < A$

$A > 1.97$

$A = 2$ 2.5 marks

$\left(\frac{15k}{B} + \frac{15k}{B}\right) * 125fF < 1600ps$ 2.5 marks

$\frac{30k}{B} * 125fF < 1600ps$

$\frac{3750ps}{B} < 1600ps$

$\frac{3750ps}{1600ps} < B$

$B > 2.34$

$B = 3$ 2.5 marks

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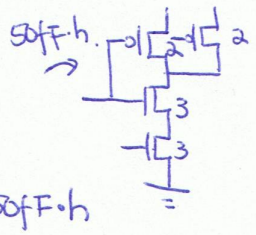
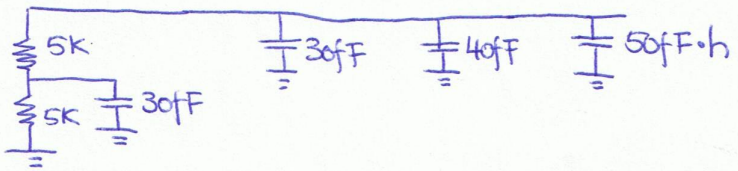
b) Worst case pull down logic eff.t

(1)



2 marks

(3)

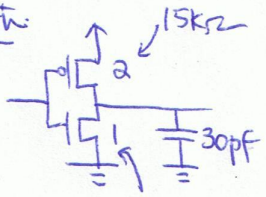


$t_{pdf} = 30fF \cdot 5K + 10k(30+40+50.h)fF$ 3marks

$= 150ps + 700ps + 500ps.h.$

$= 850ps + 500ps \cdot h$

(2) Unloaded invertr.



delay = 30pf · 15kΩ

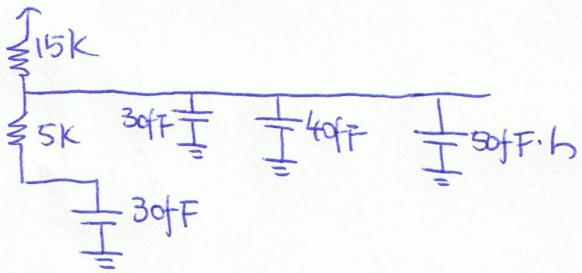
= 450ps

2marks

$df = \frac{850ps + 500ps \cdot h}{450ps} = 1.89 + 1.11h.$

Worst case pull up logic eff.t

(4)



$t_{pdr} = 30fF \cdot 15K + 15K(30fF + 40fF + 50fF.h)$ 3marks

$= 450ps + 1050ps + 750ps \cdot h$

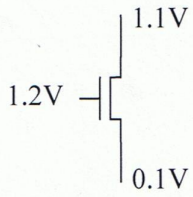
$= 1500ps + 750ps \cdot h.$

$dr = \frac{1500ps + 750ps \cdot h}{450ps} = 3.33 + 1.66h.$

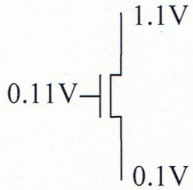
20 min

Q3: Assume V_t=0.3V, V_b=-0.1V, V_{dd}=1.2V.

a) Calculate I_{ds} for the following transistor using the Long-Channel model. (10 marks)



b) Calculate subthreshold current for the following transistor. (10 marks)



more than 0.3V

less than 0.3V

a) 1.2V

0.1V S D 1.1V

The transistor is in saturation — 4 marks

$$I_{ds} = \frac{\beta}{2} V_{GT}^2$$

$$= \frac{1048}{2}(1.2-0.1-0.3)^2$$

$$= \frac{1048}{2} 0.8^2$$

$$= 335.36\mu A.$$ — 6 marks

less than 0.3V.

G 0.11 less than 0.3V

b) 0.1 S D 1.1

The transistor is in cutoff — 4 marks

$$0.1\mu A\, 10^{\frac{0.01V + 100mV/V \cdot (1.0-1.2) - 0.083 \cdot 0.2V}{100mV/V}} \left(1-e^{\frac{-1.0}{26mV}}\right)$$

$$= 0.1\mu A\, 10^{\frac{0.01V - 20mV - 0.0166V}{100mV/V}} \left(1-e^{\frac{-1.0}{26mV}}\right)$$

$$= 0.1\mu A\, 10^{-0.266}\left(1-e^{-38.46}\right)$$

$$= 0.054\mu A$$ — 6 marks.

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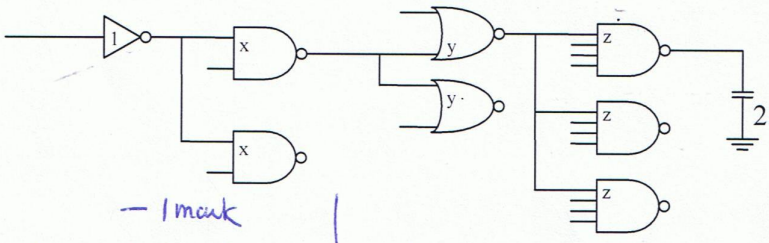
20 min

Q4:

a) Calculate the optimum path delay for the following circuit and the value of x, y, and z in order to achieve the optimum delay. (inverter: g=1, p=1; 2-input nand: g=4/3, p=2; 2-input nor: g=5/3, p=2; 4-input nand: g=6/3; p=4). (10 marks)

b) What will be the optimal delay if you can insert additional inverters at the end of the 4-input nand gate? Please also calculate the value of x, y, z, and the size of each additional inverter stage. (10 marks)



a) $H = \frac{250}{1} = 250$ — 1 mark

$G = 1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot \frac{6}{3} = 4.44$ — 1 mark

$B = 2 \cdot 2 \cdot 3 \cdot 1 = 12$. — 1 mark

$(GBH)^{1/4} = (4.44 \cdot 12 \cdot 250)^{1/4}$ — 1 mark

$= 10.746$.

$10.746 \times 4 + 1 + 2 + 2 + 4$ — 2 mark

$= 51.984$

$\frac{2 \cdot x}{1} = 10.746 \Rightarrow x = 5.373$ — 1 mark

$2 \cdot \frac{4}{3} \cdot \frac{y}{x} = 10.746 \Rightarrow y = 21.65$ — 1 mark

$3 \cdot \frac{5}{3} \cdot \frac{z}{y} = 10.746 \Rightarrow z = 46.53$ — 1 mark

$\frac{6}{3} \cdot \frac{250}{z} = 10.746 \Rightarrow 250 = 250$ ✓

1 mark for effort.

8 stages

$3.28 \times 8 + 1 + 2 + 2 + 4 + 4$

$= 39.24$

7 stages

$(13333.33)^{1/7} \times 7 + 1 + 2 + 2 + 4 +$

$= 39.18$

b) $(GBH)^{1/n} = (13333.33)^{1/n} = 3.59$ — 2 marks

$\log 3.59 = \frac{1}{n} \log (13333.33)$

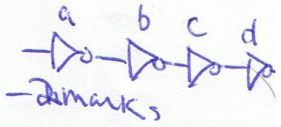
$n = \frac{\log (13333.33)}{\log 3.59}$

$n = 7.43$ stages — 1 mark

Version 1

$n \approx 8$ stages

$(GBH)^{1/8} = (13333.33)^{1/8} = 3.28$



— 2 marks

$2 \cdot \frac{x}{1} = 3.28 \Rightarrow x = 1.64$

$2 \cdot \frac{4}{3} \cdot \frac{y}{x} = 3.28 \Rightarrow y = 2.017$ — 1 mark

$3 \cdot \frac{5}{3} \cdot \frac{z}{y} = 3.28 \Rightarrow z = 1.323$

$\frac{6}{3} \cdot \frac{a}{z} = 3.28 \Rightarrow a = 2.17$ — 1 mark

$1 \cdot \frac{b}{a} = 3.28 \Rightarrow b = 7.18$ — 1 mark

$1 \cdot \frac{c}{b} = 3.28 \Rightarrow c = 23.35$ — 1 mark

$1 \cdot \frac{d}{c} = 3.28 \Rightarrow d = 76.57$ — 1 mark

$1 \cdot \frac{250}{d} = 3.28 \Rightarrow 250 \approx 257$ check ✓

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Version 2 7 stages

$(GBH)^{\frac{1}{7}} = (13333.33)^{\frac{1}{7}} = 3.88398$ — 2 marks

$2 \cdot \frac{x}{1} = 3.88 \Rightarrow x = 1.94$

$2 \cdot \frac{4}{3} \cdot \frac{y}{x} = 3.88 \Rightarrow y = 2.82$

$3 \cdot \frac{5}{3} \cdot \frac{z}{y} = 3.88 \Rightarrow z = 2.197$

— 1 mark

$\frac{6}{3} \cdot \frac{a}{z} = 3.88 \Rightarrow a = 4.2567$ — 1 mark

$1 \cdot \frac{b}{a} = 3.88 \Rightarrow b = 16.57$ — 1 mark

$1 \cdot \frac{c}{b} = 3.88 \Rightarrow c = 64.367$ — 1 mark

$1 \cdot \frac{250}{c} = 3.88 \Rightarrow 250 \approx 250$

1 mark for eqn

Formulae and Constants

$$\beta = 1048 \mu A / V^2$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & Cutoff \\ \beta(V_{GT} - V_{ds}/2)V_{ds} & V_{ds} < V_{dsat} & Linear \\ \frac{\beta}{2} V_{GT}^2 & V_{ds} > V_{dsat} & Saturation \end{cases}$$

$$\eta = 100 mV / V$$
$$k_\lambda = 0.083$$
$$S = 100 mV / V$$
$$v_T = 26 mV$$
$$I_{off} = 0.1 \mu A$$

$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k_\lambda V_{sb}}{S}} (1 - e^{\frac{-V_{ds}}{v_T}})$$