Gates (Elmore Delay)

October 28, 2020 12:47 PM

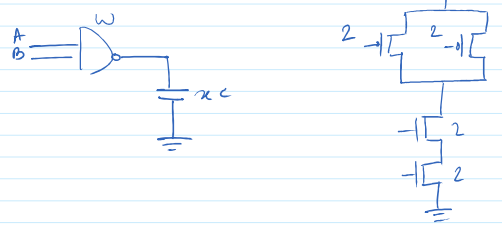
TABLE 4.2 Logical effort of common gates

Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
tristate, multiplexer	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

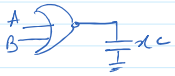
TABLE 4.3 Parasitic delay of common gates

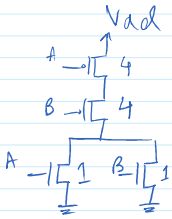
Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		2	3	4	*n*
NOR		2	3	4	*n*
tristate, multiplexer	2	4	6	8	$2n$
XOR, XNOR		8	12	16	$4n$

2-input NAND

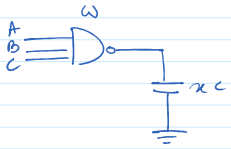


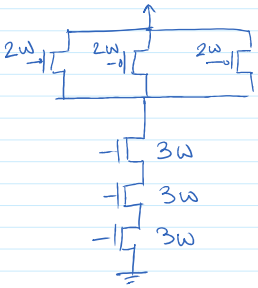
2-input NOR



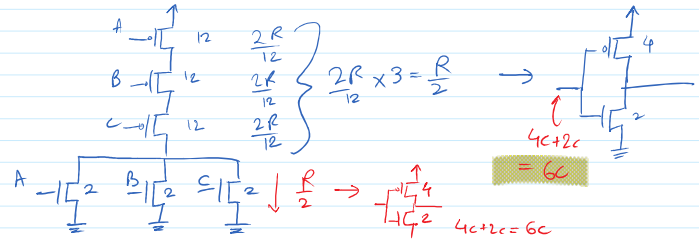


3-input NAND

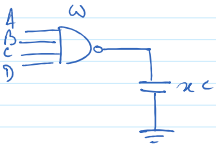


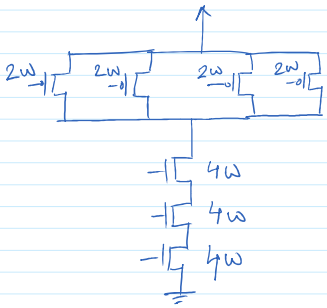


3-input NOR



4-input NAND





4-input NOR