Arm Architecture (Part 2)

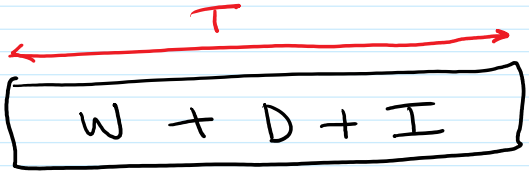
September 21, 2020 4:32 PM

- Basic concept of pipelining

What is pipelining?

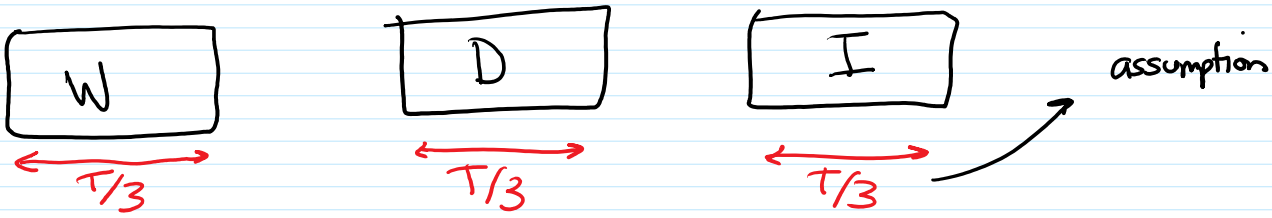
- a mechanism for overlapped execution of several input sets
  - ↳ partition some computations into a set of k sub-computations
    - nominal increase in cost of implementation
    - very significant speed up (ideally k)

A real-life example.



for $N \Rightarrow T_{total} = N \cdot T$

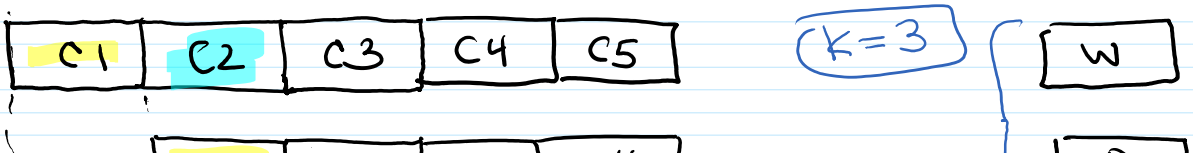
- Wash some clothes
- single machine does Wash, Dry and Iron.

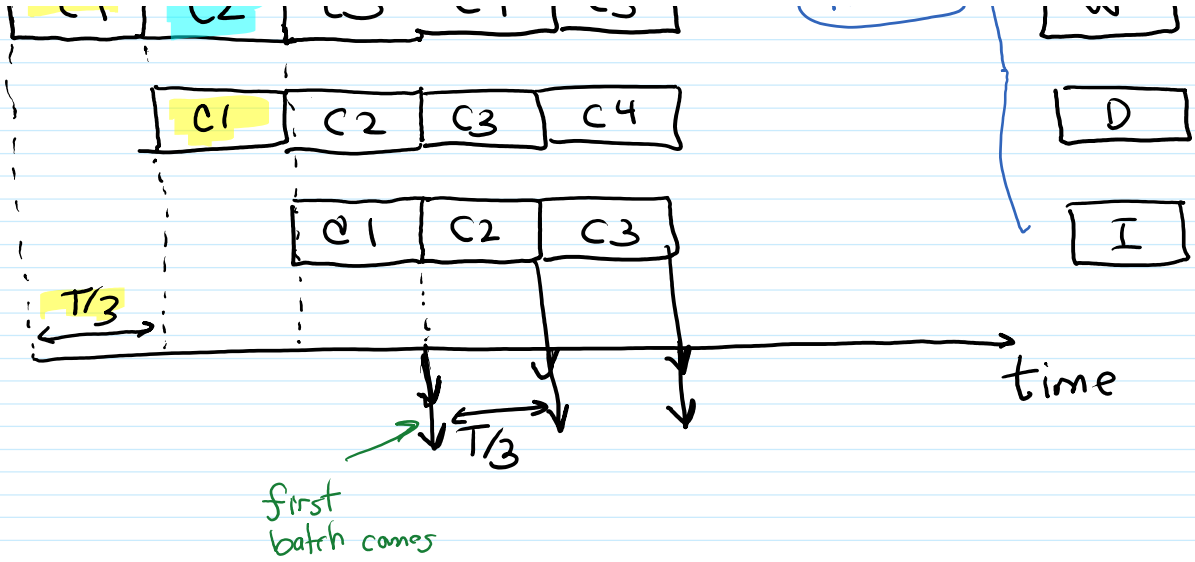


- As an alternative, we split machine into 3 smaller machines
- If we each sub-machine takes $T/3$ time, then

$$T_{total} = (2+N)\frac{T}{3} \simeq \frac{NT}{3} \quad \text{if } N \to \infty$$

Details of Pipelining





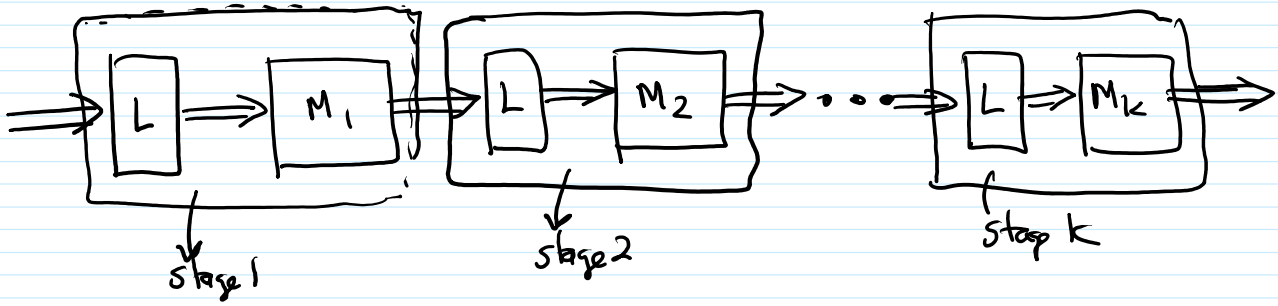
Extending Cocept to Processor Pipelining

- The same concept can be extended to processor pipelining
- If you want to increase speed by k

  Alternative 1: Replicate hardware k-times

  Alternative 2: Split the computations to k stages.

- Need for buffering
  - In hardware pipelining, we need a latch btw successive stages to hold intermediate results.



Calculations: Speed up and Efficiency

Some notations

τ → clock period of the pipeline

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t_i → delay of stage S_i

d_L → delay of the latch.

Maximum delay

$$\tau_m = \max\{t_i\}$$

$$\tau = \tau_m + d_L$$

pipeline freq $= 1/\tau$

Total time to process N data points (pipelined)

$$T_k = [(k-1) + N]\,\tau$$

$$= (k-1)\tau + N\tau$$

Equivalent non-pipelined processor:

$T_{np} = N k \tau$ (ignoring latch delays)

↳ assume time is k times larger

Speed-up of k-stages over equivalent non-pipelined processor.

$$S_k = \frac{T_{np}}{T_k} = \frac{Nk\tau}{N\tau + (k-1)\tau} = \frac{Nk}{N + (k-1)}$$

$$\approx \frac{Nk}{N} \approx k$$

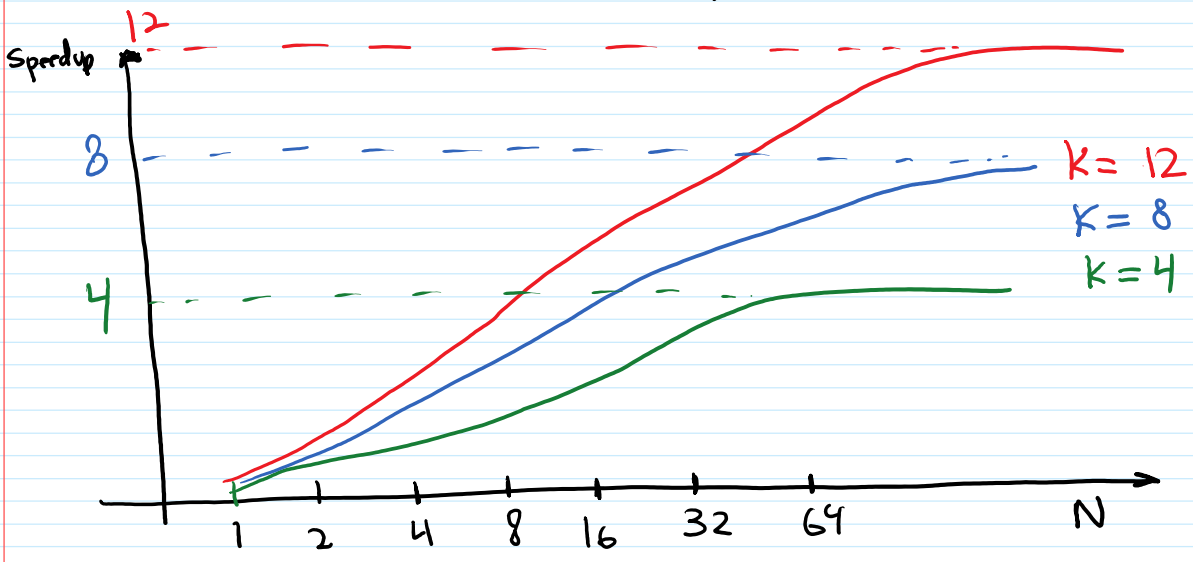
- Pipeline efficiency:

  ↳ How close is the performance to its ideal?

$$E_k = \frac{S_k}{k} = \frac{N}{N+(k-1)}$$

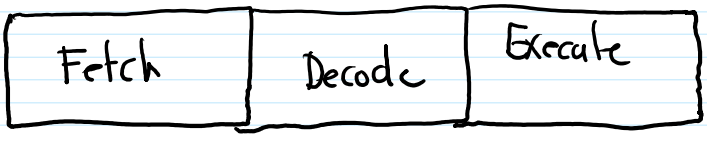
- Pipeline throughput
  - ↳ Number of operations completed per unit of time

$$H_k = \frac{N}{T_k} = \frac{N}{[(k-1)+N]\tau}$$

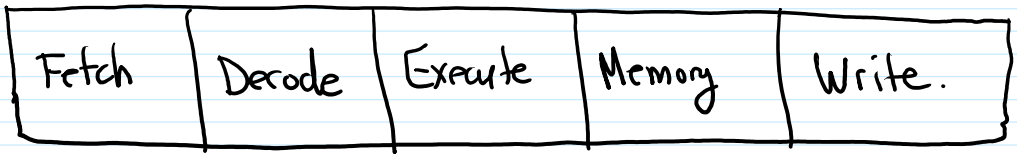


ARM pipelining Example

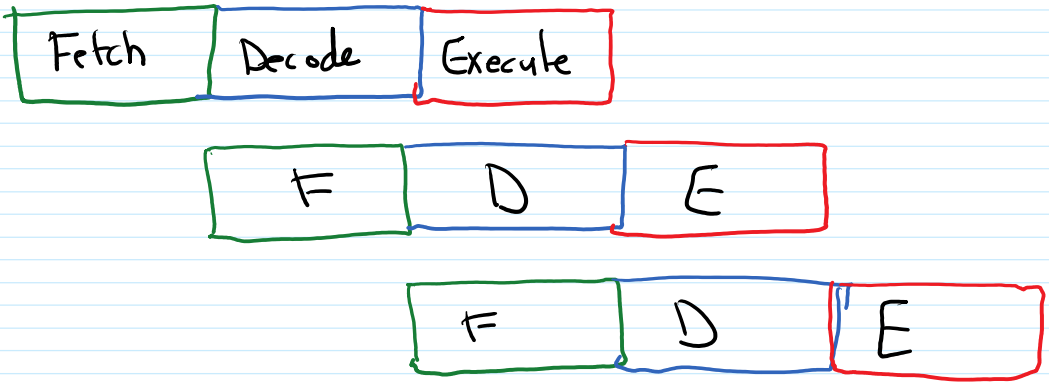
ARM7-TDMI



ARM9-TDMI



Pipelining in ARM7



Example of ARM variable cycle execution