Q1:

Design a static CMOS gate that has the following output.

$$Out = !((A+B)*C*D)$$

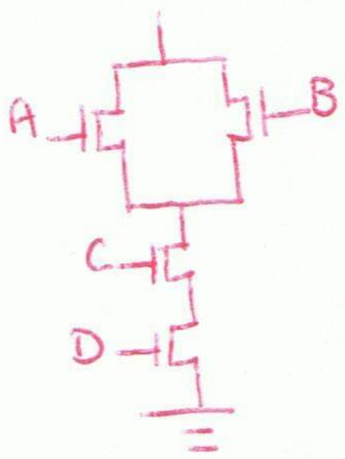
a) Draw the transistor-level schematic of your design. Sizing is not required. (8 marks)

b) Draw stick diagram of the gate that you have designed (***please minimize layout area by maximizing diffusion sharing***** and clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (8 marks)

c) Estimate the area of the gate based on your stick diagram. (4 marks)

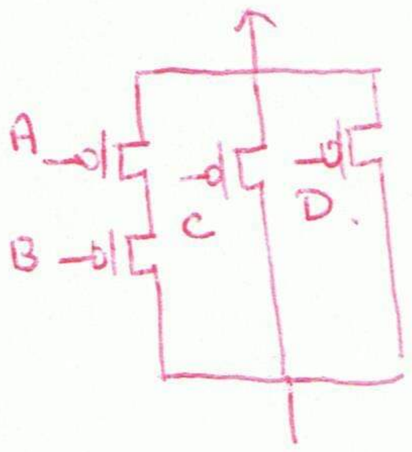
$\overline{(A+B)\cdot C\cdot D} = (\overline{A+B})+\overline{C}+\overline{D} = (\overline{A}\cdot\overline{B})+\overline{C}+\overline{D}$

Pull down



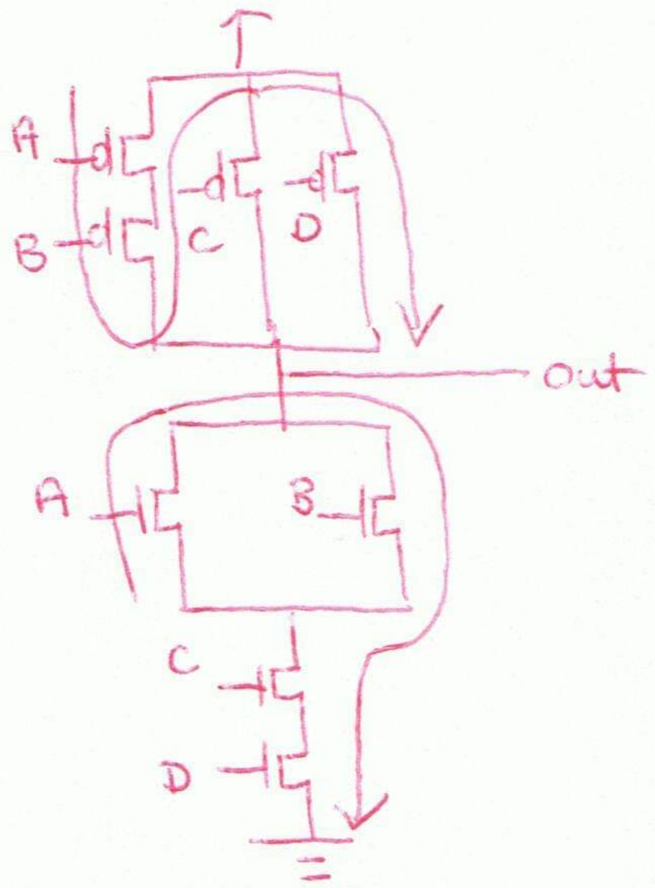
4 marks

Pull up



4 marks

Total Cicut



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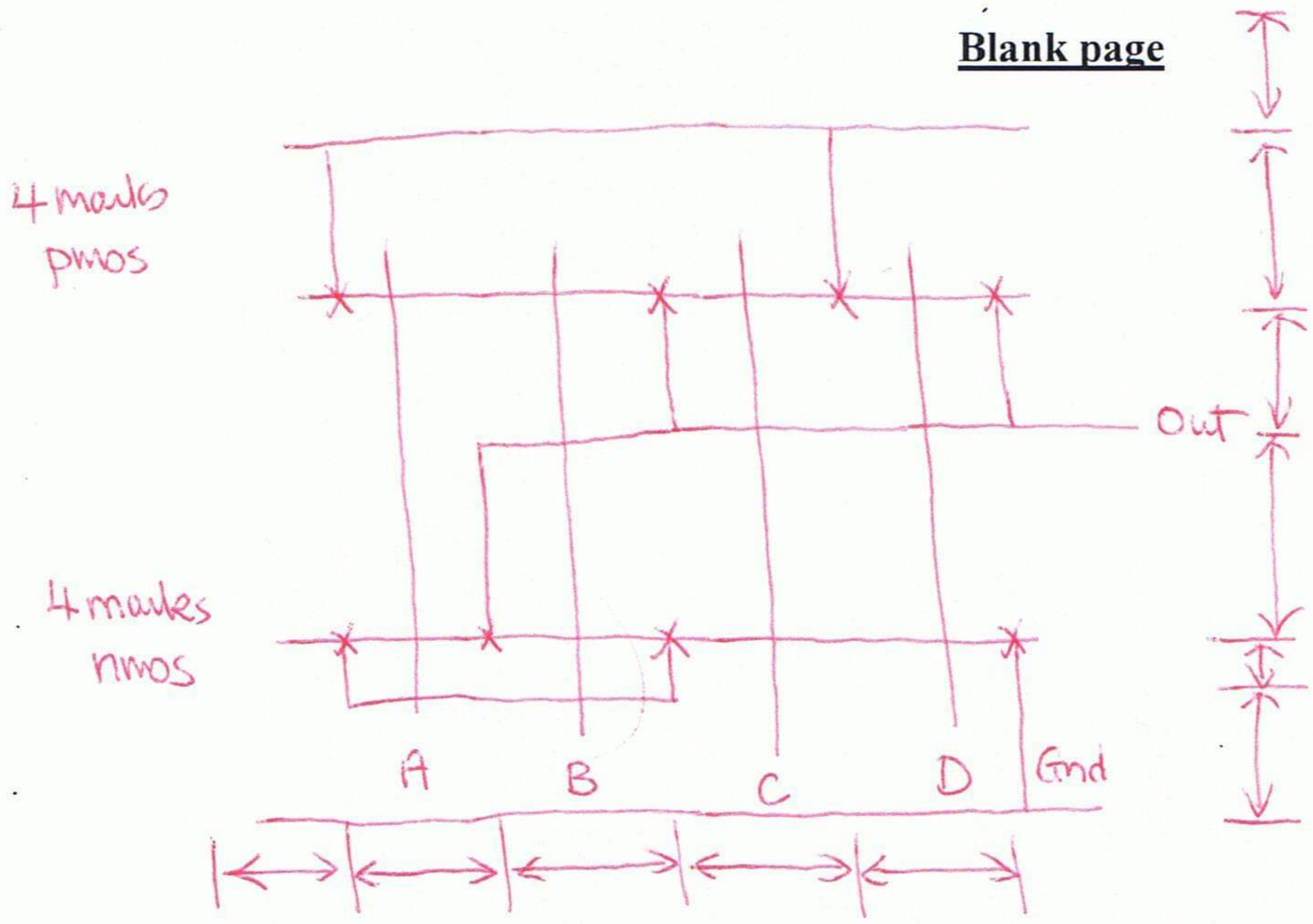


6 tracks x 8λ each
= 48λ

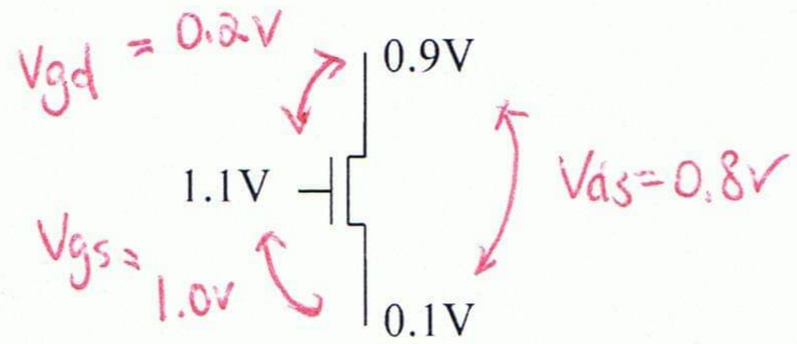
2 marks

5 tracks x 8λ each
= 40λ

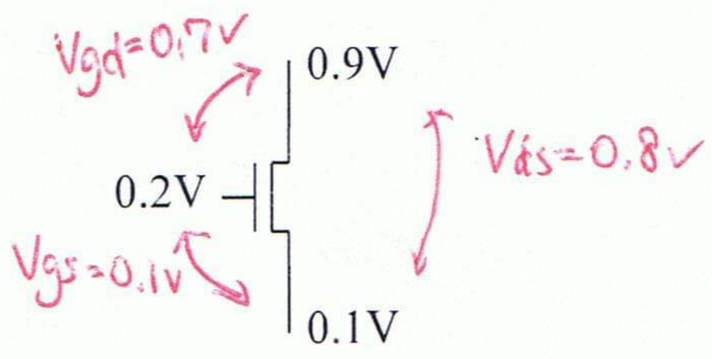
2 marks

Q2: Assume V_t=0.3V, V_{sb}=-0.1V, V_{dd}=1.2V.

a) Calculate I_{ds} for the following transistor using the Long-Channel model. (5 marks)



b) Calculate subthreshold current for the following transistor. (5 marks)



c) What should be the value of V_{sb} if one needs to reduce the subthreshold current to 20% of the value calculated in part (b) by changing the body voltage? (5 marks)

d) What will be the impact on the performance of the transistor shown in part (a) if V_{sb} is changed to the value calculated from part (c)? (5 marks)

a) $I_{ds} = 1048\,\mu A/V^2 \cdot (1.0 - 0.3)^2\,V^2 \cdot \frac{1}{2}$ 5 marks

$= \frac{513.53\,\mu A}{2} = 256.76\,\mu A$.

b) $I_{ds} = 0.1\mu A\ 10^{\frac{0.1 + 100\,mV/V\,(0.8-1.2) - 0.083(-0.1)}{100\,mV/V}} \left(1 - e^{\frac{-0.8}{36mV}}\right)$

$= 0.1\mu A\ 10^{\frac{0.1 - 0.04 + 0.0083}{0.1}} \left(1 - e^{\frac{-0.8}{0.026}}\right)$

$= 0.1\mu A\ 10^{0.683} \left(1 - e^{-30.77}\right)$

$= 0.1\mu A \cdot 4.819 \left(1 - 4.33 \times 10^{-14}\right)$

$= 0.482\,\mu A$

5 marks.

c) $I_{ds} = I_{off}\, 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd})}{S}}\, 10^{\frac{-K_\lambda V_{sb}}{S}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right)$

$10^{\frac{-K_\lambda(-0.1)}{S}} \cdot 0.2 = 10^{\frac{-K_\lambda(V_{sb})}{S}}$

$10^{\frac{0.083 \cdot 0.1}{0.1}} \cdot 0.2 = 10^{\frac{-0.083(V_{sb})}{0.1}}$ 5 marks

$0.242 = 10^{\frac{-0.083(V_{sb})}{0.1}}$

$-0.616 = -\frac{0.083(V_{sb})}{0.1}$

$V_{sb} = 0.74$ volts.

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d) $0.3 = V_{to} + 0.16(\sqrt{0.93-0.1} - \sqrt{0.93})$

$0.3 = V_{to} + 0.16(0.911 - 0.964)$

$0.3 = V_{to} + (-0.00848)$

$V_{to} = 0.30848$.

$V_t = 0.30848 + 0.16(\sqrt{0.93+0.74} - \sqrt{0.93})$

$= 0.30848 + 0.16(\sqrt{1.67} - \sqrt{0.93})$

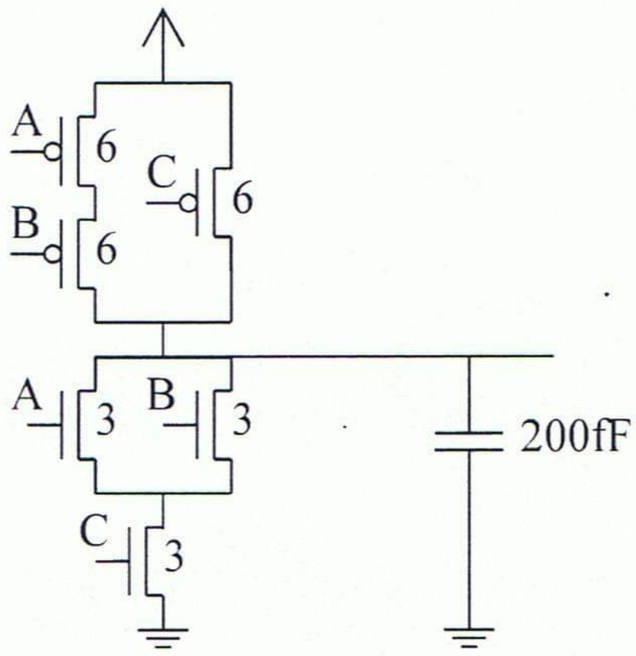
$= 0.30848 + 0.16 \cdot 0.328$

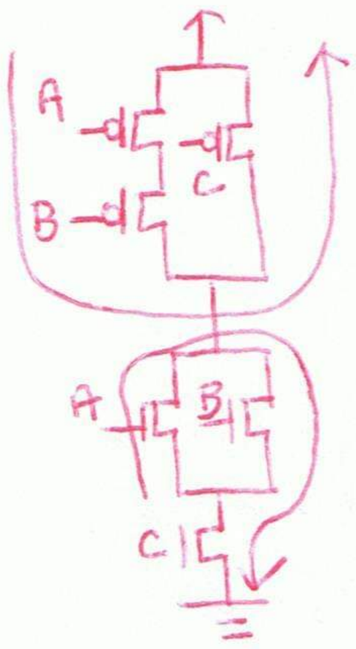
$= 0.361$

Performance penalty $\Rightarrow \dfrac{\frac{\beta}{2}(1.0-0.361)^2}{\frac{\beta}{2}(1.0-0.3)^2} = 0.833 = 83\%$ performance.

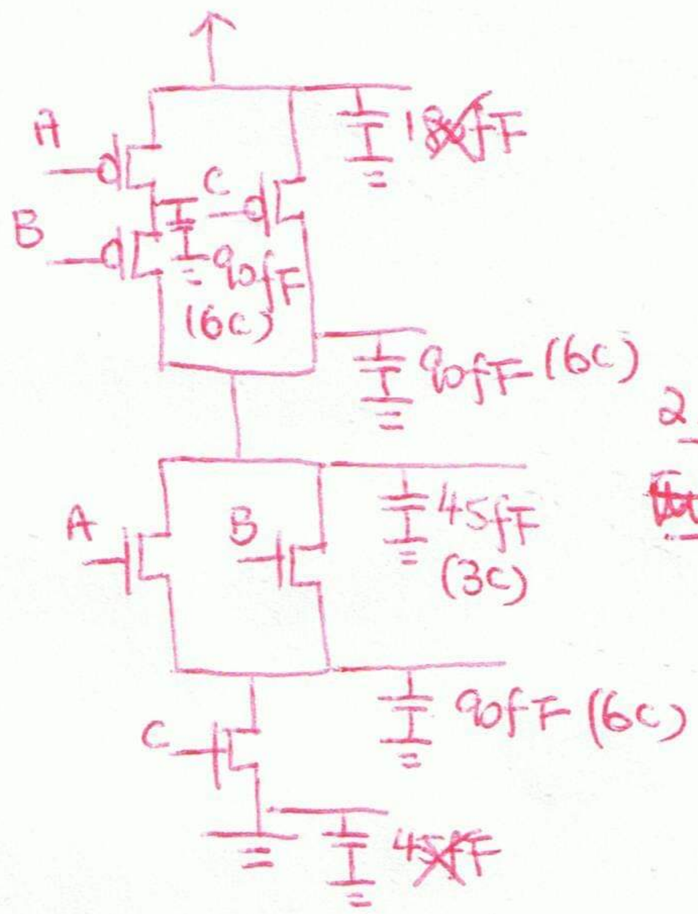
Q3:

Assume the on-resistance of a unit nMOS is 15Kohms and the on-resistance of a unit pMOS is 30Kohms. Also assume the drain, source, and gate capacitances of a unit transistor are all equal to 15fF. Using Elmore delay to calculate the delay of the gate when the input of the gate is transitioned from A=1, B=0, C=1 to A=1, B=0, C=0. ***Please assume diffusion sharing is always used to minimize layout area of the gate.*** (20 marks)



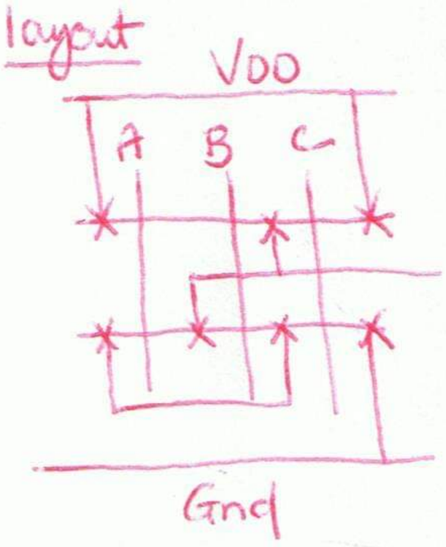


5marks



2.5 marks

layout



out of 7.5 marks
2.5 some sort of RC tree
5 wrong diffusion sharing
7.5 everything right

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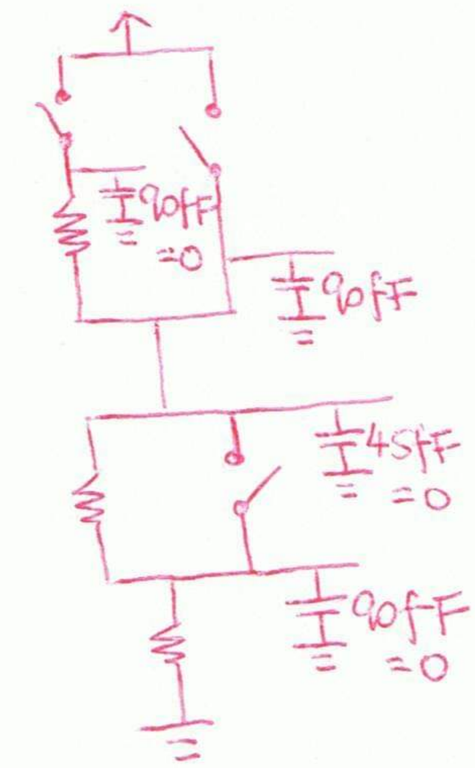
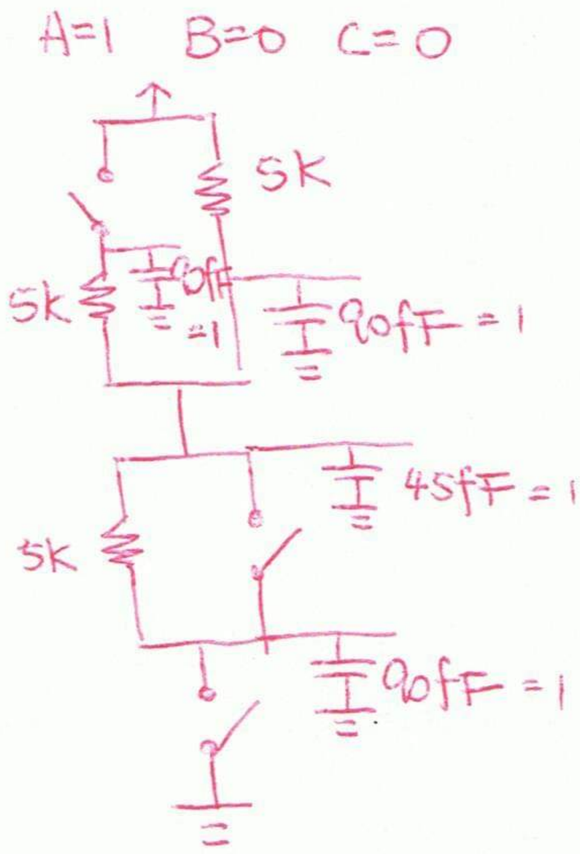
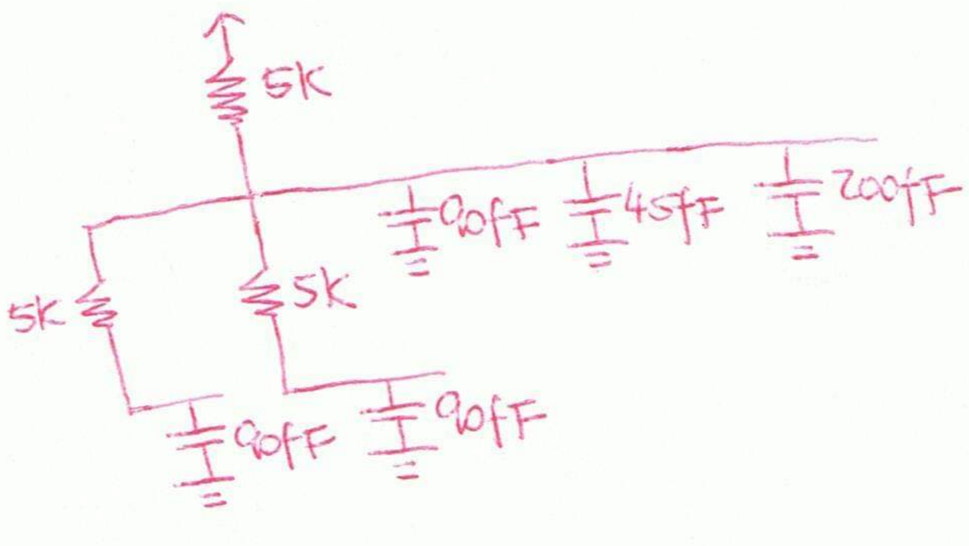






5 marks

delay = (90+45+200)fF·5K + 90fF·5K + 90fF·5K 5 marks

= (90+45+200+90+90)fF·5K

= 515fF·5K.

= 2575ps

= 2.575ns.

~~5 marks~~

2.5 marks

5 marks RC tree
10 marks equation + RC tree
12.5 marks everything correct

8 marks equation + RC tree with mistakes

Q4:

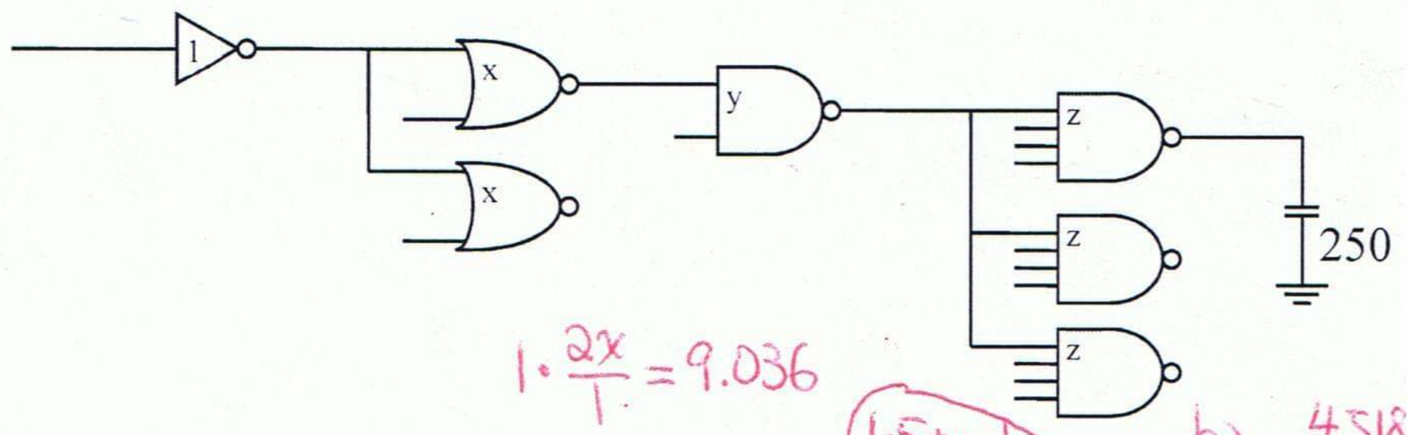
a) Calculate the optimum path delay for the following circuit and the value of x, y, and z in order to achieve the optimum delay. (inverter: g=1, p=1; 2-input nor: g=5/3, p=2; 2-input nand: g=4/3, p=2; ; 4-input nand: g=6/3, p=4). (8 marks)

b) Draw the transistor level diagram for the 2-input nor gate and clearly label the size of each transistor in the diagram. (3 marks)

c) Draw the transistor level diagram for the 4-input nand gate and clearly label the size of each transistor in the diagram. (3 marks)

d) Calculate the optimum path delay if additional inverter stages can be added between the 4-input nand gate and its load capacitance (2 marks).

e) How many additional stages should be added in part d) in order to achieve the optimum delay and what should be the size of each stage (4 marks).



a)

F = GBH

G = logic effort

B = branch effort

H = electrical effort

$G = 1 \cdot \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{6}{3}$

$B = 2 \cdot 1 \cdot 3 \cdot 1$

$H = \frac{250}{1}$

$F = GBH$

$= 1 \cdot \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{6}{3}^2 \cdot 2 \cdot 1 \cdot 3 \cdot 1 \cdot \frac{250}{1}$

$= \frac{20000}{3}$

$= 6666.67$

0.5 for effort

$(F)^{1/4} = 9.036$ (1.5 marks)

$4 \cdot 9.036 + 1 + 2 + 2 + 4 = 45.144$ (1.5 marks)

$1 \cdot \frac{2x}{1} = 9.036$ (1.5 marks)

$x = 4.518$

$\frac{5}{3} \cdot \frac{y}{4.518} = 9.036$ (1.5 marks)

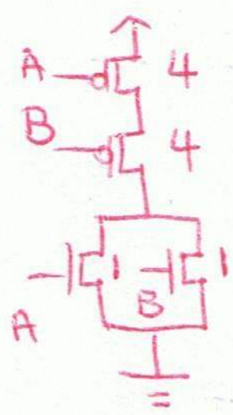
$y = 24.49$

$\frac{4}{3} \frac{3z}{24.49} = 9.036$ (1.5 marks)

$z = 55.32$

$\frac{6}{3} \frac{250}{55.32} = 9.038$ ✓

b) 4.518 units of unit inverter gate capacitance.



3C ⇒ 1

5C ⇒ $\frac{5C}{3C} = 1.67$

$\frac{4.518 \cdot 3C}{5} = 2.7108C$

$4 \times 2.7108 = 10.84C$

$\frac{2.7108C}{3C} = 0.904$ check

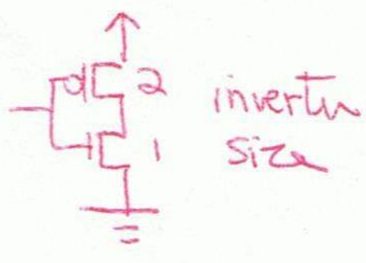
$\frac{10.84C}{3C} = 3.613$ check.

ok. nmos

ok. pmos

1.5 for pmos network

1.5 for nmos network.



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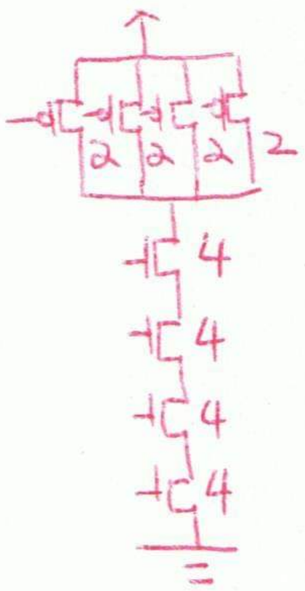
c)



$Z = 55.32$ units of unit inverter gate capacitance

$\frac{55.32 \cdot 3C}{6} \cdot 2 = 55.32C$ ok nmos

$\frac{55.32 \cdot 3C}{6} \cdot 4 = 110.64C$ ok pmos

$\frac{55.32C}{3C} = 18.44$ check

$\frac{110.64C}{3C} = 36.88$ check

(1.5 for pmos network)

(1.5 for nmos network)

d)

$F = GBH$

$= 666667$

$(F)^{1/N} = 3.59$

$(6666.67)^{1/N} = 3.59$

$N = \frac{\log(6666.67)}{\log(3.59)}$

$= 6.89$

$N = 7.$

$(6666.67)^{1/6} \cdot 6 + 1+2+2+4+2 = 37.03$

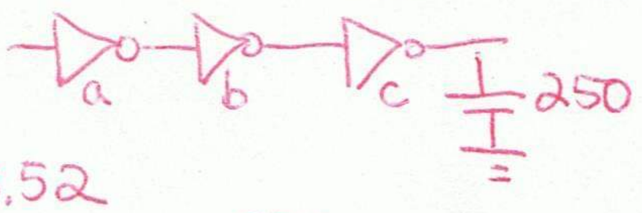
$(6666.67)^{1/7} * 7 + 1+2+2+4+3 = 33.11$ ✓

Optimal delay = 36.63

(2 marks)

$(6666.67)^{1/7} = 3.52$.
3.5178

(1 mark) 3 stages



$1 \cdot \frac{250}{C} = 3.52$

$C = \frac{250}{3.52} = 71.02$ (1 mark)
71.071

$1 \cdot \frac{71.02}{b} = 3.52$ (1 mark)

$b = 20.18$
20.1895

$1 \cdot \frac{20.18}{a} = 3.52$ (1 mark)

$a = 5.73$
5.7392

$\frac{6}{3} \frac{5.73}{z} = 3.53$

$z = 3.248$
3.26298

$\frac{4}{3} \frac{3 \cdot 3.248}{y} = 3.53$

$y = 3.68$
3.71

$\frac{5}{3} \frac{3.68}{x} = 3.53$ 0.1.

$x = 1.737$
1.7578

$1 \cdot \frac{2 \cdot 1.737}{1} = 3.47$
3.5157

Formulae and Constants

$$\beta = 1048 \mu A / V^2$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & Cutoff \\ \beta(V_{GT} - V_{ds}/2)V_{ds} & V_{ds} < V_{dsat} & Linear \\ \frac{\beta}{2} V_{GT}^2 & V_{ds} > V_{dsat} & Saturation \end{cases}$$

$$\eta = 100mV/V$$
$$k_\lambda = 0.083$$
$$S = 100mV/V$$
$$v_T = 26mV$$
$$I_{off} = 0.1\mu A$$

$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k_\lambda V_{sb}}{S}} (1 - e^{\frac{-V_{ds}}{v_T}})$$

$$\gamma = 0.16$$
$$\emptyset_s = 0.93V$$
$$V_t = V_{t0} + \gamma(\sqrt{\emptyset_s + V_{sb}} - \sqrt{\emptyset_s})$$