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COE608: Computer Organization and Architecture

Mid-Term Exam, Winter 2014

Name: **Student #:**

Total time allowed: 80 minutes. **Total Marks: 70**

i) The midterm exam consists of five questions and it has five pages. Answer all questions.

ii) An instruction set sheet for the MIPS processor is allowed for your reference.

iii) Estimated time for each question is equivalent to the marks assigned to it.

iv) Some questions may contain special instructions. Please ensure that you read them carefully.

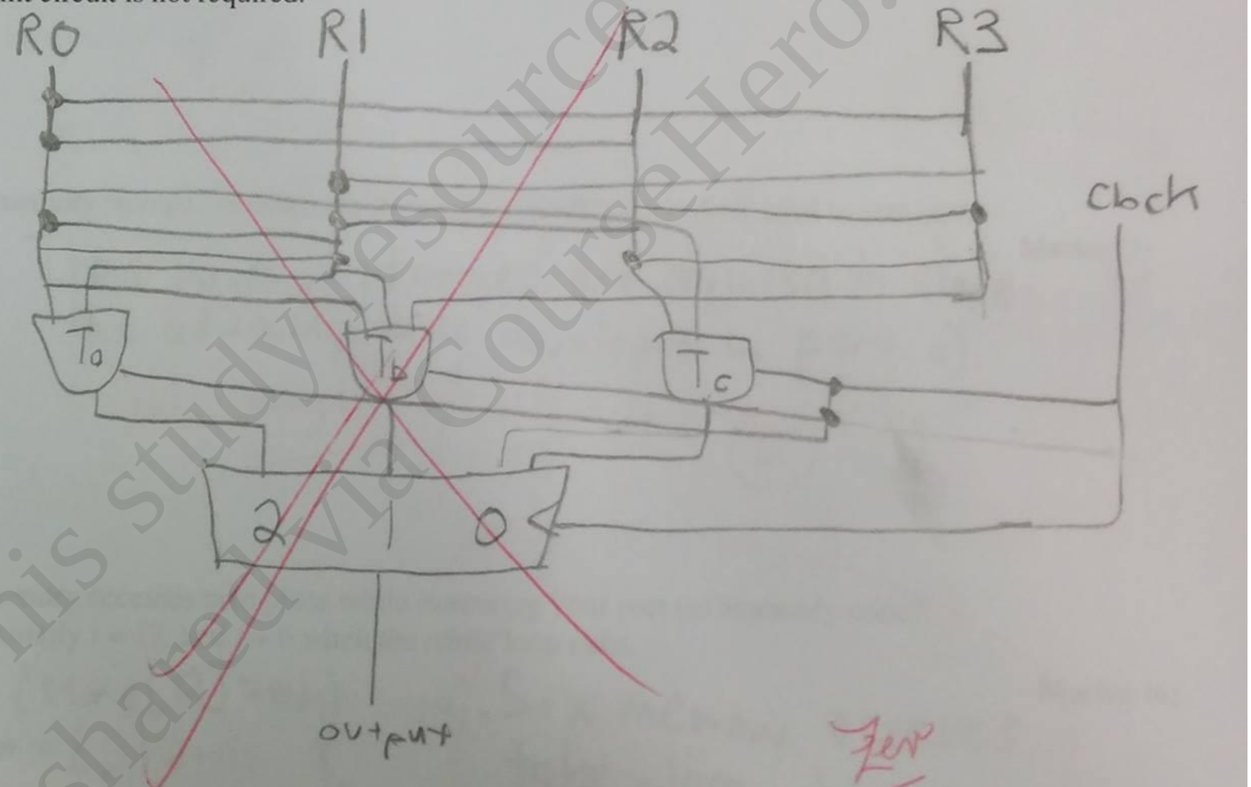
v) Your answer should be concise, to the point and in the space provided.

Q-1. Develop an optimal (i.e. minimum hardware) point-to-point interconnection datapath containing four 1-bit registers (R0, R1, R2 and R3) and suitable size multiplexers that facilitate the following register transfers. Assume that only one set of the transfers (Ta, Tb or Tc) can take place at a time.

Ta: R1 <= R3, R0 <= R2, R2 <= R1
Tb: R3 <= R2, R0 <= R1, R1 <= R0
Tc: R0 <= R3, R2 <= R3

Marks: (12)

Draw the datapath circuit only and show the control signals at all the control points of the datapath. The control unit circuit is not required.



Zero

=6

Q-2. Consider the following *While* loop code sequence in a C-like language:

```
while (store[i] == k)
  i -= 1;
```

Assume that *i* and *k* are integers stored in registers $t0 and $s5, base address of the *store* array (i.e. store[0]) is in register $s4 and the *store* array is of integer type.

(a) Write MIPS assembly code for the above *While* loop with minimum number of instructions.

Marks: (8)

→lw $t0, 4($s4);

→beq $t0, $s5; ?

→~~sub~~ $t0, $t0, -1;

Addi

loading from store[1]

2

(b) How much memory storage is required to store your assembly code developed in part (a)?

Marks: (3)

Three memory storages are required to store the assembly code developed in part a).

How many bytes/words ?

2

(b) How many memory accesses take place while executing your part (a) assembly code? Assume that initially *i* = 12, and *i* = 6 when the *while* loop exits.

Marks: (6)

while (store[12] == k)
i -= 1; 12→11 ↑
11→10 6
11→9
10→8
8→7
7→6

∴ Six memory accesses take place when part a assembly code is executed.

2

= 4

Q-3. (a) Determine a single precision, IEEE 754 floating-point standard representation of $4/3 = (1.333333)_{10}$

Marks: (8)

$$\frac{4_{10}}{3_{10}} = \frac{100_2}{11_2} = 9.0909$$

000|0111010|0010|1001|1100

1001

1.001×10^3

~~n=130-127~~

~~Exponent: 130~~

10000010

0 = positive number

$0.0909 \times 2 = 0.1818 \times 2 = 0.3636$

$0.3636 \times 2 = 0.7272$

$0.7272 \times 2 = 1.4544$

$0.4544 \times 2 = 0.9088$

$0.9088 \times 2 = 1.8176$

$0.8176 \times 2 = 1.6352$

$0.6352 \times 2 = 1.2704$

$0.2704 \times 2 = 0.5408$

$0.5408 \times 2 = 1.0816$

$0.0816 \times 2 = 0.1632$

$0.1632 \times 2 = 0.3264$

$0.3264 \times 2 = 0.6528$

$0.6528 \times 2 = 1.3056$

$0.3056 \times 2 = 0.6112$

$0.6112 \times 2 = 1.2224$

$0.2224 \times 2 = 0.4448$

$0.4448 \times 2 = 0.8896$

$0.8896 \times 2 = 1.7792$

$0.7792 \times 2 = 1.5584$

$0.5584 \times 2 = 1.1168$

$0.1168 \times 2 = 0.2336$

$0.2736 \times 2 = 0.4672$

2

~~0 | 1000 0010 | 000 1011 1010 0010 1001 1100~~

(b) Determine the decimal value of the following single precision (IEEE 754 Standard) floating point binary number.

Marks: (4)

0	0101 1001	011 1010 0000 0000 0000 0000

positive number

64+16+8+1 = 89

~~127-89=38~~

~~100110~~

$+2^{-2}+2^{-3}+2^{-4}+2^{-6} = 1_{10} = 0.4531_{10}$

2

$\therefore (38.4531)_{10}$

1.4531×2^{-38}

cycles/sec X cycles/instruction

Q-4. (a) List at least two advantages and one disadvantage of a multi-cycle CPU as compared to single-cycle CPU design. **Marks: (6)**

Advantages → it allows for better processing efficiency in the computing process, faster computing experience

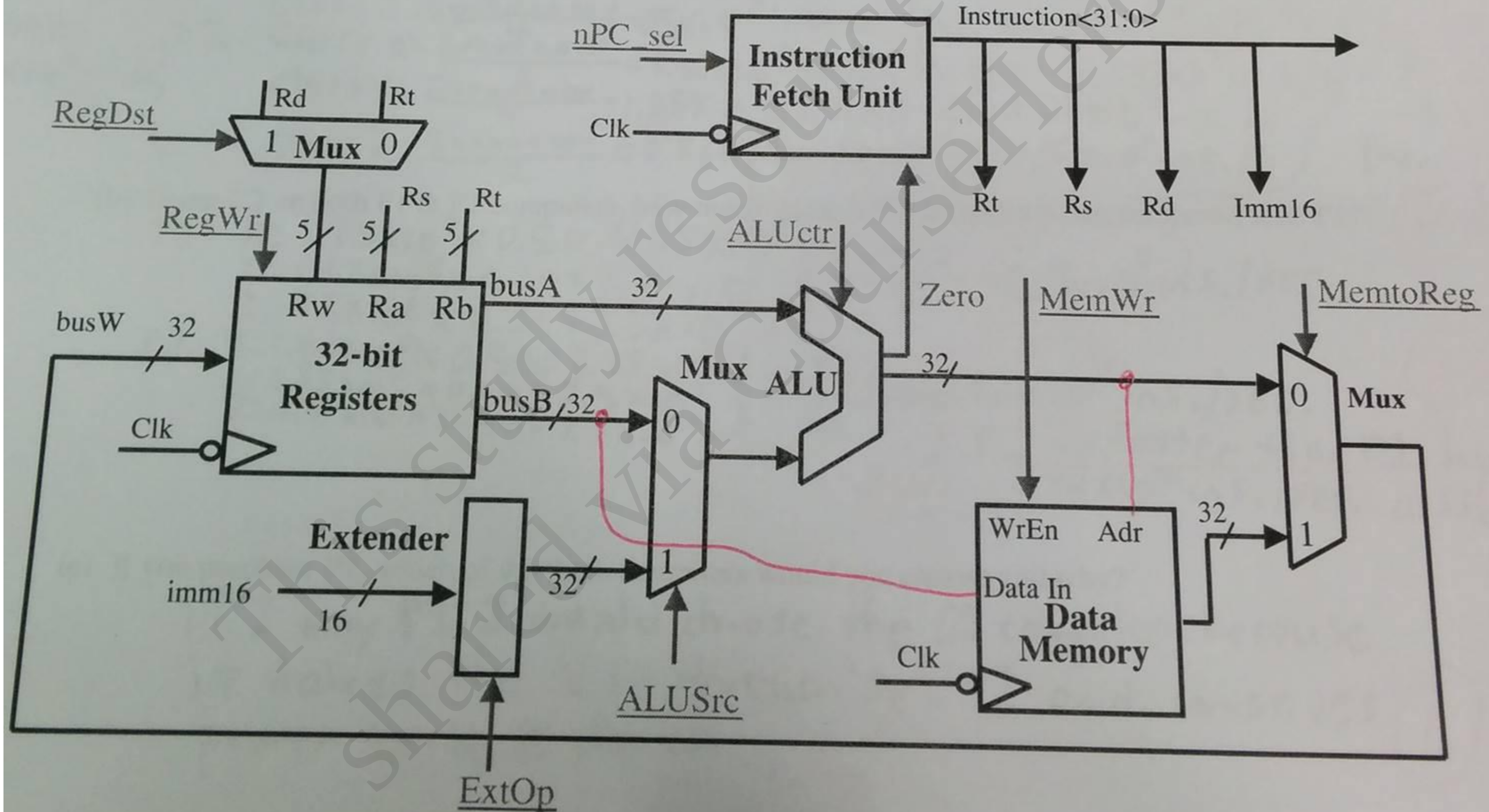
→ allows for ~~dual~~, quad-core configuration

3

Disadvantages → higher CPI than single CPU which indicates more cycles and power wasted for each instruction being processed

(b) A partial datapath of a single-cycle CPU is given below. Amend the datapath to implement the load and store word (LW and SW) instructions. Justify your amendments/changes in the datapath.

Marks: (7)



Zero

=6

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Q-5. Consider two different computer implementations, P1 and P2 of the same Instruction Set Architecture. There are three classes of instructions (X, Y, and Z) in the instruction set. P1 has a clock rate of 1 GHz and P2 has a clock rate of 500 MHz. Three different compilers C1, C2 and C3 have been developed for both computers. C1 compiler is produced by the makers of P1; C2 compiler is produced by the makers of P2, where C3 compiler is produced by an independent compiler vendor. The average CPI for each class of instruction on P1 and P2 for the three compilers are given in the following table:

cycles per instruction

Inst. Class	CPI on P1	CPI on P2	Instruction mix for compiler C1	Instruction mix for compiler C2	Instruction mix for compiler C3
X	8	3	20%	50%	20%
Y	6	4	50%	20%	30%
Z	4	2	30%	30%	50%

Assume that each compiler uses the same number of instructions for a given benchmark program and the instruction mix is provided in the above table.

Marks: (5+5+3+3)

(a) Using C1 compiler on both P1 & P2 computers, how much faster is P1 computer when compared to P2?

Average: 6.1×10^7 ins./sec.

P1: Class X: $\frac{1,000,000,000 \text{ cycles/s}}{8 \text{ cycles/instruc.}}$ = 1.25×10^8 instruc./sec. × 0.20 = 2.5×10^7 instruc./sec.

Class Y: $\frac{1000000000}{6}$ = 1.67×10^8 instruc./sec. × 0.50 = 8.3×10^7 instruc./sec.

Class Z: $\frac{1000000000}{4}$ = 2.5×10^8 instruc./sec. × 0.30 = 7.5×10^7 instruc./sec

Average: 1.705×10^8 ins./sec.

P2: Class X: $\frac{500000000}{3}$ = 1.67×10^8 ins./s × 0.20 = 3.3×10^7 ins./s

Class Y: $\frac{500000000}{4}$ = 1.25×10^8 ins./s × 0.50 = 6.25×10^7 ins./s

Class Z: $\frac{500000000}{2}$ = 2.5×10^8 ins./s × 0.30 = 7.5×10^7 ins./s

∴ P1 computer is slower than P2.

2

(b) Using C2 on both P1 & P2 computers, how much faster is P2 computer when compared with P1?

P1: X: 1.25×10^8 × 0.50 = 6.25×10^7
Y: 1.67×10^8 × 0.20 = 3.34×10^7
Z: 2.5×10^8 × 0.30 = 7.5×10^7
$\frac{X+Y+Z}{3}$ = 5.7×10^7 ins./sec.

2

P2: X: 1.67×10^8 × 0.50 = 8.35×10^7
Y: 1.25×10^8 × 0.20 = 2.5×10^7
Z: 2.5×10^8 × 0.30 = 7.5×10^7
$\frac{X+Y+Z}{3}$ = 6.12×10^7 ins./sec.

∴ P2 is faster than P1 by a 0.42×10^7 ins./sec. difference.

How

(c) If you purchase P1, which of the three compilers would you choose and why?

If I buy P1 I would choose the C2 compiler because it halves the X instruction's CPI and conserves power in X, Z classes.

why

1

(d) If you purchase P2, which of the three compilers would you choose and why?

If I buy P2 I would choose the C1 compiler because of reductions in CPI at larger margins.

1

why