COE718: Hardware Software Codesign of Embedded Systems

Midterm Examination Fall 2014

Student Name and ID:_____

Total Time Allowed: 70 Minutes **Maximum Marks: 50**

i. The examination has 4 pages and 4 questions. Answer all the questions.
ii. To earn maximum credit, your answer must be concise, to the point and in the given space.
iii. All questions are not of the same difficulty and value. Consider this when allocating time for their solutions.

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1. (a) van Neumann and Harvard architectures are being employed in the design of embedded processors. Explain briefly the main differences between these two architectures. Which of these architectures is suitable for high performance CPUs?
Justify your answer by providing examples of CPUs that are based on each of the architecture.

MARKS: 7+4

1. (b) ARM CPU are the most popular embedded computing for a large number of real world application. List and explain at least two such applications that use an ARM CPU core.

2. **(a)** ARM Cortex M3 CPU has a much faster response time to multiple interrupts as compared to some other CPUs. Explain briefly how the faster response is achieved in Cortex M3 CPU?

MARKS: 6

(b) ARM CPUs (e.g. ARM7TDMI or Cortex M3) has been designed targeting handheld devices. Identify at least two specific features of ARM CPU programming/architecture that facilitate smaller size code? Justify your answer in detail.

MARKS: 6

4. Indicate (in the space provided) whether the following are TRUE or FALSE. To obtain full marks for each question, include ***SHORT*** comments in support of your answer.

MARKS: 12 (2 each)

(a) ARM Cortex M3 CPU is based on Harvard architecture.
TRUE ___ or FALSE ___?

_____

_____

(b) SystemC can be used for embedded system modeling at the transaction level.
TRUE ___ or FALSE ___?

_____

_____

(c) ARM Cortex M3 CPU employs an efficient technique to access bit-wise status/data information from peripheral devices.
TRUE ___ or FALSE ___?

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_____

(d) ARM Cortex M3 CPU is a 16-bit processor with 16 registers.
TRUE ___ or FALSE ___?

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_____

(e) PLL block is a critical component to realize a CPU soft core (e.g. NIOS-II) on an FPGA device.
TRUE ___ or FALSE ___?

_____

_____

(f) Conditional execution is a useless feature of ARM CPUs for compact application code.
TRUE ___ or FALSE ___?

_____

_____

4. (a) Consider a periodic task set with the following three independent tasks, where C is the execution time and T is time period of a task.

Task P1: C1 = 10, T1 = 60
Task P2: C2 = 25, T2 = 50
Task P3: C3 = 15, T3 = 150

Are these tasks are schedulable if RMS (Rate Monotonic Scheduling) based priority is employed? Justify your answer by providing complete details of your solution.

MARKS: 7

4. (b) Add the following fourth task to the task set of part (a)

Task P4: C4 = 15, T4 = 75

Verify if the system with four tasks is schedulable or not. Provide all the details of your approach and the solution.

MARKS: 8