Popular Arm Architecture

ARM7 → 3 pipeline stages (fetch/decode/execute)

ARM9 → compatible with ARM7
5 pipeline stages

ARM10 → 6 stages (fetch / issue / decode / execute / memory / write)

	ARM7	ARM9	ARM10	ARM11
year	1995	1997	1999	2001
pipeline depth	3	5	6	8
Typical freq. (Mhz)	80	150	260	335
Power (mW/Mhz)	0.06	0.19	0.5	0.4
Throughput (MIPS/MHz)	0.97	1.1	1.3	1.2
Architecture	VN	H	H	H

ARM architecture vs. RISC Archeture

Major Design Features: (RISC based architectures)

Instructions → reduced set / single cycle / fixed length

Pipeline → decode in one stage / no need for micro code

Instructions → reduced set / single cycle / short length

Pipeline → decode in one stage / no need for microcode

ARM features

- ARM architecture is different from pure RISC
- some of these differences are:

1) Variable Cycle → execution of certain instructions

2) Thumb mode of operation → 16 bit operation