Ryerson University
Department of Electrical and Computer Engineering
ELE734: LOW-POWER DIGITAL INTEGRATED CIRCUITS
Final Examination, December 13, 2012
Duration: 3 hours

Student's Name: .....

Student's Number: ..... **Section: .....**

NOTES:

1. This is a **Closed Book** examination. No aids other than the approved calculators and **1 sheet (2 pages) of aid sheet** are allowed.
2. Answer all questions.
3. **No questions are to be asked** in the examination hall. If doubt exists as to the interpretation of any question, the student is urged to submit with the answer paper, a clear statement of any assumptions made.

Question No.	*Mark of each question*	*Mark obtained*
Q1	20	
Q2	20	
Q3	20	
Q4	20	
Q5	20	
Q6	20	
Total (Out of 120):		

Q1:

Design a static CMOS gate that has the following output.

*Out = !((A+B)*C)*

a) Draw the transistor-level schematic of your design. Size the transistors to provide a worst case pull-up and pull-down resistance of R (assuming a unit nmos transistor has the resistance of R and a unit pmos transistor has the resistance of 2R). (10 marks)

b) Draw stick diagram of the gate (please clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (8 marks)

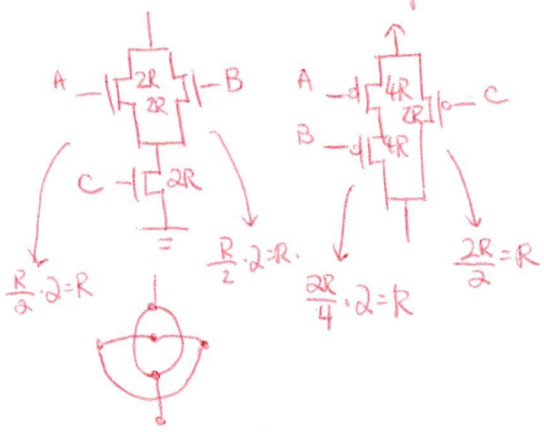
c) Estimate the area of the gate based on your stick diagram. (2 marks)

a) $Out = \overline{(A+B)\cdot C}$ ✓ ⇒ Pull down network 1 mark

$= (\overline{A+B}) + \overline{C}$

2marks $= (\overline{A}\cdot\overline{B}) + \overline{C}$ ✓ ⇒ Pull up network. 2marks

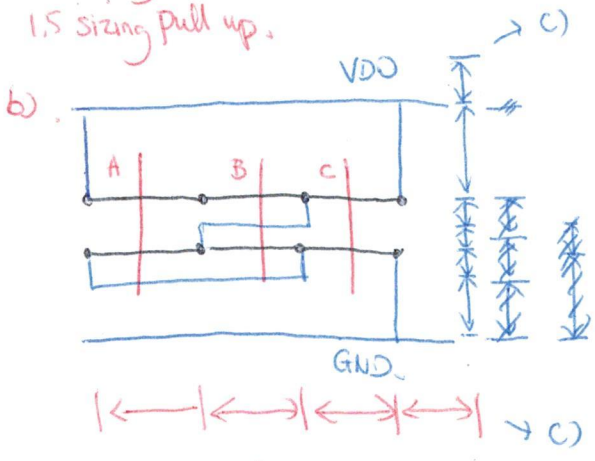
Pull down network Pull up network 2marks



1.5 sizing pull down

1.5 sizing pull up.

b)



4

6

32 48

$4\times 6 = 24$

$= 24\cdot 8\lambda\cdot 8\lambda$

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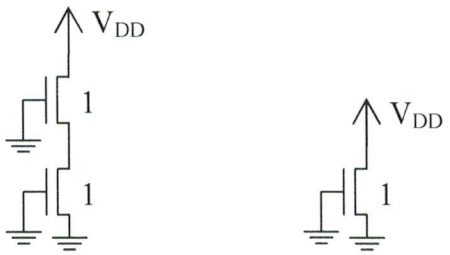
Q2:

Calculate the amount of current that is consumed by the left circuit as a percentage of the current that is consumed by the right circuit. (20 marks)



$$I_{sub} = I_{off}\, 10^{\frac{\eta(V_X - V_{DD})}{n}} = I_{off}\, 10^{\frac{-V_X + \eta((V_{DD}-V_X)-V_{DD}) - K_r V_X}{n}}$$ — 5 marks

$$\eta(V_X - V_{DD}) = -V_X + \eta((V_{DD}-V_X)-V_{DD}) - K_r V_X$$

$$\eta V_X - \eta V_{DD} = -V_X + \eta V_{DD} - \eta V_X - \eta V_{DD} - K_r V_X$$

$$\eta V_X + V_X + \eta V_X + K_r V_X = \eta V_{DD}$$

$$V_X = \frac{\eta V_{DD}}{1 + 2\eta + K_r}$$ — 5 marks

$$I_{sub} = I_{off}\, 10^{\eta\left(\frac{\eta V_{DD}}{1+2\eta+K_r} - V_{DD}\right)}$$

$$= I_{off}\, 10^{\eta\left(\frac{\eta V_{DD} - 1 - 2\eta - K_r}{1+2\eta+K_r} V_{DD}\right)}$$

$$= I_{off}\, 10^{-\eta V_{DD}\left(\frac{1+\eta-K_r}{1+2\eta+K_r}\right)}$$

$$\approx I_{off}\, 10^{-\eta V_{DD}}.$$

By a factor of $10^{\eta V_{DD}}$. — 5 marks.

Answer = 50% ⇒ 3 marks

~~Answer = 90% less ⇒~~

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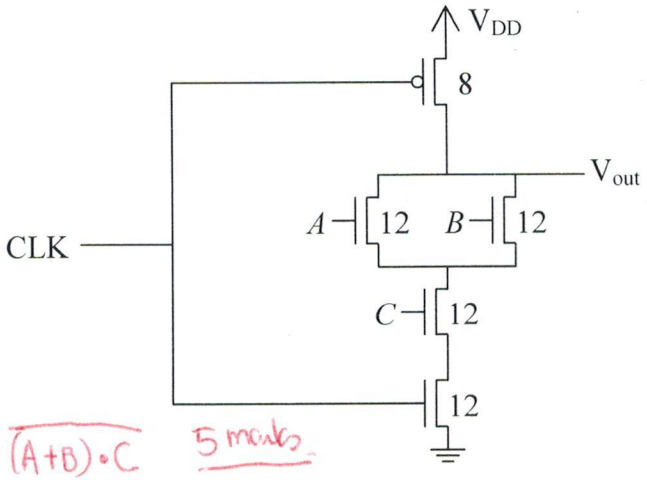
Q3:

Consider the following circuit?

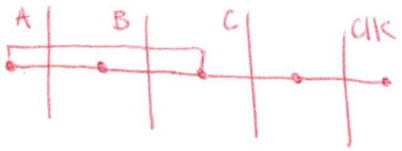
a) What function is performed by the gate? (5 marks)

b) What is the worst case logic effort of the gate (please consider only the falling transition and account for all of the internal capacitances of the gate)? (7.5 marks)

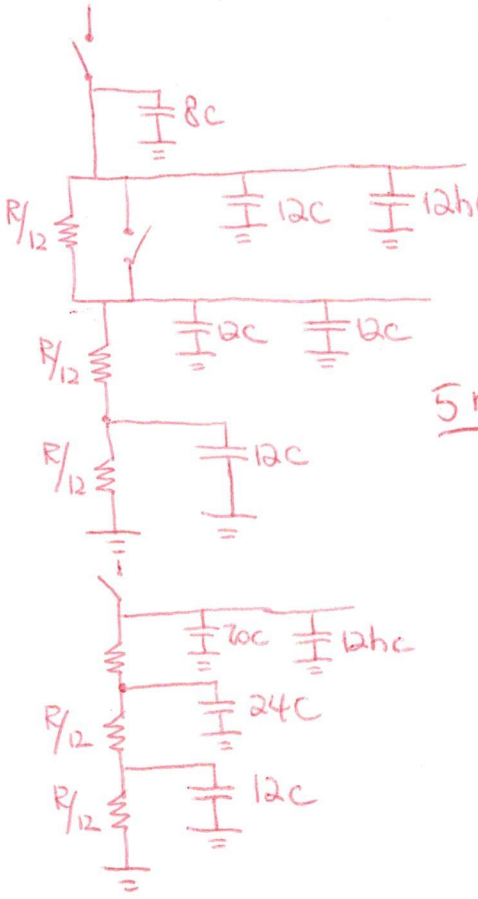
c) What is the worst case parasitic delay of the gate (please consider only the falling transition and account for all of the internal capacitances of the gate)? (7.5 marks)



a) Function performed $\overline{(A+B)\cdot C}$ 5 marks



b)



5 marks

$$\text{delay} = (12hC + 20C)\cdot\frac{R}{12}\cdot 3 + 24C\left(\frac{R}{12}\cdot 2\right) + 12C\frac{R}{12}$$

$$= 3RCh + 5RC + 4RC + RC$$

$$= 3hRC + 10RC$$

5 marks

$$\frac{\text{delay}}{3RC} = \frac{3hRC + 10RC}{3RC} = 1\cdot h + \frac{10}{3}$$

logic effort = 1

c) parasitic delay = $\frac{10}{3}$.

$\Rightarrow$ 5 marks

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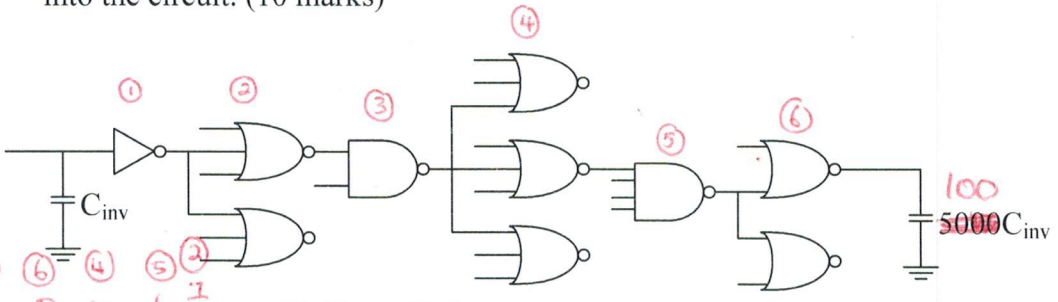
Q4:

For the following circuit:

a) Calculate optimum delay and size of the transistors without increase the number of stages in the circuit. C_{inv} is the input capacitance of a minimum size inverter (inverter: g=1, p=1; 2-input nand: g=4/3, p=2; 2-input nor: g=5/3, p=2; 3-input nor: g = 7/3, p = 3; 4-input nand: g = 6/3, p = 4, R_{eff}=10Kohm for unit nmos, C_{eff}=0.1fF for a unit transistor). (10 marks)

b) Calculate optimum delay and size of the transistors by inserting additional stages into the circuit. (10 marks)



① ③ ⑥ ④ ⑤ ②

a) $G = 1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot \frac{7}{3} \cdot \frac{6}{3} \cdot \frac{7}{3} = 10.37 \cdot \frac{7}{3} = 24.20$

$B = 2 \cdot 1 \cdot 3 \cdot 1 \cdot 2 = 12$

$H = \frac{100 C_{inv}}{C_{inv}} = 100$

$F = GBH = 29040$

$(F)^{1/6} = 5.54$ 7 marks

$5.54 \cdot 6 = 48.24$

$+1+2+2+3+4+3 = 48.24$

1.5 mark

$3RC = 3 \cdot 10k \cdot 0.1f$ 1.5 mark

$= 3ps$

$48.24 \cdot 3ps = 144.72$.

sizing for each stage.

...

b). stage ratio of 3

$\frac{\log 29040}{\log 3} = 9.35$ stages. 7 marks

$\frac{\log 29040}{\log 4} = 7.41$ stages.

$\ln 29040 = 10.27$ stages

$\approx 10 \cdot 3 = 30$.

$\approx 30 \cdot 3ps = 90ps$

sizing 3 marks

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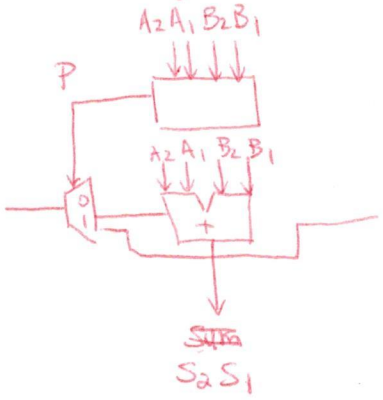
Q5:

a) Design a 8-bit wide carry skip adder, with 4 2-bit wide blocks. (12 Marks)
b) Identify the gates that are on the critical path in your design. (8 Marks)

a) A single 2 Bit wide block



4 marks

4 marks for identity 2-bit full adder

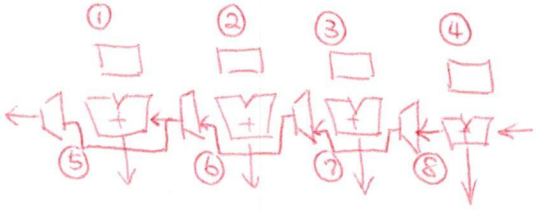
$A_2A_1B_2B_1$	P
0000	0
0001	1
0011	2
0101	1
0110	2
0111	3
1001	2
1010	3
1011	4
1100	3
1101	4
1110	5
1111	6

$\bar{A}_2\bar{A}_1B_2B_1 + \bar{A}_2A_1B_2\bar{B}_1 +$

$A_2\bar{A}_1\bar{B}_2B_1 + A_2A_1\bar{B}_2\bar{B}_1$

$= (A_2 \oplus B_2) \cdot (A_1 \oplus B_1)$

4 marks



critical path adder 8 → mux 8
→ mux 7
→ mux 6
→ adder 5

8 marks

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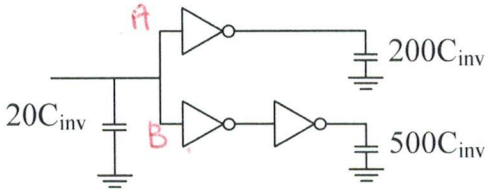
Q6:

Find the sizes of the following three inverters if we want equal delay through both branches (assume the parasitic delay of the inverters are equal to 0). (20 marks)



$2\cdot\left(\frac{500}{B}\right)^{1/2}+0=\frac{200}{A}+0$

10 marks

$2\cdot\left(\frac{500}{B}\right)^{1/2}=\frac{200}{A}$

$\left(\frac{500}{B}\right)^{1/2}=\frac{100}{A}$

$\frac{500}{B}=\frac{10000}{A^2}$

$\frac{500}{20-A}=\frac{10000}{A^2}$

$\frac{1}{20-A}=\frac{20}{A^2}$

$A^2=400-20A$

$A^2+20A-400=0$

$\frac{-20\pm\sqrt{400+4\cdot400}}{2}$

$=\frac{-20\pm\sqrt{2000}}{2}$

$=\frac{-20+44.72}{2}$

$=12.36.$

$B=20-12.36=7.64$ 5 marks

$\frac{200}{12.36}=16.18$

$2\cdot\left(\frac{500}{7.64}\right)^{1/2}=16.18$ 5 marks

sizing of the gates.

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