



Quiz Submissions - Final Exam

Vatsal Shreekant (username: vatsal.shreekant)

Attempt 1

Written: Dec 14, 2020 8:30 AM - Dec 14, 2020 10:37 AM

Submission View

Your Final Exam has been submitted successfully.

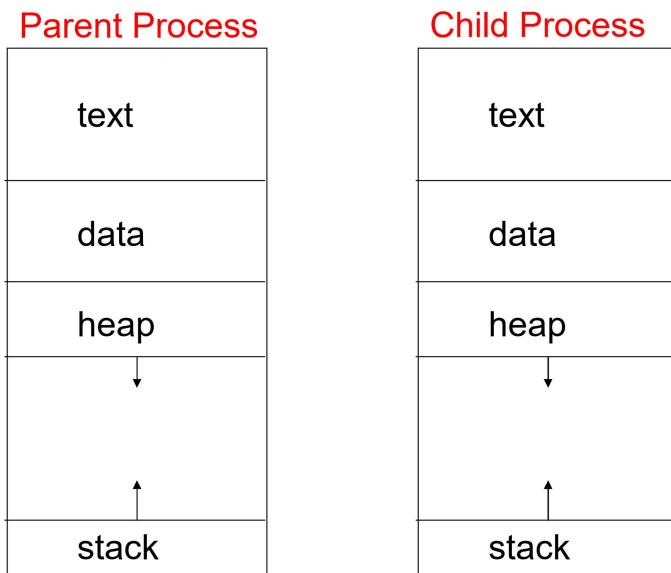
An announcement will be made once grades are ready for viewing.

Good luck on your other exams!

Question 1

0 / 1 point

The following shows a parent and child process.



What does the text content refer to?

- The entire program
- The data associated with the program
- The machine level program instructions
- None of these answers

Question 2**1 / 1 point**

In class, we discussed that a instruction can be broken down into instruction fetch (IF), instruction decode (ID), instruction execute (IE), memory operation (MEM) and write back (WB).

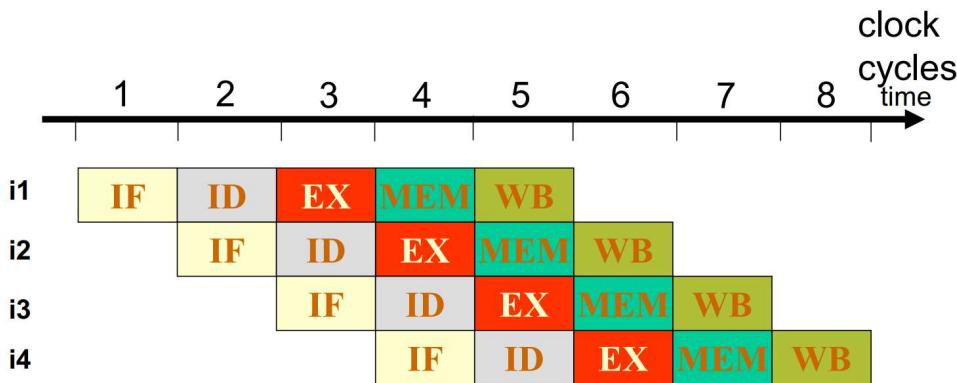


Which of the the above stage(s) is ALWAYS required in an instruction?

- Fetch and execute
- Decode and execute
- Fetch only
- Fetch and decode

Question 3**1 / 1 point**

The following shows the instruction execution for a program using pipeline processing. If the number of the instructions in this program is very large (continued after i4) what is the pipeline speedup achieved with this processor compared to a non-piplined processor?



- 5
- 5 cycles
- 2
- 3
- 4

Question 4**1 / 1 point**

In a program running on an ARM processor, after an instruction is executed, the value of program counter (PC) is incremented by 4. The instruction that executed was likely

- Loop
- Sequential code
- Jump to a target
- Function call

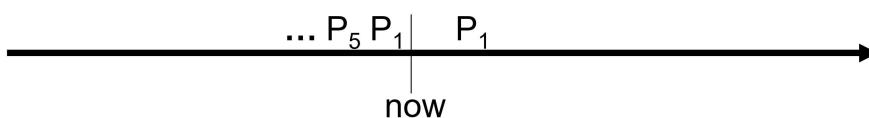
Question 5**1 / 1 point**

A method to mitigate stalls in control hazards is to have specialized hardware that guesses and executes the next instruction after the conditional branch. If in a particular hardware, the program counter is designed to increment by 4 Bytes in a 32 bit instruction set, this means that the hardware is predicting that

- None of these answers
- The branch may or may not be taken, need more information
- The branch will be taken
- The branch will not be taken

Question 6**1 / 1 point**

A process timeline is being shown in the image below



"now" indicates a page fault occurring. What kind of page replacement policy is likely being used by this computer system have?

- LRU - Least recently used
- FIFO - First in first out

MRU - Most recently used

None of these answers

Question 7

1 / 1 point

Well designed page replacement policies make use of:

None of these answers

Temporal locality

Both spacial and temporal locality

Spacial locality

Question 8

0 / 1 point

Assume that the current instruction running on a processor has a conditional branch. In a pipelined processor that does not have any solutions for branched instructions, the earliest the next instruction can execute is in the

Fetch stage

Write back stage

Memory operation stage

Execute stage

Decode stage

Question 9

0 / 1 point

A RISC based processor has three types of instructions only. Type 1 instructions execute in 3 clock cycles, Type 2 instructions execute in 4 clock cycles or and Type 3 instructions execute in 5 clock cycles.

Assume you have a program that has 100 instructions executing on this processor. In this program 30% of instructions are of Type 1, 40% are of Type 2 and 30% are of Type 3. What is the **pipeline speedup** achieved running this program through a 5 stage piplined processor compared to a non-piplined processor system?

None of these answers

3.85

4

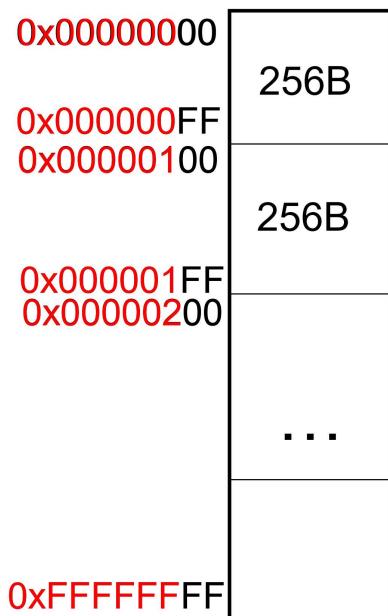
0.25

3

Question 10

1 / 1 point

How many address exist within one page in the following page setup?



255

1024

256

511

None of these answers

Question 11

0 / 1 point

The ratio of cache memory size in comparison the main memory size is in the order of:

thousands

hundreds

millions

billions

Question 12

0 / 1 point

In modern operating systems, the theoretical speed-up that pipelining affords relies largely on the assumption that

An instruction can be divided into multiple sub-tasks

Memory can be accessed at speeds of the processor

Processor can be delayed for certain number of cycles

The ALU speed is comparable to the processor speed

Question 13

1 / 1 point

In class, we discussed that a instruction can be broken down into instruction fetch (IF), instruction decode (ID), instruction execute (IE), memory operation (MEM) and write back (WB).



Which of the these stage(s) may not present in all instruction?

Execute and memory operation

Decode and write back

Decode and memory operation

Fetch and decode

Question 14

0 / 1 point

Which of the following is a good policy to follow for replacing pages?

- The most recently accessed page should be replaced
- The least recently accessed page should be replaced
- The most recently updated page should be replaced
- Pages closest to recently used page should be repalced

Question 15**0 / 1 point**

In order for pipelining to be implemented, the hardware in a traditional processes must be changed to:

- Have buffers after each instruction stage
- Have a new modified ALU unit
- Have different cache memories for fetch and memory operation stages
- All of the above

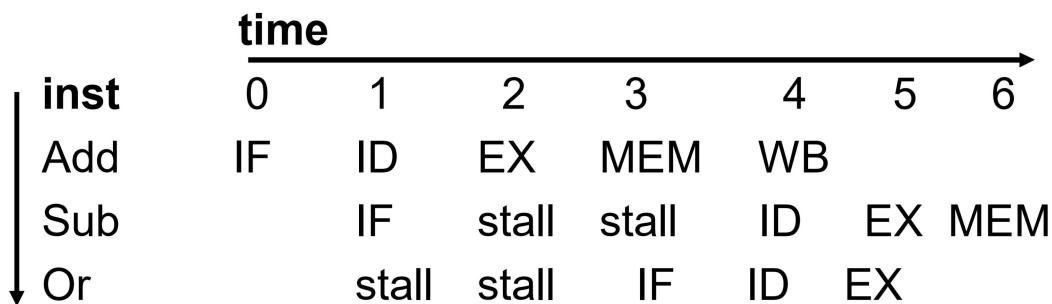
Question 16**1 / 1 point**

Assume that linear search is being used to find an address in the Cache Directory of Cache Memory. If the Cache Directory is of size 1024, in the worst case scenario, how many comparisons must be done when the processor wants to know if a particular address exists in Cache Memory?

- 1023
- 10
- 9
- 1024
- 1

Question 17**0 / 1 point**

What kind of **pipeline hazard** is being remedied in the following instructional pipeline?



collision

→ data hazard

✗ structural hazard

control hazard

Question 18

0 / 1 point

What instruction(s) often display temporal locality?

✗ Functions

→ Loops and functions

Sequential code

Loops

Question 19

0 / 1 point

What is the worst case scenario in a badly designed page replacement policy?

→ Page that will be processed next is replaced

✗ Page that is currently needed is replaced causing an infinite loop

Page that does not change often is replaced

None of these answers

Question 20**1 / 1 point**

Most page tables have a modified bit or dirty bit column. What is the purpose of this bit?

- Indicates whether the page exists in memory or not
- Indicates whether the page has been modified recently
- None of these answers
- Indicates whether a virtual page exists for a process or not

Question 21**1 / 1 point**

The following shows three processes executing a critical section of code based on Mutex Lock

P1

```
while(Test&Set(L));  
    Critical Section  
    L=0;
```

P2

```
while(Test&Set(L));  
    Critical Section  
    L=0;
```

P3

```
while(Test&Set(L));  
    Critical Section  
    L = 0;
```

Assume that process P2 is in the critical section. What must be true about process P1 and P3?

- P1 is executing the instruction while(Test&Set(L)) and P3 is executing L=0;
- P3 is executing the instruction while(Test&Set(L)) and P1 is executing L=0;
- Both processes are executing the instruction while(Test&Set(L))
- None of these answers

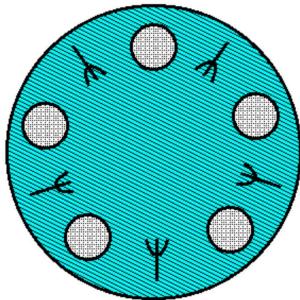
Question 22**1 / 1 point**

The following shows the instruction execution for a program using pipeline processing. What is fill time of this pipeline?

- 4 cycles
- 2 cycles
- 5 cycles

3 cycles 1 cycle**Question 23****0 / 1 point**

The classic philosopher problem in the context of concurrent programming is an example of:

 deadly embrace deadlock mutex lock threads**Question 24****1 / 1 point**

In a program running on an ARM processor, after an instruction is executed, the value of program counter (PC) is incremented by eight (32). The instruction that executed was likely

 Loop If else statement Jump to a target Sequential code**Question 25****1 / 1 point**

The ideal pipeline speedup in pipelined processors cannot be achieved because:

 pipeline hazards do not allow for ideal execution

- the hardware implementation is very complex
- it takes more than one cycle to execute each pipeline stage
- the number of pipeline stages is very limited

Question 26**1 / 1 point**

In modern computer systems, the processors operate in time scales of:

- femto-seconds
- micro-seconds
- milli-seconds
- nano-seconds

Question 27**1 / 1 point**

When an instruction requires the same hardware unit at the same time as another instruction stage, this is known as a

- structural hazard
- collision
- data hazard
- control hazard

Question 28**1 / 1 point**

What is the difference between a Round Robin (RR) policy and a Priority Based policy?

- Round robin does not take into account time spent using a processor
- None of these answers
- Round Robin does not consider all processes to be equal at all times

- Priority based does not consider all processes to be equal at all times

Question 29

0 / 1 point

Why does the following implementation of Mutex Lock not work properly?

```
AcquireLock(L)
    while (L==1);
    L=1;
```

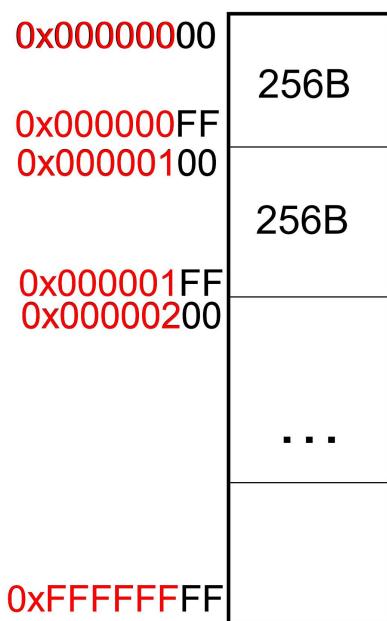
```
ReleaseLock(L)
    while(L);
    L=0;
```

- None of these answers
- Another process can access the lock variable L and change it
- The process can become preempted after a while loop executes
- When two processes are trying to acquire lock, a metastable situation can occur and both change L value at the same time

Question 30

0 / 1 point

How many virtual pages exist in the following page setup?



- None of these answers

- 65535
- 1048575
- 511
- 255

Question 31**1 / 1 point**

Which of the following methods for Inter Process Communication (IPC) takes the longest time.

- Main memory variable sharing
- Messaging
- A pipe
- File variable sharing
- Cache memory variable

Question 32**0 / 1 point**

Theoretically, perfect pipelining can reduce CPI (Cycles per instruction) of a program to what value?

- between 1-2
- Depends on the range of cycles for different instructions
- The number of cycles of the simplest instruction
- 1

Question 33**1 / 1 point**

Cache memory is most likely to be packaged with which of the following hardware?

- Main memory

Processor ALU Input/Output Device**Question 34****1 / 1 point**

Assume that a binary search is being used to find an address in the Cache Directory of Cache Memory. If the Cache Directory is of size 1024, in the worst case scenario, how many comparisons must be done when the processor wants to know if a particular address exists in Cache Memory?

 1024 1023 1 9 10**Question 35****1 / 1 point**

In class, we discussed that an instruction can be broken down into instruction fetch (IF), instruction decode (ID), instruction execute (IE), memory operation (MEM) and write back (WB).



However, not all instructions will require all stages. Which of the the following instrutions do not require a memory operation?

 ADD R1, R2, R3 LDR R1,[R2] None of these answers LDMIA [r3,r5,r6]

Question 36**1 / 1 point**

In modern operating systems, process scheduling policies try to

- give priority to the largest programs
- give priority to programs least recently used
- minimize average program execution time
- allow fair use of processor time for each process

Question 37**0 / 1 point**

What is the major problem with the FIFO (first in first out) page replacement policy?

- Hard to find time associated with process used
- Not efficient, same set of processes get routinely replaced
- Very computationally intensive
- None of these answers

Question 38**1 / 1 point**

The following shows three processes executing a critical section of code based on Mutex Lock

P1

```
while(Test&Set(L));  
    Critical Section  
    L=0;
```

P2

```
while(Test&Set(L));  
    Critical Section  
    L=0;
```

P3

```
while(Test&Set(L));  
    Critical Section  
    L = 0;
```

Assume that process P1 has just finished executing L=0. Which of the other processes will acquire lock next?

- P2 as it is in the next set of instructions
- None of these answers
- P3 as it is quicker than P2 due to L=0

- P2 or P3 depending which executes first

Question 39**0 / 1 point**

A thread can best be described as

- A lightweight process executing under a parent process
- A process which with other threads forms a program
- Another name for a process
- Another name for a program

Question 40**1 / 1 point**

How many memory addresses are typically in a Cache Directory?

- Hundred of thousands
- Thousands
- Billions
- Millions

Question 41**1 / 1 point**

What is the main component of interlock hardware used to

- ALU unit
- Comparators
- Processor
- Flip-flops

Question 42**1 / 1 point**

Assume that the CPU slice time for a particular computer system is two (2) seconds. What must be true about process times in this scenario?

- Each process will execute on the processor anywhere from 1 to 2 seconds before being evicted by the OS.
- Each process will execute on the processor for a maximum of 2 seconds
- Each process will execute on the processor for at least 2 seconds.
- Each process will execute on the processor for 2 seconds before being evicted by the OS

Question 43

0 / 1 point

What must be true about a **hash function**?

- The value stored in a hash table at the index outputed by the hash function may not match the input to the hash function.
- The value stored in a hash table at the index given by the hash function will match the input to the hash function.
- The index number outputed by the hash function may not be within the range of indices of the hash table.
- Each input to a hash function results in a unique output index number.

Question 44

1 / 1 point

The following shows a piece of code using a semaphore.

```
S=a;  
P(S);  
    Critical section code;  
V(S);
```

If I want to have a mutex lock created, what should be the value of a?

- Depends on the critical code being executed
- 0

1 None of these**Question 45****1 / 1 point**

In a single processor computer system, how many processes can be running at the same time?

 2 Depends on the number of processes in the waiting state 1 Depends on the number of cores**Question 46****0 / 1 point**

What is special about a Test&Set instruction in an instruction set.

 None of these answers ✗ Uses a temporary variable that allows for safe locking ➔ All instructions will be executed regardless of preemption policy All instructions other than hardware interrupts will be executed**Question 47****0 / 1 point**

In a non-preemptive scheduling policy, how does processor time get shared between different processes?

 OS preempts the process once in a while There is no mechanism for sharing, one process will execute forever ✗ Hardware will preempt the processes once in a while ➔ Processes are preempted when accessing hard disk

Question 48**0 / 1 point**

In dynamic instruction scheduling, the instruction queue contains a list of instructions that can be executed. How does an operating system likely choose the next instruction to execute?

- FIFO
- Lease recently used
- Most independent instruction
- Most recently accessed

Question 49**0 / 1 point**

Which of the following statements is true about a process?

- Each process constitutes a single program in execution
- Each process executes based on priority it holds
- Each process has its own unique virtual address space
- Each process runs on a processor until its task is finished

Question 50**1 / 1 point**

What kind of time is being shown in the following diagram?

- Wallclock time
- Elapsed time
- Virtual time
- User time
- Real time

Question 51**1 / 1 point**

Ideally, process management aims to make utilization of the processor approach

100% (1-n)% (where n is the number stages) None of these answers 0%**Question 52****0 / 1 point**

Assume that in a program, 50% of the time a branch is taken. In a pipelined processor using delayed branching with a single branch delay slot, on average, what is the number of stalled cycles?

 .5 cycle 0.33 cycles ➔ 0.67 cycles Don't know, need more information**Question 53****0 / 1 point**

Assume that the three (3) least significant bits are being used for constructing the hash function in Cache Memory. Accordingly, how many different hash indexes would this function produce??

0101110000101000
0101110000101001
0101110000101010
0101110000101011
0101110000101100

A

- 5
 - 2
 - 8
 - 4

Question 54

1 / 1 point

What does the valid bit in a page table entry represent?

- Indicates whether the page exists in memory or not
 - Indicates whether a virtual page exists for a process or not
 - Indicates whether the page has been modified recently
 - None of these answers

Question 55

1 / 1 point

In terms of physical size, which of the following computer system components takes the least amount of space?

- Main memory
- Magnetic hard disk drive
- Cache memory
- Processor

Question 56**0 / 1 point**

In class, we discussed that a instruction can be broken down into instruction fetch (IF), instruction decode (ID), instruction execute (IE), memory operation (MEM) and write back (WB).



In which of the the above stages is likely that the zero flag checked?

- Write back
- Memory operation
- Fetch
- Decode
- Execute

Question 57**1 / 1 point**

What is the best hash function to use in Cache Memory hardware to look up values in a the Cache Directory?

- Use the least significant bits of the address being looked up
- Use the intermediate bits of the address being looked up
- Add all the bits up of the address being looked up

- Use the most significant bits of the address being looked up

Question 58**1 / 1 point**

Non-preemptive scheduling policies are often seen in which operating systems?

- Windows
- None of these answers
- MacOS
- Unix
- Linux

Question 59**1 / 1 point**

In the context of concurrent programming, what is the difference between Busy waiting locks and blocked processes (blocks)?

- None of these answers
- Blocks require OS support, busy waiting does not
- There is no difference, both achieve the same thing
- Busy waiting requires operator support, locks do not

Question 60**1 / 1 point**

A data structure in a computer system architecture is

- A complex dataset such as class object
- A set of functions
- A set of primitive data
- An entity containing data and operation on the data

Question 61**1 / 1 point**

Assume that we have a register R4 that contains the value 1024. The memory address 1024 holds the value 5024. What will be the contents of register R8 when the following command is executed?

LDR R8, [R4, #24]!

- 5004
- None of these answers
- 4076
- 5000
- 5024

Question 62**1 / 1 point**

Different instructions in a program may take different number of clock cycles to execute. Assume that instructions in a program take 3, 4 or 5 cycles to complete depending on the specific instruction. Based on this, what is the CPI - Cycles Per Instruction - of programs written with these instructions without pipelining.

- Between 3-5
- Close to 1
- between 1-2
- larger than 5

Question 63**0 / 1 point**

Assume that a hash function is being used to find an address in the Cache Directory of Cache Memory. If the Cache Directory is of size 1024, in the worst case scenario, how many comparisons must be done when the processor wants to know if a particular address exists in Cache Memory?

- 10
- 1024

9 1 1023**Question 64****1 / 1 point**

Can the order of the following instructions be changed in a program without losing the overall meaning?

ADD R1, R2, R3**SUB R6, R2, R4** No, the instructions are output dependent No, the instructions are anti-dependent No, the instructions are true dependent Yes, the instructions are completely dependent**Question 65****0 / 1 point**

Which of the following data hazard solutions can completely eliminate stalls and achieve ideal pipeline speedups?

 Instruction scheduling Forwarding or bypassing Load delay slot Interlocking and stalling**Question 66****1 / 1 point**

Which of the following pipeline data hazard solutions puts the onus on the programmer to avoid possible hazards?

Interlocking and stalling



Forwarding or bypassing

Load delay slot

Instruction scheduling

None of these choices

Question 67**0 / 1 point**

What is the major problem with the LRU (Least Recently Used) page replacement policy?

Not efficient, processes that are least recently used tend to be needed in the future

None of these answers

Very computationally intensive

Hard to find time associated with process used

Attempt Score:59.7 %**Overall Grade (highest attempt):**59.7 %

Done