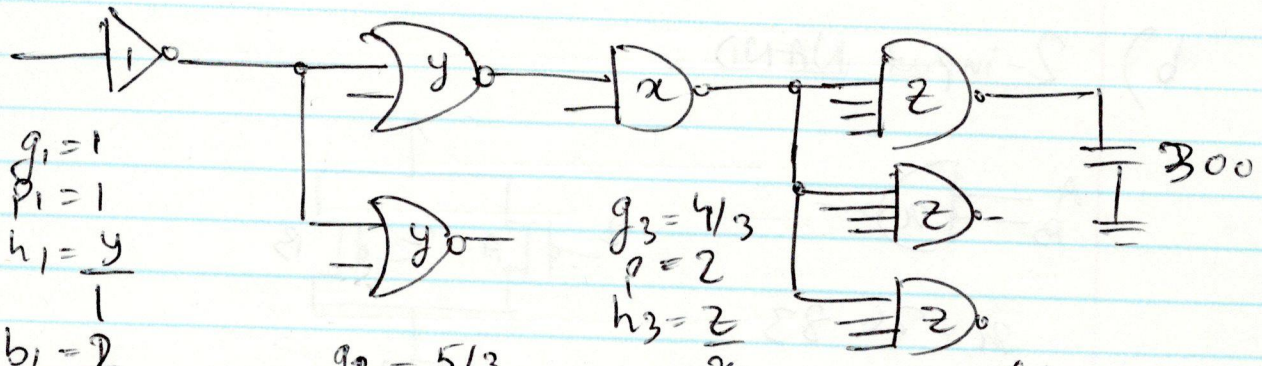
Q-3)



$g_1 = 1$
$p_1 = 1$
$h_1 = \frac{y}{1}$
$b_1 = 2$

$g_2 = 5/3$
$p_2 = 2$
$h_2 = \frac{x}{y}$
$b_2 = 1$

$g_3 = 4/3$
$p = 2$
$h_3 = \frac{z}{x}$
$b_3 = 3$

$g_4 = 6/3$
$p_4 = 4$
$h_4 = \frac{300}{z}$
$b_4 = 1$

a) $F = GBH$

$G = (1)\left(\frac{5}{3}\right)\left(\frac{4}{3}\right)\left(\frac{6}{3}\right) = 4.44$

$B = (2)(1)(3)(1) = 6$

$H = \left(\frac{y}{1}\right)\left(\frac{x}{y}\right)\left(\frac{z}{x}\right)\left(\frac{300}{z}\right) = 300$

$F = 8000$

$(F)^{1/N} = (8000)^{1/4} = 9.457$

$D_{min} = N(F)^{1/N} + \sum_i p_i$

$= (4)(8000)^{1/4} + 1 + 2 + 2 + 4$

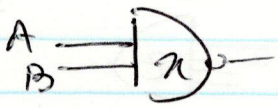
$D_{min} = 46.83$

$g_4 b_4 h_4 = \left(\frac{6}{3}\right)(1)\left(\frac{300}{z}\right) = 9.457$; $z = 63.44$

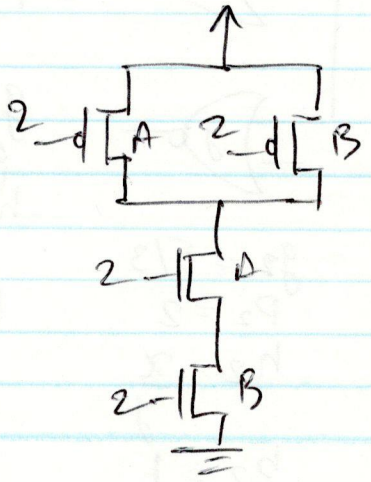
$g_3 b_3 h_3 = \left(\frac{4}{3}\right)(3)\left(\frac{z}{x}\right) = 9.457$; $x = 26.83$

$g_2 h_2 b_2 = \left(\frac{5}{3}\right)(1)\left(\frac{x}{y}\right) = 9.457$; $y = 4.728$

b) 2-input NAND



$x = 26.83$



PMOS: $26.83 \times \frac{2}{4} = 13.415$

width $= 13.415 \times 3C = 40.245C$

NMOS: $2683 \times \frac{2}{4} = 13.415$

width $= 13.415 \times 3C = 40.245C$

c) Optimum path delay

$(F)^{1/N} = (8000)^{1/N} = 3.59$

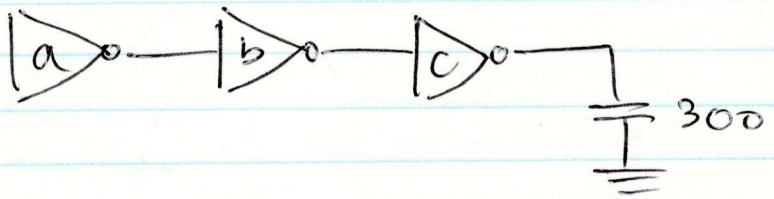
$\frac{\log 8000}{\log 3.59} = 7.03 \approx 7$

$D_{min} = (7)(8000)^{1/7} + 1+2+2+4+1+1+1$

$D_{min} = 37.27$

VATSAL SHREEKANT, 500771363

d) Since N=7 in part (c), hence 3 more stages/ inverters are to be added after the 4-input NAND.



$(8000)^{1/7} = 3.61$

$$\frac{300}{C}(1) = 3.61$$

$$\therefore C = 83.102$$

$$\frac{C}{b} = 3.61$$

$$\therefore b = 23.02$$

$$\frac{b}{a} = 3.61$$

$$\therefore a = 6.37$$

$$\left(\frac{6}{3}\right)\left(\frac{9}{z}\right) = 3.61$$

$$\therefore z = 3.53$$

$$\left(\frac{4}{3}\right)(3)\frac{z}{x} = 3.61$$

$$\therefore x = 3.91$$

$$\left(\frac{5}{3}\right)\left(\frac{x}{y}\right) = 3.61$$

$$\therefore y = 1.805$$