**Q1:**

Design a static CMOS gate that has the following output.

*Out = !(AB+CD)*

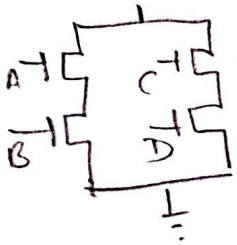
a) Draw the transistor-level schematic of your design. Sizing is not required. (5 marks)

b) Draw stick diagram of the gate you designed (please clearly label metal, poly, n-diffusion and p-diffusion regions on your stick diagram). (10 marks)

c) Estimate the area of the gate based on your stick diagram. (5 marks)

a) $Z = \overline{(AB+CD)}$ NMOS network.

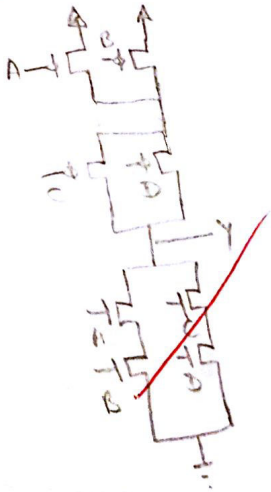
Pull up.




$Z = \overline{A \cdot B + C \cdot D}$

$= \bar{A}+\bar{B} \cdot \bar{C}+\bar{D}$

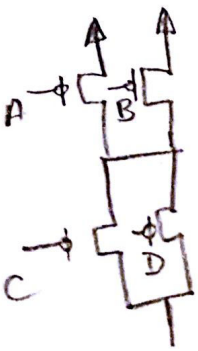
Together.



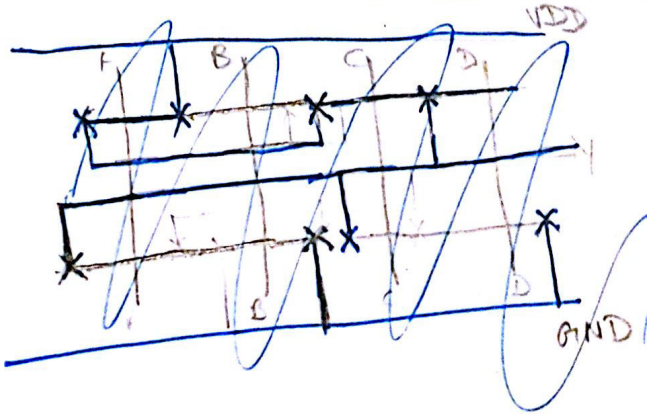

+5

NMOS

Pull down




b)



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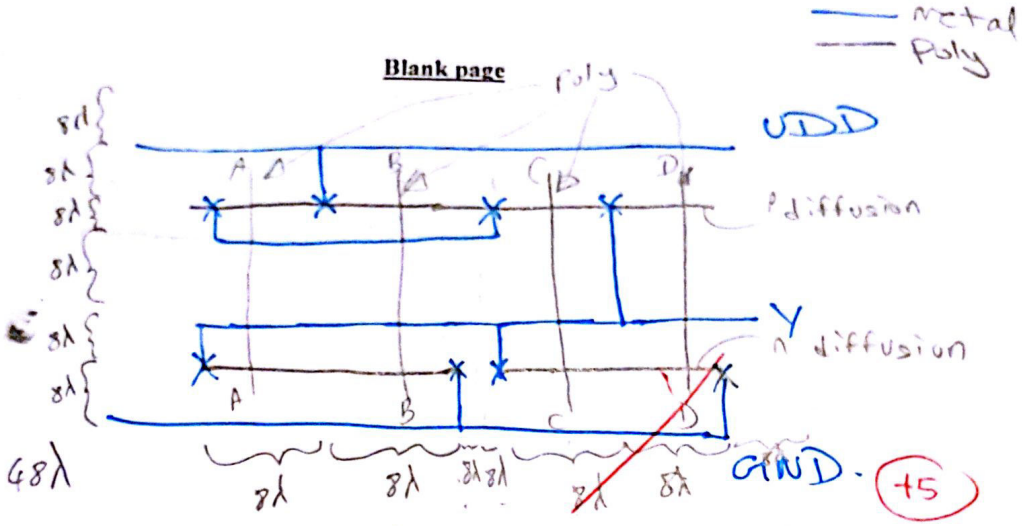



+5

$7 \times 8\lambda = 56\lambda$

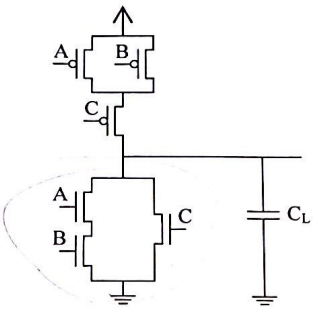
$48\lambda \times 56\lambda = 2688\lambda^2$ is the area of the gate based on my diagram

+3

**Q2:**

The on resistance of a unit nMOS is 12.5Kohms and the on resistance of a unit pMOS is 30Kohms. The following CMOS gate is driving a load ($C_L$) of 125fF. Assume the drain and source capacitance of each transistor is 0F.

a) Size the gate to have a $t_{pdr} < 1900ps$ and $t_{pdf} < 1600ps$. (10 marks)
b) Sketch the layout of the nMOS connected to B. (5 marks)
c) Sketch the layout of the pMOS connected to B. (5 marks)




nMOS $R_n = 12.5k\Omega$.
pMOS $R_p = 30k\Omega$.

$t_{pdr} < 1900ps$ ...1
$t_{pdf} < 1600ps$ ...1

$1\mu s = 1F$.

a) (+1.5)

$(C_L + C_f) R_n < 1600ps$ ...1

$(C_L + C_R) R_p < 1900ps$ (+1.5)

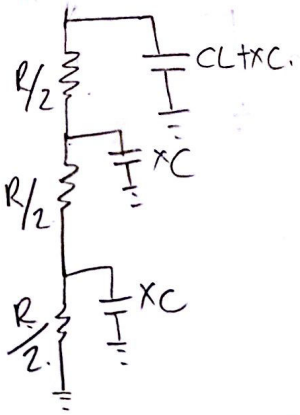
$C_f = \frac{1600\Omega s}{12.5k\Omega} - 125fF$

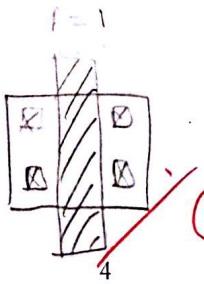
$= 3 \times 10^{-15} = 3F$

$C_R = \frac{1900ps}{30k\Omega} - 125fF$

$= 6.166 \times 10^{-14} = 61.6F$

b)




(+2)

4

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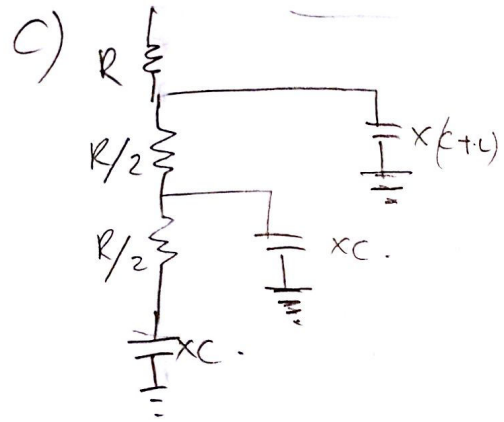
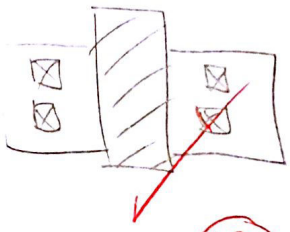
c)

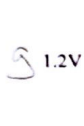


+2

**Q3:**

Calculate $I_{ds}$ using the long channel model for the following transistor. Assume $V_t$=0.3V and $\beta$=262W/L $\mu A/V^2$. (20 marks)




$I_{ds}$ NMES. I-V characteristics:

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta(V_{GT} - V_{ds}/2)V_{ds} & V_{ds} < V_{gt} \quad \text{linear} \\ \frac{\beta V_{GT}^2}{2} & V_{ds} > V_{GT} \quad \text{saturation} \end{cases}$$

$V_{ds} = V_d - V_s = 0.8 - 0.7 = 0.1V$.

$V_{GT} = V_{gs} - V_t = 0.5V - 0.3V = 0.2V$.

$V_{gs} = V_g - V_s = 1.2 - 0.7 = 0.5V$

$V_{ds} = 0.1V$. } $V_{ds} < V_{gt}$ ⇒ linear region (+10)

$V_{gt} = 0.2V$ }

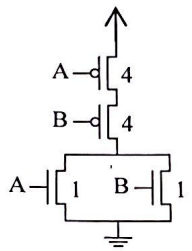
$$I_{ds} = \beta(V_{GT} - V_{ds}/2)V_{ds} \quad (+5)$$

$$= (262)(0.2 - \frac{0.1}{2})0.1$$

$$= 3.93A$$

**Q4:**

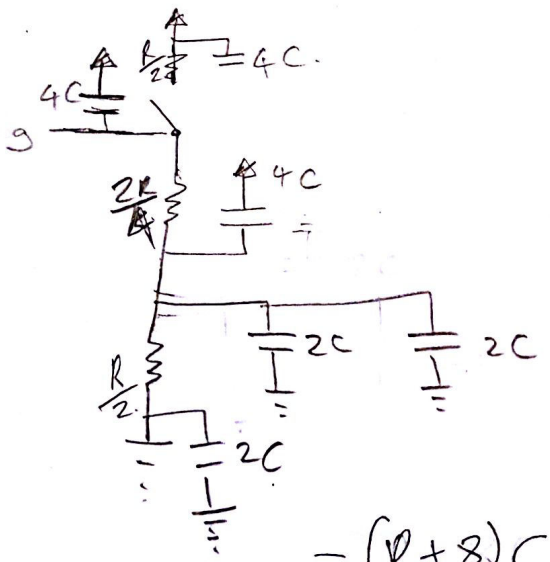
Calculate the worst case pull-up and pull-down logic effort and the parasitic delay of the following gate (please account for all internal diffusion capacitances in your calculations). (20 marks)




Pull up.

discharge

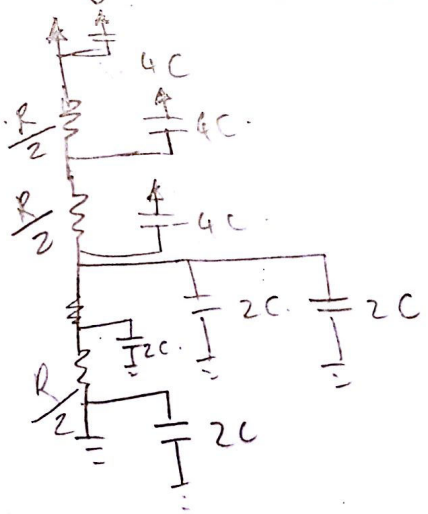
A=1 B=0




$= (R+8)C$

charge.

A=1 B=1



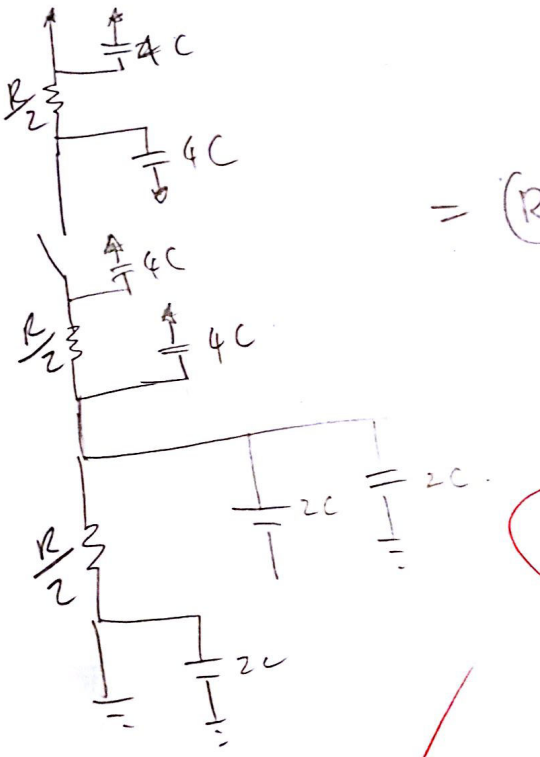

$= (2R+8)C$

Blank page

Pull down.

charge

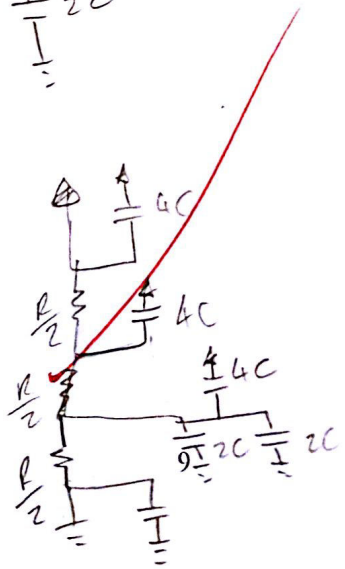
A=0 B=1.




$= (R + 8)C$

+3 for effort

discharge.



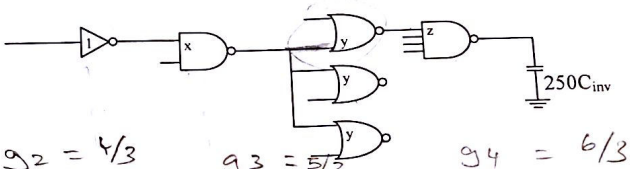

$A = \left(\frac{3R}{2} + 8\right)C$

**Q5:**

a) Calculate the optimum path delay for the following circuit, where the inverter in the circuit is a unit inverter and $C_{inv}$ is the input capacitance of a unit inverter. (inverter: g=1, p=1; 2-input nand: g=4/3, p=2; 2-input nor: g=5/3, p=2; 4-input nand: g=6/3; p=4). (5 marks)

b) Draw the CMOS structure of the nor gate and clearly label the size of each transistor on your drawings. (10 marks)

c) What will be the optimal delay if you can insert additional inverters at the end of the 4-input nand gate? (5 marks)




$g_1 = 1$ $\quad h_1 = \frac{x}{1}$ $\quad p_1 = 1$

$g_2 = 4/3$ $\quad h_2 = \frac{3y}{x}$ $\quad p_2 = 2$

$g_3 = 5/3$ $\quad h_3 = \frac{2z}{y}$ $\quad p_3 = 2$

$g_4 = 6/3$ $\quad h_4 = \frac{250\,c_{in}}{z}$ $\quad p_4 = 4$

$F = G_1B_1H_1$

$= \left(\frac{x}{1}\right)\left(\frac{4}{3}\right)\left(\frac{3y}{x}\right)(2)\left(\frac{5}{3}\right)\left(\frac{z}{y}\right)(2)\left(\frac{6}{3}\right)\left(\frac{250\,c_{in}}{z}\right)(4)$

$= \left(\frac{4}{3}\right)(4)\left(\frac{5}{3}\right)(6)(250)(4) = \left(\frac{20}{9}\right)(24)(1000)$

$= 53333.333\,c_{in}$

$F^{1/4} = (53333.333\,c_{in})^{1/4} = 15.196\,c_{in}$ (+3)

$15.196 = \log_{4/3} h_1 p_1$

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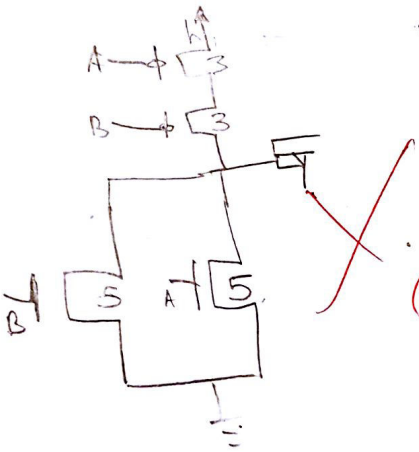
b) NOR Gate.

$g_1 h_1 p_1 = 15.196 C_{in} = h_1$




$h_2 = \frac{3Y}{X} = \frac{3Y}{h_1} = \frac{3Y}{15.196 C_{in}}$

$3Y = (h_2)(15.196 C_{in})$.

+3

c) if more inverters are added, the optimal delay would not change, as they have.

$g_1 = 1$

$p_1 =$

+1