

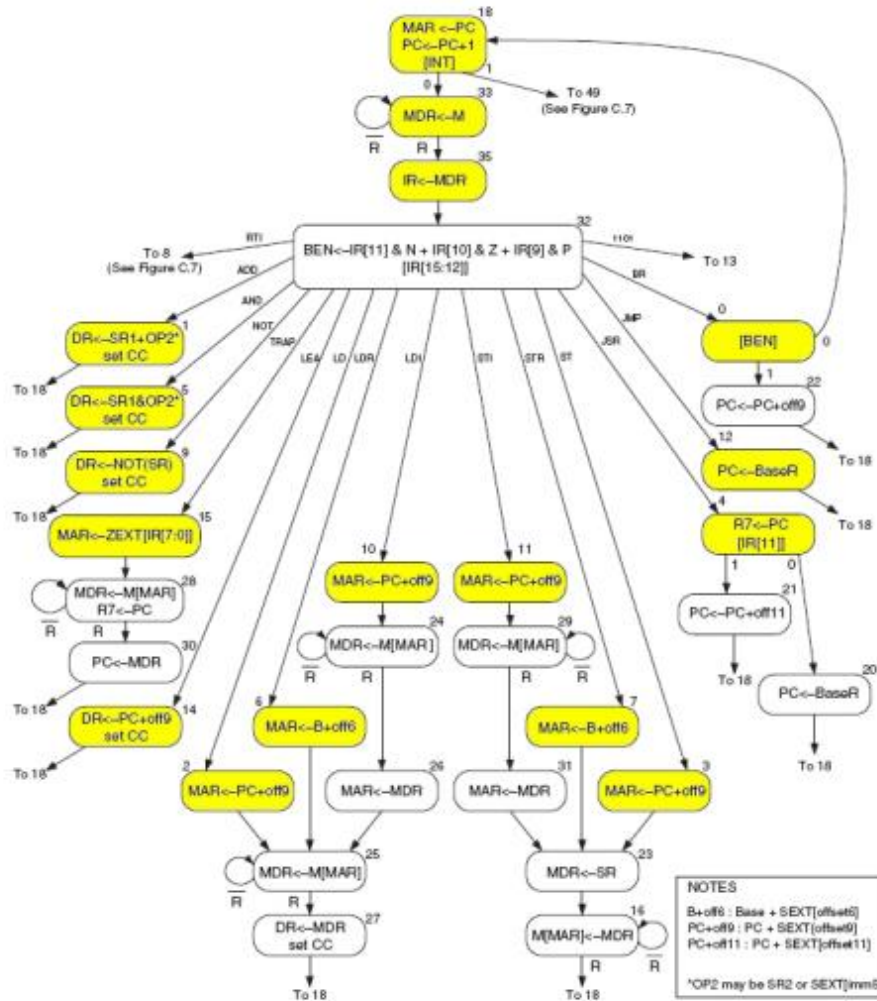
LC-3 Instruction Set

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ADD ⁺	0001				DR			SR1		0	00			SR2			DR ← SR1 + SR2; set NZP
ADD ⁺	0001				DR			SR1		1				imm5			DR ← SR1 + SEXT(imm5); set NZP
AND ⁺	0101				DR			SR1		0	00			SR2			DR ← SR1 AND SR2; set NZP
AND ⁺	0101				DR			SR1		1				imm5			DR ← SR1 AND SEXT(imm5); set NZP
BR	0000			n	z	p											IF ((n·N)+(z·Z)+(p·P)) THEN PC ← PC + SEXT(PCoffset9)
JMP	1100				000			BaseR						000000			PC ← BaseR
JSR	0100			1													R7 ← PC PC ← PC + SEXT(PCoffset11)
JSRR	0100			0		00		BaseR						000000			R7 ← PC PC ← BaseR
LD ⁺	0010				DR												DR ← M[PC + SEXT(PCoffset9)]; Set NZP
LDI ⁺	1010				DR												DR ← M[M[PC + SEXT(PCoffset9)]]; Set NZP
LDR ⁺	0110				DR			BaseR						offset6			DR ← M[BaseR + SEXT(offset6)]; Set NZP
LEA ⁺	1110				DR												DR ← PC + SEXT(PCoffset9); Set NZP
NOT ⁺	1001				DR			SR						111111			DR ← NOT(SR); Set NZP
RET	1100				000			111						000000			PC ← R7
RTI	1000																IF (PSR[15]==0) THEN PC ← M[R6]; R6 ← R6 + 1; TEMP ← M[R6]; R6 ← R6 + 1; PSR ← TEMP
ST	0011				SR												M[PC + SEXT(PCoffset9)] ← SR
STI	1011				SR												M[M[PC + SEXT(PCoffset9)]] ← SR
STR	0111				SR			BaseR						offset6			M[BaseR + SEXT(offset6)] ← SR
TRAP	1111				0000												R7 ← PC PC ← M[ZEXT(trapvect8)]

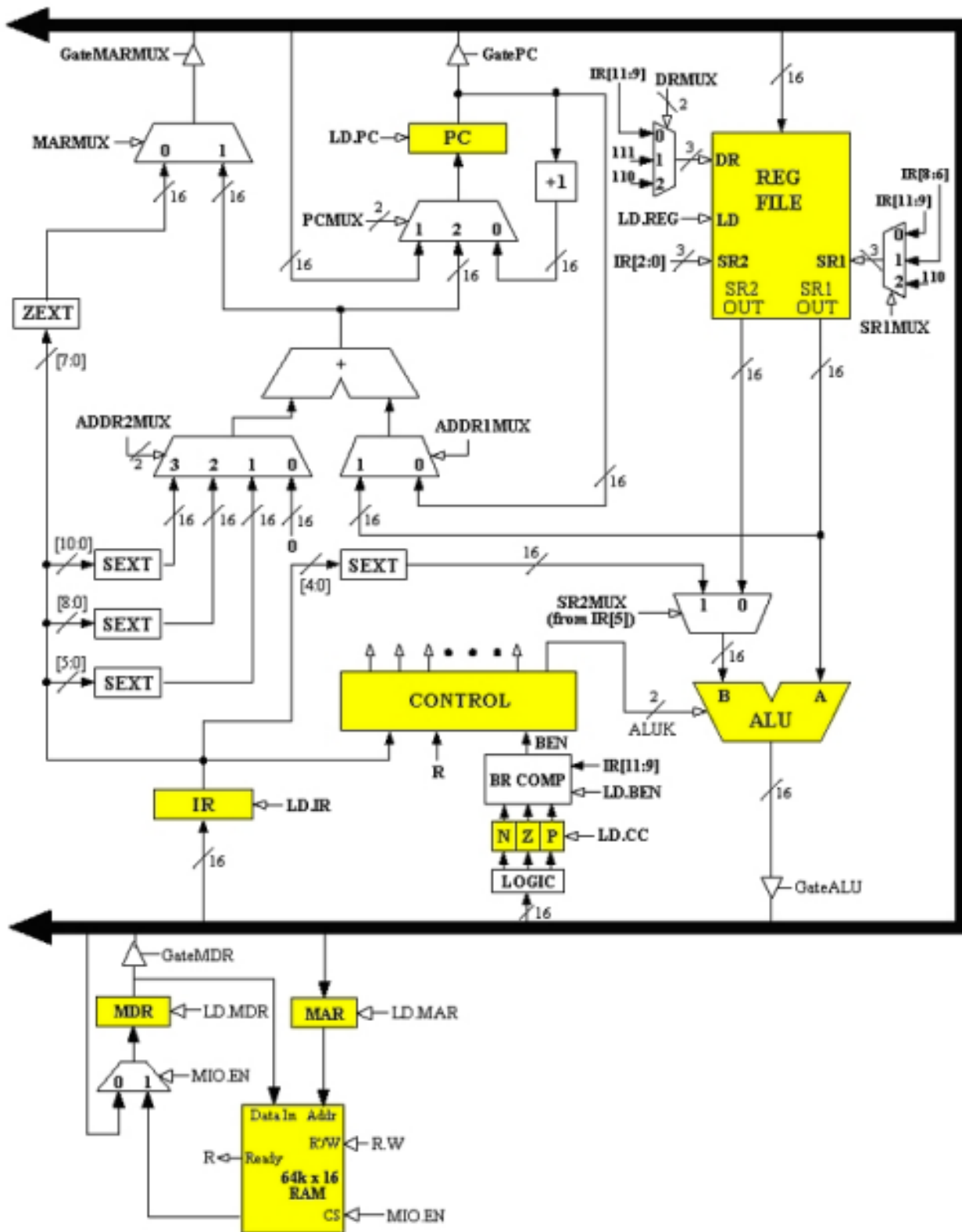
superscript "+" denotes instructions that update the condition bits NZP

LC3 ISA

LC-3 FSM



LC-3 Datapath



Signal	Description	Signal	Description
LD.MAR	= 1, MAR is loaded	LD.CC	= 1, updates status bits from system bus
LD.MDR	= 1, MDR is loaded	GateMARMUX	= 1, MARMUX output is put onto system bus
LD.IR	= 1, IR is loaded	GateMDR	= 1, MDR contents are put onto system bus
LD.PC	= 1, PC is loaded	GateALU	= 1, ALU output is put onto system bus
LD.REG	= 1, register file is loaded	GatePC	= 1, PC contents are put onto system bus
LD.BEN	= 1, updates Branch Enable (BEN) bit		
MARMUX	$\begin{cases} = 0, \text{ chooses ZEXT IR}[7:0] \\ = 1, \text{ chooses address adder output} \end{cases}$	MIO.EN	$\begin{cases} = 1, \text{ Enables memory,} \\ \quad \text{chooses memory output for MDR input} \\ = 0, \text{ Disables memory,} \\ \quad \text{chooses system bus for MDR input} \end{cases}$
ADDR1MUX	$\begin{cases} = 0, \text{ chooses PC} \\ = 1, \text{ chooses reg file SR1OUT} \end{cases}$	R.W	$\begin{cases} = 1, M[\text{MAR}] < \text{MDR when MIO.EN} = 1 \\ = 0, \text{ MDR} < M[\text{MAR}] \text{ when MIO.EN} = 1 \end{cases}$
ADDR2MUX	$\begin{cases} = 00, \text{ chooses "0...00"} \\ = 01, \text{ chooses SEXT IR}[5:0] \\ = 10, \text{ chooses SEXT IR}[8:0] \\ = 11, \text{ chooses SEXT IR}[10:0] \end{cases}$	ALUK	$\begin{cases} = 00, \text{ ADD} \\ = 01, \text{ AND} \\ = 10, \text{ NOT A} \\ = 11, \text{ PASS A} \end{cases}$
PCMUX	$\begin{cases} = 00, \text{ chooses PC} + 1 \\ = 01, \text{ chooses system bus} \\ = 10, \text{ chooses address adder output} \end{cases}$	DRMUX	$\begin{cases} = 00, \text{ chooses IR}[11:9] \\ = 01, \text{ chooses "111"} \\ = 10, \text{ chooses "110"} \end{cases}$
SR1MUX	$\begin{cases} = 00, \text{ chooses IR}[11:9] \\ = 01, \text{ chooses IR}[8:6] \\ = 10, \text{ chooses "110"} \end{cases}$		