Python Developer Python Developer Server Repaired Enginner - Synnex San Jose, CA 3.5+ years of experience in Hardware troubleshooting, Embedded, Firmware and Software industry. Worked on PCB design, schematic layout and troubleshooting for Motherboard, CPU, DIMMs and power supply. Self-motivated, multi-tasking, quick learner, good leadership and communication skill Work Experience Python Developer Schneider - Green Bay, WI June 2018 to Present " Developed entire frontend and backend modules using Flask Web Framework, HTML, CSS, JS, jQuery, Bootstrap and MapR DB for internal web application. " Write Python scripts to load data from Apache Logs into MapR DB collections table and render to web UI portal. " Experience working on Anaconda Platform for large scale data processing and Conda for package management and environment management. " Good knowledge of Python libraries such as Numpy, Panda and Bokeh for visualization. Server Repaired Engineer Synnex - Fremont, CA April 2017 to Present Performed Server component installations, cabling, testing, troubleshooting, repairs, calibrations. Handled the responsibility of trouble shooting in server e.g. mother boards, DIMMs, CPUs, NIC and Riser cards, Soiled state drive, SAS controller and upgrade operating system according to server version. Detailed understanding of error information SEL Log error, BMC stability, thermal issues, burned -in testing and hardware SKU firmware driver issues. Performing POST test for recently built or upgraded servers to see if all new hardware has registered. Hardware and Embedded Systems Engineer February 2015 to July 2015 Extensive experience in the design, simulation, characterization, and testing of different microcontrollers (8051 and ARM) and circuits. PCB Validation Engineer PCB Planet June 2013 to February 2015 Worked on schematic diagram and technical functions included validation on PCB designing, testing, modifying, fabricating, multi-level design circuit boards including both surface mount AND through-hole technology in pre-production stage Evaluated and debugging design error between Track - Track Spacing, Pad - Track Spacing, Drill - Drill Clearance, Mask - Track Clearance, Pad / Trace - Edge clearance, Single Tracks, Customer panel (Sub panel / Array), Thermal pads, Via, Tented via, Unterminated Traces / Hanging Traces or Single Tracks in PCB board Detailed understanding of error information and then given appropriate suggestion for customer supports and maintain the system to solve their

problems Embedded System Engineer(Intern) Vector(Ind.) Lmt - Hyderabad, Telangana January 2013 to June 2013 Developed software for car security system in C, C++ and Assembly Language Responsible for Linux system I/O programming such as TCP/IP, UDP Education MS in Electrical Engineering Northwestern Polytechnic University September 2015 to April 2017 Skills PCB (2 years), VERILOG (2 years), UNIX (1 year), AUTO CAD (Less than 1 year), CAD (Less than 1 year), Python (2 years), C++ (2 years), Embedded C (1 year), Verilog (1 year), System Verilog (1 year), Cadence Allegro (1 year), Django, Flask, C, Javascript, Restful, Linux Links https://www.linkedin.com/in/jigar-shah-system-engineer/ Additional Information " Programming Languages: C, C++, Embedded C, UNIX Shell Scripting, System Verilog, Keil (8051 & ARM) " Scripting Language: Python " Protocols: PCIe, USB, Ethernet, DDR, I2C, SPI " EDA/CAD/Software tools: U-cam PCB checking tool, Synopsys design compiler, OrCAD PCB Designer, Cadence Allegro PROJECTS Silicon Validation Board Diagram and interface with different module Tools/Languages: OrCAD-PCB-Design " Designed architecture circuit module which interconnects with different microcontrollers, power Supply, RJ connector, POR Chip, Transformer schematic & layout design and then checked DRC rules in that circuit. " Routed the board and added a text to identify the board and connectors in those circuits Analysis of Circuit Design using SOC encounter Tools/Languages: Cadence SOC Encounter " Converted a Verilog file into Gate Level Design and Synthesized Circuit " Analysis of backend design, floor planning, power, clock distribution and checked DRC rules for improve production accuracy and cost " Checked design architecture and automatic and manual routing in single side, double side circuit Test automation script Tools/Languages: Python " Developed a python base script that analyzed garbled data generated by PCB schematic tools e.g. Drill, SMD Pad, and Silk Screen to store that information into different file. " Added the constant number of the value given by the user and maintained the required spacing using the script

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