Intern Intern Intern Houston, TX VLSI Design Engineering graduate looking for full time opportunities in RTL design/verification/Physical Design. Knowledge of ASIC design flow, Static Timing Analysis (STA), CMOS Design, FPGA, ATPG, Design for testability, BIST, Basics of Computer Architecture, Bus protocols (APB, AHB, I2C) Work Experience Intern Xilinx - Hyderabad, Telangana May 2017 to March 2018 Involved in writing and modifying Perl scripts. Filed Bug reports, verified RTL fixes, analyzed test results and performed coverage analysis. Mastered all back-end design tools including but not limited to floor-planning, place & route, LVS, DRC, static timing, clock-tree balancing, power grid analysis and layout, extraction, and signal integrity Python Developer Hyderabad, Telangana November 2012 to March 2015 Backend scripting/ parsing using Python and perl Designed and developed data management system using MySQL. Built application logic using python 2.7. Designed a web-based system to improve business intelligence, logistics, manage inventory and sales, and forecast demand. The system will be used by over one hundred employees in surat. Documented the simulation steps for debug using shell scripting. Industrial Intern Steel Plant - Visakhapatnam, Andhra Pradesh October 2011 to February 2012 Reviewed the Television Broadcasting process which gave deep insight into the signal processing. Studied the transmission of the signals and how they are processed after reception to show the picture on Television screen and gained knowledge on how it broadcasts on digital terrestrial transmitters. Education Bachelor of Technology in Electronics and Communication Engineering Jawaharlal Nehru Technological University - Kakinada, Andhra Pradesh November 2015 to April 2017 Master of Science in VLSI Design Jawaharlal Nehru Technological University - Kakinada, Andhra Pradesh

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