DDR Validation Engineer DDR Validation Engineer DDR Validation Engineer Santa Clara, CA Seeking a challenging career position in the field of Validation and emulation, Computer Architecture and Digital VLSI/ASIC Design. Work Experience DDR Validation Engineer Google - Mountain View, CA November 2018 to March 2019 Enabled Dynamic Self refresh and Dynamic Clock Control on airbrush IP and found out power savings and memory latencies in State 9. Did this experiments on all frequencies of DDR. ? Ran bandwidth tests to validate the QOS register and BRB arbitration registers in memory controller to see BW shift between read and write DMA channels of IPUand between ports(IPU and PCIe ports). ? Tried to enable PASR to see power saving delta's. ? Debugged with engineers on the stress test failing scenarios. System Validation Engineer(SVE Team) Qualcomm - San Diego, CA January 2018 to September 2018 Owner of Vmin tests across all rails of SOC for SVE team. ? Worked towards health of all Vmin tests by building convex workspaces, executing tests, reporting out problems to IP owners, filing jira's and responsible for releasing Vmin tests to HVV team for data collection. ? Did pathfinding experiments like trying out new vectors for different sub-systems in convex, doing 2D shmoo's and reporting issues to make the SVE Vmin ecosystem better for future. ? Also worked with Convex team in reporting out issues to make Vmin tests work smoothly. ? Worked on CPU Correlation devices to match SVE results with ATE and SPT teams. Tried buffer size experiments on vectors and shmoo hole check experiments. Used to present data to team and to SVE CPU team. ? Also responsible for delivering Fmax tests to HVV for data collection. ? Also did MEMVEX failing pattern experiments and running Vmin tests at different temperatures to correlate data with other teams. Circuit and System Validation Engineer Qualcomm - San Diego, CA May 2017 to January 2018 Ramped up on HDD document for DDRPHY. ? Worked on building a tool called DDRPHYVIEW tool, which will populate the circuit with coarse and fine values and generate timing diagrams. ? Generated read and write eyes using the DART tool for analysis of FF and SS parts. ? Responsible for delivering DDRPHY firmware memory training code for product after product ? Ramped up on DSF Design verification for debug purposes. This involves running simulations, checking FSDB waveforms to check problems and then take the settings and try it on firmware to debug issues that come up. Python Developer North

Dome Solutions July 2016 to May 2017 Doing predictive analysis and what if big data analysis for business solutions for client Maxwell. The environment is HDFS, Spark Machine Learning lib, MapReduce, hive, pig, Kafka and Sqoop. Design Verification engineer Qualcomm - Bengaluru, Karnataka September 2015 to May 2016 Generating vectors, evcd files and converting them to bin files for ATE testers. Running RTL, RTL+VECTOR, GLS and VT simulations on pre-silicon environment. This involves RTL validation, running simulations, loading waveforms and debugging if there was an issue. Was responsible for 180 vectors of total. BIOS Debug Engineer BIOS Validation Engineering - Bengaluru, Karnataka July 2014 to May 2015 Part of BIOS validation team. Ramped up on BIOS source code to debug the BIOS sightings. ? Also responsible for building a power measurement capability for BIOS debug. ? Created a mind-mapping diagram of BIOs and a high-level document for doing exploratory testing of BIOS. It includes all the features in Silicon, platform and devices. ? Enabled Pre-silicon BIOS automation environment, so that the BIOS test case automation can be done in Pre-silicon environment. This work was Demo'ed in Intel Oregon Demo day. ? Worked on SGX execution and automation of test cases. ? Ramped up on PCH, ME and responsiveness test cases and worked on automation acceptance. ? Worked on developing firmware workarounds for Post silicon validation for certain bug fixes. ? Debug failing tests and then work with developers and architects to resolve bugs. AHEAD driver for Blu SKYLAKE CPU 2015 to 2015 2015). Was responsible for defining the Test-Plan & Methodologies, which laid the foundation for Architecture data and providing Proof of concept. The Architecture data in detail consists of CPU C & P-state residencies and unhalted CPU Clock cycle distribution over processes, DMI Link state residencies; DRAM Traffic (bandwidth) numbers, Platform and component Power numbers and GT & CPU overlap percentages. Conducted these experiments on Existing and next Generation Platforms with different Windows Operating Systems & various configurations of Interest and all with HD-Media Playback. ? Contributed to the efforts of showcasing power savings on the platform using READ-AHEAD driver for Blu-ray. Further validated the RA-driver on existing Platforms with different Windows OS and identified bugs which helped in optimizing the RA driver using WinDBG. ? Working on Audio-Input path workload characterization for Power and Performance optimizations for

next generation platforms. ? Laid the foundation in majoring the initial architecture data for LPD experiments on ATOM-based Platforms. Developed Menlow & Montevina based systems for conducting Power & Performance measurements to showcase the power savings on LPD Vs HPD Platforms. ? Developed Montevina-based system to conduct DRAM compression and Partial DRAM power down experiments, to understand the CPU power and time consumed in compressing and decompressing the memory dump of one of the DIMMs. ? Developed VI's in Labview to monitor multiple Voltage rails on Platform at a rate of 2u secs and also developed Perl scripts for post processing the data. ? Gained valuable hands-on experience with the tools like ITP, NOA Tool, LA, GPUVIEW, NETDAQ, NI-DAQ & LABVIEW, ? Xperf, Platune, SEP, Vtune and Perfmon. Post Silicon Validation Engineer Platform Validation Engineering - Folsom, CA August 2012 to October 2013 Was part of the Memory controller Validation team. Ramped up on SOC Validation Methodologies and Memory controller debug. Familiar with DDR and LPDDR3 protocol. Worked with Pre-silicon Team for RTL bugs and closing/solving sightings. Worked on DDR debug, DDR training and PVT execution. Ran regression tests as well. Used JTAG based debug tools (ITP). ? Developed some stand-alone python scripts which will set DDRCTS triggers for various states on ACC bus. ? Worked on POWER-ON i.e. silicon bring-up and enabling. ? Debugged low-level software and hardware issues and implemented drivers and test content. ? Worked in solving bugs on memory controller and system agent. ? Worked in executing test cases on emulation platforms generation over generations and also worked on emulation development as well. ? Familiar with PCIe and Ethernet protocol. Power and Performance Engineer (Platform Architecture) Intel, Jones Farm February 2010 to August 2012 Worked on Media Playback power & performance characterization and presented the findings at cross functional forums at Intel. ? Worked on third party NEC & FRESCO usb3 power & performance evaluation on Intel platforms. ? Worked in developing a bulk camera prototype in embedded C (CYPRESS Company) to showcase the power benefit. ? Worked on analyzing network (LAN & Wifi) interrupts for doing power & performance evaluations. Used protocol analyzer to analyze the network traffic. Ramped up on TCP-IP protocol. ? Developed, tested and validated emulation platform. Validated PCIe OBFF feature on slim-river

board using Greenspond FPGA. Made changes in RTL in modifying the path (PM Req and PM sync messages) using GPIO's and with BLA tool. ? Characterized and presented HTML5 power & performance impact on Intel Platforms. Internship Intel, Jones Farm - Folsom, CA 2008 to January 2010 Education MS in Electrical & Electronics Engineering California State University December 2009 BS in Electrical & Electronics Engineering JNTU May 2006 Skills analyzer (2 years), FUELS (1 year), JTAG (1 year), Labview (1 year), Perl (1 year) Certifications/Licenses Driver's License Additional Information SKILL SET: ? HDLs: Verilog, VHDL, SystemVerilog, UVM ? Languages and Scripts: C, C++, Assembly, PERL, Python, TCL, Primetime, MATLAB ? Tools: Oscilloscope, Logic Analyzer, Protocol Analyzer, Xperf, Perfmon, NETDAQ, NI -DAQ SEP, GPUVIEW, PSpice, ModelSim, XILINX ISE tool, JTAG ITP, Vtune, Labview,WinDBG Synopsys Design Analyzer, VCS compiler, L-edit and Platune, Wireshark and Microsoft Network Monitor, spectrum and Network analyzer ? Operating Systems: Windows, Linux.

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