Digital Designer/Embedded Firmware Developer/ Python Scripter Digital Designer/Embedded Firmware Developer/Python Scripter Firmware/Logic/FPGA Designer Plano, TX EXPERTISE: Digital Logic Design FPGAs Mixed-Signal Integrated Circuits Python Script Expert Device Drivers and laboratory software Embedded Software Development Systems Integration PCBs Authorized to work in the US for any employer Work Experience Digital Designer/Embedded Firmware Developer/ Python Scripter Texas Instruments (contract through Talent 101) - Dallas, TX June 2016 to December 2018 Digital design engineer on a mixed-signal power management device. Designed three Verilog modules and simulated with Cadence s Incisive simulator. Created a multi-device simulation testbench to simulate a new communication block. Developed a Python based ARM cortex M0+ device emulator to allow pre-silicon debugging of embedded ROM code. Simulates code from the Keil tool set. Developed ROM code to program/erase flash memory. Developed Python digital signature analysis to validate battery pack authenticity. Developed a Python based Verilog code generator for a register file from an XML description. Wrote a Python script to generate Verilog AMS interface modules. Wrote Python script to analyze device parasitics to quantify noise in a new mixed-signal device. VP Engineering AMS/Texas Advanced Optical Solutions - Plano, TX October 2007 to December 2015 Worked with customers to establish product requirements and consolidate them into device specifications and development plans. Primary architect and lead the IC mixed-signal development team. Products included various optical sensors. Created custom laboratory characterization equipment using stepper motors and a PLC. Developed both Python and C based laboratory environments to validate and debug new devices. Developed bring-up/validation printed circuit boards. Wrote the CAD flow used by all TAOS devices. VP/GM Broadcom Corporation - Santa Clara, CA September 2005 to July 2007 General manager of the embedded and secure processor (ESP) and chipset and storage infrastructure (CSI) lines of business. Led the ESP team in a transition from being a high-end niche microprocessor business into a high volume security business with multiple wins at a major PC OEM in addition to a leading point-of-sale terminal vendor. Director of PQ3/PQ4 Operation Motorola Semiconductor/Freescale Semiconductor - Austin, TX 2002 to 2005 Product manager for

the PowerQUICC3 product line, leading the product line from incubation to a product line with over $400M in design wins. Specifically hired as part of the leadership team to bring the Networking Division back from the 2000 industry meltdown. Initial focus was to regain customer trust in Motorola and to reduce R&D spend down to acceptable levels. Once the first PQ3 device was released to the mask shop, shifted focus to developing the newest PowerQUICC product line business. Engineering Director Zilog Inc - Austin, TX 1999 to 2002 Managed Austin site, a processor development team, and the CAE department. Led a twenty-two person engineering team spread across three US locations and two international locations. Developed the architecture for a new for multi-core embedded communication device. Led the design team. Device was production worthy on first silicon. Sr Member of Technical Staff Motorola Semiconductor (Freescale) - Austin, TX 1988 to 1997 Started a new design team focused on embedded processing communication and networking. Managed the development of Motorola s first 100Mbps Ethernet embedded device. Was the architect and lead developer of Motorola s first 10Mbps Ethernet embedded device. Represented Motorola at both the IEEE Ethernet standards committee and the ANSI TP-PMD/FDDI standards meetings (the latter was adopted by the 100Mbps Ethernet standard). Networking Design Manager SGS-Thompson MicroElectronics/ UTC Mostek - Carrollton, TX 1983 to 1988 Hired as the initial design engineer in a new group focused on digital networking devices. Was responsible for the development and direction of the 1Mbps Ethernet product line. Developed a X25 wide area network protocol controller. Developed a logic simulator and CAD flow. Member of Technical Staff AT&T Bell Laboratories - Denver, CO 1979 to 1983 Member of an exploratory systems development group examining integration of packet switch technology within the PBX circuit-switch environment. Education MSEE Purdue University Bachelor's in Electrical Engineering Cal Poly State University - San Luis Obispo, CA Skills Digital and mixed-signal chip development experience. (10+ years), Front-end specification and RTL Verilog design. (10+ years), Embedded Firmware Development (C, Arm/Keil tools, Arduino). (10+ years), Directed/random self-checking Verilog simulation test bench generation. (10+ years), Embedded processor/micro-controller design and integration. (10+ years), Processor emulators (Arm Cortex M0+, 8080, Bendix G15).

(10+ years), Incisive NCSim, VCS, NC-Verilog, Verilog-XL, SureCov, Icarus Verilog. (10+ years), Revision control using CVS, Git, and DesignSync. (10+ years), Custom, mixed-signal, and FPGA chip design. (10+ years), Scripts for CAD flows (Python, Unix Shell). (10+ years), Verilog hierarchy generators (C). (10+ years), Verilog register map generator (Python). (1 year), Voting member of the IEEE Ethernet standards committee for 15 years. (10+ years), Pre-/Post- sales customer interface to gather requirements and to support post-silicon. (10+ years), Project management (including project estimation and budget). (10+ years), PCB development. (6 years), C, Linux, Uart, Embedded, Fpga, Debug, Microcontrollers, Debugging Patents Signal Conditioning Circuit for a Light Sensor, a Sensor Arrangement and a Method for Signal Conditioning for a Light Sensor (#20140252212) Light Sensor Arrangement and Method for Temperature Compensation in a Light Sensor Arrangement (#10006806) 2018-06 Context Switching Pipelined Microprocessor (#6915414) Apparatus and Method for Encoding Data in a Fiber Data Distributed Interface (FDDI) (#5655078) Method for Switching Data Flow in a Fiber Distributed Interface (FDDI) System (#5539733) Local Area Network Data Processor System Containing a Quad Elastic Buffer and Layer Management (ELM) Integrated Circuit and Method of Switching (#5442628) Arbitration Among Multiple Users of a Shared Resource (#5263163) Variable Length Packet Switching System (#4704606) Clock Recovery Circuit (#4694196) Multiphase Packet Switching System (#4656627) Distributed Packet Switching System (#4631534) Method and apparatus for generating a hierarchical interconnection description of an integrated circuit design and using the description to edit the integrated circuit design (#5892682) 1999-04

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