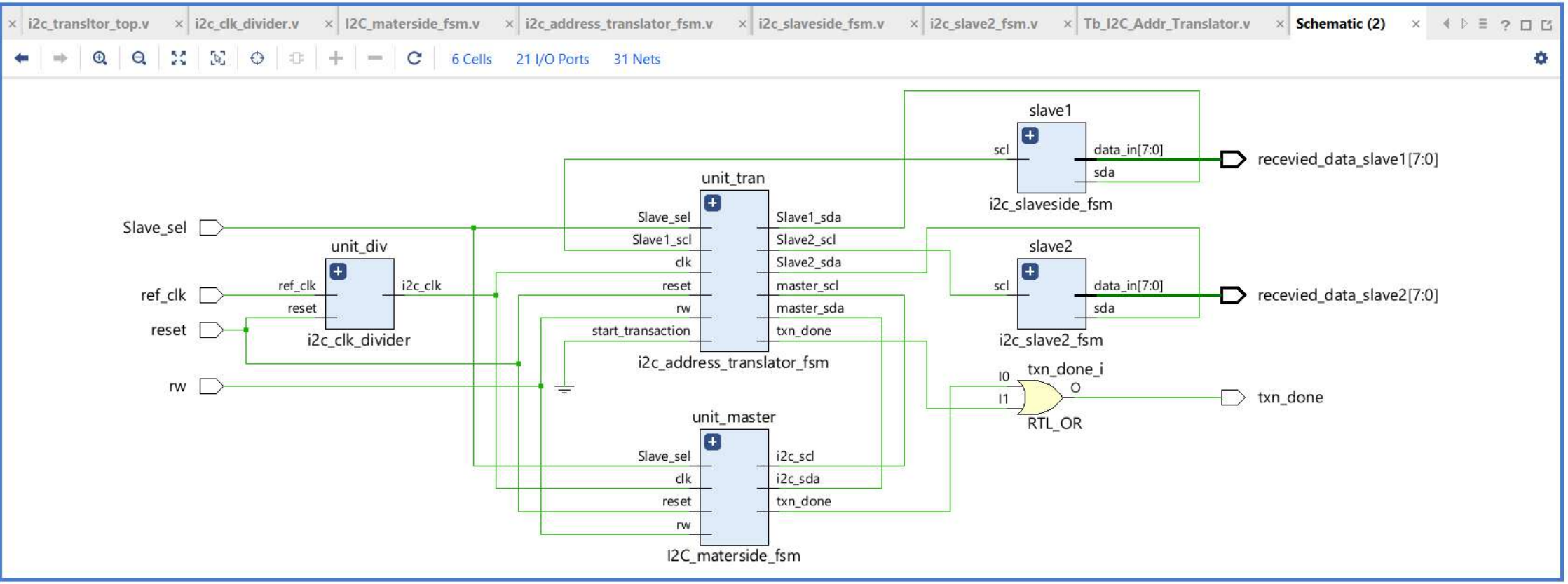
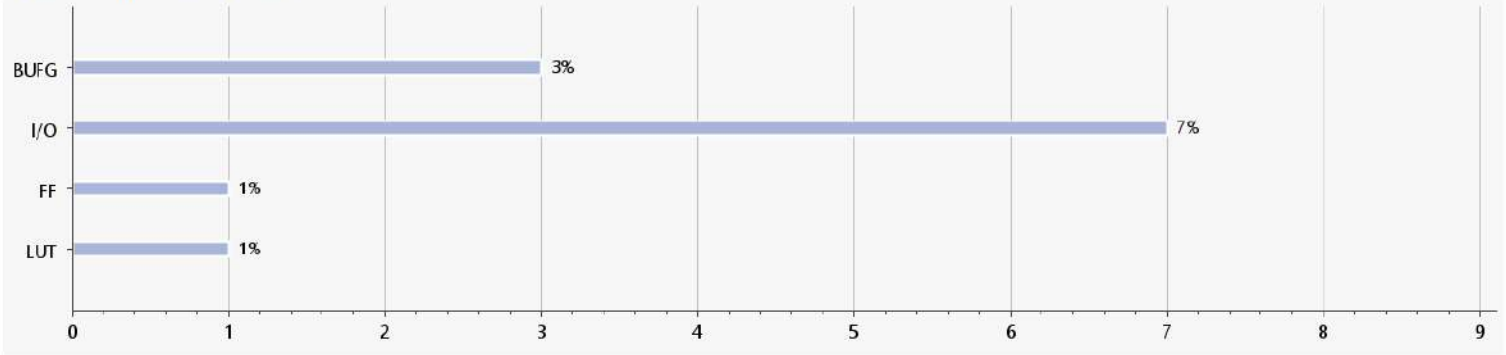

i2c_transltor_top.v
i2c_clk_divider.v
I2C_materside_fsm.v
i2c_address_translator_fsm.v
i2c_slaveside_fsm.v
i2c_slave2_fsm.v
Tb_I2C_Addr_Translator.v
Schematic (2)
6 Cells
21 I/O Ports
31 Nets
Slave_sel
ref_clk
reset
rw
unit_div
ref_clk
reset
i2c_clk
i2c_clk_divider
unit_tran
Slave_sel
Slave1_scl
clk
reset
rw
start_transaction
Slave1_sda
Slave2_scl
Slave2_sda
master_scl
master_sda
txn_done
i2c_address_translator_fsm
unit_master
Slave_sel
clk
reset
rw
i2c_scl
i2c_sda
txn_done
I2C_materside_fsm
slave1
scl
data_in[7:0]
sda
i2c_slaveside_fsm
recevied_data_slave1[7:0]
slave2
scl
data_in[7:0]
sda
i2c_slave2_fsm
recevied_data_slave2[7:0]
txn_done_i
I0
I1
O
RTL_OR
txn_done

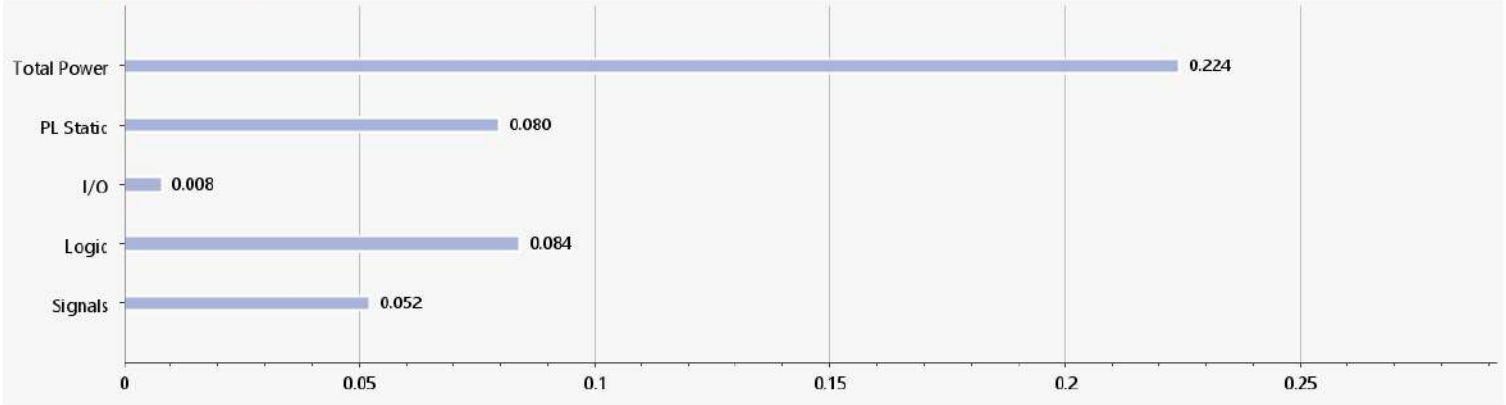
Project Summary | Schematic | i2c_transitor_top.v | i2c_clk_divider.v | I2C_materside_fsm.v | i2c_address_translator_fsm.v | i2c_slaveside_fsm.v | i2c_slave2_fsm.v | Tb_I2C_Addr_Translator.v | Schemat

Overview | **Dashboard** | + Add Gadget

Utilization (synth_1, Synth Design)



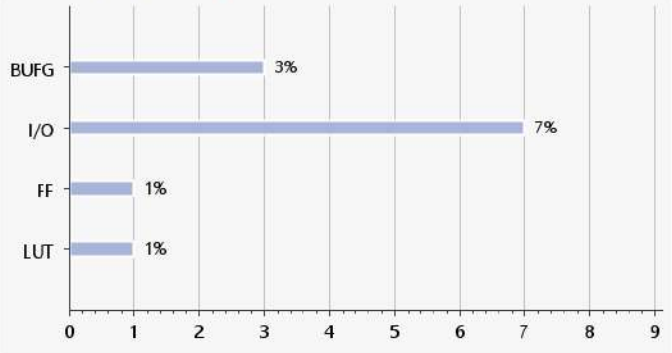
Power (impl_1, Route Design)



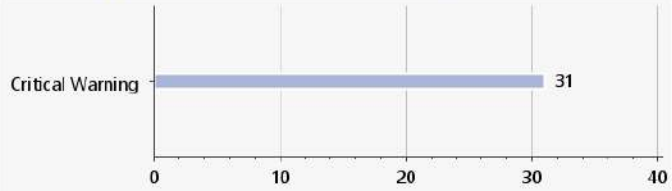
DRC (impl_1, Route Design)

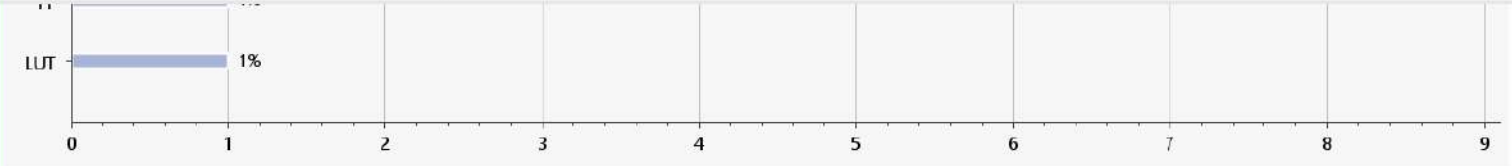
Timing (impl_1, Route Design)

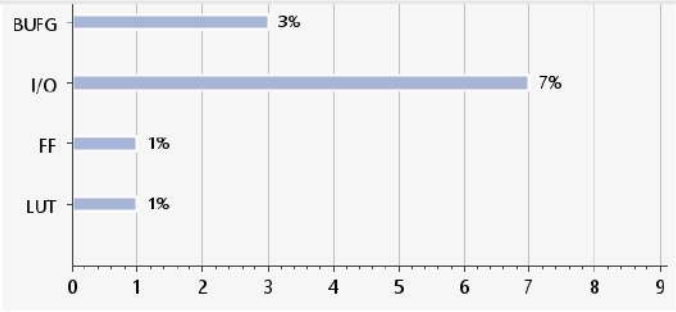
Utilization (impl_1, Place Design)



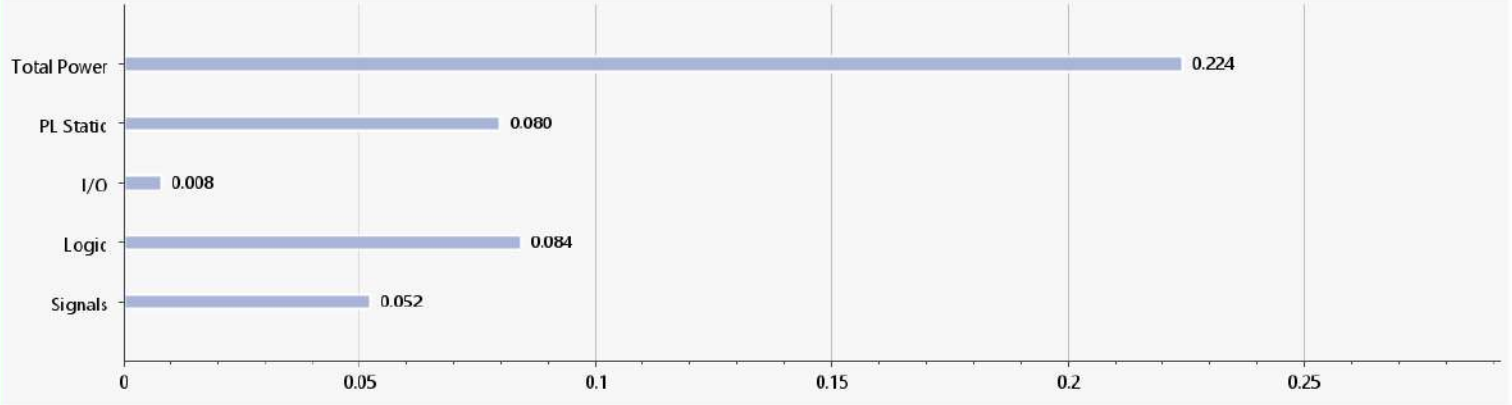
Methodology (impl_1, Route Design, Critical Warning)



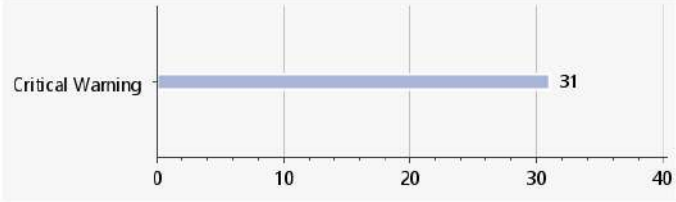




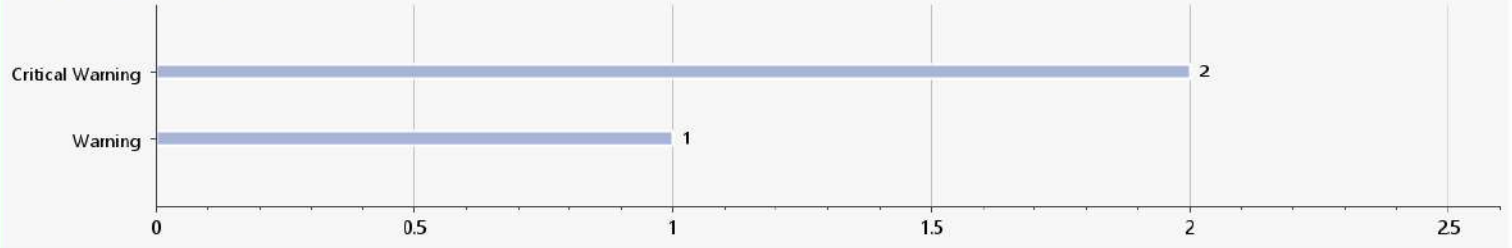
Power (impl_1, Route Design)



Methodology (impl_1, Route Design, Critical Warning)

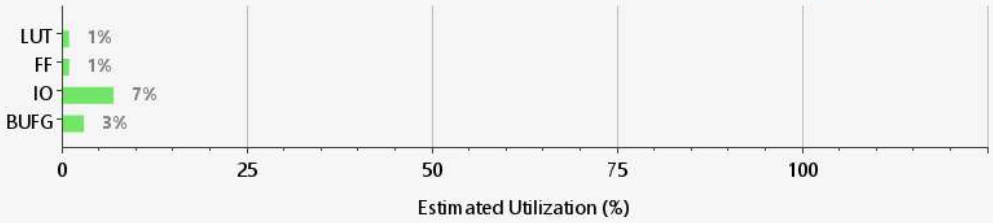


DRC (impl_1, Route Design)

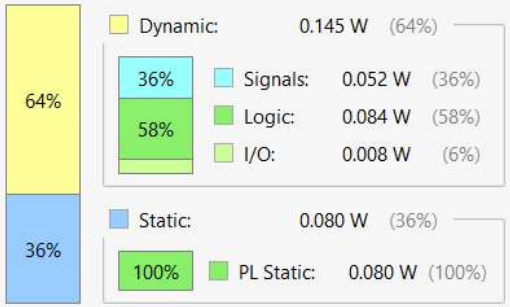


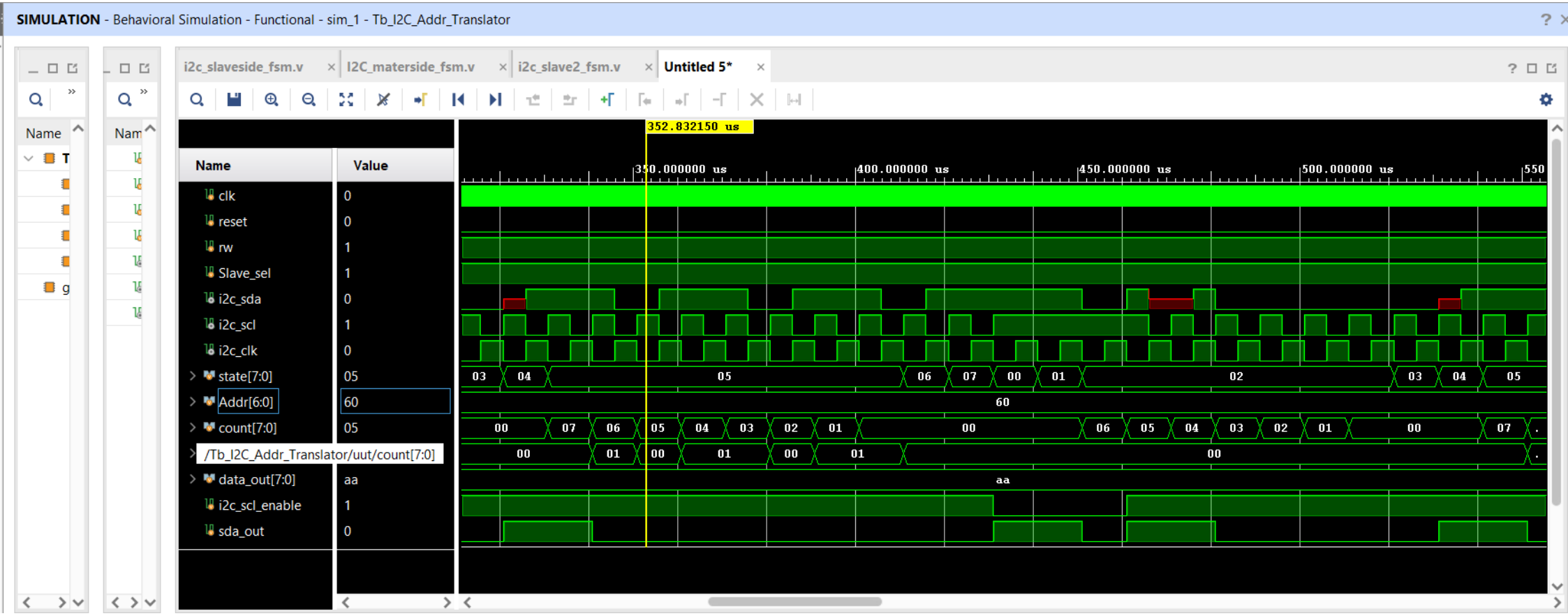
Utilization — **Post-Synthesis** | Post-Implementation

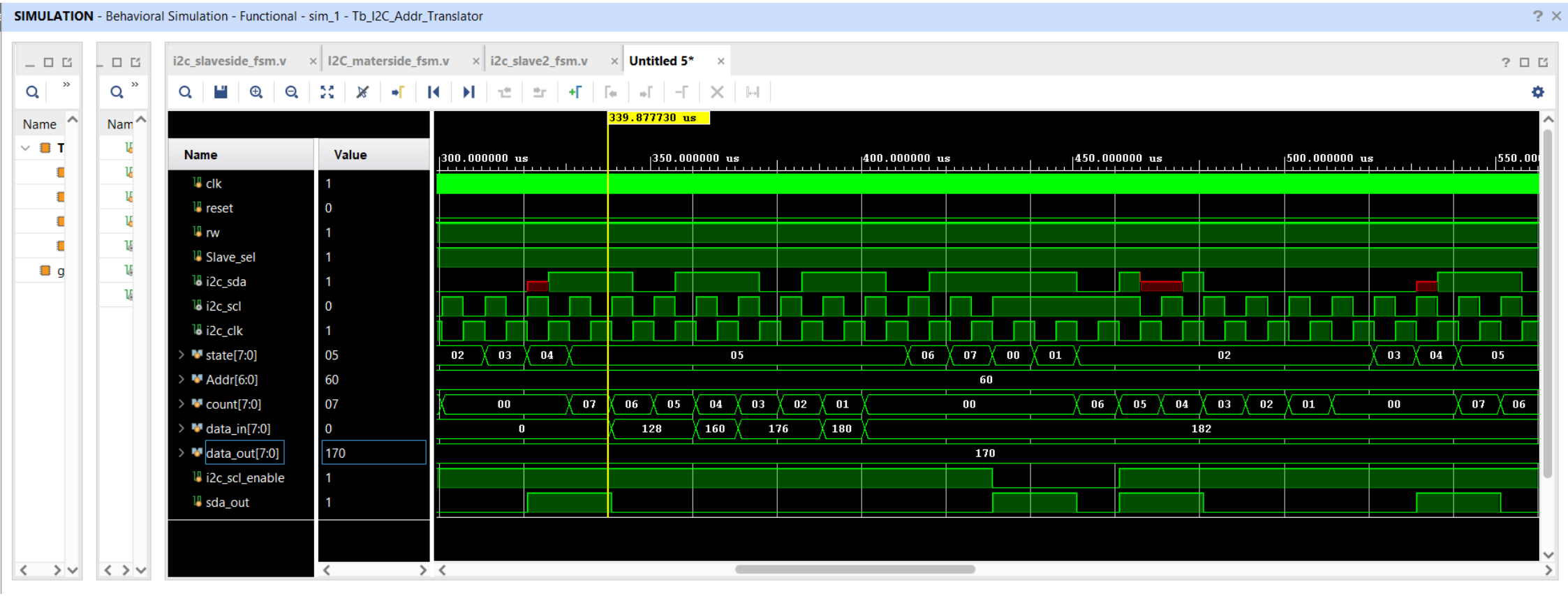
Graph | Table

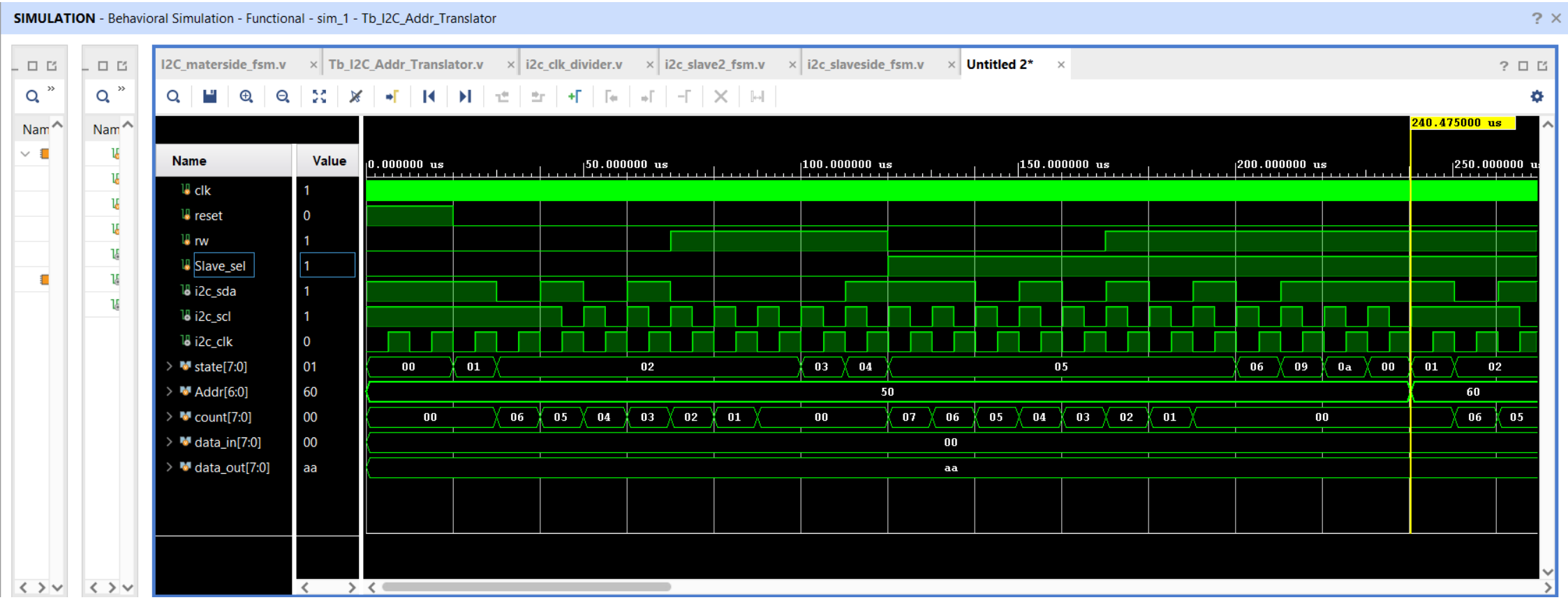


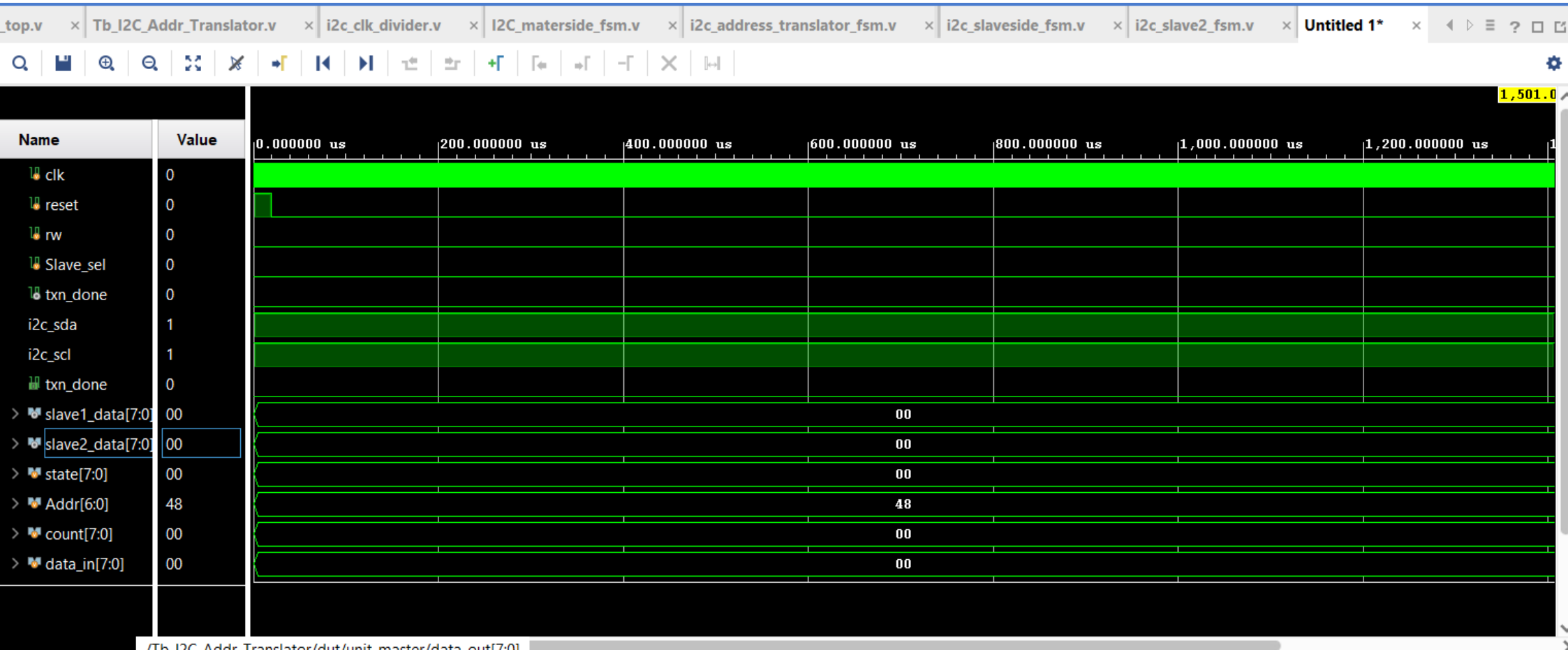
Power — Summary | **On-Chip**




SIMULATION - Behavioral Simulation - Functional - sim_1 - Tb_I2C_Addr_Translator
i2c_slaveside_fsm.v
I2C_materside_fsm.v
i2c_slave2_fsm.v
Untitled 5*
352.832150 us
350.000000 us
400.000000 us
450.000000 us
500.000000 us
Name
Value
clk
reset
rw
Slave_sel
i2c_sda
i2c_scl
i2c_clk
state[7:0]
Addr[6:0]
count[7:0]
/Tb_I2C_Addr_Translator/uut/count[7:0]
data_out[7:0]
i2c_scl_enable
sda_out
0
1
05
60
aa


SIMULATION - Behavioral Simulation - Functional - sim_1 - Tb_I2C_Addr_Translator
i2c_slaveside_fsm.v
I2C_materside_fsm.v
i2c_slave2_fsm.v
Untitled 5*
339.877730 us
300.000000 us
350.000000 us
400.000000 us
450.000000 us
500.000000 us
Name
Value
clk 1
reset 0
rw 1
Slave_sel 1
i2c_sda 1
i2c_scl 0
i2c_clk 1
state[7:0] 05
Addr[6:0] 60
count[7:0] 07
data_in[7:0] 0
data_out[7:0] 170
i2c_scl_enable 1
sda_out 1


SIMULATION - Behavioral Simulation - Functional - sim_1 - Tb_I2C_Addr_Translator
I2C_materside_fsm.v
Tb_I2C_Addr_Translator.v
i2c_clk_divider.v
i2c_slave2_fsm.v
i2c_slaveside_fsm.v
Untitled 2*
Name
Value
clk 1
reset 0
rw 1
Slave_sel 1
i2c_sda 1
i2c_scl 1
i2c_clk 0
state[7:0] 01
Addr[6:0] 60
count[7:0] 00
data_in[7:0] 00
data_out[7:0] aa
0.000000 us
50.000000 us
100.000000 us
150.000000 us
200.000000 us
240.475000 us
00 01 02 03 04 05 06 09 0a 00 01 02
50 60
00 06 05 04 03 02 01 00 07 06 05 04 03 02 01 00 06 05
00
aa


_top.v
Tb_I2C_Addr_Translator.v
i2c_clk_divider.v
I2C_materside_fsm.v
i2c_address_translator_fsm.v
i2c_slaveside_fsm.v
i2c_slave2_fsm.v
Untitled 1*
Name
Value
clk
0
reset
0
rw
0
Slave_sel
0
txn_done
0
i2c_sda
1
i2c_scl
1
txn_done
0
slave1_data[7:0]
00
slave2_data[7:0]
00
state[7:0]
00
Addr[6:0]
48
count[7:0]
00
data_in[7:0]
00
0.000000 us
200.000000 us
400.000000 us
600.000000 us
800.000000 us
1,000.000000 us
1,200.000000 us
1,501.0
00
00
00
48
00
00