

PART A: Introduction			
Program: Certificate		Class: B.C.A.	Year: I Year
Session: 2025-26			
Subject: Computer Applications			
1.	Course Code		
2.	Course Title	Computer Architecture (Theory)	
3.	Course Type (Core Course/DSE/Minor/MD-ID/SEC/VOC)	Major –I (Core Course)	
4.	Pre-Requisite (if any)	To study this course, a student must have basic knowledge of Computers.	
5.	Course Learning Outcomes (CLO)	After the completion of this course, a successful student will be able to do the following: <ol style="list-style-type: none"> 1. Understand the basic structure, operation and characteristics of digital computer. 2. Design simple combinational digital circuits based on given parameters. 3. Familiarity with working of arithmetic and logic unit. 4. Know about hierarchical memory system including cache memories and virtual memory. 5. Know the contributions of Indians in the field of computer architecture and related technologies. 	
6.	Credit Value	Theory – 4 Credits	
7.	Total Marks	Max. Marks : 30 + 70	Min. Passing Marks: 35

PART B: Content of the Course		
No. of Lectures (in hours per week): 2 Hrs. per week		
Total No. of Lectures: 60 Hrs.		
Module	Topics	No. of Lectures
I	Indian Knowledge System: Ancient Indian Contribution in Computer Architecture: Pingala's "Chandahśāstra", Panini Sanskrit Grammar. Modern Contribution: Dr. Vinod Dhami, Dr. Ajay Bhat, Dr. Vinod Khosla, Dr. Vijay P Bhatkar. Suggested Activities: Debate on Pingala's "Chandahśāstra", Panini Sanskrit Grammar. Solve real-world problems inspired by PARAM's computational models. Discuss on Indian contributions to computing,	02



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II	<p>Fundamentals of Digital Electronics: Decimal, Binary, Octal, Hexadecimal, Number System Conversions, Binary Arithmetic, Addition and subtraction of BCD, Octal Arithmetic, Hexadecimal Arithmetic, Binary Codes, Decimal Codes, Error detecting and correcting codes, ASCII, EBCDIC, Excess-3 Code, The Gray Code.</p> <p>Logic Gates, Boolean Algebra, Map Simplification, Combinational Circuits, Sequential Circuits, simple combinational circuit design problems.</p> <p><i>Suggested Activities: Assignment on number systems, Verifying logic gates through truth tables,</i></p>	12
III	<p>Combinational Circuits: Half Adder and Full Adder, Subtractor, Decoders, Encoder, Multiplexer, Demultiplexer.</p> <p>Sequential Circuits: Flip-Flops- SR Flip-Flop, D Flip-Flop, J-K Flip-Flop, T Flip-Flop.</p> <p>Register: 4 bit register with parallel load, Shift Registers- Bidirectional shift register with parallel load Binary.</p> <p>Counters: 4 bit synchronous and Asynchronous binary counter.</p> <p><i>Suggested Activities: Designing combinational circuits, Hands-on session on designing adders and multiplexers, use simulation software to design basic combinational circuits, Students work in teams to optimize logic circuits for efficiency, Debate on advancements in digital logic design.</i></p>	12
IV	<p>Basic Computer Organization: Instruction codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycles, Memory Reference Instruction, Input - Output & Interrupts, Instruction formats, Addressing modes, Instruction codes, Machine language, Assembly language.</p> <p>Register Transfer and Micro operations: Register Transfer Language, Register Transfer, Bus & Memory Transfer, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations.</p> <p><i>Suggested Activities: Understand how processors access operands in memory, Implement AND, OR, XOR operations at the bit level, explore Panini's rule-based grammar and compare it with modern instruction set design, debate on addressing modes and their use cases.</i></p>	12
V	<p>Processor and Control Unit: Hardwired vs. Micro programmed Control Unit, General Register Organization, Stack Organization, Instruction Format, Data Transfer & Manipulation, Program Control, Introductory concept of RISC, CISC, advantages and disadvantages of both.</p> <p>Pipelining: concept of pipelining, introduction to Pipelined data path and</p>	12



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	control – Handling Data hazards & Control hazards.	
	<i>Suggested Activities: Debate on Hardware vs. Microprogrammed Control, Assignment on designing a simplified processor. Discussion on RISC vs. CISC architectures, Analyze how modern processors handle instruction execution.</i>	
VI	Memory and I/O Systems - Peripheral Devices, I/O Interface. Data Transfer Schemes - Program Control, Interrupt, DMA Transfer, I/O Processor. Memory Hierarchy , Processor vs. Memory Speed, High-Speed Memories, Main memory, Auxiliary memory, Cache Memory, Associative Memory, Interleaving, Virtual Memory, Memory Management. Ancient Manuscript Storage (Nalanda, Takshashila Libraries): Similarity to hierarchical memory and indexing methods. <i>Suggested Activities: Understanding memory allocation in modern computers, Compare manuscript storage methods with modern hierarchical memory, Field Visit (if possible): Visit a digital archive/library to understand memory organization.</i>	10

PART C: Learning Resources

Textbooks, Reference Books, Other Resources

Suggested Readings:

Textbooks:

1. Gerard G. Emch, R. Sridharan, M. D. Srinivas: Contributions to the History of Indian Mathematics, Hindustan Book Agency, Vol. 3, 2005.
2. Udayan S. Patankar & Sunil M. Patankar: Elements of Vedic Mathematics, TTU Press, Tallinn 2018.
3. M. Morris Mano: “Computer System Architecture”, PHI.
4. Heuring Jordan: “Computer System Design & Architecture” (A.W.L.).
5. Donald P Leach, Albert Paul Malvino, Goutam Saha: “Digital Principles & Applications”, Tata McGraw Hill Education Private Limited, 2011 Edition.
4. मध्य प्रदेश हिन्दी ग्रंथ अकादमी की पुस्तकें।

Reference Books:

1. William Stalling, “Computer Organization & Architecture”, Pearson Education Asia.
2. V. Carl Hamacher, “Computer Organization”, TMH
3. Tannenbaum, “Structured Computer Organization”, PHI.
6. Er. Rajiv Chopra, “Computer Architecture”, Revised 3rd Edition, S. Chand & Company Pvt. Ltd



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Suggested Digital Platforms & Web links:
https://epgp.inflibnet.ac.in
https://www.eshiksha.mp.gov.in/mpdhe
Suggested Equivalent Online Courses:
https://nptel.ac.in/courses/106/105/106105163/
https://nptel.ac.in/courses/106/106/106106166/
https://nptel.ac.in/courses/106/106/106106134/

Part D: Assessment and Evaluation		
Suggested Continuous Evaluation Methods:		
Maximum Marks:		100
Continuous Comprehensive Evaluation (CCE):		30 Marks
University Exam (UE):		70 Marks
Internal Assessment: Continuous Comprehensive Evaluation (CCE)		Total Marks: 30
External Assessment: University Exam Section Time: 03.00 Hours	Section (A) : Very Short Questions Section (B) : Short Questions Section (C) : Long Questions	Total Marks: 70



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PART A: Introduction			
Program: Certificate		Class: B.C.A.	Year: I Year
Session: 2021-22			
Subject: Computer Applications			
1.	Course Code		
2.	Course Title	Computer Architecture (Practical)	
3.	Course Type (Core Course/DSE/Minor/MD-ID/SEC/VOC)	Major - 1 (Core Course)	
4.	Pre-Requisite (if any)	Nil	
5.	Course Learning Outcomes(CLO)	After the completion of this course, a successful student will be able to do the following: <ol style="list-style-type: none"> 1. Realization of the basic logic and universal gates. 2. Verify the behavior of logic gates using truth tables. 3. Implement Binary-to -Gray, Gray-to -Binary code conversions. 4. Design half and full adder circuit using basic gates. 5. Design and construct flip flops and verify the excitation tables. 	
6.	Credit Value	Practical - 2 Credits	
7.	Total Marks	Max. Marks: 100	Min. Passing Marks: 35

PART B: Content of the Course		
No. of Lab. Practical's (in hours per week): 1 Hrs. per week		
Total No. of Labs: 30 Hrs.		
	Suggestive list of Practical's	No. of Labs.
	<ol style="list-style-type: none"> 1. Verification and interpretation of truth table for AND, OR, NOT gates 2. Verification and interpretation of truth table for NAND, NOR gates 3. Verification and interpretation of truth table for Ex-OR, Ex-NOR gates 4. Study of half adder using XOR and NAND gates and verification of its operation 5. Study of full adder using XOR and NAND gates and verification of its operation 6. Study of half subtractor and verification of its operation 7. Study of full subtractor and verification of its operation 8. Realization of logic functions with the help of NAND -Universal Gates 	30 Hrs.



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	9. Realization of logic functions with the help of NOR -Universal Gates 10. Verify the truth table of RS flip-flops using NAND and NOR gates 11. Verify the truth table of JK flip-flops using NAND and NOR gates 12. Verify the truth table of T and D flip-flops using NAND and NOR gates 13. Implementation of 4x1 multiplexer using logic gates 14. Implementation of 1x4 demultiplexer using logic gates 15. Verify Gray to Binary conversion using NAND gates only 16. Verify Gray to Binary conversion using NAND gates only	
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Suggested Readings		
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Reference Books: <ol style="list-style-type: none"> William Stalling, “Computer Organization & Architecture”, Pearson Education Asia. V. Carl Hamacher, “Computer Organization”, TMH Tannenbaum, “Structured Computer Organization”, PHI. Er. Rajiv Chopra, “Computer Architecture”, Revised 3rd Edition, S. Chand & Company Pvt. Ltd 		
Suggested Digital Platforms Web links:		
https://epgp.inflibnet.ac.in https://www.eshiksha.mp.gov.in/mpdhe		
Suggested equivalent online courses		
https://nptel.ac.in/courses/106/105/106105163/ https://nptel.ac.in/courses/106/106/106106166/ https://nptel.ac.in/courses/106/106/106106134/		



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PART D: Assessment and Evaluation

Suggested Continuous Evaluation Methods:

Internal Assessment	Marks	External Assessment	Marks
Class Interaction/Quiz		Viva voce practical	
Attendance		Practical record file	
Assignments (Charts/ Model/Seminar/Rural Services/ Technology Dissemination/Report of Excursion/Lab visit/ Survey/Industrial Visit)		Table work/Experiment	
Total	30		70



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