OBJECTIVE:- To design a stopwatch with following specifications

- 4 digit display showing seconds and $\frac{1}{100}$ seconds
- One push button switch to go through three state in cycle, viz. RESET, START and STOP sequentia

DESCRIPTION:-

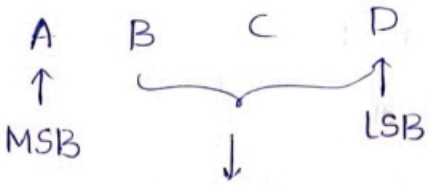
- State-1 (RESET) :- shows display 00.00 and stopwatch is ready to count.
- State-2 (START):- The switch when pressed during RESET starts the watch and display is updated every $1/100$ second, the watch keeps counting till the switch is pressed again and then goes to state-3
- State-3 (STOP):- counting stops and freezes. watch remains in stop condition, till the switch is pressed again. Pressing switch during STOP condition RESETs the display and the process repeats from state-1.

PROCEDURE:-

→ We need to make 4 digit (16 bit) fully synchronous BCD counter.

→ We will use four 74161 counters to make the 16 b BCD counter by cascading them.

→ We have 4 digit (16 bit) to be display



this three counters counts upto 0 to 9 whereas MSB counts from 0 to 5, as we have 60 seconds for a 1 minute.

→ the last three counters reset when they encounter "10" the MSB clears to 0 when it encounters "6."

→ When "D" counts from 0 to 9, as its reaches "9", it enables the counter "C". As both counters "C" and "D" reach "9", they enable "B". As three of A, B, C, D reach "9" they enable "A". Enable from one counter is passed to other.

→ All the counters get the same clock, hence they are synchronous.

→ For B, C, D, they get cleared to "0" when the digit reaches 1001 (9). A gets cleared when it reaches (0110)(6)

CLOCK GENERATOR :-

→ For making clock we use 555 timer. under astable operation (no stable state).

→ Clock generator of 10 ms period using 555 timer.

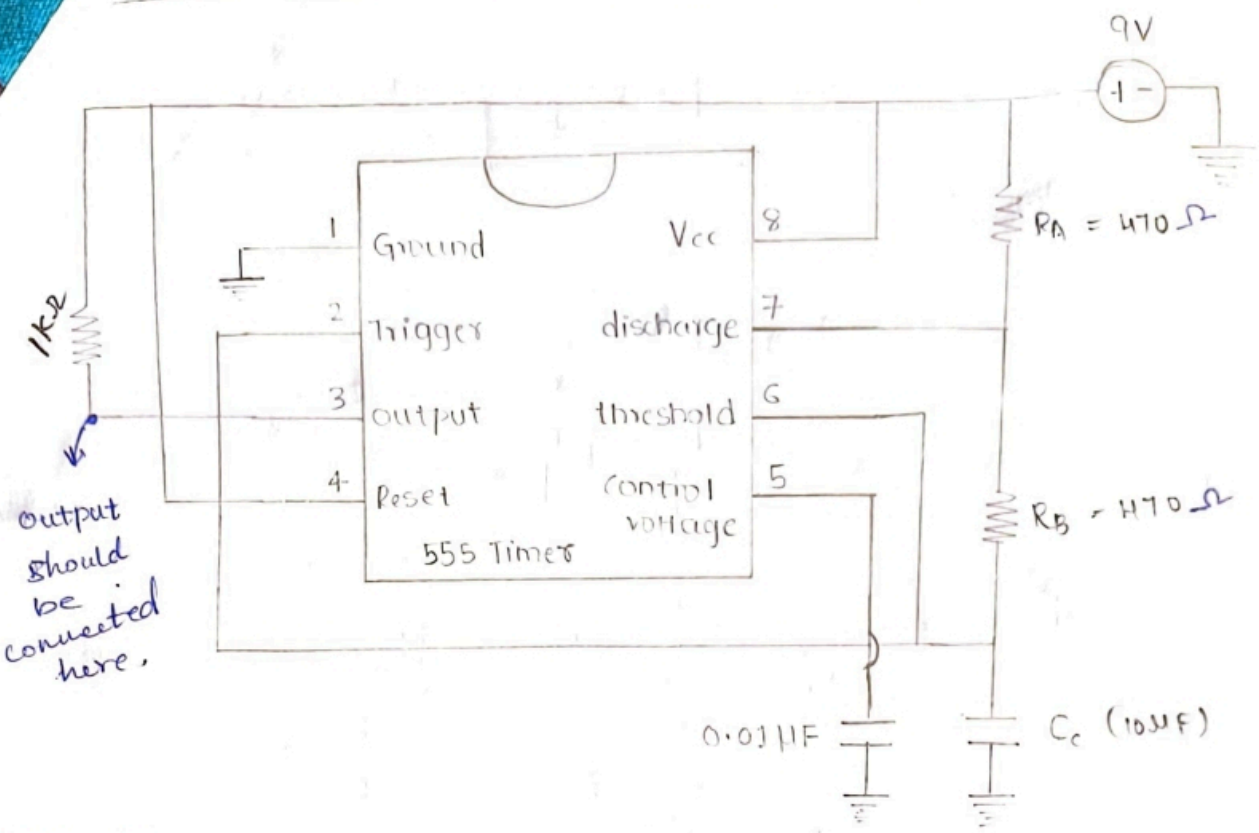
$$\text{Frequency} = \frac{1}{\text{time period}} = \frac{1000}{10}\ \text{Hz} = 100\ \text{Hz}.$$

$$\text{frequency} = \frac{1.44}{(R_A + 2R_B)C_C} = 100\ \text{Hz}.$$

$$C_C\ (\text{capacitance in } \mu\text{F}) \Rightarrow \frac{1.44}{(R_A + 2R_B)C_C} = 10^2 \times 10^{-6}$$

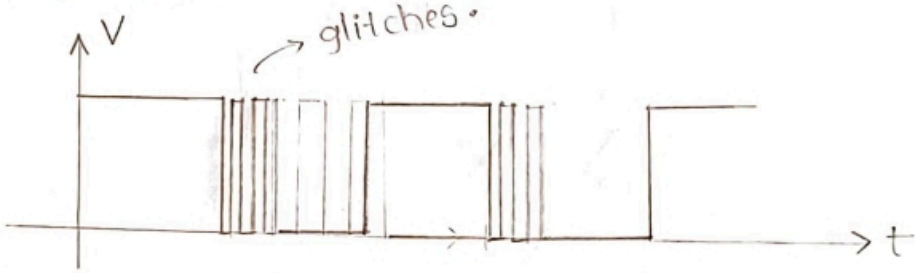
$$14400 = C_C(R_A + 2R_B)$$

$C_C = 10\ \mu\text{F}$; $R_A = $ ~~1105~~ 470 Ω, $R_B = $ ~~550 Ω~~ 470 Ω.

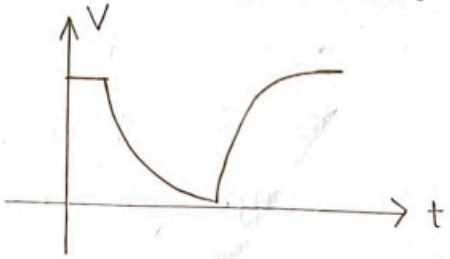


Switch debouncing circuit :-

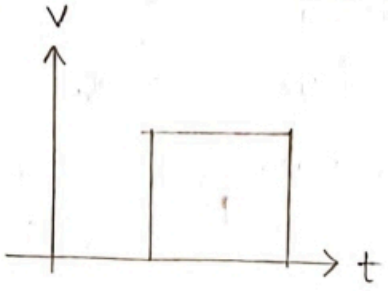
→ When we simply use switch in a circuit, we get unsteady responses as followed.



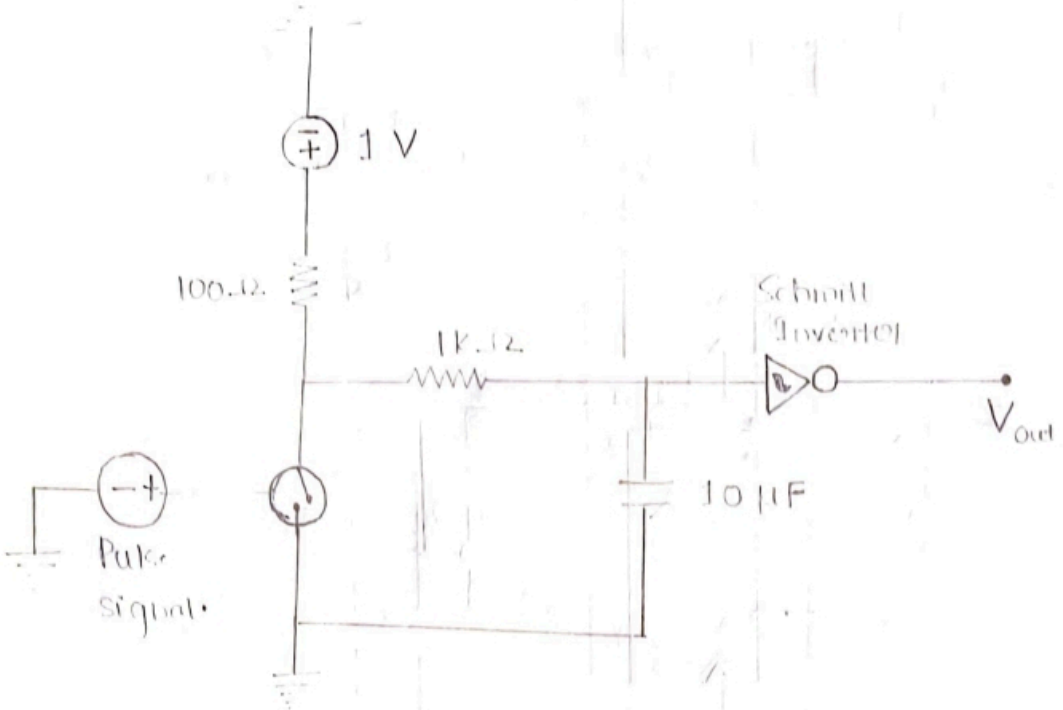
→ After making a RC arrangement, the response is smooth but not perfect is as follows:



→ After adding schmitt inverter, we get the response as:-



a perfect debouncing switch is obtained



PUSH BUTTON :-

We have stated before that, we have 3 states

RESET - 10

START - 00

STOP - 01

We can use same 74161 as BCD counter here also with Q_3 and Q_2 grounded, such that we get 2-bit counter.

→ Clock should be working START (00) state only for counting

→ Initially counter is set to 0000 i.e cleared.

→ Hence we are in START state ~~ready to~~ counting

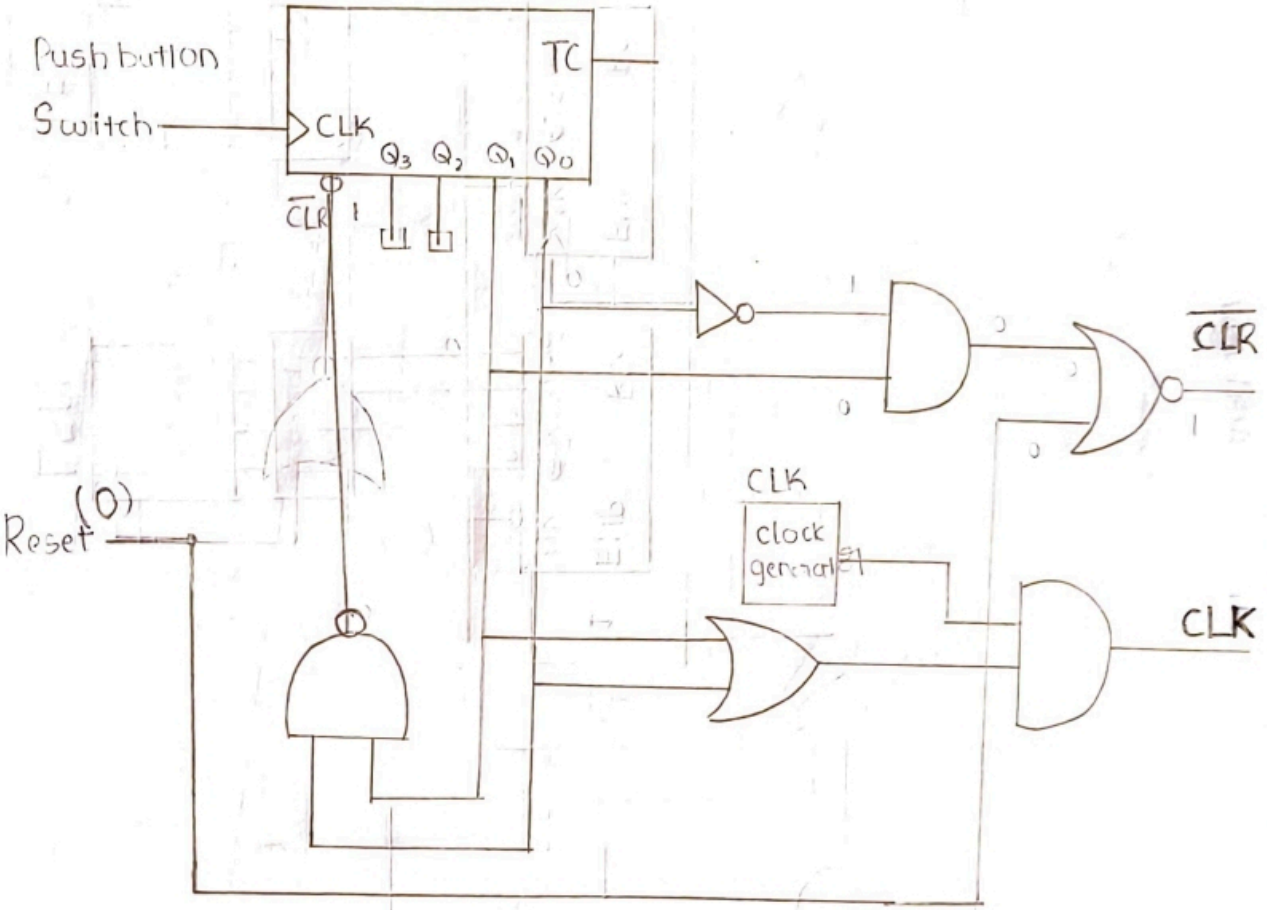
→ When we push the switch it starts counting.

→ When we push the switch it goes to 01 state, stop the counting, display the value. (stop the common clock)

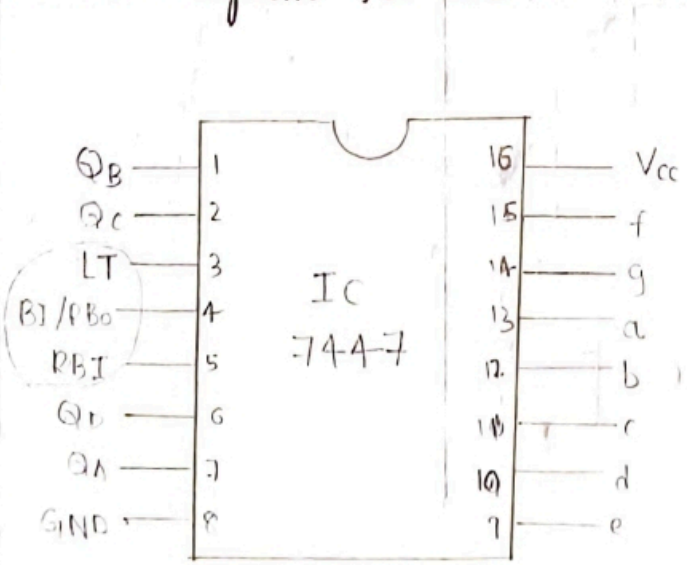
→ When we push the switch again, it ~~re~~ goes to 10 state, it resets again.

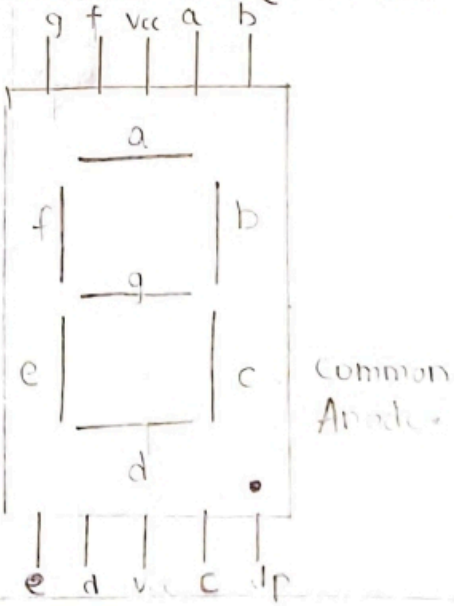
→ the counters all are set to cleared state. and also reset our switch counter to zero. (as we encounter 10 state).

Condition	Q_1	Q_0	$\overline{CLR}$	EN.
START	0	0	1	
STOP	0	1	1	
RESET	1	0	0	

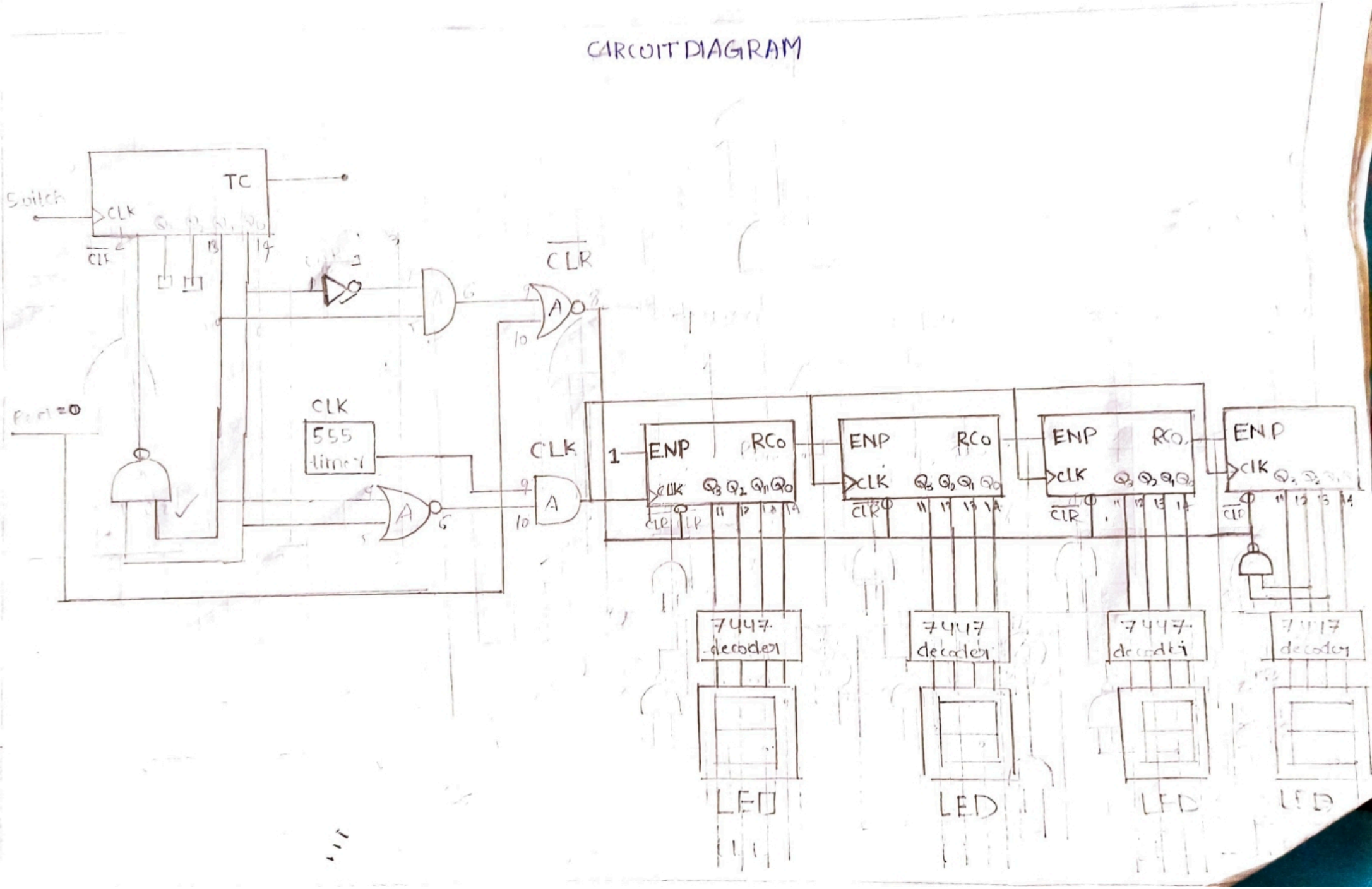


circuit diagram for BCD to 7-segment decoder IC (7447):-





CIRCUIT DIAGRAM



s and other elements required :-

1. IC - 74161 - 1
2. IC - 74160 - 4
3. IC - 74HC14 - Schmitt inverter - 1
4. capacitor - 10 μF - 2
   0.01 μF - 1
5. Resistor - ~~1110~~ 470 Ω - 2
   100 Ω - 1
   1K Ω - 1
6. NE555 timer - 1
7. Switch.
8. 7-segment display common anode - 4
9. IC - 7447 - 4
10. 7408 (AND) - 2
11. 7404 (NOT) - 1
12. 7400 (NAND) - 1
13. ~~7402 (OR)~~
14. 7402 (NOR) - 1

Internal diagram of 74161 / 74160.