CS 232 - Assignment 2

1) Design an 8x3 Encoder. Vector 'i' is the input, 'en' is the enable pin and 'z' is the output. **This entire circuit must be designed using only 2x1 MUXES. The MUXES themselves can be designed using either basic gates or behavioural code can be used.**

   entity EightbyThreeEncode is
           port (i : in std_logic_vector(7 downto 0);
           en: in std_logic;
           z : out std_logic_vector(2 downto 0));
   end entity;

2) Design a 3x8 Decoder. Vector 'i' is the input, 'en' is the enable pin and 'z' is the output. **This entire circuit must be designed using only NAND gates in a structural way. The NAND gates themselves must be designed using only structural code.**

   entity ThreebyEightDecode is
           port (i : in std_logic_vector(2 downto 0);
           en: in std_logic;
           z : out std_logic_vector(7 downto 0));
   end entity;

Things required in Submission:

1. All VHDL files of top-level and sub-components (.vhd or .vhdl files).
2. Screenshot of Waveforms (Few input patterns are sufficient).
3. A report explaining how you designed (pdf format).

Submission rules:

1. **Deadline:** Saturday (22nd Jan 2022), 23:59 pm.
2. Create a folder named **lab2** (all small letters and no spaces).
3. Inside the above-mentioned folder create 2 more folders named **q1** and **q2** (all small letters and no spaces).

4. Inside the folder, **q1** put all the .vhd or .vhdl files of both top-level entity and sub-components. Also in the same folder put the related waveform screenshots and pdf report related question1. Do the same thing for **q2.**
5. Finally, before you submit the lab1 folder on moodle you will be zipping it. The zip file should have your id number as the name. For eg: if your id is 184070026 then your zip file will be 184070026.zip