CS232 Week2 Q2

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1 Design

1.1 Design of NAND gate

The NAND gate is designed by combining AND and NOT gates. It has input ports a, b and output port c

$$c = \overline{a \cdot b}$$

1.2 Design of Decoder

We first create AND and OR gates using NAND gates as follows

$$\overline{a} = NAND(a, a)$$
$$a \cdot b = \overline{NAND(a, b)}$$

Then, for each output of the encoder, we construct in the following fashion

$$z_0 = \overline{i_2} \cdot \overline{i_1} \cdot \overline{i_0} \quad z_1 = \overline{i_2} \cdot \overline{i_1} \cdot i_0$$
$$z_2 = \overline{i_2} \cdot i_1 \cdot \overline{i_0} \quad z_3 = \overline{i_2} \cdot i_1 \cdot i_0$$
$$z_4 = i_2 \cdot \overline{i_1} \cdot \overline{i_0} \quad z_5 = i_2 \cdot \overline{i_1} \cdot i_0$$
$$z_6 = i_2 \cdot i_1 \cdot \overline{i_0} \quad z_7 = i_2 \cdot i_1 \cdot i_0$$