

CS 232 - Assignment 3

Design Rules:

- 1) For all questions, only structural VHDL code is permitted.*
- 2) Also for every question, the top-level entity description is given in the question itself. It must be used exactly as it is in your code without changing the entity name or any of the port names and the port names must be in the same order.*

- 1) Design a 1-bit full-adder. 'a' and 'b' are the two 1-bit numbers that are to be added. 'cin' is the input carry that should be added with 'a' and 'b'. 'sum' and 'cout' are the sum and carry outputs respectively. **This can be designed only in a structural way using only 1-bit half-adders and OR gates. It is mandatory to use the 1-bit half-adder for designing (i.e. at least one instance of 1-bit half-adder must be used.) The 1-bit half-adder itself must be designed only in a structural way using any basic gates.**

```
entity OnebitFullAdd is
    port ( a, b, cin : in std_logic;
          sum, cout: out std_logic);
end entity;
```

- 2) Design a 4-bit ripple carry adder. 'a' and 'b' are the two 4-bit unsigned numbers that are to be added. 'cin' is a single-bit input carry that should be added with 'a' and 'b'. 'sum' is the 4-bit unsigned addition output and 'cout' is the single-bit output carry. **This can be designed only in a structural way using only instances of the 1-bit full-adder designed in the previous question (i.e. question 1 of assignment 3.) No other component or gate is permitted.**

```
entity FourbitRipCarAdd is
    port ( a, b : in std_logic_vector (3 downto 0);
          cin: in std_logic;
          sum : out std_logic_vector (3 downto 0);
          cout: out std_logic);
end entity;
```

- 3) Design a 4-bit ripple carry adder-subtractor. 'a' and 'b' are the two 4-bit unsigned numbers that are to be added. Here 'cin' is not an input carry like in the previous question but it is a mode selection bit. If cin=0 then 'a' and 'b' should be added (a+b). If cin=1 then 'b' should be subtracted from 'a' (a-b). 'sum' is the 4-bit unsigned addition or subtraction output and 'cout' is the single-bit output carry. **This can be designed only in a structural way using the 4-bit ripple carry adder designed in the previous question (i.e. question 2 of assignment 3) and basic gates. At least one instance of the 4-bit ripple carry adder must be used along with**

any other basic gates necessary.

entity FourbitRipCarAddSub is

port (a, b : in std_logic_vector (3 downto 0);

cin: in std_logic;

sum : out std_logic_vector (3 downto 0);

cout: out std_logic);

end entity;

Things required in Submission:

1. All VHDL files of top-level and sub-components (.vhd or .vhd files).
2. Screenshot of Waveforms (Few input patterns are sufficient).
3. A report explaining how you designed (pdf format).

Submission rules:

1. **Deadline:** Tuesday (1st Feb 2022), 23:59 pm.
2. Create a folder named **lab3** (all small letters and no spaces).
3. Inside the above-mentioned folder create 2 more folders named **q1**, **q2** and **q3** (all small letters and no spaces).
4. Inside the folder, **q1** put all the .vhd or .vhd files of both top-level entity and sub-components. Also in the same folder put the related waveform screenshots and pdf report related question1. Do the same thing for **q2 and q3**.
5. Finally, before you submit the lab3 folder on moodle you will be zipping it. The zip file should have your id number as the name. For eg: if your id is 184070026 then your zip file will be 184070026.zip