

"In pursuit of Technical Excellence"



# Electronics Design Technology

## Lab Manual

Department of Electronics and Telecommunication Engineering **Government  
college of Engineering, Aurangabad**  
(An Autonomous Institute of Government of Maharashtra)



**GECA**

In pursuit of Technical Excellence

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**Government College of Engineering, Aurangabad**  
**शासकीय अभियांत्रिकी महाविद्यालय, औरंगाबाद**



**Department of Electronics and**  
**Telecommunication Engineering**

**ET3006: Lab Electronics design Technology**

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**Enrollment No.:** BE19F04F021

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**Class:** Electronics and Telecommunication (Third Year)

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**Academic Year:** 2021-2022

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**Electronics and Telecommunication Department, Government  
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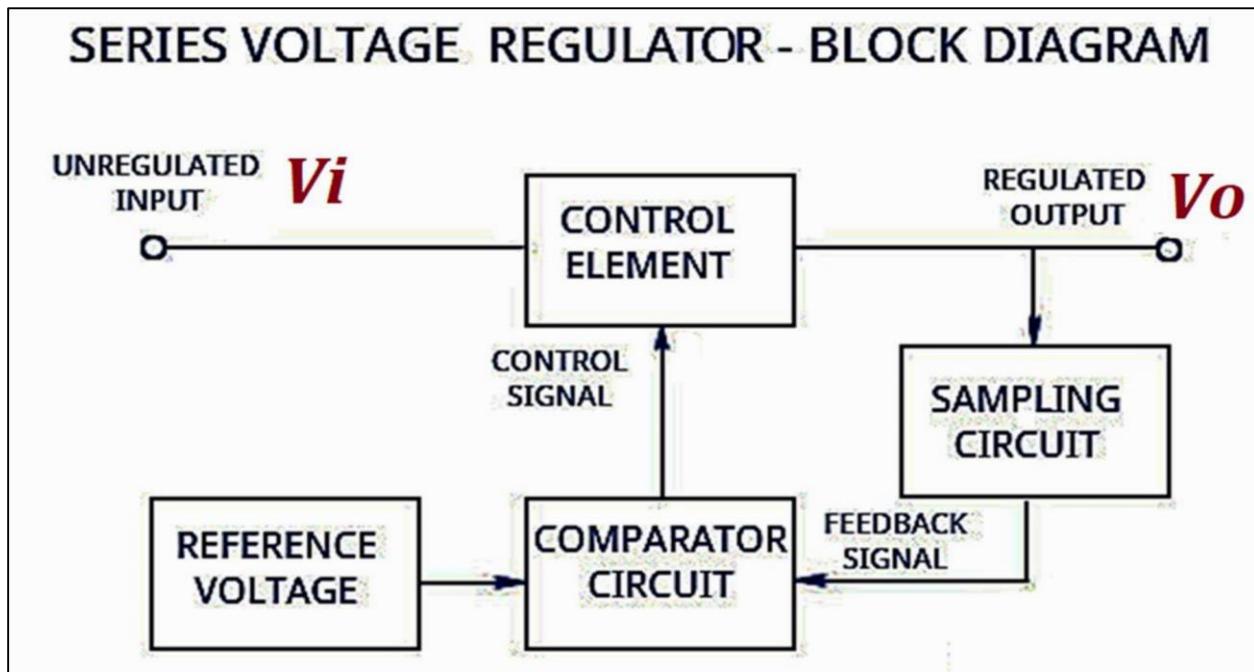
<b>Experiment no:</b>	<b>Title of Experiment</b>
1.	To design regulated power supply.
2.	To design Dual Tracking regulator.
3.	To design Common Emitter Amplifier.
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# Experiment no: 1

**Aim:** To Design Regulated Power supply.

**Software Requirements:** Proteus.

**Theory:** A regulated power supply is a circuit that keeps constant output voltage across o/p terminals irrespective of any changes in load current or input voltage. Regulation is ability of regulator to maintain constant output voltage. Voltage regulators are of different types such as, fixed positive voltage regulator, fixed negative voltage regulator, adjustable voltage regulator and switching voltage regulator.



Theoretical Solution :

- Design a voltage regulator using IC 7809 where  $I_L = 1\text{mA}$ ,  $f = 50\text{Hz}$  and  $\gamma = 10^\circ$ .

selection of filters  $C_i$  and  $C_o$

$$C_i = 0.22\mu\text{F} \quad \text{and} \quad C_o = 0.1\mu\text{F}$$

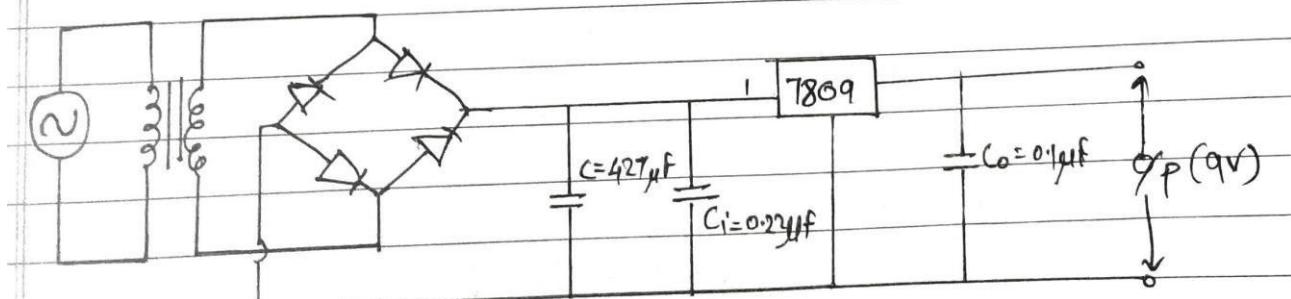
Calculating value of  $C$ ,

$$\begin{aligned} C &= \frac{1}{4\sqrt{3} R L f \gamma} & R_L &= \frac{V_{dc}}{I_{dc}} = \frac{3 \times 9}{2} = 13.5\text{V} \\ & & & I_{dc} \\ \therefore C &= \frac{1}{4\sqrt{3} \times 13.5 \times 50 \times 0.1} & \therefore R_L &= \frac{13.5}{0.2} \\ & & & I_{dc} = 0.2\text{A} \\ & & & \\ \therefore C &= 427\mu\text{F} \end{aligned}$$

Calculating value of  $V_m$ ,

$$V_m = \sqrt{V_{dc} \times \frac{\pi}{2}} = \sqrt{13.5 \times \frac{\pi}{2}} = 21.2\text{V}$$

Output Voltage must be  $+9\text{V}$ .



9V voltage regulator using IC 7809.

2. Design a voltage regulator with IC 723 where output voltage is +5V and  $I_{L\max} = 200 \text{ mA}$ .  $V_{in\max} = 7.4 \text{ V}$ .

Calculating values of  $R_1$  and  $R_2$ ,

$$V_o = 5 \text{ V}$$

$$V_{ref} = 7.15 \text{ V}$$

$$V_o = V_{ref} \times \frac{R_2}{R_1+R_2}$$

$$5 = 7.15 \times \frac{R_2}{R_1+R_2}$$

$$\therefore \frac{R_2}{R_1+R_2} = 0.6993$$

$$\text{let, } R_1 = 10 \text{ k}\Omega$$

$$\therefore \frac{R_2}{R_2+10} = 0.6993$$

$$\therefore R_2 = 0.6993 (R_2+10)$$

$$= 0.6993 R_2 + 6.993$$

$$6.993 = (1 - 0.6993) R_2$$

$$\therefore R_2 = \underline{23.255 \text{ k}\Omega}$$

$$R_3 = R_1 || R_2$$

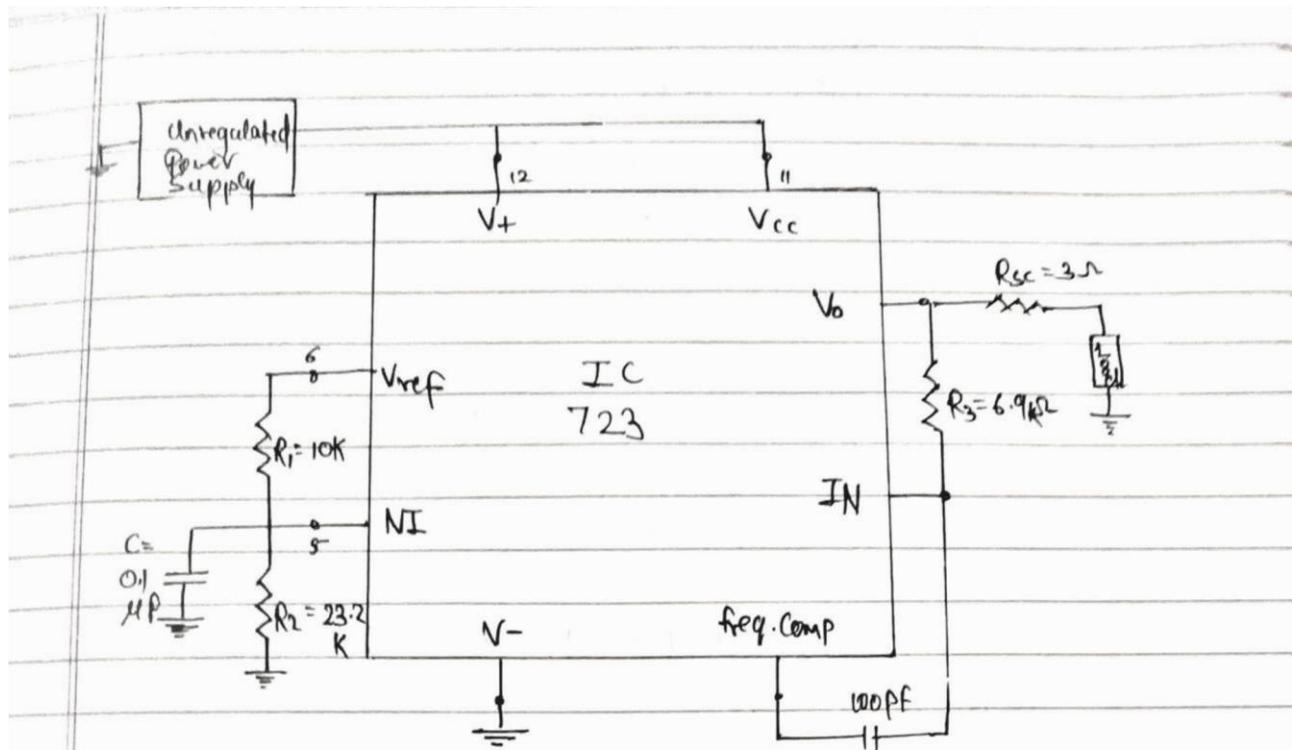
$$= \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 23.255}{10 + 23.255} = \underline{6.9927 \text{ k}\Omega}$$

$$R_{SC} = \frac{V_{sense}}{I_{L\max}} = \frac{0.6}{0.2} = 3 \Omega$$

Justification of design:

$$\begin{aligned} P_{d(max)}(I_C) &= (V_{in\max} - V_o) I_{L\max} \\ &= (V_{in\max} - (V_o + I_{L\max} R_{SC})) I_{L\max} \\ &= (7.4 - 5.6) \times 200 \times 10^{-3} \\ &> 1.8 \times 200 \times 10^{-3} \end{aligned}$$

$$P_d(max) = 0.36 \text{ W} < 0.8 \text{ W} \quad \therefore \text{Design is Safe \& Justified.}$$



+5V voltage regulator using IC 723.

3. Design a Voltage regulator using LM317 for output Voltage of 14V-30V.  $R_1 = 240\Omega$ ,  $I_{adj} = 100\mu A$ .

Selection of  $C_1$  and  $C_2$ ,  
 $C_1 = 0.1\mu F$  and  $C_2 = 0.1\mu F$ .

Selection of Input Voltage  $V_{in}$ ,

$$V_{in} \geq V_{out} + 10\% \cdot V_{out}$$

$$\therefore V_{in} \geq 14 + 10\% \times 14 \geq 15.4V$$

$$\therefore V_{in} > 30 + 10\% \times 30 \geq 33V$$

$\therefore V_{in}$  should be 33V.

Calculating  $R_2$ ,

$$V_0 = V_{ref} \left( 1 + \frac{R_2}{R_1} \right) + R_2 \times I_{adj}$$

for 14V,

$$\therefore 14 = 1.25 \left( 1 + \frac{R_2}{240} \right) + R_2 \times 10^{-4}$$

$$\therefore 14 = 1.25 + 0.0052 R_2 + 10^4 R_2$$

$$\therefore 12.75 = 5.3 \times 10^3 R_2$$

$$\therefore R_2 = 2.4 \text{ k}\Omega.$$

for 30V,

$$30 = 1.25 + 0.0052 R_2 + 10^4 R_2$$

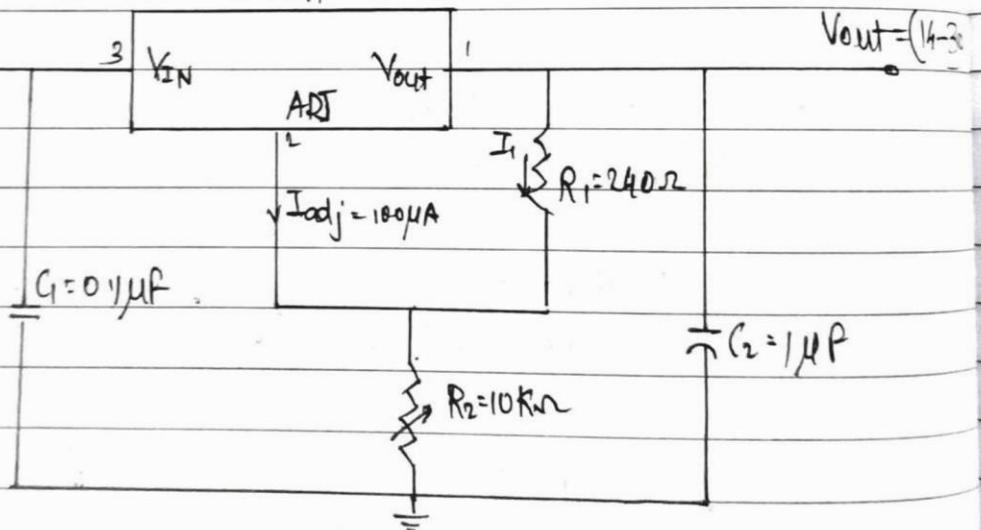
$$\therefore 28.75 = 5.3 \times 10^3 R_2$$

$$\therefore R_2 = 5.42 \text{ k}\Omega.$$

$\therefore R_2$  is Potentiometer of 10k $\Omega$  for adjusting  $V_{out}$  from 14 V to 30 V.

LM317

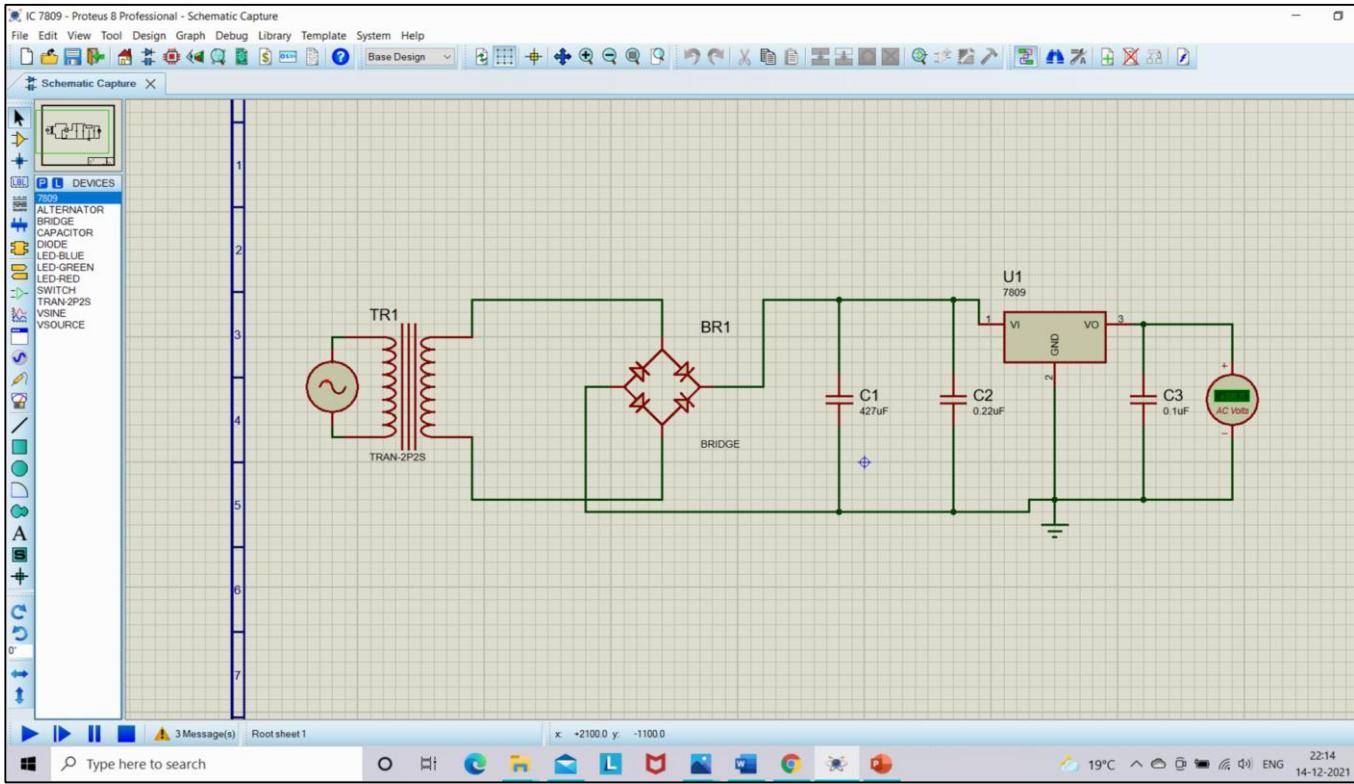
$V_{in} = 33V$



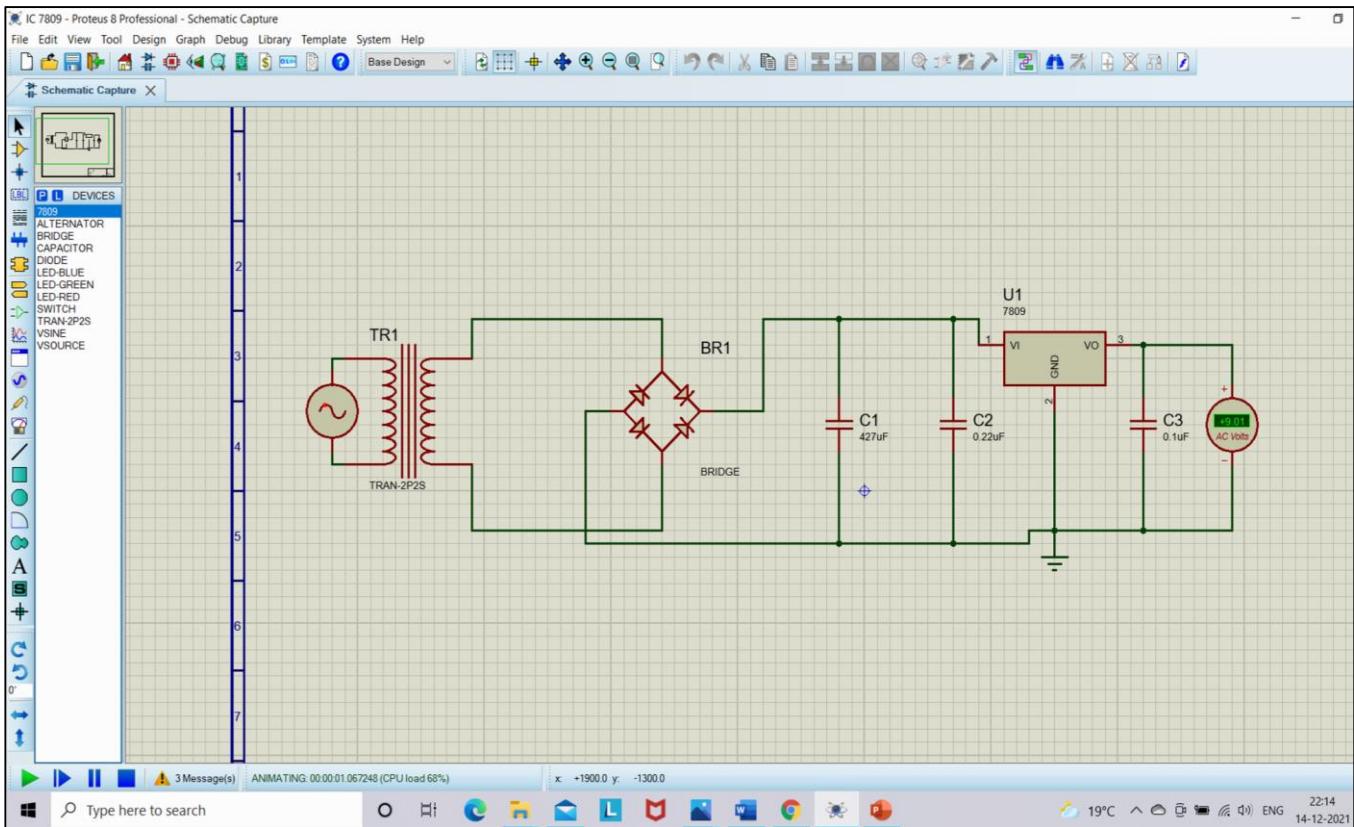
Adjustable voltage regulator using LM317.

# Proteus Circuit:

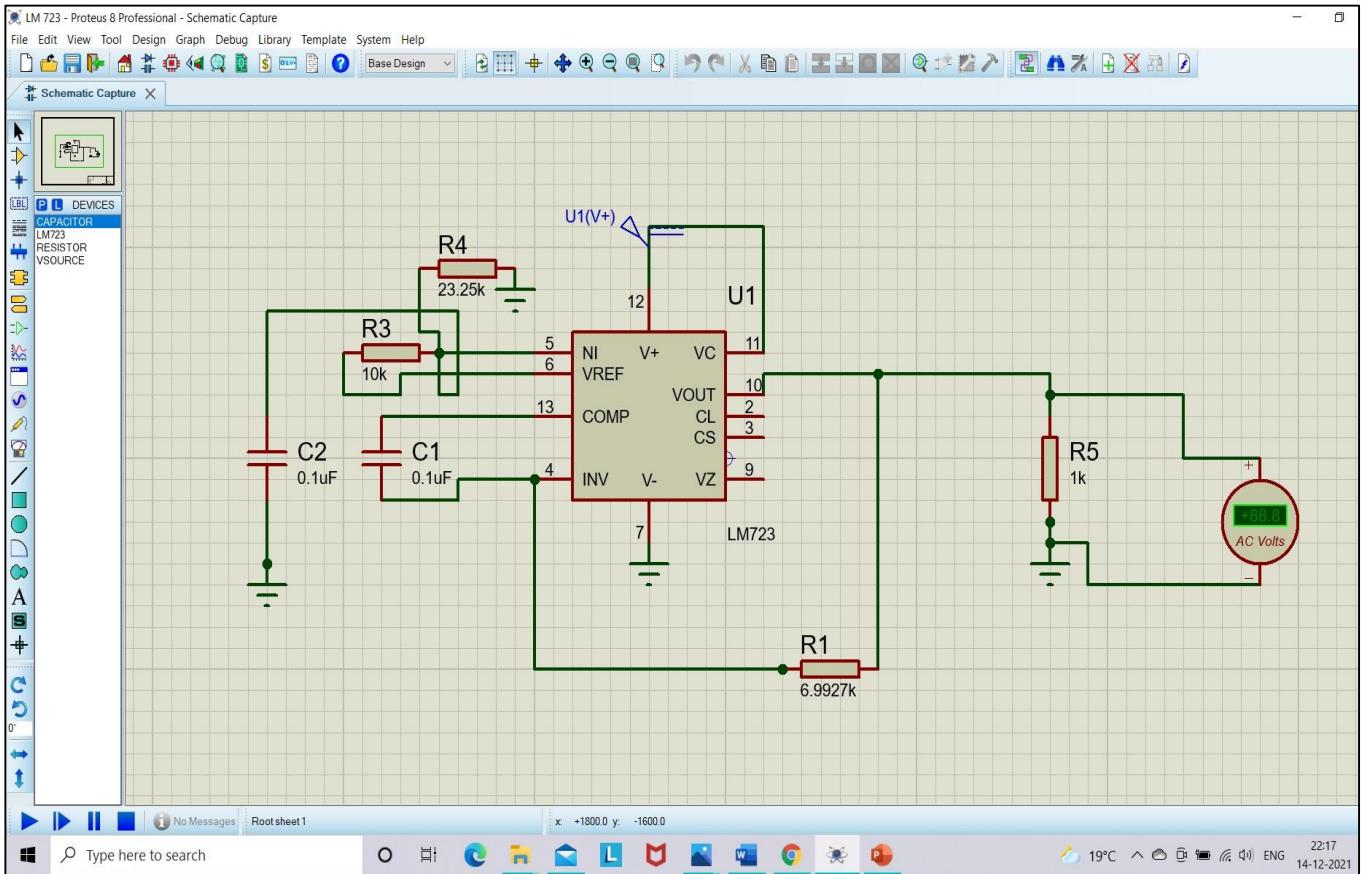
## 1. IC 7809



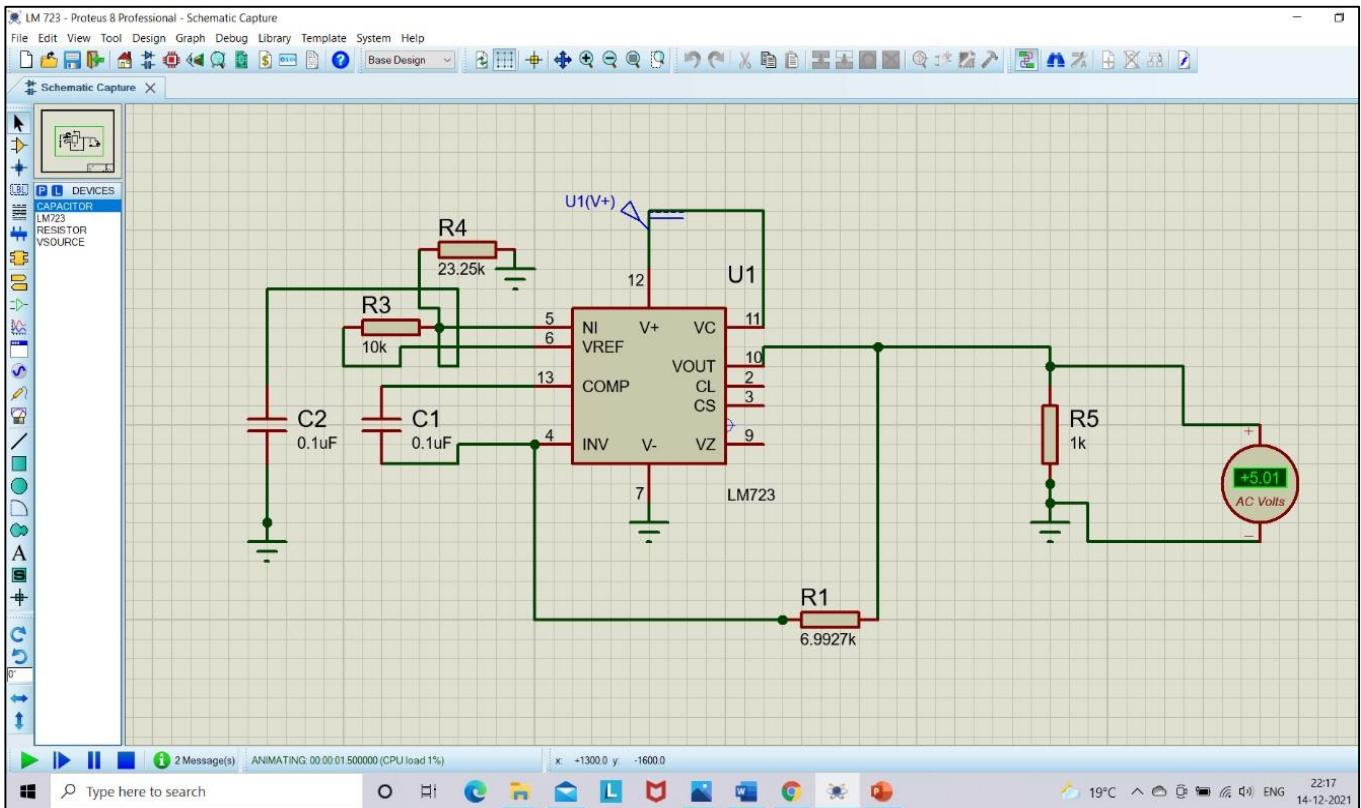
Output:



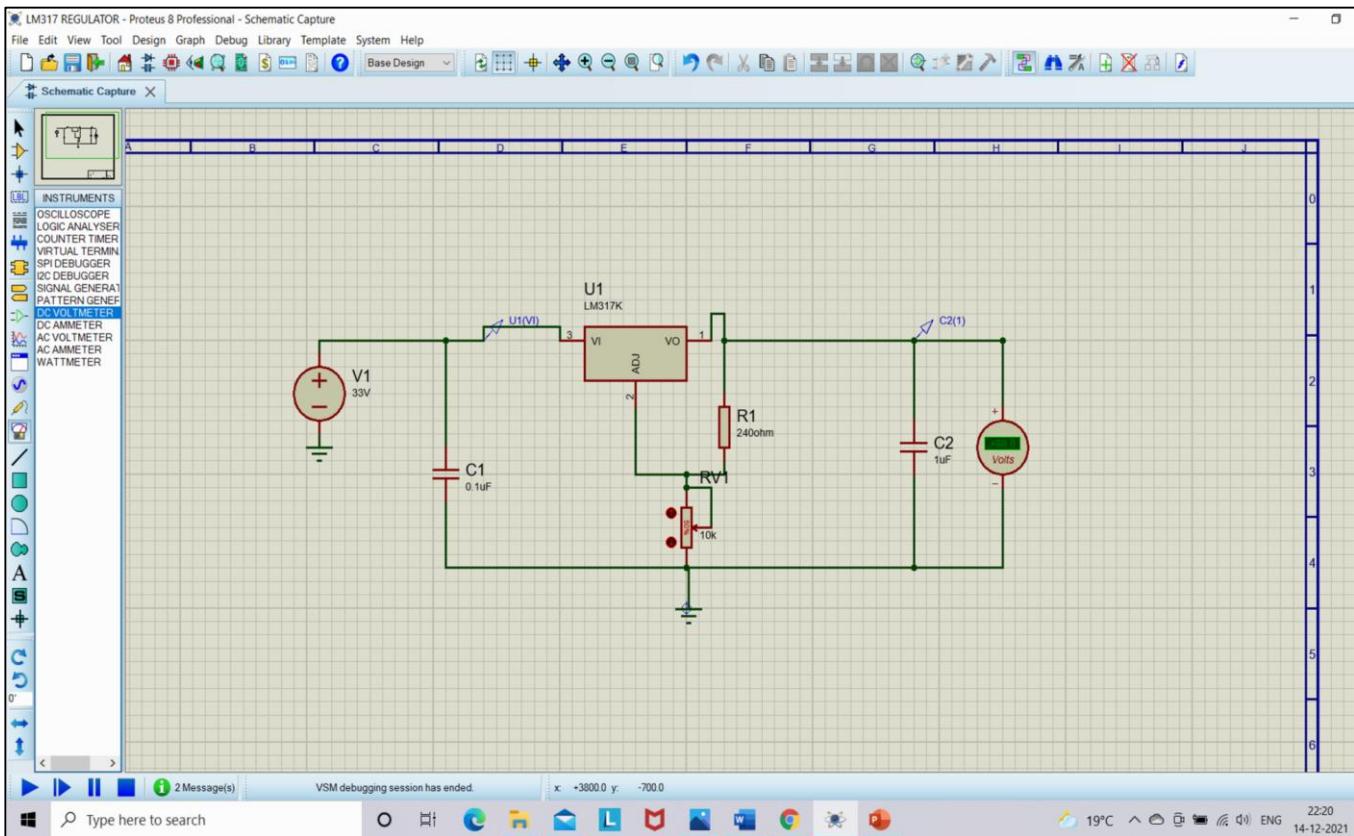
## 2. IC 723 –



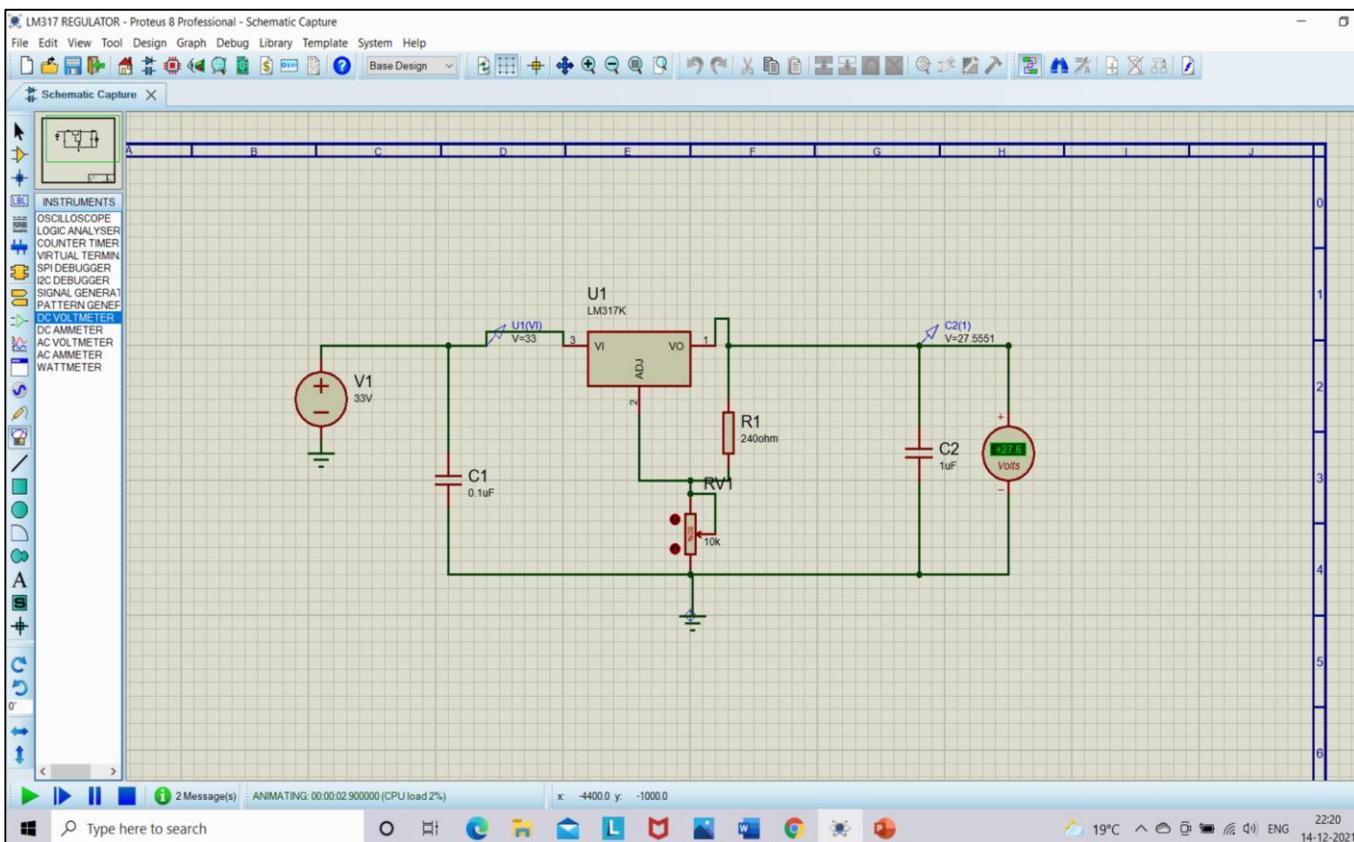
Output:



### 3. LM 317 -



Output:



## **Results:**

<b>Regulator</b>	<b>Desired output</b>	<b>Practical output</b>
IC 7809	9 V	9.01 V
IC 723	5 V	5.01 V
LM 317	27 V	27.6 V

## **Conclusion:**

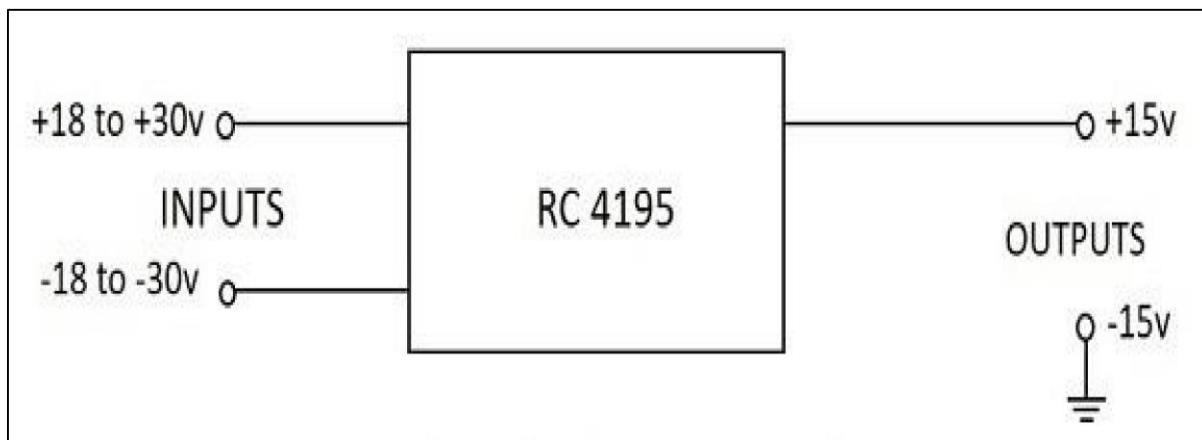
- We have designed the voltage regulator using IC 7809 for output voltage 9V where both desired and practical (obtained) values are verified and almost equal.
- We have designed the voltage regulator using IC 723 for output voltage 5V where both desired and practical (obtained) values are verified and almost equal.
- We have designed the voltage regulator using LM 317 for output voltage range 14V-30V where both desired and practical (obtained) values are verified and almost equal.

## Experiment no: 2

**Aim:** To Design Dual tracking regulator.

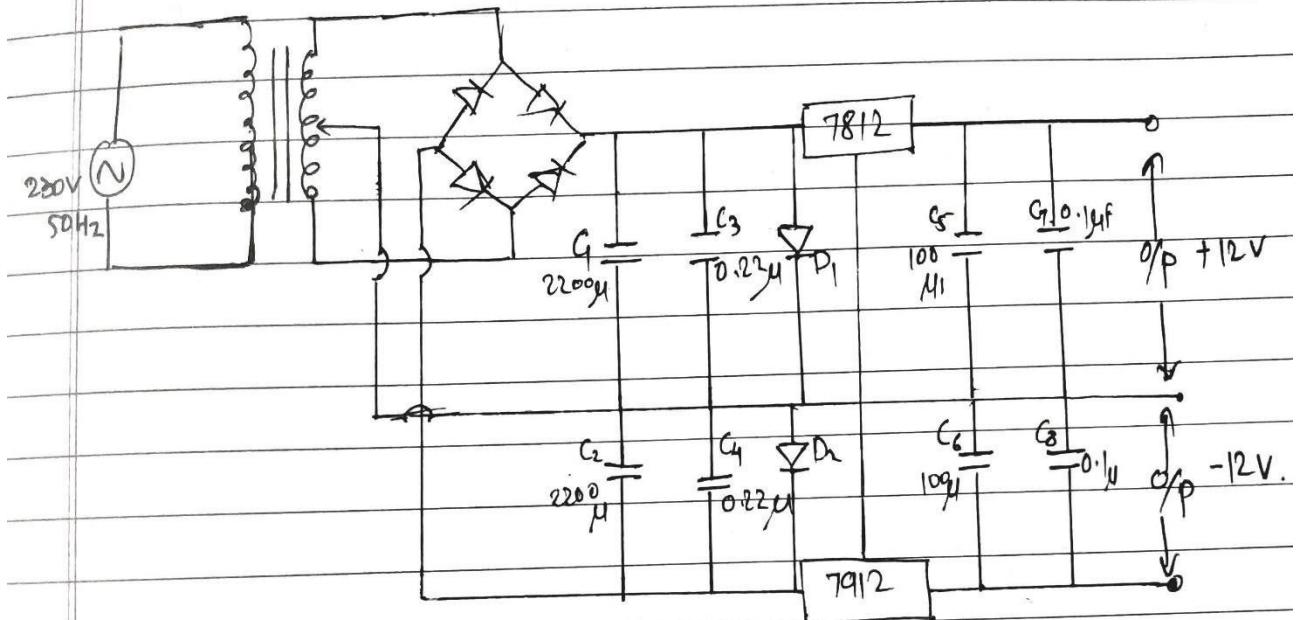
**Software Requirements:** Proteus.

**Theory:** A dual-tracking regulator is used when split-supply voltages are needed. These provide equal positive and negative output voltages. For example, the RC4195 IC provides D.C. outputs of +15v and -15v. This needs two unregulated input voltages such as the positive input may vary from +18v to +30v and negative input may vary from -18v to -30v.

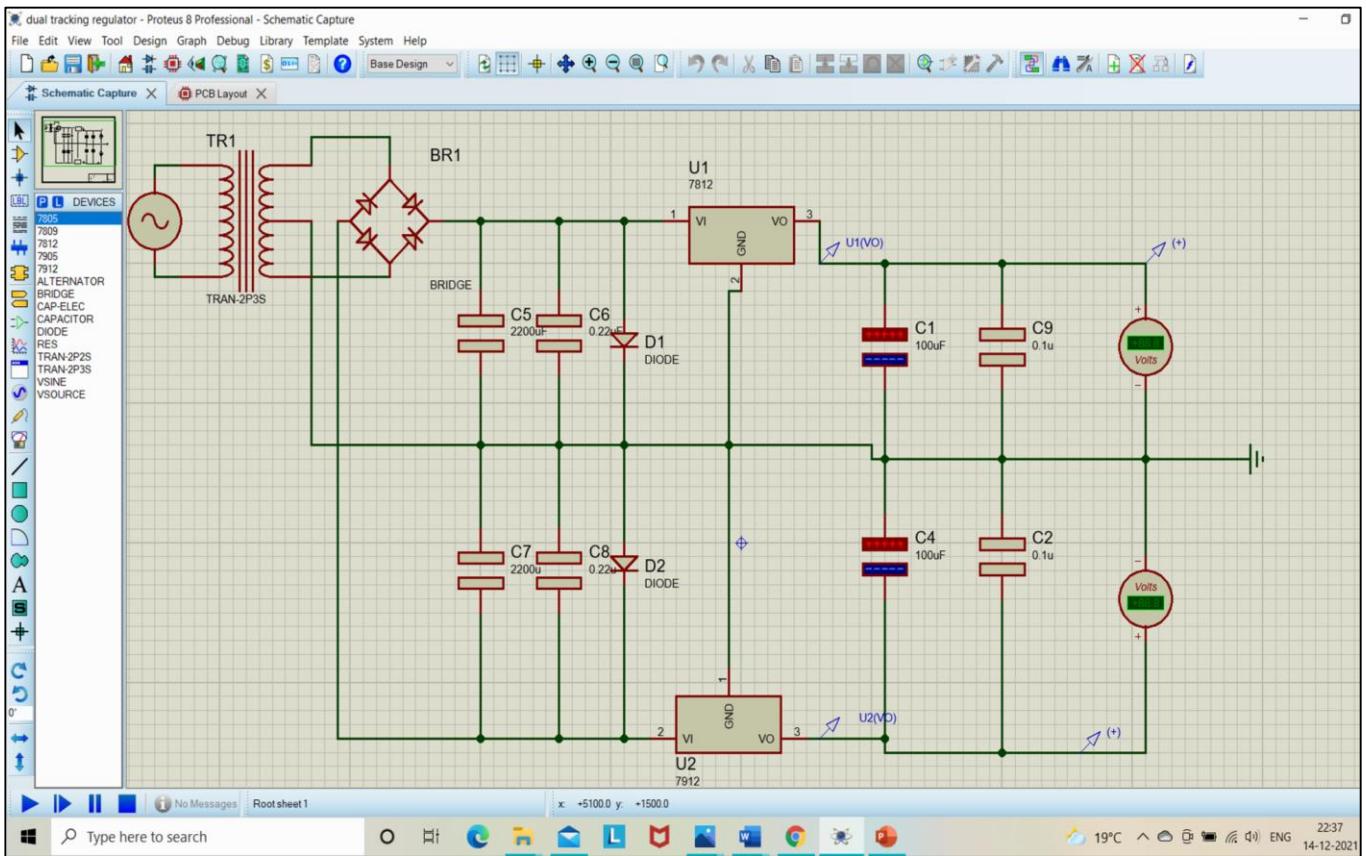


The above image shows a dual-tracking RC4195 IC regulator. The adjustable dual-tacking regulators are also available whose outputs vary between two rated limits. Bipolar or dual voltage supplies can be easily designed with the help of two 3-terminal regulators. Oppositephase ac is provided by the transformer's secondary and a grounded centre tap. The single full-wave bridge converts these into positive and negative dc voltages (with respect to the grounded centre tap). The output of the rectifier circuit is filtered with the help of capacitors C1 and C2.

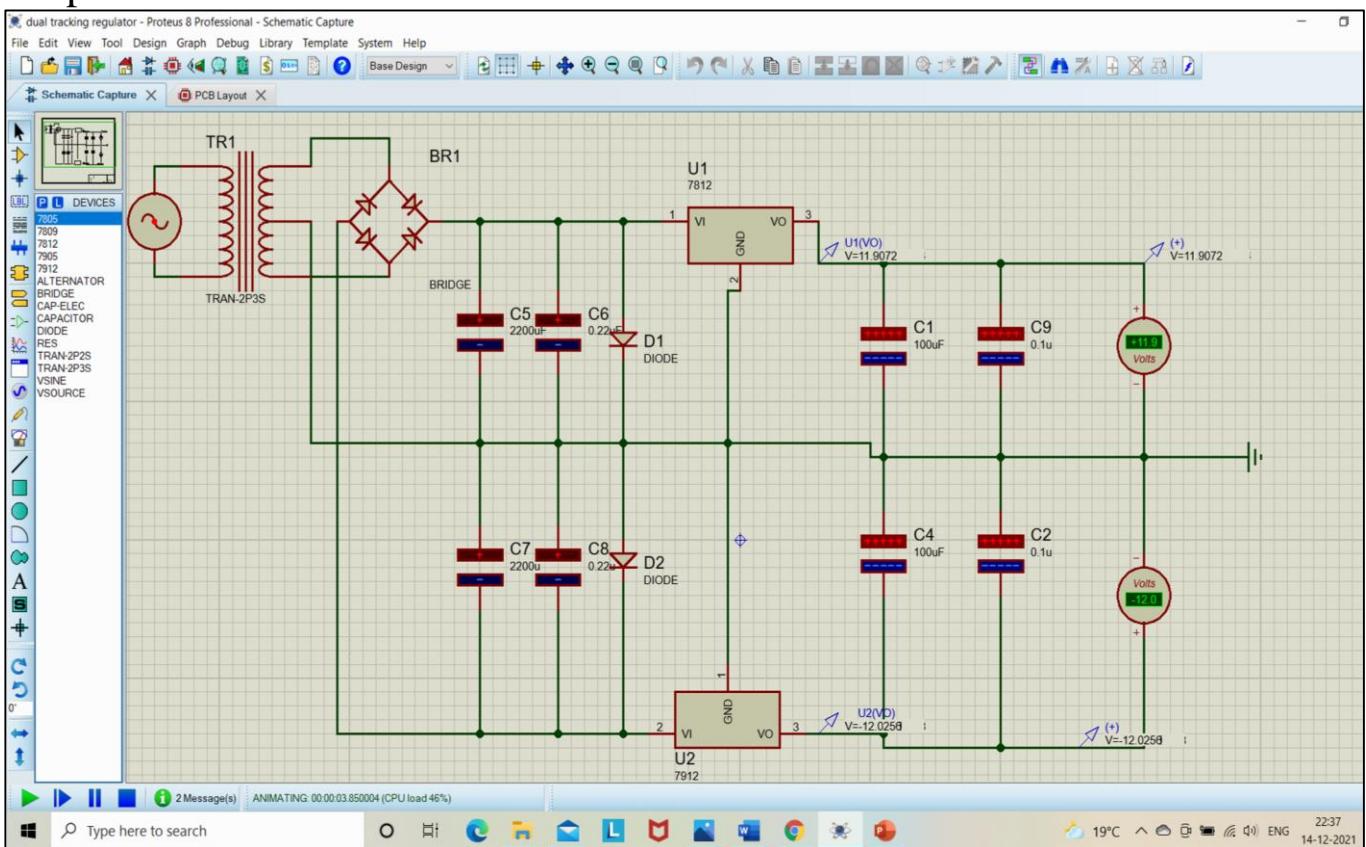
Dual Tracking regulator:



## Proteus Circuit:



## Output:



## **Results:**

<b>Regulator</b>	<b>Desired</b>	<b>Practical</b>
Output voltage	+12 v, -12 v	+11.99 v, -12 v

## **Conclusion:**

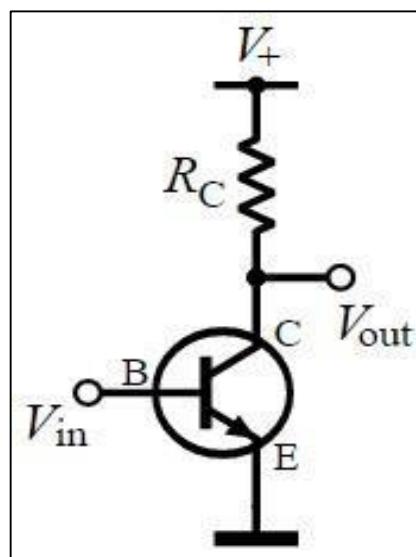
- We have designed the Dual tracking voltage regulator using IC 7812 and IC 7912 for output voltage +12V and 12V where both desired and practical (obtained) values are verified and almost equal.

## Experiment no: 3

**Aim:** To Design Common Emitter Amplifier.

**Software Requirements:** Proteus.

**Theory:** The common emitter amplifier is a three basic singlestage bipolar junction transistor and is used as a voltage amplifier. The input of this amplifier is taken from the base terminal, the output is collected from the collector terminal and the emitter terminal is common for both the terminals. The basic symbol of the common emitter amplifier is shown below.



The single stage common emitter amplifier circuit shown above uses what is commonly called “Voltage Divider Biasing”. This type of biasing arrangement uses two resistors as a potential divider network across the supply with their centre point supplying the required Base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits.

### Theoretical Calculations:

Design a Common-Emitter amplifier where gain is 150

$$\text{Gain} = -\frac{R_C}{r_E}$$

$$150 = \frac{R_C}{r_E}$$

$$\therefore R_C = 150 r_E.$$

$$V_{CC} = I_C R_C + V_{CEQ} + I_E R_E$$

$$I_{CQ} = I_C = 2.5 \text{ mA.}$$

$$r_E = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{2.5 \text{ mA}}$$

$$\therefore I_E \approx I_C.$$

$$\therefore r_E = \frac{25 \text{ mV}}{2.5 \text{ mA}} = 10 \Omega.$$

$$\therefore R_C = 150 \times r_E = 150 \times 10 = 1.5 \text{ k}\Omega.$$

$$V_{CE} = V_C - V_E = 5 \text{ V.}$$

$$\therefore V_{CE} - I_C R_C = V_C$$

$$12 - (2.5 \times 1.5) = V_C$$

$$\therefore V_C = 12 - 3.75 = \underline{\underline{8.25 \text{ V}}}$$

$$V_C - V_E = 5$$

$$\therefore V_E = 8.25 - 5 = \underline{\underline{3.25 \text{ V}}}$$

$$V_E = I_E R_E$$

$$\therefore 3.25 = 2.5 \times 10^{-3} \times R_E$$

$$\therefore R_E = 1.4 \text{ k}\Omega$$

$$V_{BE} = V_B - V_E$$

$$\therefore 0.7 = V_B - 3.25$$

$$\therefore V_B = 3.95 \text{ V.}$$

$$V_B = V_{CC} + \frac{R_2}{R_1 + R_2}$$

$$\therefore \frac{R_2}{R_1 + R_2} = \frac{4.2}{12}$$

$$\therefore \frac{R_2}{R_1 + R_2} = 0.35.$$

let,  $R_2 = 10\text{k}\Omega$ .

$$\therefore \frac{10}{R_1 + 10} = 0.35$$

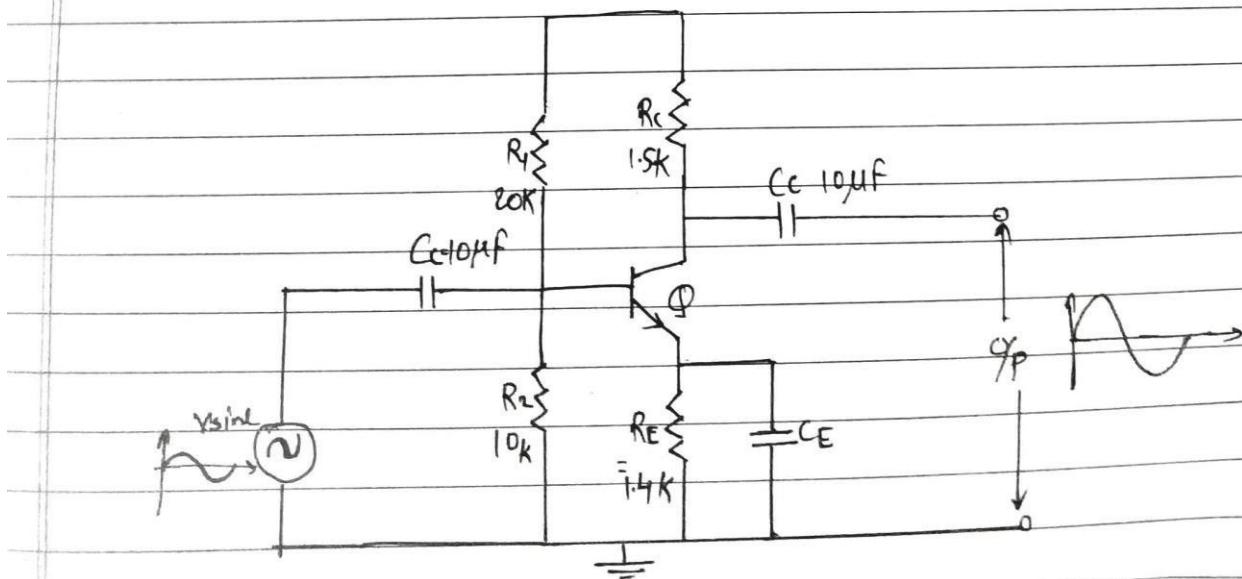
$$\therefore R_1 = 18.57\text{k}\Omega$$

$$\therefore \underline{R_1 \approx 20\text{k}\Omega}$$

Selection of  $C_C$  and  $C_E$ .

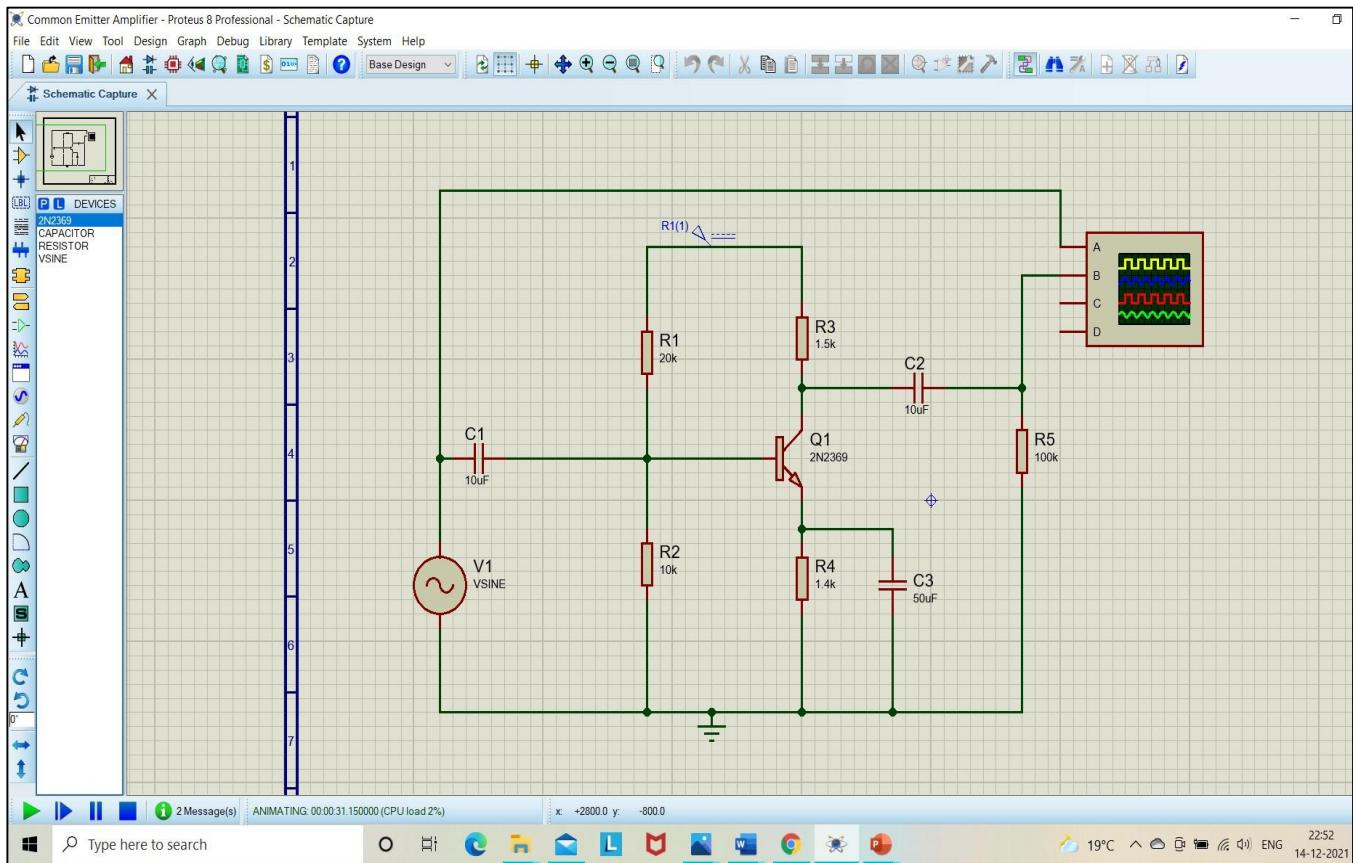
$$C_C = 10\mu\text{F}$$

$$\text{and } C_E = 50\mu\text{F}$$

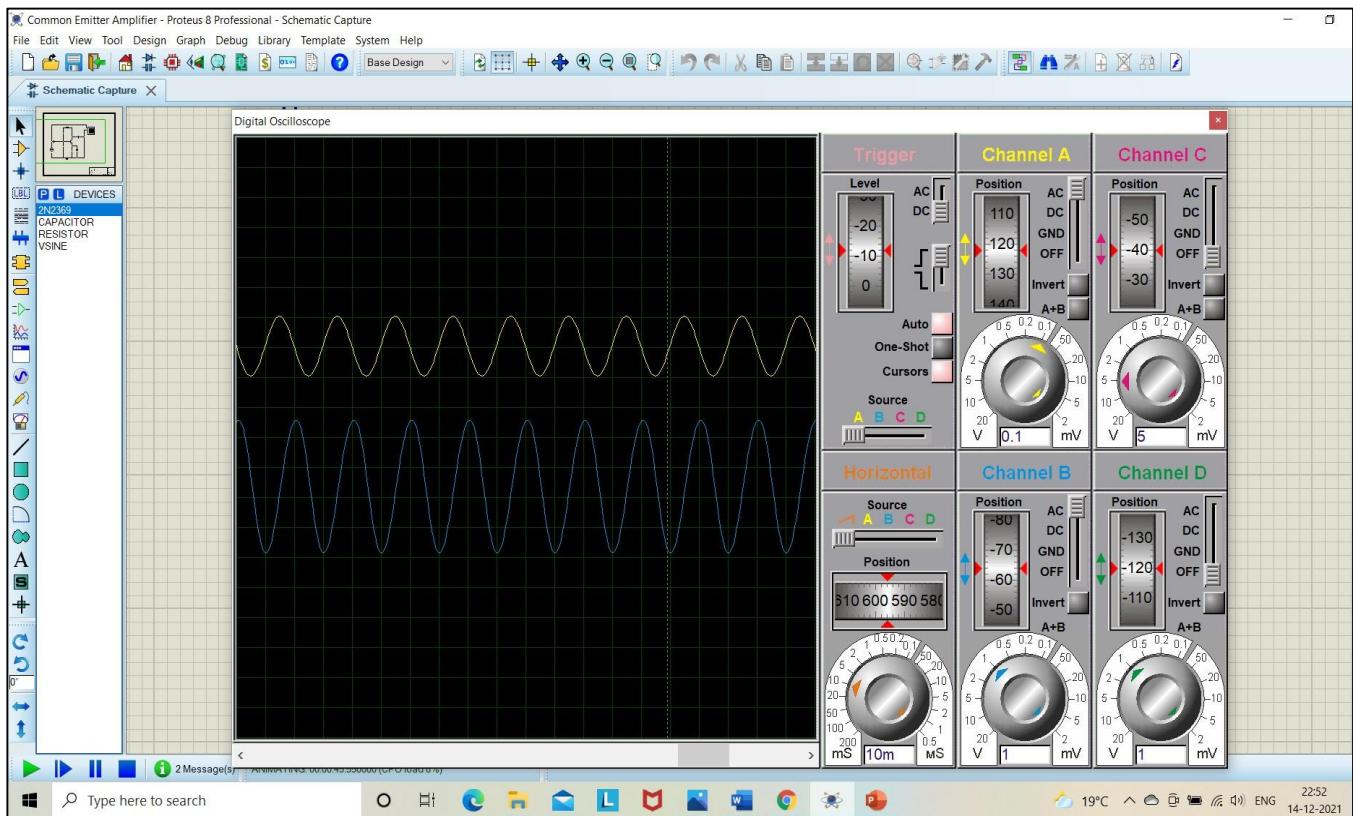


Common Emitter Amplifier.

## Proteus Circuit:



## Output:



## **Conclusion:**

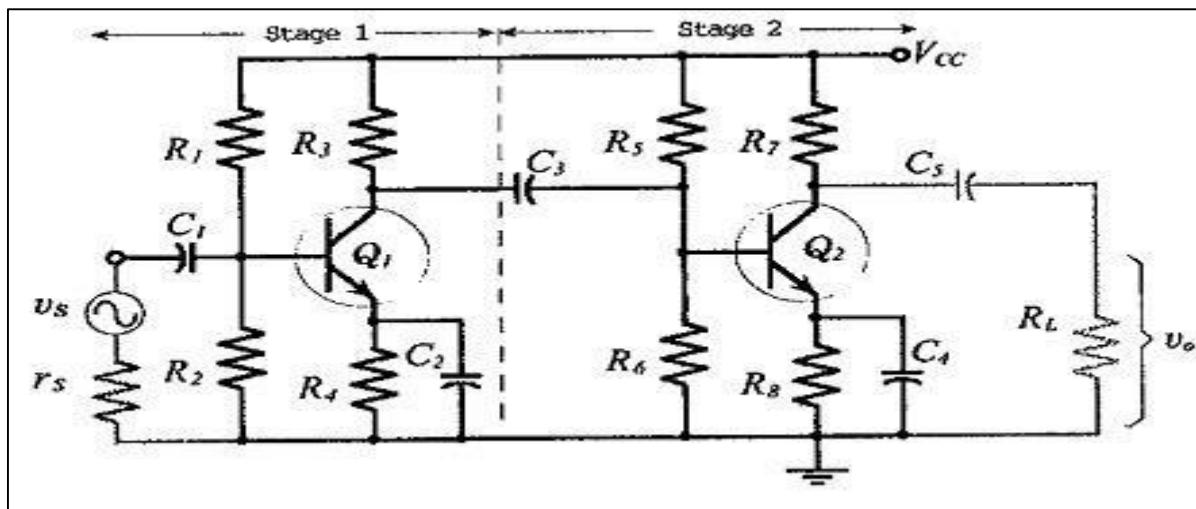
- we have seen how does a Common Emitter Amplifier (CEA) configuration behave. At first, a simplified circuit is presented to get introduced to the main aspects of this amplifier.
- The CEA present high voltage and current gains that are enhanced by the presence of a derivation capacitance in the emitter branch, it also presents high input and output impedance, making it suitable as a universal amplifier for many applications.
- One other characteristic, specific only to CEAs is the phase inversion of  $180^{\circ} = \pi$  rad between the input and output signals.

## Experiment no: 4

**Aim:** To Design two-stage Common Emitter Amplifier with RC coupling.

**Software Requirements:** Proteus.

**Theory:** The signal is applied to the input of Stage-1, and the load is coupled to the output of Stage-2. The signal is amplified by Stage-1, and the output of Stage-1 is amplified by Stage-2, so that the overall voltage gain is much greater than the gain of a single stage. A Capacitor Coupled Two Stage CE Amplifier circuit is shown in Fig.



Stage-1 is capacitor-coupled (via  $C_3$ ) to the input of Stage-2. The signal is applied to the input of Stage-1, and the load is coupled to the output of Stage-2. The signal is amplified by Stage-1, and the output of Stage-1 is amplified by Stage-2, so that the overall voltage gain is much greater than the gain of a single stage. As illustrated by the circuit waveforms in Fig, the signal voltage is phase-shifted through 180° by Stage-1, and through a further 180° by Stage-2. Consequently, the overall phase shift from input to output is zero (or 360°).

## Theoretical Calculations:

To Design a two-stage Common-Emitter Amplifier with following Specifications:

$$V_{CC} = 20V, I_{CEQ} = 10mA$$

$$h_{ie} = 2.5k\Omega$$

$$V_{BE} = 0.6V.$$

$$S = 3, f = 20 \text{ to } 20 \text{ kHz.}$$

$$R_L = 1k\Omega$$

$$\text{and } R_S = 5\Omega.$$

Calculating  $R_E, R_1, R_2, R_4$ :

$$V_{RE} = \frac{1}{10} V_{CC} = \frac{20}{10} = 2V.$$

$$R_E = \frac{V_{RE}}{I_E} = \frac{2}{10mA} = 200\Omega.$$

$$\therefore R_E = 200\Omega.$$

$$V_{R2} = V_{RE} + V_{BE}$$

$$= 2 + 0.6$$

$$V_{R2} = 2.6V$$

$$R_2 = \frac{V_{R2}}{I_{R2}}$$

$$I_{R2}$$

$$= \frac{2.6}{1mA}$$

$$I_{R2} = 10\% \text{ of } I_{CEQ}$$

$$= 10\% \text{ of } 10mA$$

$$I_{R2} = 1mA$$

$$R_2 = 2.6k\Omega$$

$$V_{CC} = V_{R1} + V_{R2}$$

$$V_{R1} = V_{CC} - V_{R2} = 20 - 2.6 = 17.4V.$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{17.4}{1} = 17.4k\Omega.$$

$$V_{RC_1} = V_{CC} - V_{CEQ} - V_{RE}$$

$$= 20 - 10 - 2$$

$$V_{RC_1} = 8 \text{ V}$$

$$R_{C_1} = \frac{V_{RC_1}}{I_{RC_1}} = \frac{8}{10 \text{ mA}}$$

$$R_{C_1} = 0.8 \text{ k}\Omega$$

Calculating  $C_C$ ,  $C_1$ ,  $C_2$  and  $C_{CE}$ :

$$X_{C_1} = \frac{1}{f_0} = \frac{2.5 \text{ k}\Omega}{10}$$

$$X_{C_1} = 250 \text{ }\mu\text{F}$$

$$G = \frac{1}{2\pi f X_{C_1}} = \frac{1}{2\pi \times 20 \times 250}$$

$$C_1 = 31 \mu\text{F}$$

$$X_{C_2} = \frac{1}{f_0} (R_{C_1} \parallel R_L)$$

$$= \frac{(800 \times 1000)}{10 \times 1800}$$

$$X_{C_2} = 44.4 \text{ }\mu\text{F}$$

$$C_2 = \frac{1}{2\pi f X_{C_2}} = \frac{1}{2\pi \times 20 \times 44.4}$$

$$C_2 = 176.8 \mu\text{F}$$

$$X_{CE} = \frac{1}{f_0} [R_{C_1} + (R_3 \parallel R_4)]$$

$$= \frac{1}{f_0} [800 + (17.4 \parallel 19.6)]$$

$$X_{CE} = 306.2 \text{ }\mu\text{F}$$

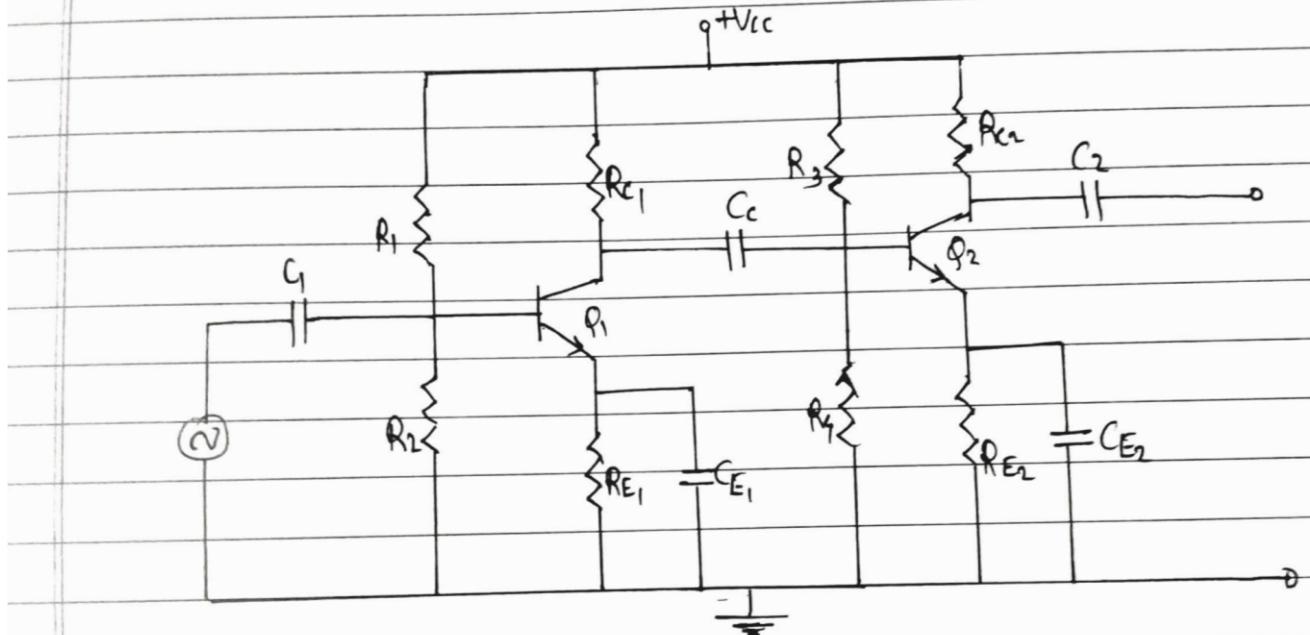
$$\therefore C_C = \frac{1}{2\pi \times 20 \times 306.2} \rightarrow 26.5 \mu\text{F}$$

$$X_{CE} = \frac{1}{10} R_E$$

$$X_{CE_1} = \frac{200}{10} = 20 \Omega$$

$$C_E = \frac{1}{2\pi \times 10 \times 20}$$

$$\therefore C_E = \underline{397.8 \mu F}$$



$$R_1 = R_3$$

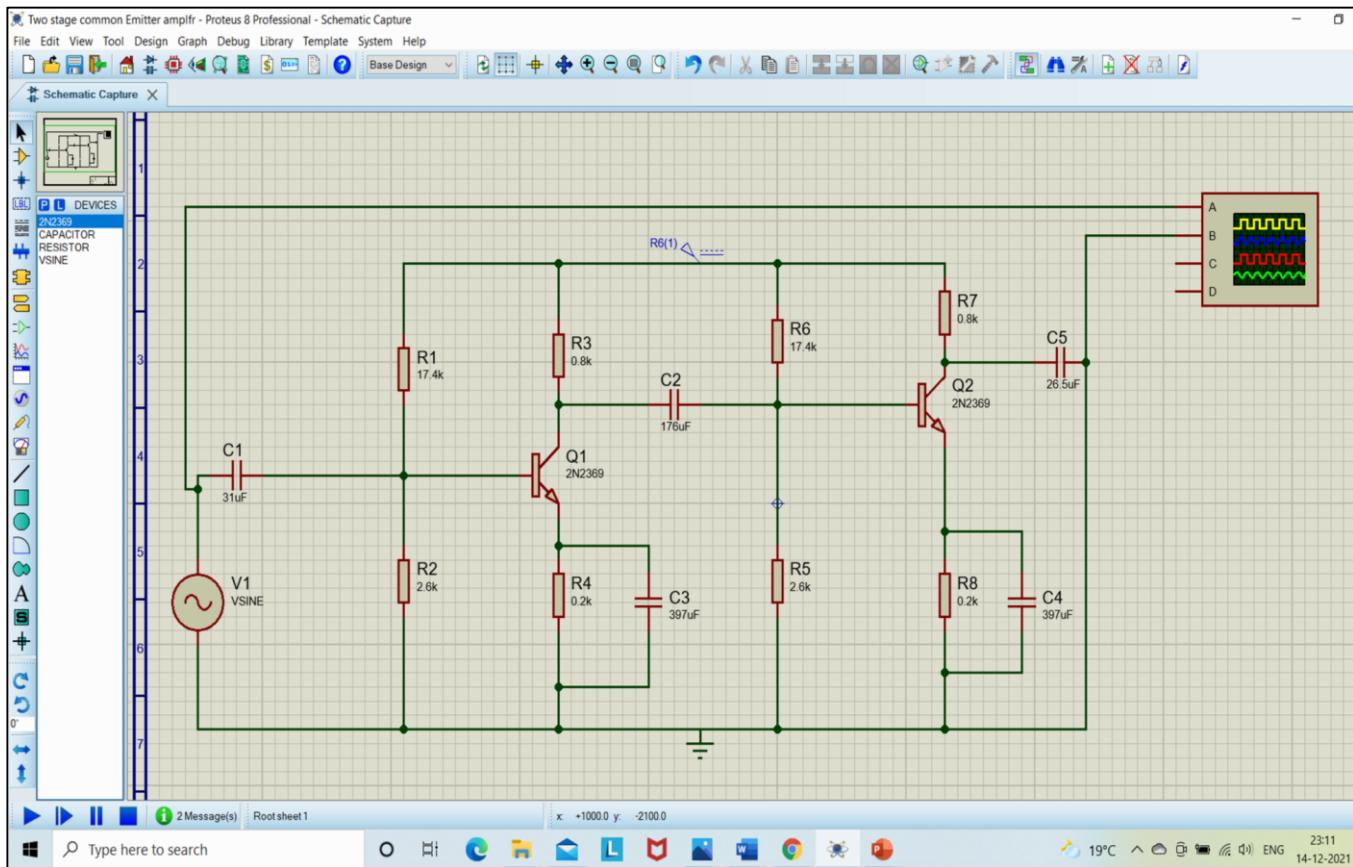
$$R_2 = R_4$$

$$R_C_1 = R_C_2, C_E_1 = C_E_2$$

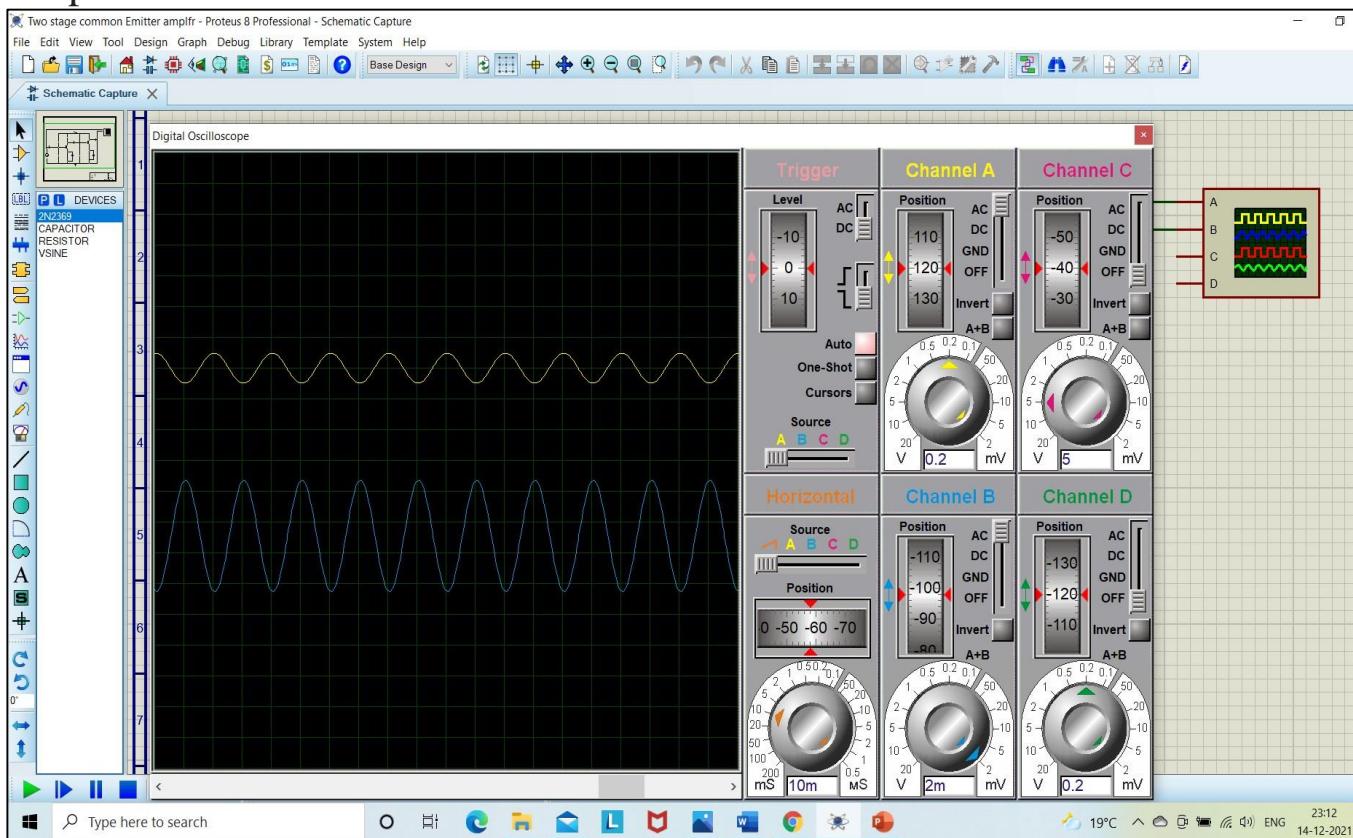
and  $R_{E_1} = R_{E_2}$ .

Two-stage Common Emitter Amplifier.

## Proteus Circuit:



## Output:



## **Conclusion:**

- The Impact of input and output loading can be minimized by two amplifiers with appropriate input and output characteristics.
- Multistage can be used to create amplifiers with high resistance, low output resistance and large gains.
- A multistage amplifier using two or more single stage common emitter amplifiers is used in high gain applications like audio amplifiers, etc.

## **Experiment no: 5**

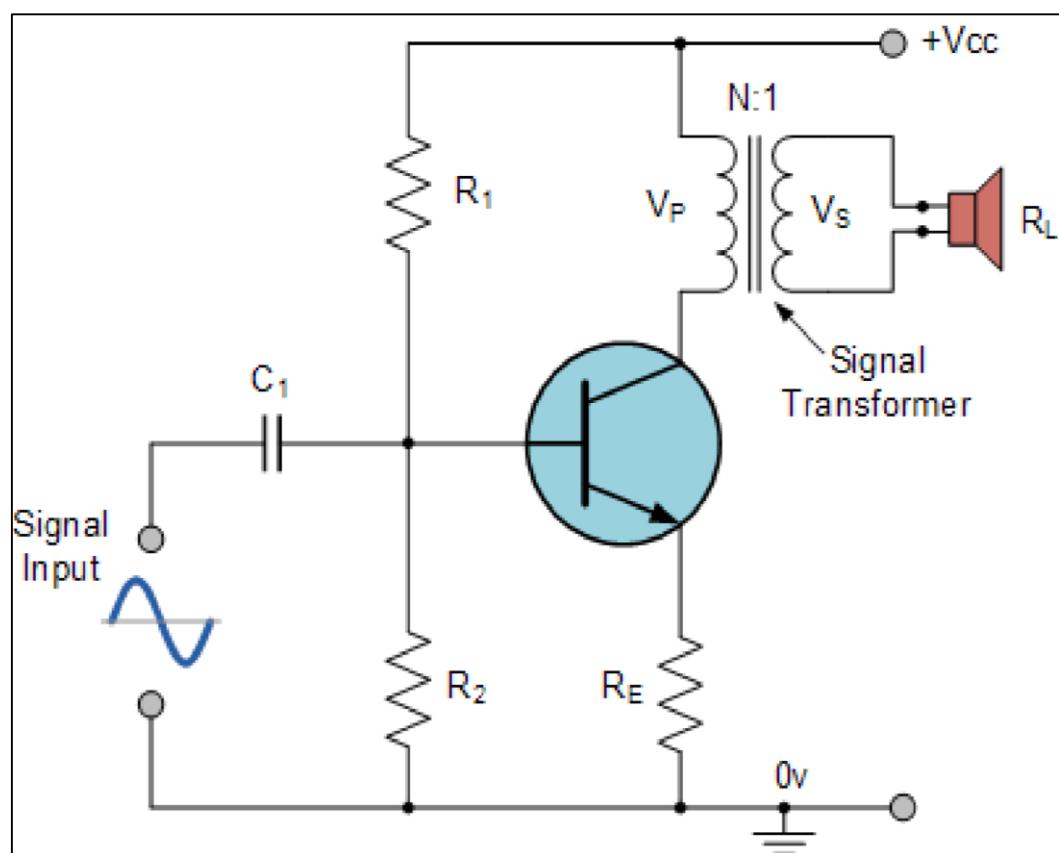
**Aim:** To Design Class-A power Amplifier.

**Software Requirements:** Proteus.

**Theory:** The most commonly used type of power amplifier configuration is the Class A Amplifier. The Class A amplifier is the simplest form of power amplifier that uses a single switching transistor in the standard common emitter circuit configuration as seen previously to produce an inverted output. The transistor is always biased “ON” so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude of the output signal.

This means then that the Class A Amplifier configuration is the ideal operating mode, because there can be no crossover or switch-off distortion to the output waveform even during the negative half of the cycle. Class A power amplifier output stages may use a single power transistor or pairs of transistors connected together to share the high load current. Single Stage Amplifier Circuit is the simplest type of Class A power amplifier circuit. It uses a single-ended transistor for its output stage with the resistive load connected directly to the Collector terminal. When the transistor switches “ON” it sinks the output current through the Collector resulting in an inevitable voltage drop across the Emitter resistance thereby limiting the negative output capability.

## Transformer-coupled Amplifier Circuit



## Theoretical Calculations:

Design a Class -A-Transformer coupled power Amplifier for:  
 $V_{CC} = 12V$ ,  $n = 2.2$ ,  $\text{load} = 4\Omega$ , DC primary resistance  $20\Omega$ ,  
 Gain  $\beta = 50$ .

$$\text{let, } V_C' = 0.2 V_{CC} = 2.4V$$

$$V_C' = I_C R_{py} \therefore I_C = \frac{V_C'}{R_{py}} = \frac{2.4}{20} = 0.1A.$$

$$\text{Set } V_{CEQ} = 0.5 V_{CC} = 6V.$$

$$V_E' \approx 0.3 V_{CC}$$

$$V_E' = V_{CC} - V_{CEQ} - V_C' = 12 - 6 - 2.4 = 4V.$$

$$V_E' = I_E R_E.$$

$$\therefore R_E = \frac{V_E'}{I_E} \approx \frac{V_E'}{I_C} = \frac{4}{0.1} = 40\Omega. \quad \dots (I_E \approx I_C)$$

$$\text{Now, } \frac{V_{CC} R_2}{R_1 + R_2} - (0.1 - 0.7) - V_E' = 0.$$

$$V_{CC} K - 0.8 - V_E' = 0.$$

$$\therefore 12K = 4.8$$

$$\therefore K = 0.4.$$

$$\therefore \frac{R_2}{R_1 + R_2} = 0.4.$$

$$\text{let, } R_2 = 10K\Omega \therefore R_1 = 15K\Omega.$$

$$I_{CQ} = I_{C\max} = 4I_C = 0.1A.$$

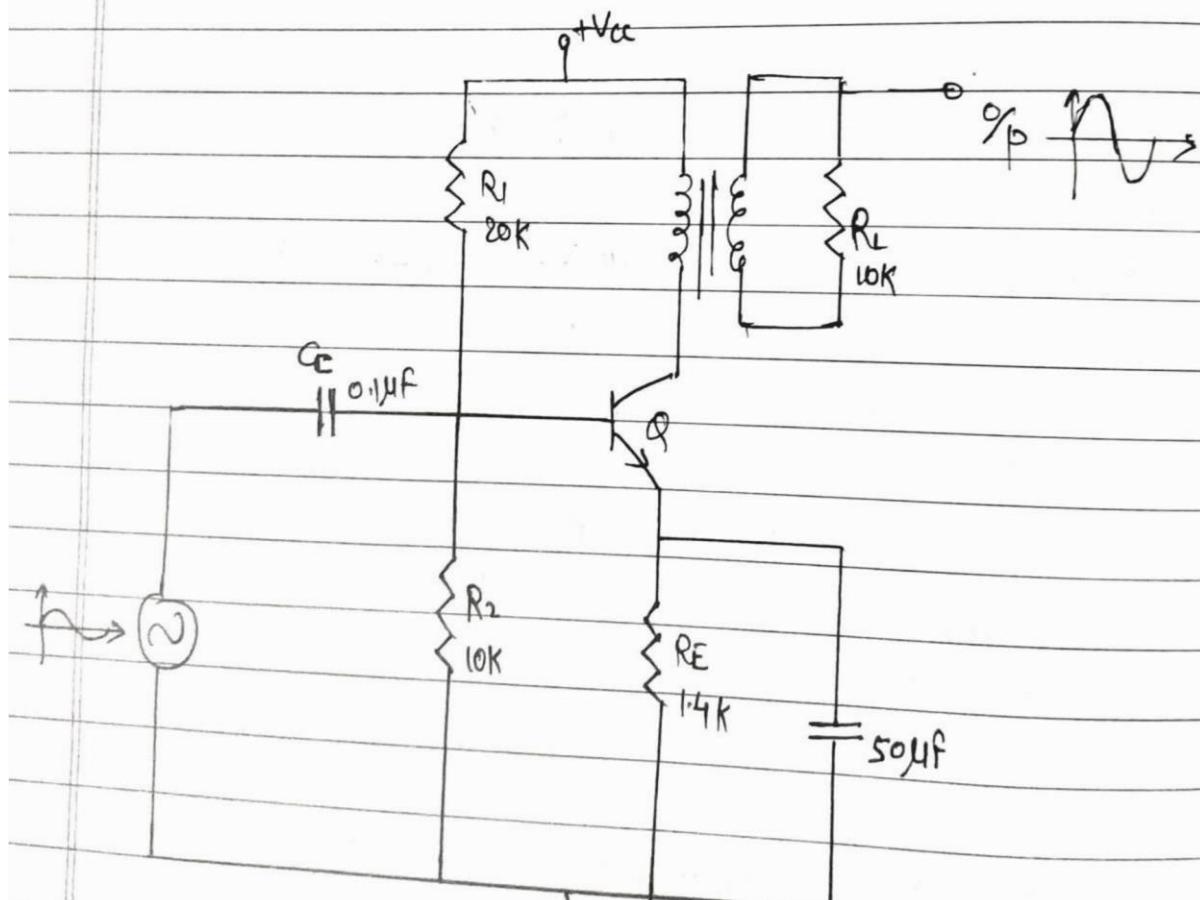
$$R_{L(QD)} = R_L' + R_{py} = n^2 R_L + 20 = 4.9 \times 4 + 20 = 41.2\Omega.$$

$$\Delta V_{CE} = \Delta I_C \cdot R_{L(QD)} = 0.1 \times 41.2 = 4.1V.$$

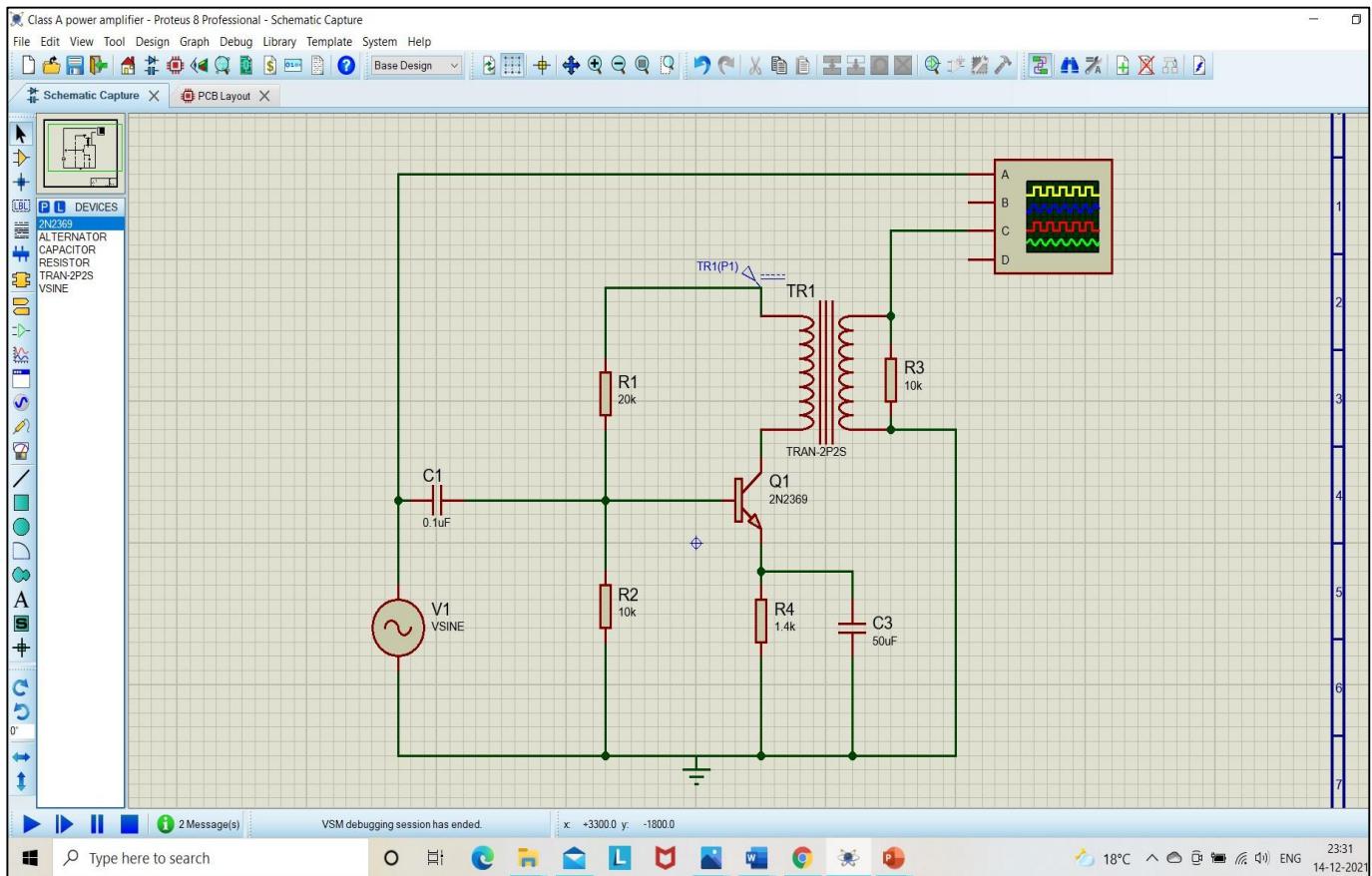
$$\text{Power rating of Transistor, } P_d = \Delta V_{CE} \cdot \Delta I_C = 4.1 \times 0.1 = 0.41W.$$

Stability of design;  
 Here  $R_2 = 10\text{ k}\Omega$   $R_1 = 15\text{ k}\Omega$   
 $R_B = R_1 \parallel R_2 = 6\text{ k}\Omega$ .

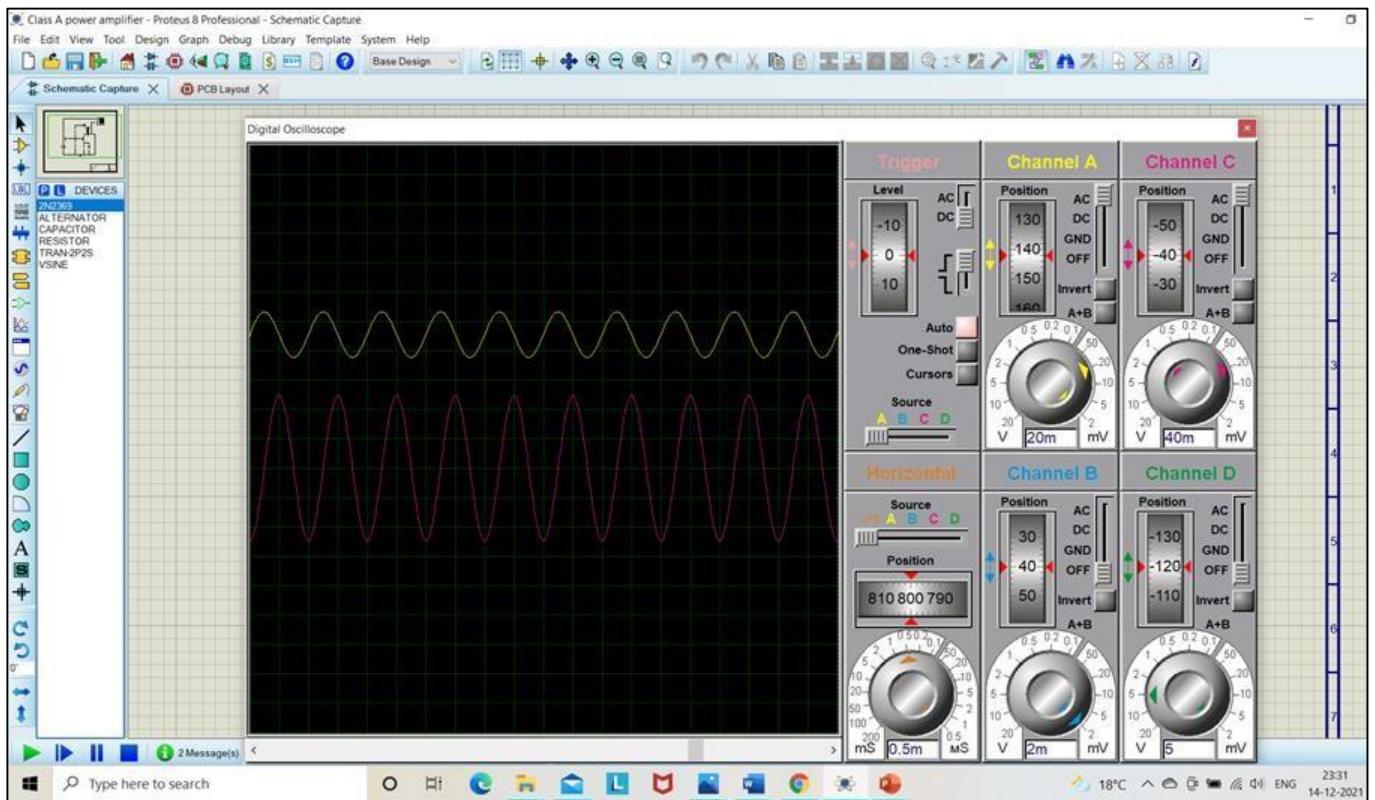
$$\begin{aligned} \text{Stability factor is } S &= \frac{(1+\beta) [ (R_B/R_E) + 1 ]}{(1+\beta) + (R_B/R_E)} \\ &= \frac{(1+50) [ 6/0.04 + 1 ]}{(1+50) + (6/0.04)} \\ &= 38.1 \end{aligned}$$



## Proteus Circuit:



## Output:



## **Conclusion:**

- we have seen that Class A amplifiers are biased such as 100 % of the input signal can be used for the amplification process. Moreover, they present a rather low efficiency, but a faithful reproduction of the signal.

## **Experiment no: 6**

**Aim:** To Design Class-B power Amplifier.

**Software Requirements:** Proteus.

**Theory:** To improve the full power efficiency of the previous Class A amplifier by reducing the wasted power in the form of heat, it is possible to design the power amplifier circuit with two transistors in its output stage producing what is commonly termed as a Class B Amplifier also known as a push-pull amplifier configuration.

Push-pull amplifiers use two “complementary” or matching transistors, one being an NPN-type and the other being a PNP-type with both power transistors receiving the same input signal together that is equal in magnitude, but in opposite phase to each other. This results in one transistor only amplifying one half or  $180^\circ$  of the input waveform cycle while the other transistor amplifies the other half or remaining  $180^\circ$  of the input waveform cycle with the resulting “two halves” being put back together again at the output terminal.

Then the conduction angle for this type of amplifier circuit is only  $180^\circ$  or 50% of the input signal.

### Theoretical Calculations:

for Class-B Amplifier providing 20V peak signal and load resistor 16Ω. V<sub>cc</sub> of 30V is given. Calculate input power, Output power and efficiency of amplifier.

$$P_{dc} = V_{cc} \times I_{dc}$$

$$I_{dc} = \frac{I_m}{\sqrt{2}} \quad \left| \quad I_m = \frac{V_m}{R_L} = \frac{20}{16} = 1.25 \text{ A.} \right.$$

$$P_{dc} = \underline{30 \times 1.25 / \sqrt{2}} = 30 \times 0.397$$

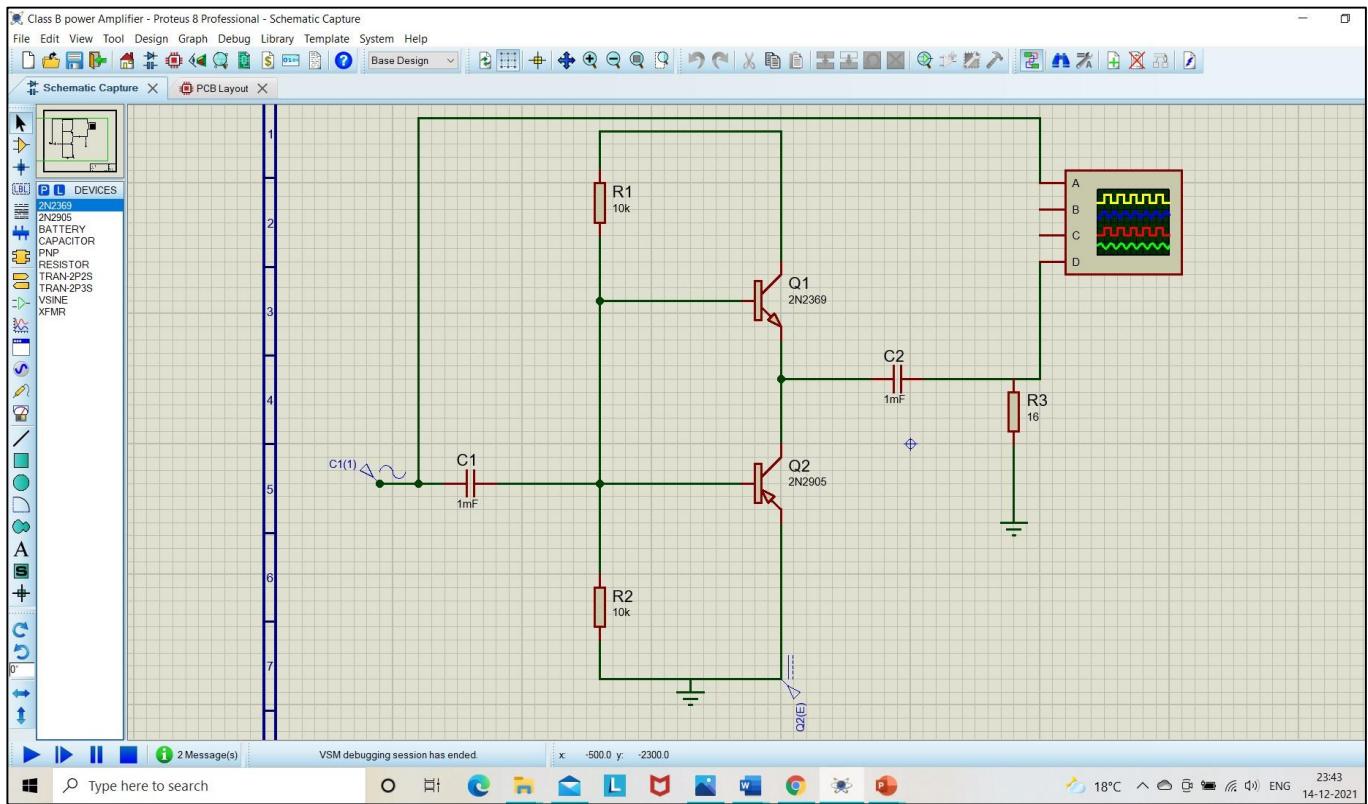
$$\underline{P_{dc} = 11.9 \text{ W}}$$

$$\begin{aligned} P_{dc} &= (I_{rms})^2 (R_{rms}) \\ &= \frac{1}{2} \times \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} \end{aligned}$$

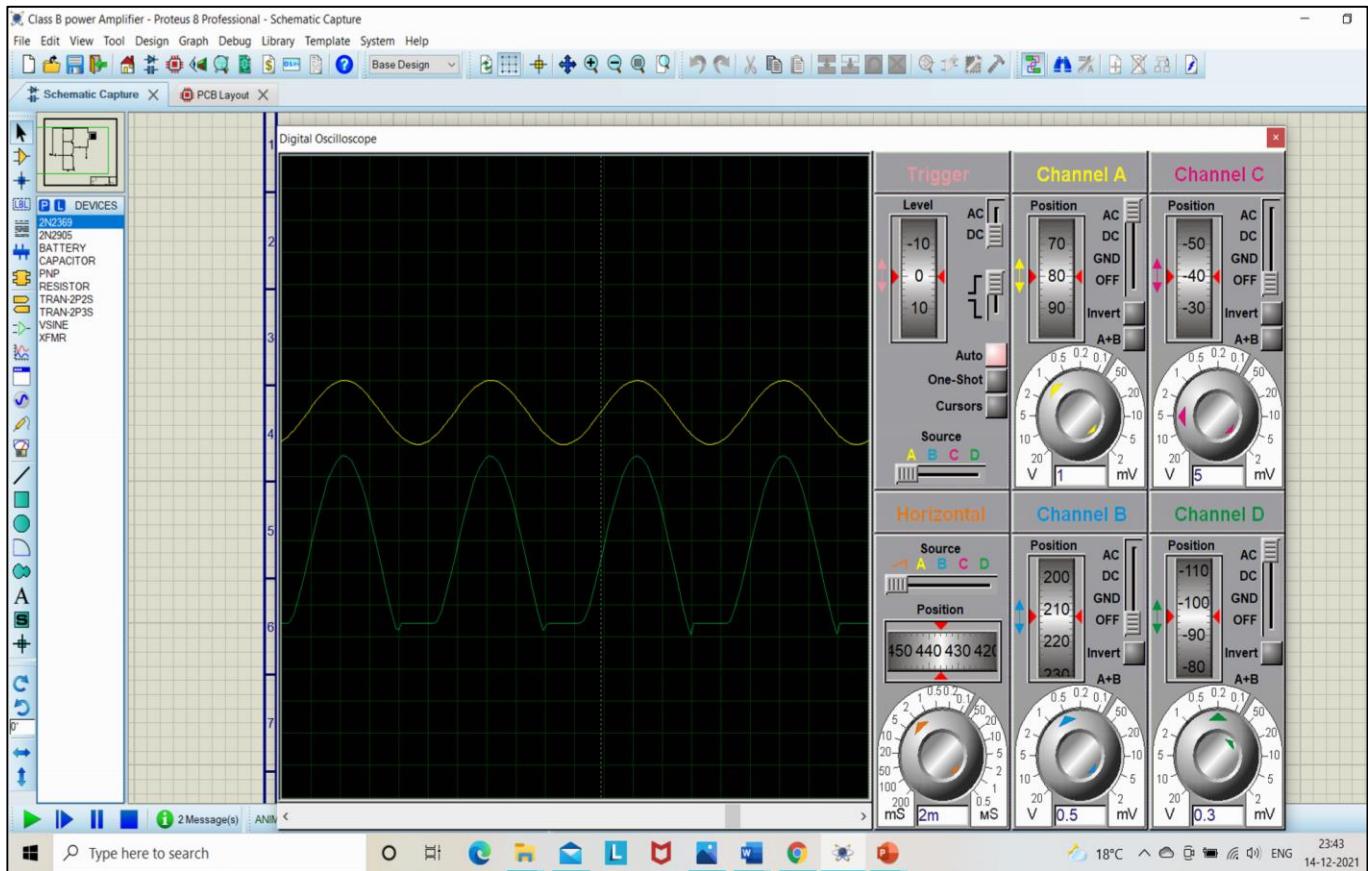
$$\underline{P_{dc} = 6.25 \text{ W}}$$

$$\begin{aligned} h &= \frac{P_{dc} \times 100}{P_{dc}} = \frac{6.25}{11.9} \times 100 \\ &= 0.525 \times 100 \\ \therefore h &= \underline{52.5 \%} \end{aligned}$$

## Proteus Circuit:



## Output:



## **Conclusion:**

- It presents only a  $180^\circ$  conduction angle and does not reproduce the signal faithfully.
- we learned a method to calculate the Class B efficiency.
- This increase in efficiency is due to the low  $180^\circ$  conduction angle that allow the transistors to only absorb power from the supply when an AC input signal is indeed present.

## Experiment no: 7

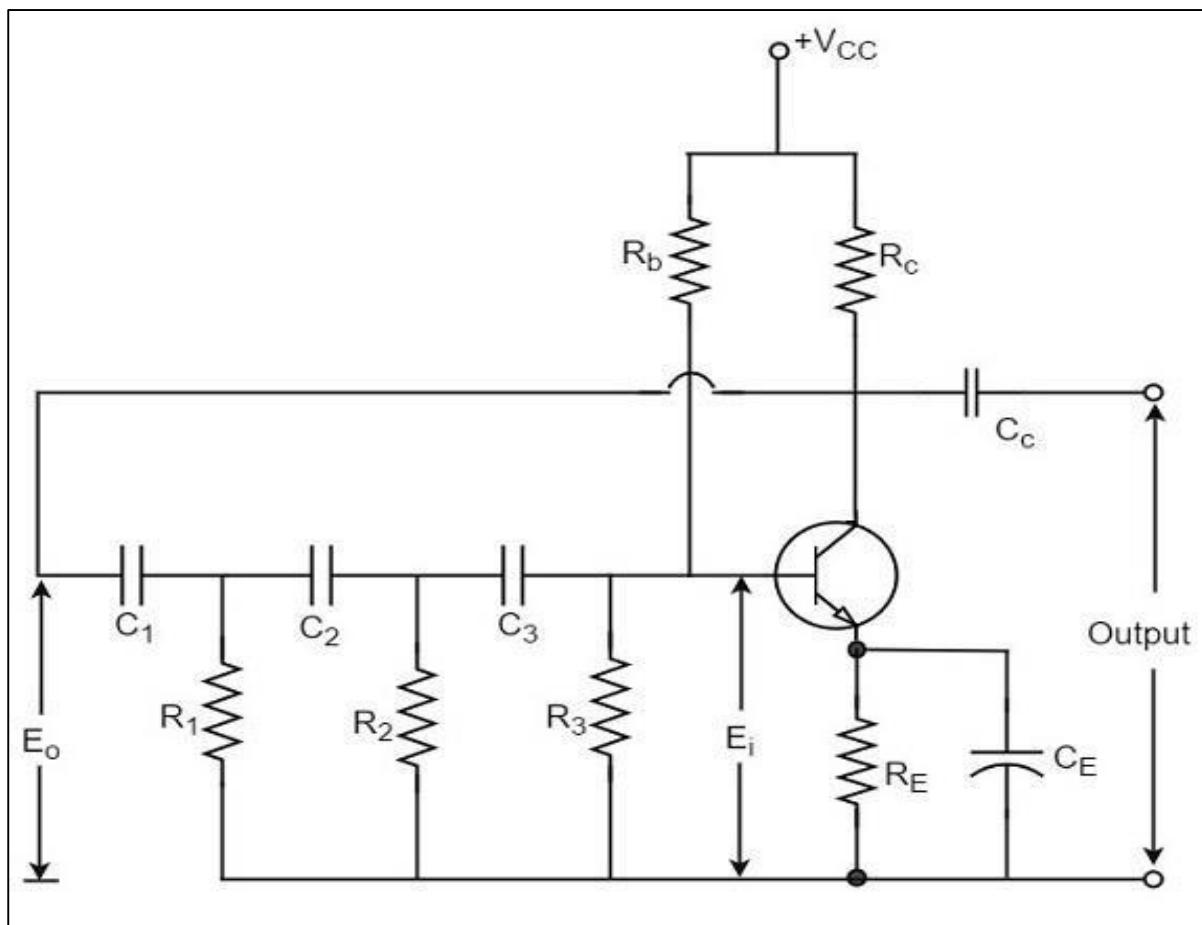
**Aim:** To Design Phase shift and Wein-bridge oscillator.

**Software Requirements:** Proteus.

**Theory:** Phase shift oscillator –

A phase-shift oscillator is a linear electronic oscillator circuit that produces a sine wave output. It consists of an inverting amplifier element such as a transistor or op amp with its output fed back to its input through a phase-shift network consisting of resistors and capacitors in a ladder network.

The following circuit diagram shows the arrangement of an RC phase-shift oscillator.

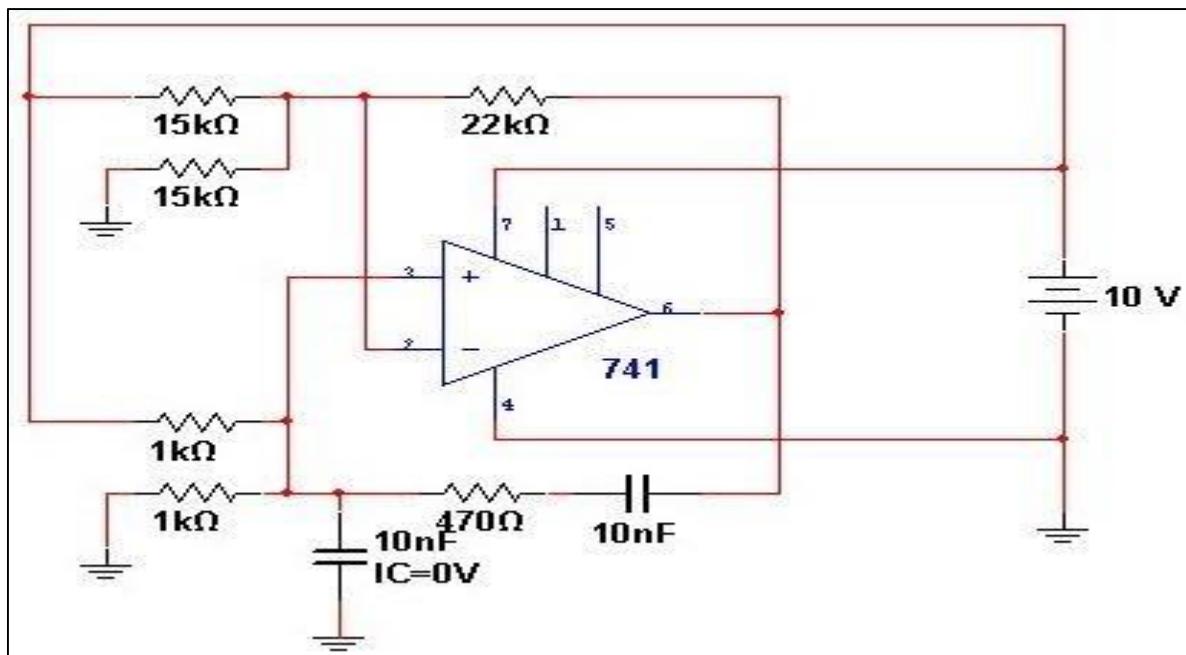


Wien Bridge Oscillator –

Wien Bridge Oscillator is an oscillator which uses RC network so as to produce a sine wave at the output. These are basically the lowfrequency oscillator that generates audio and sub audio frequency that ranges between 20 Hz to 20 KHz.

This oscillator circuit uses the Wien bridge to provide feedback with the desired phase shift. It gives highly stable oscillation frequency and does not vary much with supply or temperature variation.

The bridge comprises four resistors and two capacitors. The oscillator can also be viewed as a positive gain amplifier combined with a bandpass filter that provides positive feedback. Automatic gain control, intentional non-linearity and incidental non-linearity limit the output amplitude in various implementations of the oscillator



Theoretical Calculations:

Design a Wein bridge oscillator to produce a sine wave of 1 kHz.

$$f = \frac{1}{2\pi \sqrt{R_1 C_1 R_2 C_2}}$$

Let,  $R_1 = R_2$  and  $C_1 = C_2$ .

$$\therefore f = \frac{1}{2\pi R C}$$

$$\therefore 1 \text{ kHz} = \frac{1}{2\pi R C}$$

$$2\pi R C = \frac{1}{10^3}$$

Let,  $C = 0.01 \mu F$

$$\therefore R = 15.9 k\Omega$$

$$\therefore R_1 = R_2 \approx 15 k\Omega$$

$$\begin{array}{l} R_3 = 2 \\ R_4 \end{array}$$

$$\therefore \text{If } R_4 = 1 k\Omega \quad R_3 = 2 k\Omega$$

$R_3$  is Potentiometer of  $4.7 k\Omega$  for fine corrections.

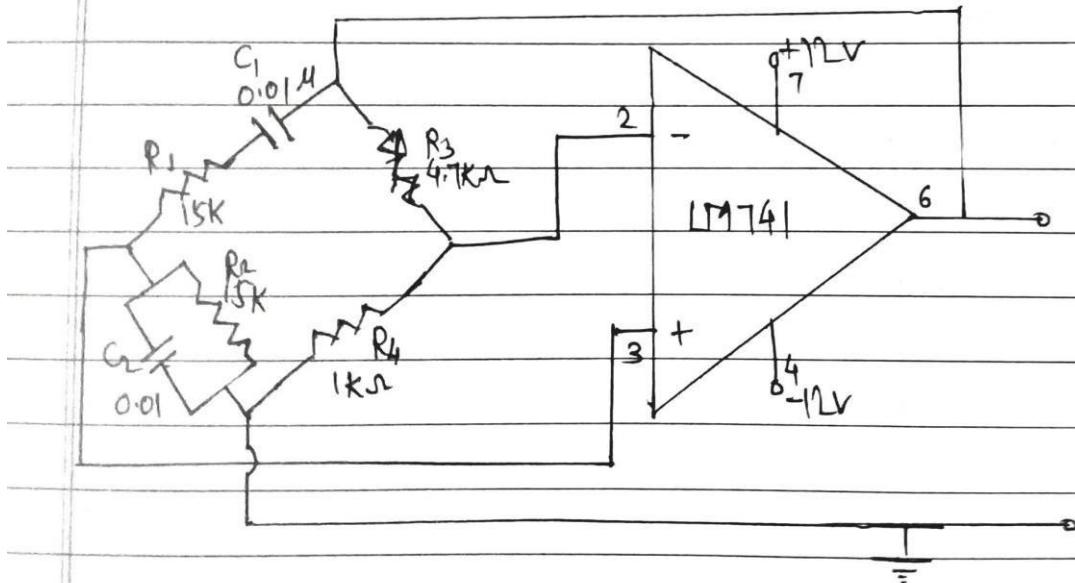
frequency of waveform in Proteus.

$$T = t_1 - t_2 \dots \text{ (completion of 1 cycle)} \\ = 58.35\text{ms} - 57.30\text{ms}$$

$$T = 1.05\text{ms}$$

$$\therefore f = \frac{1}{T} = \frac{1}{1.05 \times 10^{-3}} = 952.3\text{Hz.}$$

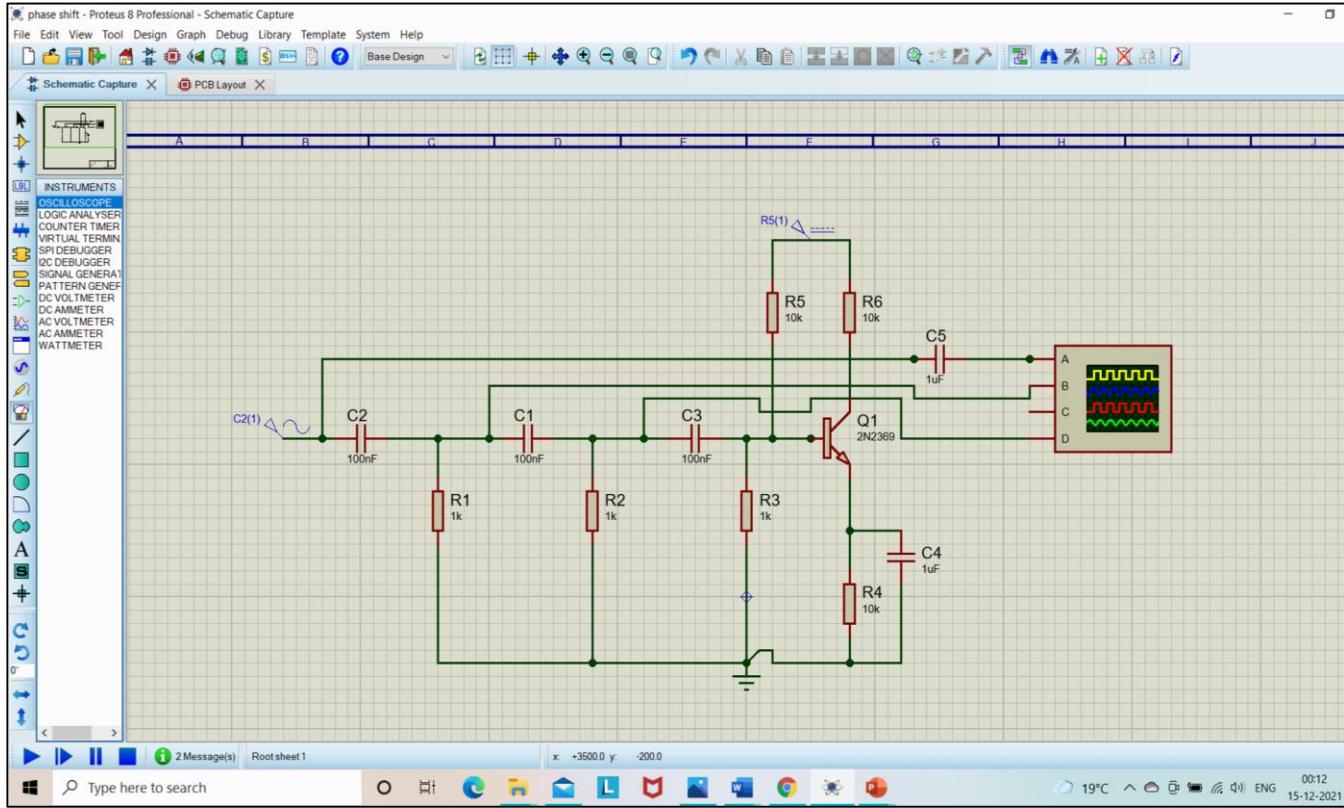
∴ frequency in Proteus = 952.3 Hz



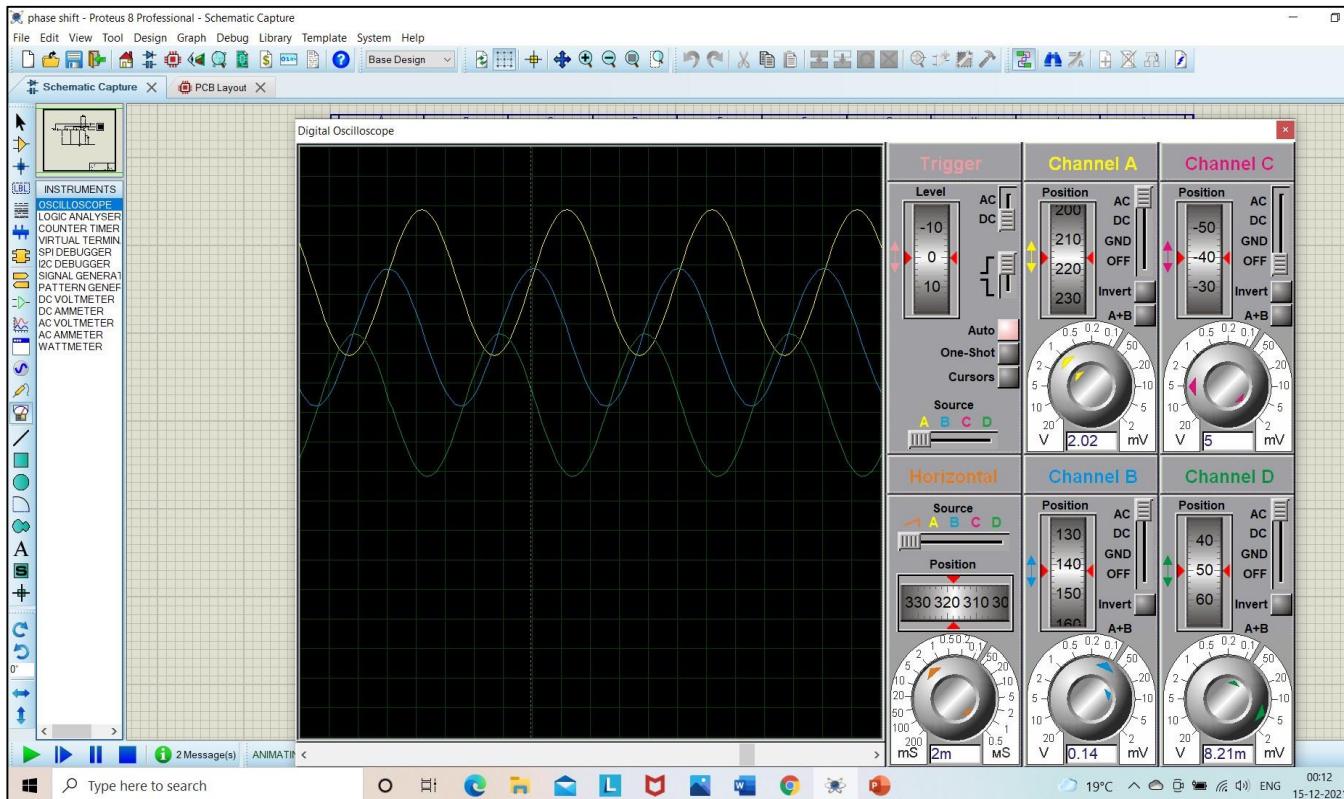
Wein-bridge Oscillator.

# Proteus Circuit:

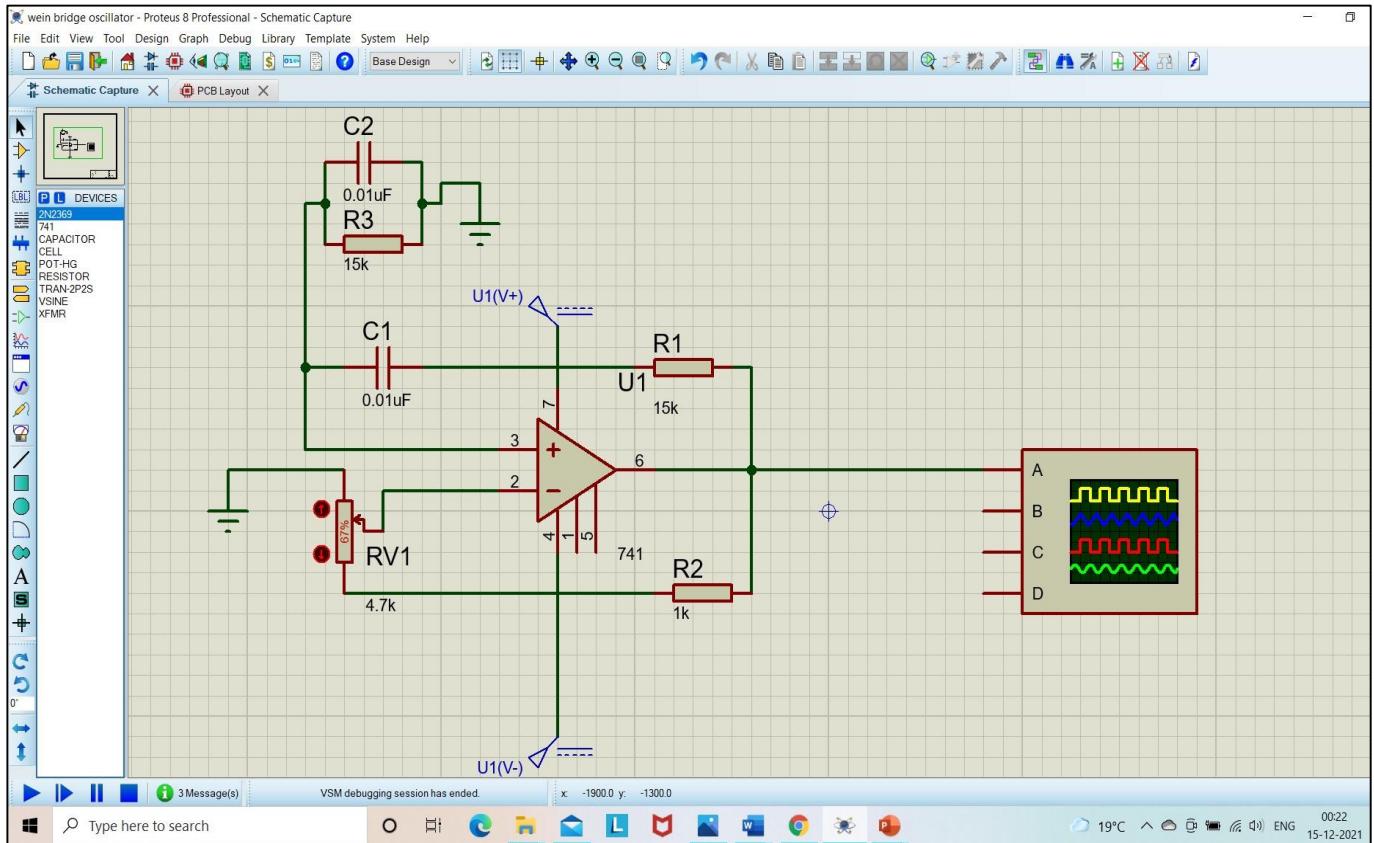
## 1. Phase shift Oscillator:



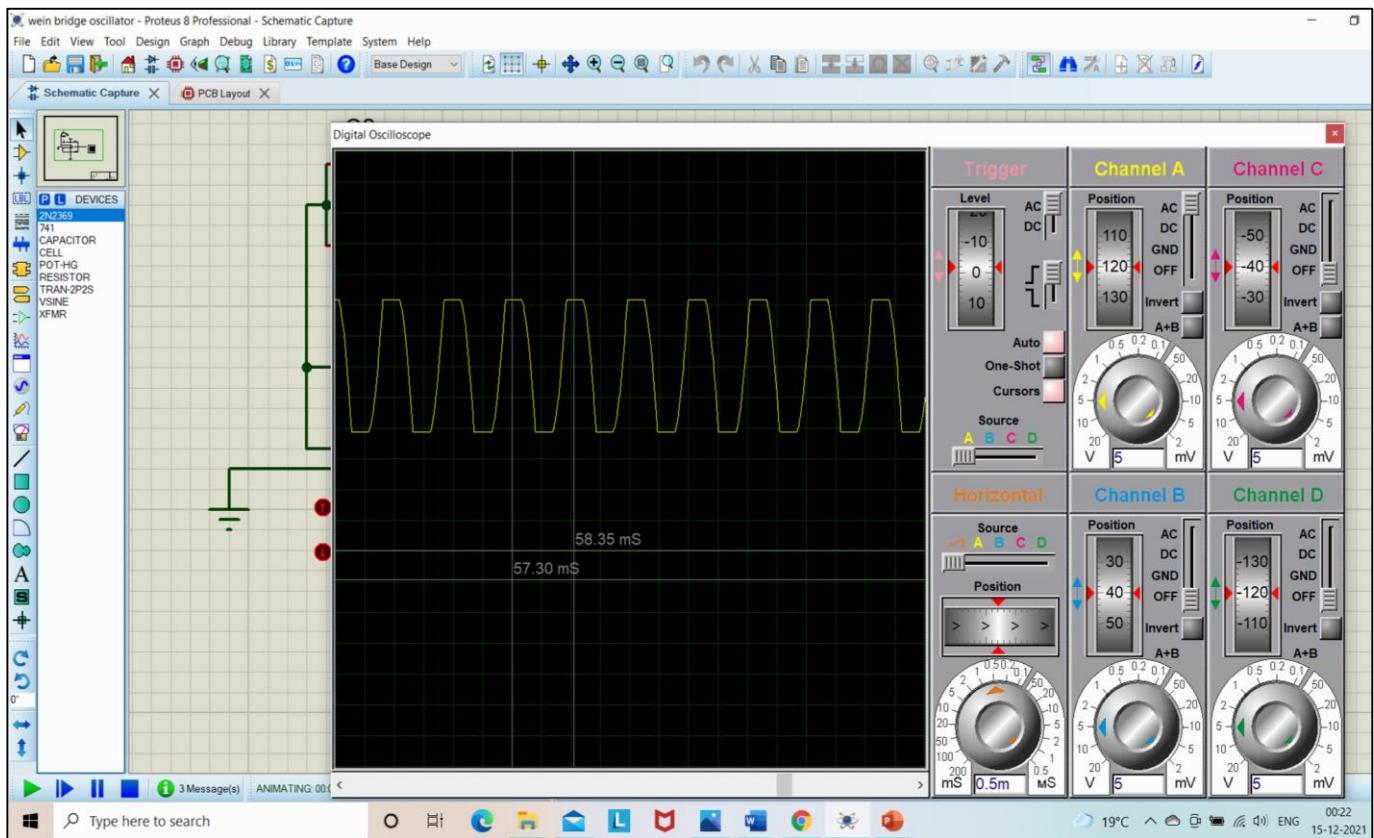
Output:



## 2. Wein bridge oscillator:



Output:



## **Results:**

<b>Oscillator</b>	<b>Calculated frequency</b>	<b>Practical frequency</b>
Wein bridge	1kHz	952.3Hz

## **Conclusion:**

1. The advantages of RC phase shift oscillator are as follows –
  - It does not require transformers or inductors.
  - It can be used to produce very low frequencies.
  - The circuit provides good frequency stability.
2. Wein bridge oscillator can be used to generate Sine waves of frequency of comparatively small range i.e., 20Hz-20kHz.

## Experiment no: 8

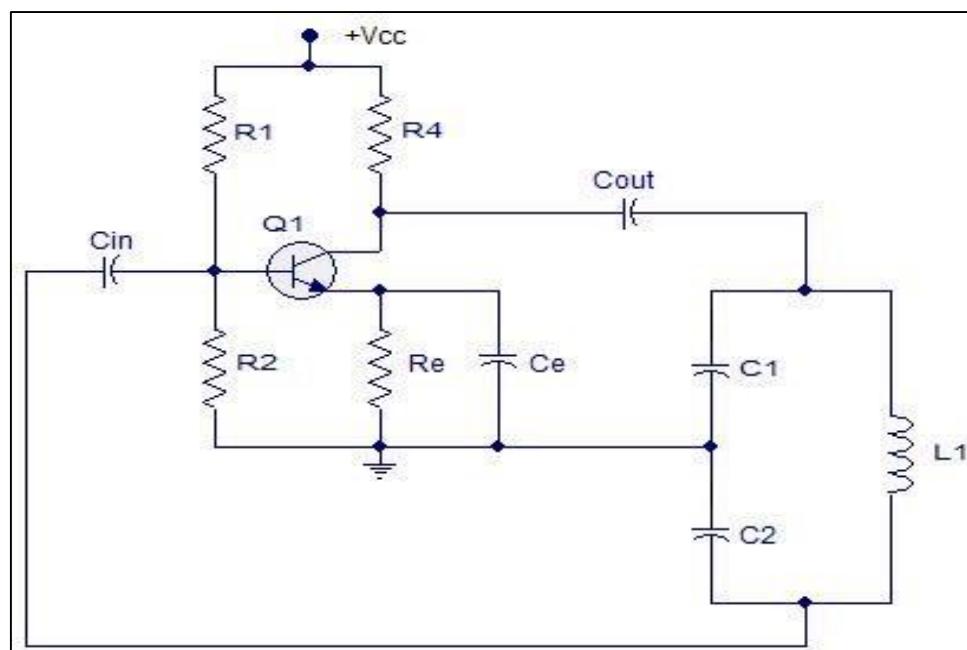
**Aim:** To Design Colpitts and Hartley oscillator.

**Software Requirements:** Proteus.

**Theory:** Colpitts oscillator –

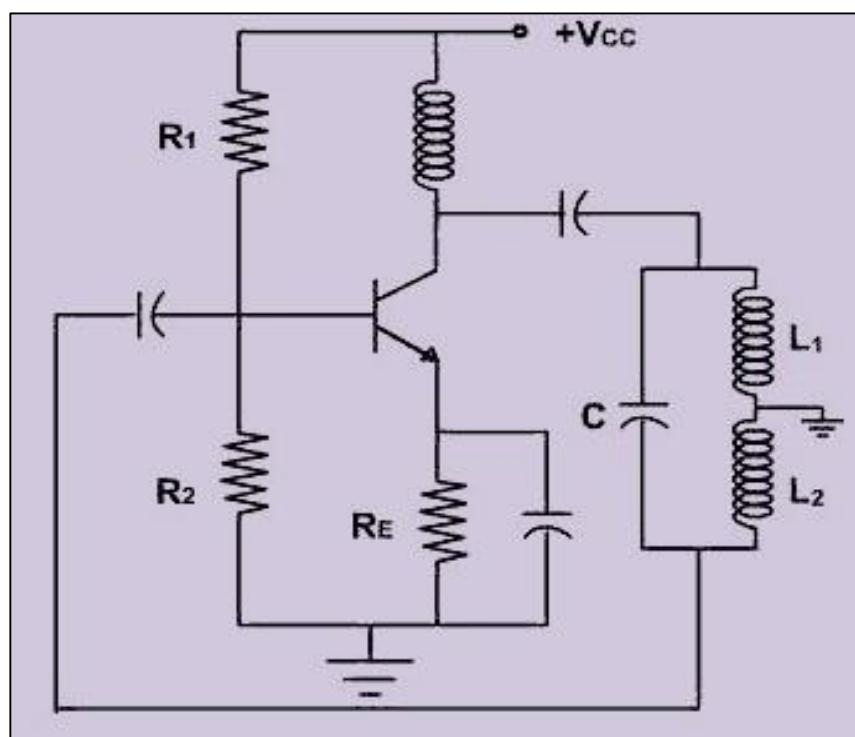
Oscillator is an amplifier with the positive feedback and it converts DC input signal into AC output waveform with certain variable frequency drive and certain shape of output waveform (like sine wave or square wave, etc) by using the positive feedback instead of input signal. It consists of a tank circuit which is an LC resonance sub circuit made of two series capacitors connected in parallel to an inductor and frequency of oscillations can be determined by using the values of these capacitors and inductor of the tank circuit.

This oscillator is almost similar to Hartley oscillator in all aspects; hence, it is termed as electrical dual of Hartley oscillator and is designed for the generation of high frequency sinusoidal oscillations with the radio frequencies typically ranging from 10 kHz to 300MHz. The major difference between these two oscillators is that it uses tapped capacitance, whereas the Hartley oscillator uses tapped inductance.



Hartley oscillator –

The Hartley oscillator is an electronic oscillator circuit in which the oscillation frequency is determined by the tuned circuit consisting of capacitors and inductors, that is, an LC oscillator. The Hartley oscillator was invented by Hartley while he was working in the Research Laboratory of the Western Electric Company. The circuit was invented in 1915 by American engineer Ralph Hartley. The personal feature of the Hartley oscillator is that the tuned circuit consists of a single capacitor in parallel with two inductors are in series or a single tapped inductor, and the feedback signal needed for oscillation is taken from the centre connection of the two inductors.



## Theoretical Calculations:

1. Design a Colpitts Oscillator to produce a sine waveform of 71 KHz. if  $C_1 = C_2 = C = 0.1 \mu F$ .

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\begin{aligned}C_{eq} &= \frac{C_1 C_2}{C_1 + C_2} = \frac{0.1 \times 0.1}{0.1 + 0.1} \\&= \frac{0.01}{0.2}\end{aligned}$$

$$= \frac{1}{20}$$

$$C_{eq} = 0.05 \mu F$$

$$f = \frac{1}{2\pi\sqrt{L \times 0.05 \times 10^{-6}}}$$

$$\begin{aligned}\therefore L &= \frac{1}{(f \times 2\pi \sqrt{0.05 \times 10^{-6}})^2} \\&= \frac{1}{(71 \times 10^3 \times 2\pi \sqrt{0.05 \times 10^{-6}})^2} \\ \therefore L &= 100.49 \mu H.\end{aligned}$$

frequency in Proteus simulation:

$$T = t_1 - t_2 \quad \dots \text{(Time for one cycle)}$$

$$= 180.5 \mu s - 166 \mu s$$

$$T = 14.5 \mu s.$$

$$\therefore f = \frac{1}{T} = \frac{1}{14.5 \mu s} = 68.16 \text{ KHz.}$$

2. find the frequency of Hartley oscillator is values  
of  $L_1$  is  $20\mu H$ ,  $L_2$  is  $2mH$  and  $C$  is  $14\text{pF}$ .

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

$$L_{eq} = L_1 + L_2 = 20\mu H + 2mH = 2.02\text{mH}.$$

$$\therefore f = \frac{1}{2\pi\sqrt{2.02 \times 10^{-3} \times 14 \times 10^{-12}}}$$

$$= \frac{1}{2\pi\sqrt{28.28 \times 10^{-15}}}$$

$$= \frac{1}{2\pi\sqrt{5.817 \times 10^{-8}}}$$

$$= \frac{1}{105.62 \times 10^{-8}}$$

$$\therefore f = 946.7 \text{ KHz.}$$

frequency in Proteus simulation;

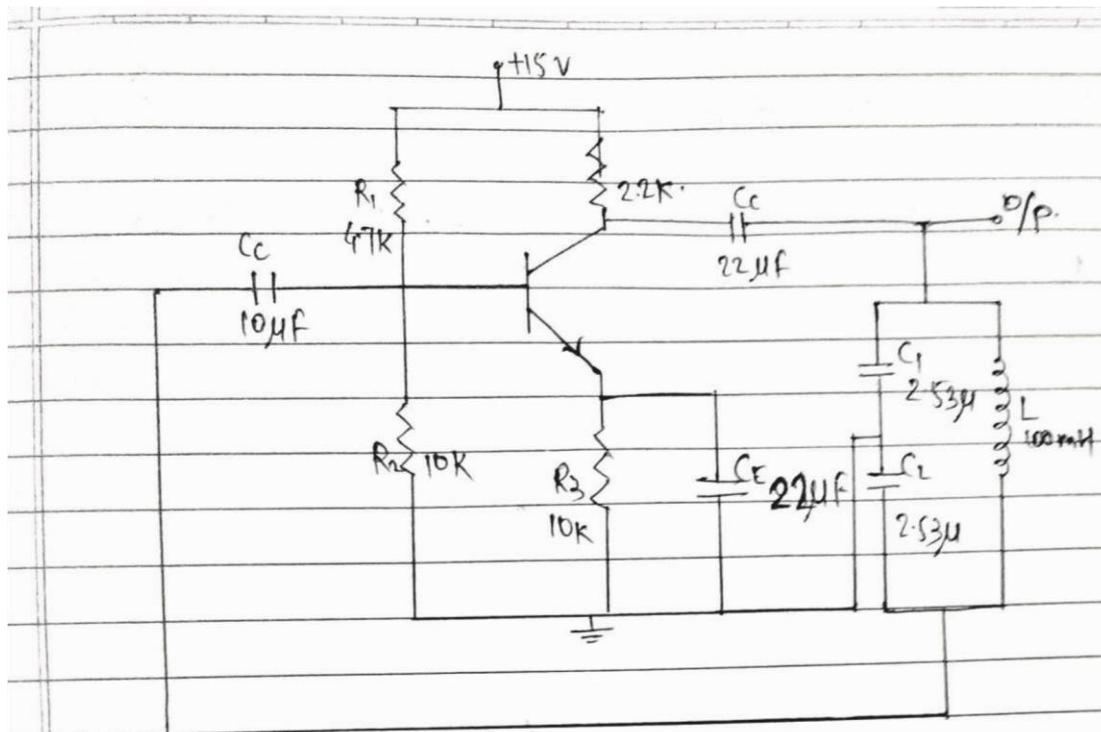
$T = t_1 - t_2 \dots$  (Time for one cycle)

$$= 4.06\mu s - 3\mu s.$$

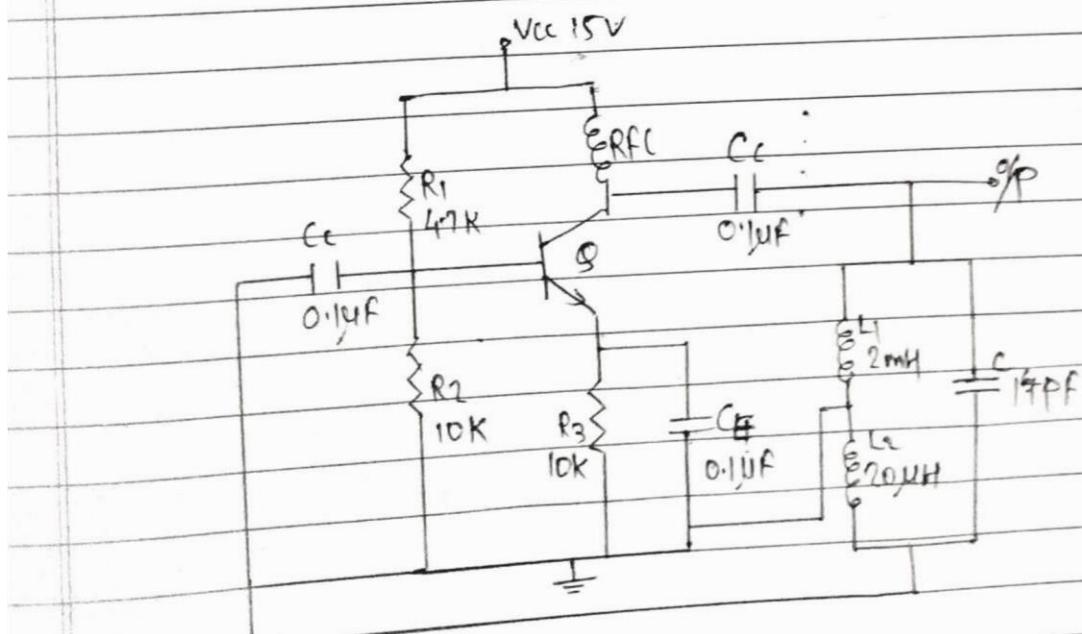
$$T = 1.06\mu s.$$

$$\therefore f = \frac{1}{T} = \frac{1}{1.06 \times 10^{-6}} = 0.943 \times 10^6$$

$$\therefore f = 943.3 \text{ KHz}$$



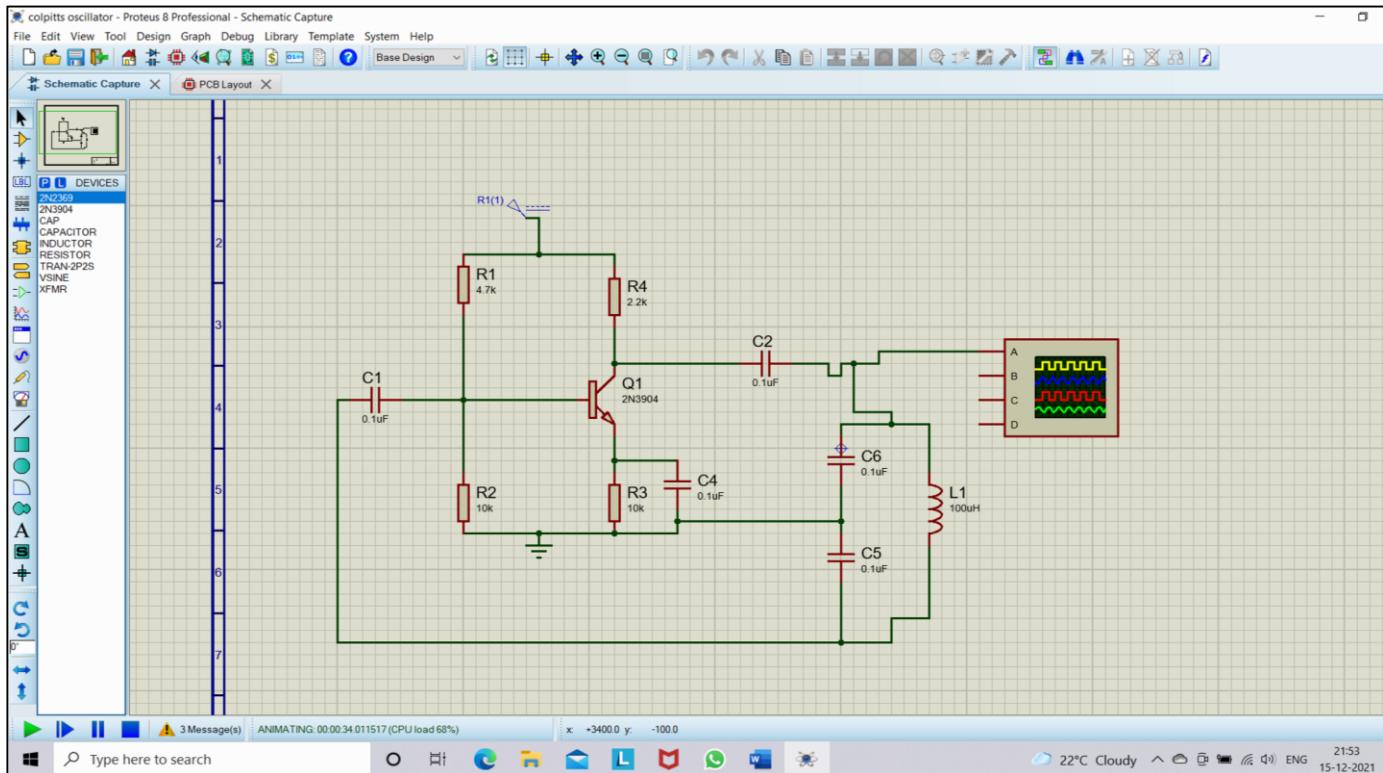
Colpitts Oscillator



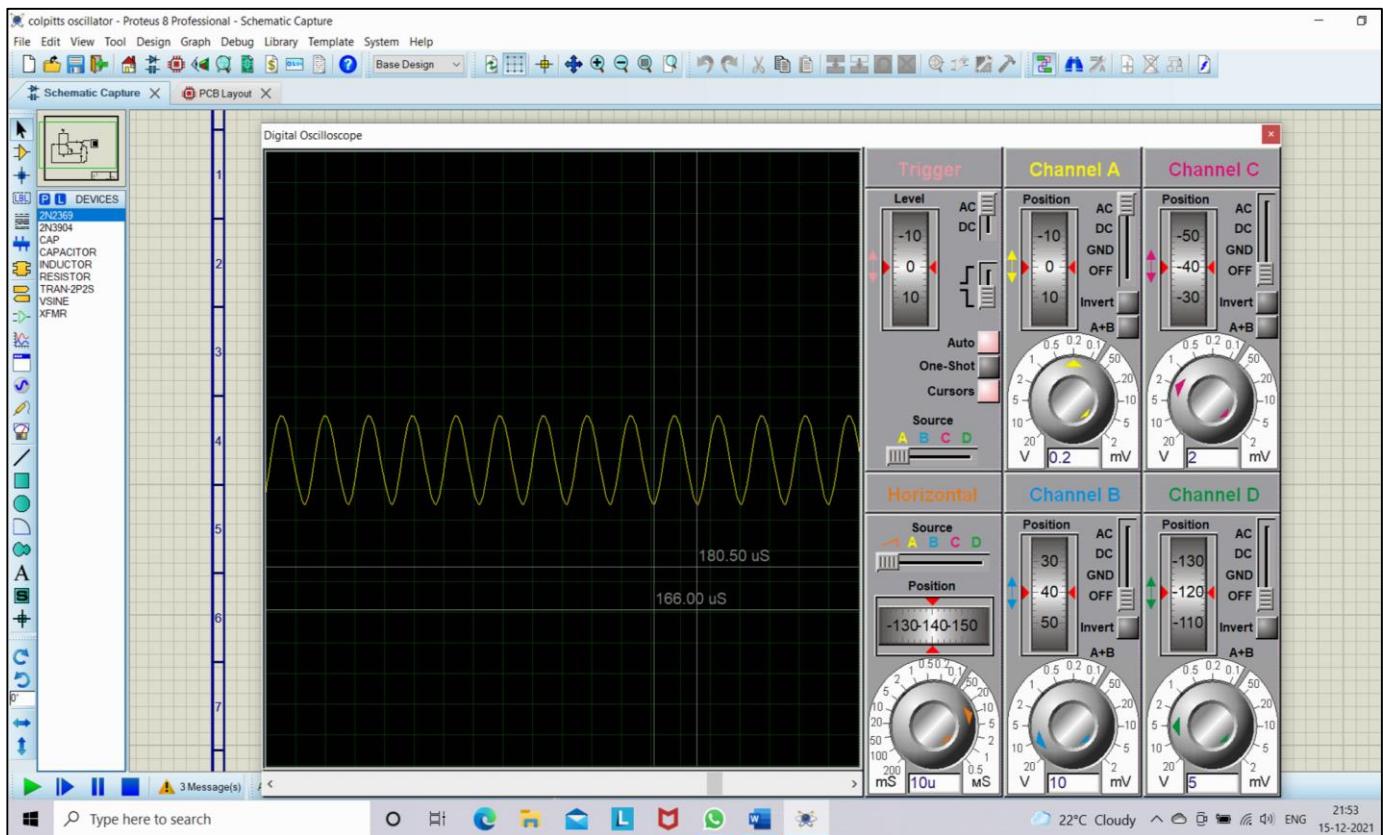
Hartley Oscillator

## Proteus Circuit:

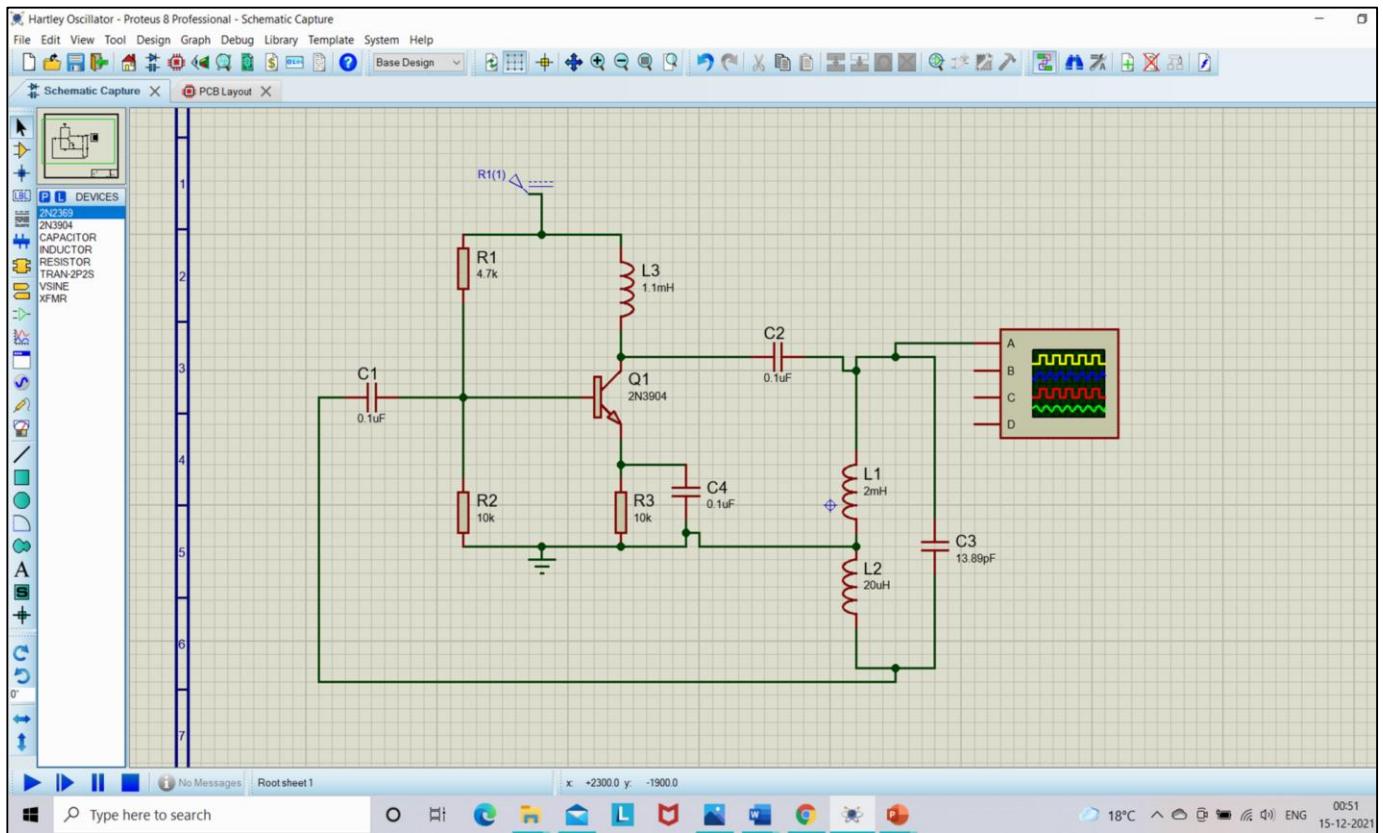
### 1. Colpitts oscillator –



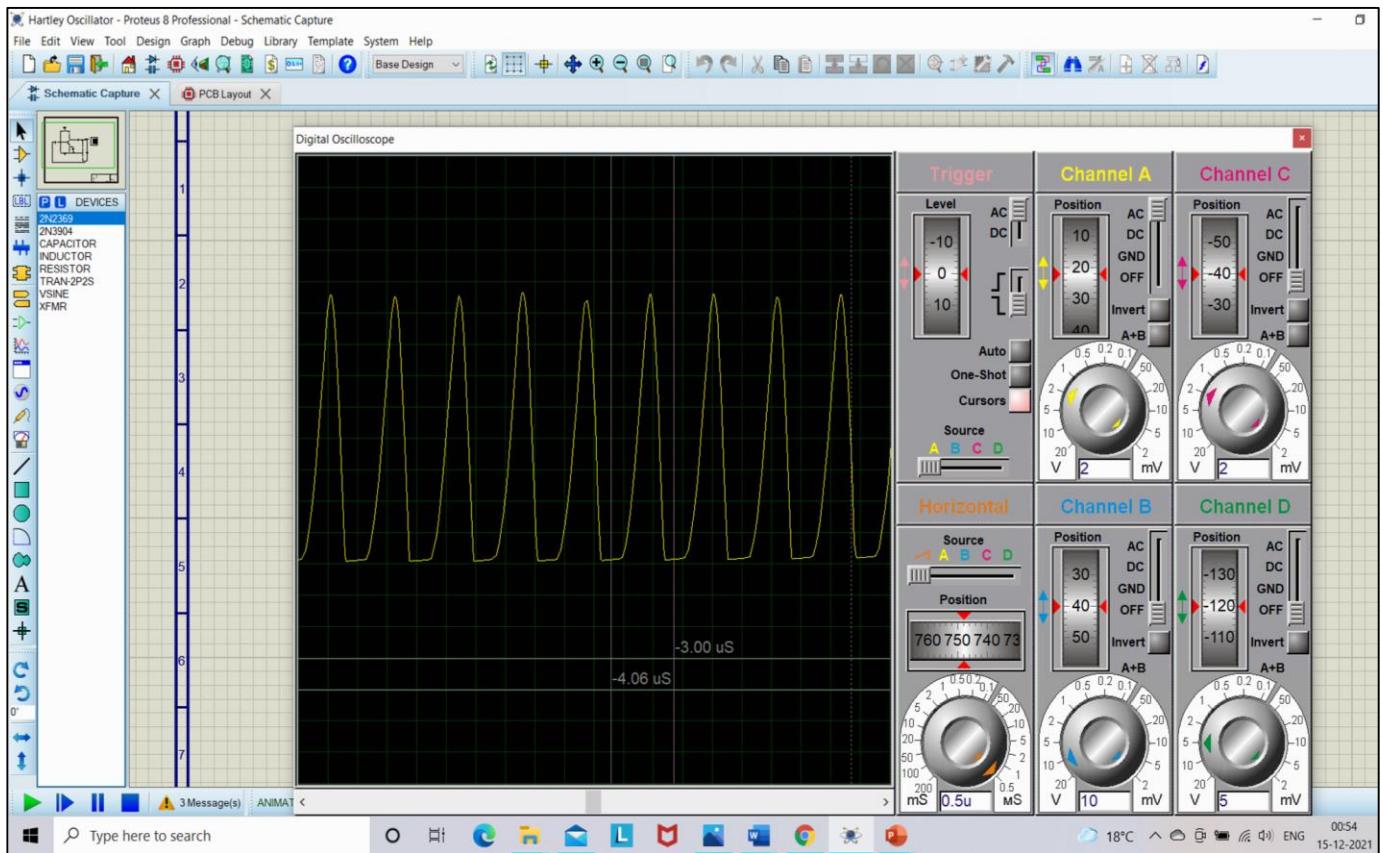
Output:



## 2. Hartley oscillator –



Output:



## **Results:**

<b>Oscillator</b>	<b>Calculated frequency</b>	<b>Practical frequency</b>
Colpitts	71kHz	68.96kHz
Hartley	946.7kHz	943.3kHz

## **Conclusion:**

- The Colpitts oscillator does not appear to be an inherently better topology than the differential pair oscillator.
- For example, some of the current supplied by the transistor to overcome the loss in the resonator flows through  $C_2$  making this topology less efficient than the differential LC oscillator. This should result in a lower figure of merit.
- However, even though the Colpitts does not offer inherently better phase than the current biased oscillator, it is still a useful circuit in application where exceptional phase noise is required dictating a high  $Q$  off-chip single-pin resonator.
- This Hartley Oscillator configuration has a tuned tank circuit with its resonant coil tapped to feed a fraction of the output signal back to the emitter of the transistor.
- Since the output of the transistor's emitter is always “in-phase” with the output at the collector, this feedback signal is positive. The oscillating frequency which is a sine-wave voltage is determined by the resonance frequency of the tank circuit.

## **Experiment no: 9**

**Aim:** To Design Class-AB power Amplifier.

**Software Requirements:** Proteus.

**Theory:** Class AB amplifiers combine Class A and Class B to achieve an amplifier with more efficiency than Class A but with lower distortion than class B. This is achieved by biasing both transistors so they conduct when the signal is close to zero (the point where class B amplifiers introduce non-linearities).

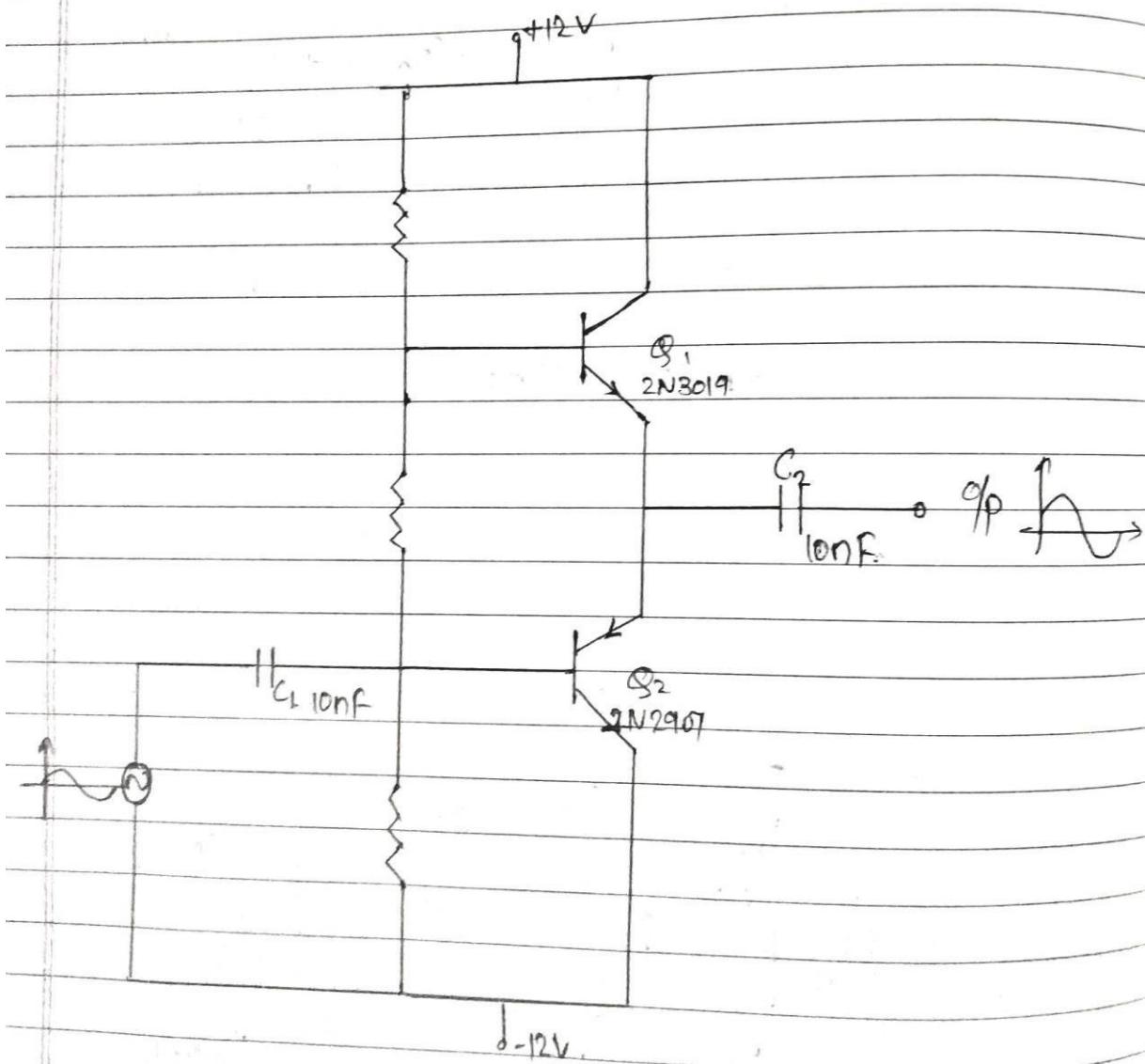
The transistors transition to class B operation for large excursions.

So, for small signals both transistors are active, acting like a class A amplifier. For large signal excursions, only one transistor is active for each half of the waveform, acting like a class B amplifier.

This approach means that the amplifier sacrifices a certain amount of potential efficiency for better linearity - there is a much smoother transition at the crossover point of the output signal. In this way, Class AB amplifiers sacrifice some of the efficiency for lower distortion. Accordingly, class AB is a much better option where a compromise between efficiency and linearity is needed.

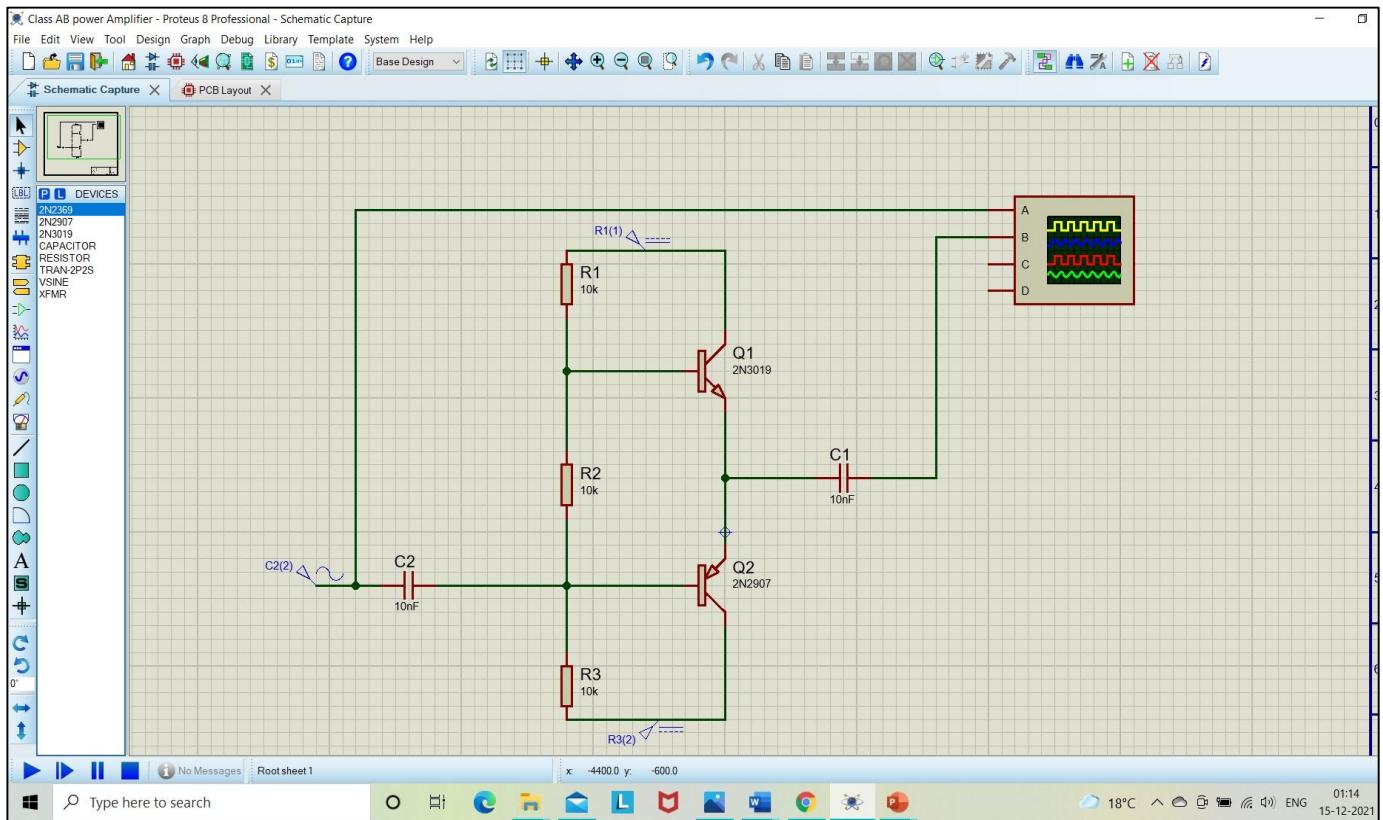
Theoretical calculations:

Design class AB Transistor amplifier with given data.  
 $R_1 = 10\text{ k}\Omega$ ,  $R_2 = 10\text{ k}\Omega$ ,  $R_3 = 10\text{ k}\Omega$ . ~~State~~  $V_{cc} = 12\text{ V}$   $-V_{ic} = -12\text{ V}$

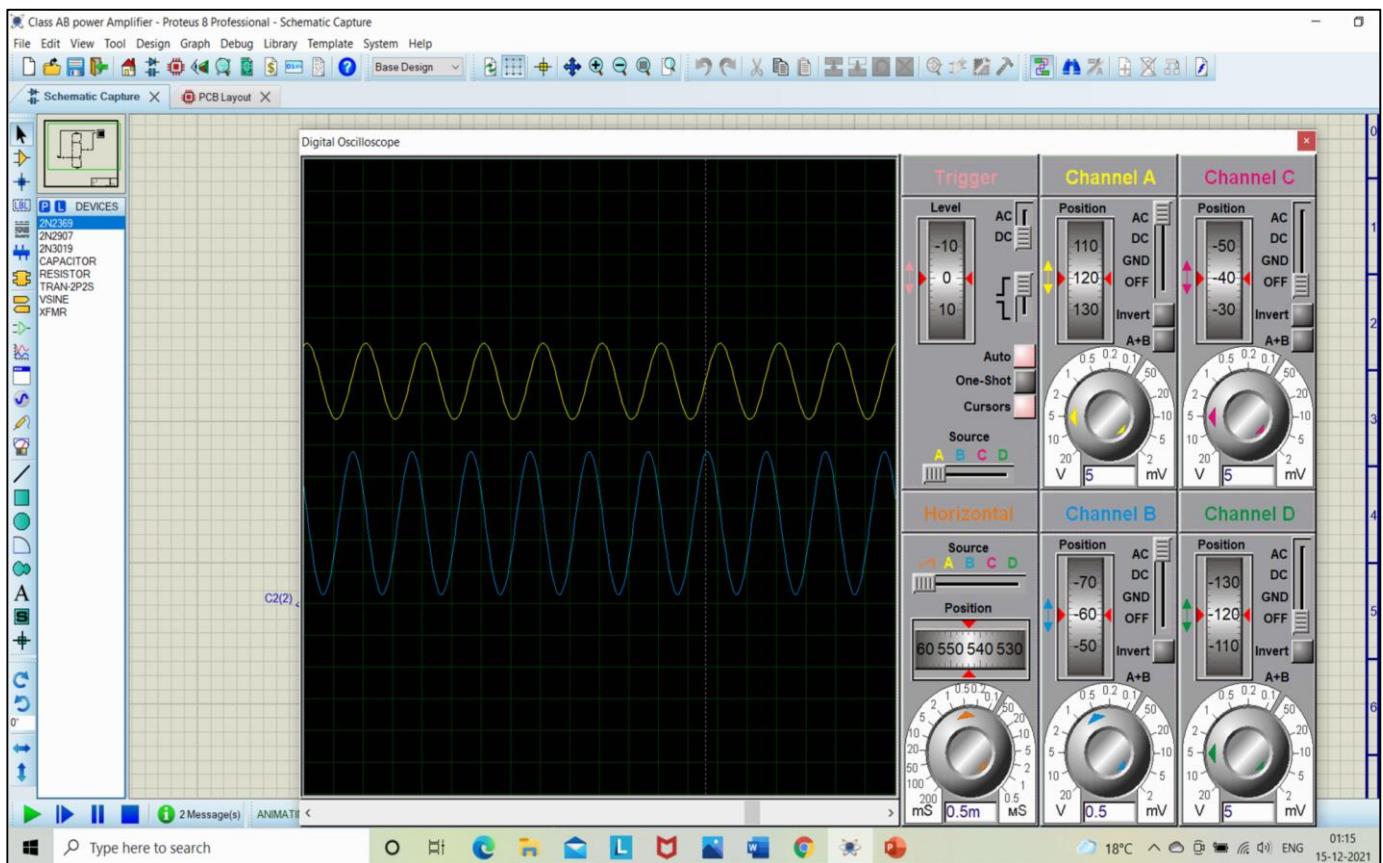


Class-AB-Power Amplifier.

## Proteus Circuit:



## Output:



## **Conclusion:**

- We have seen that class AB amplifiers contrast with class A and class B amplifiers since they do not have a unique operating point but rather an operating zone delimited by the class A quiescent point and the cut-off point (class B operating point).
- The location of the operating point along this zone will dictate both the conduction angle and the efficiency of the amplifier.
- The class AB configuration is nowadays the most common in electronic circuits since it combines the advantages of class A and class B amplifiers without their disadvantages.

## **Experiment no:10**

**Aim:** To Design Simulation of Traffic Lights Control system on Proteus.

**Software Requirements:** Proteus, Keil micro-vision IDE.

**Report of the Project:**

### Abstract

It is a Simulation of Traffic lights control system using 8051- microcontroller. It displays Traffic lights at a Ring Road and how they light in synchronization after particular interval of time. Keil Micro-vision IDE is used to program 8051-microcontroller and upload hex file to the simulation in the proteus software.

### Introduction

A traffic light control system is simulated using Proteus. It is controlled using 8051-microcontroller. The lights glow as per the real life traffics rules in synchronization. Assembly language program is used to control the 8051 actions. Hex file of program is created using Keil Microvision IDE. The File is uploaded to the 8051microcontroller in Proteus.

### Proteus Components:

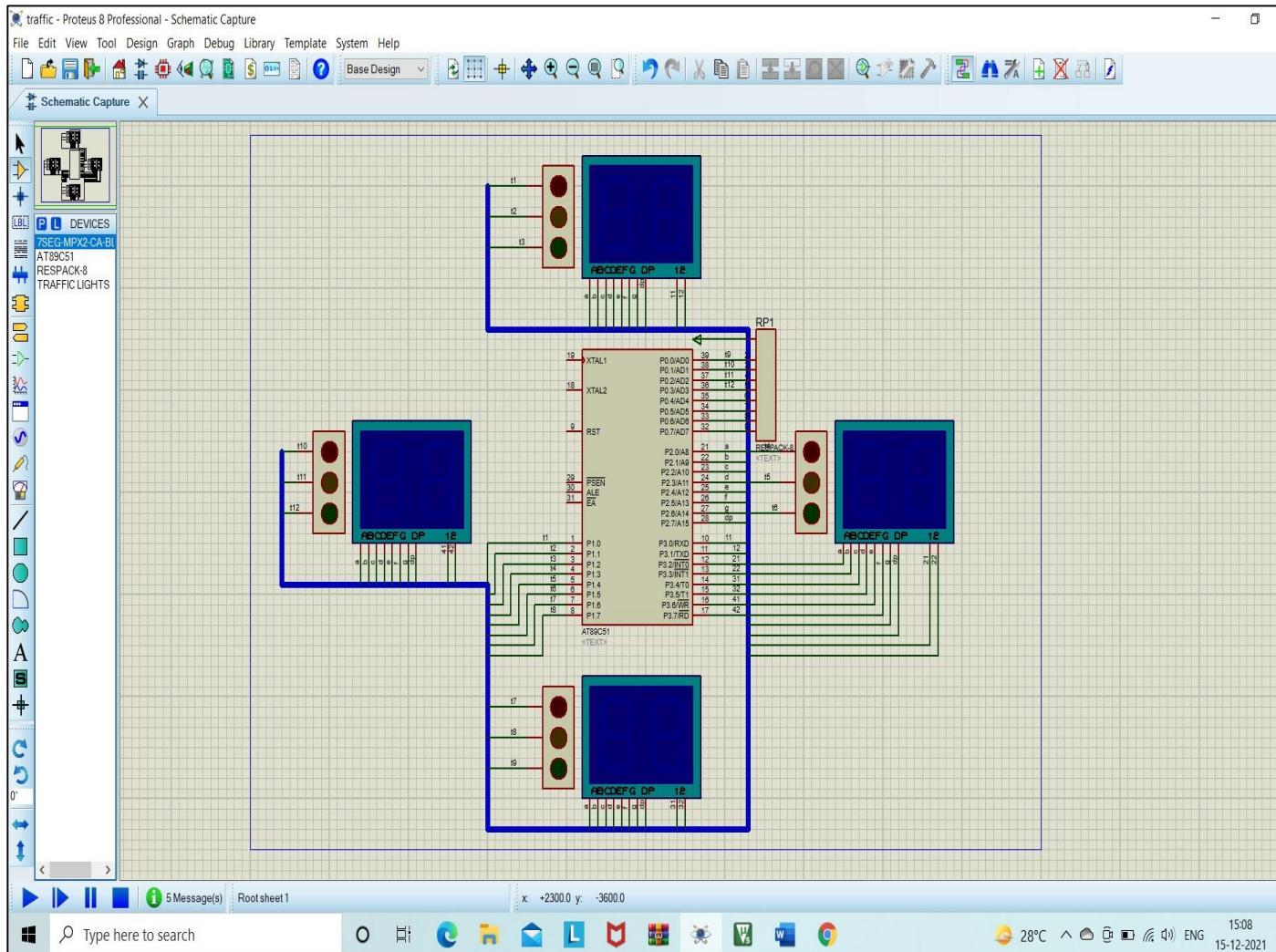
- 1) **7-SEG-MPX2-CA-BLUE:** It is 7-segment control display panel used to display time of particular light i.e., red, yellow or green.
- 2) **AT89C51:** It is 8051-microcontroller used to control whole process of system.
- 3) **RESPACK-8:** Respack is a device just similar to resistance box used for the variation of the resistances as per use of the circuit but there is subtle difference in the respack that is the resistance present in it are of same value and here the respack used RESPACK-8 which consists of 8 resistances of equal value i.e., 1 K ohm.
- 4) **Traffic lights:** They lights similar to Traffic lights having lights RED, YELLOW, GREEN.

### Working of Simulation:

Once runed the simulation in Proteus software, it automatically starts glowing lights and shows timing on 7-seg display.

Firstly, GREEN light glows in one road light and YELLOW in its adjacent road lights and other two are RED. It glows for 10 sec and then turns RED as programed, at that time adjacent yellow is turned green and next one is turned yellow so, that two of four are still red and one GREEN and one YELLOW. This process runs continuously. Thus, it is exact simulation of Traffic light control system in real life.

## Proteus Circuit:



## 8051 Assembly Program:

ORG 00H	MOV 41H,A	SETB P3.2	
LJMP MAIN	MOV 42H,B	CLR P3.3	
ORG 300H A1:	SETB P3.0	MOV A,44H	
TBL: 0C0H,0F9H,0A4H,0B  0 H,99H,92H,82H,0F 8  H,80H,90H  ;7seg data for comm. anode type	DB CLR P3.1 A,@A+DPTR MOV A,41H  MOVC  P2,A MOV  ACALL DELAY	MOVC  MOV P2,A  ACALL DELAY	
MOV		P3,#00H	
ORG 30H	ACALL DELAY	SETB P3.3	
MAIN:	MOV MOV	P3,#00H	CLR P3.2
P2,#00H SETB	P3.1 MOV A,45H		
MOV P3,#00H	CLR P3.0 MOVC		
ACALL FRONT	MOV A,42H	A,@A+DPTR	
MOV MOVC	MOV P2,A		
DPTR,#TBL	A,@A+DPTR	ACALL DELAY	
CLR A MOV	P2,A MOV	P3,#00H	
MOV 40H,#10	ACALL DELAY	MOV A,46H	
MOV 43H,#10	MOV P3,#00H	MOV B,#10	
MOV 46H,#20	SJMP X3 DIV AB		
MOV 49H,#20 X2:	SJMP X1 MOV	47H,A	
MOV R0,#35 X3:	MOV A,43H MOV	48H,B	
MOV R6,#30	MOV B,#10 SETB	P3.4	
MOV R7,#40	DIV AB CLR P3.5		
X1: MOV A,40H	MOV 44H,A MOV	A,47H	
MOV B,#10	MOV 45H,B	MOVC	
DIV AB	A,@A+DPTR		

MOV P2,A	CLR P3.6 X4: DJNZ R7,L1
ACALL DELAY	MOV A,51H LJMP MAIN
MOV P3,#00H	MOVC L1: LJMP X1 A,@A+DPTR
SETB P3.5	DELAY: MOV R4,#5 MOV P2,A
CLR P3.4 H2:	MOV
MOV A,48H	ACALL DELAY R5,#0FFH
MOVC A,@A+DPTR	MOV P3,#00H H1: DJNZ R5,H1
MOV P2,A	DJNZ R0,X2 DJNZ R4,H2
ACALL DELAY P1,#54H	MOV R0,#35 RET
MOV P3,#00H	DJNZ 40H,Q1 FRONT: MOV
MOV P0,#02H	MOV 40H,#20
MOV A,49H Q1: RET	DJNZ 43H,Q2
MOV B,#10	MOV 43H,#10
RIGHT: MOV DIV AB	ACALL RIGHT

P1,#0A1H

MOV 50H,A Q2: DJNZ 46H,Q3

MOV P0,#02H

MOV 51H,B MOV 43H,#20

RET

SETB P3.6 MOV 46H,#10

BACK: MOV

CLR P3.7 Q3: DJNZ 49H,Q4 P1,#09H

MOV A,50H MOV 49H,#10 MOV P0,#05H

MOVC ACALL BACK RET

A,@A+DPTR

Q4: DJNZ R6,X4 LEFT: MOV

MOV P2,A P1,#4AH ACALL LEFT

ACALL DELAY MOV P0,#08H

MOV 40H,#10

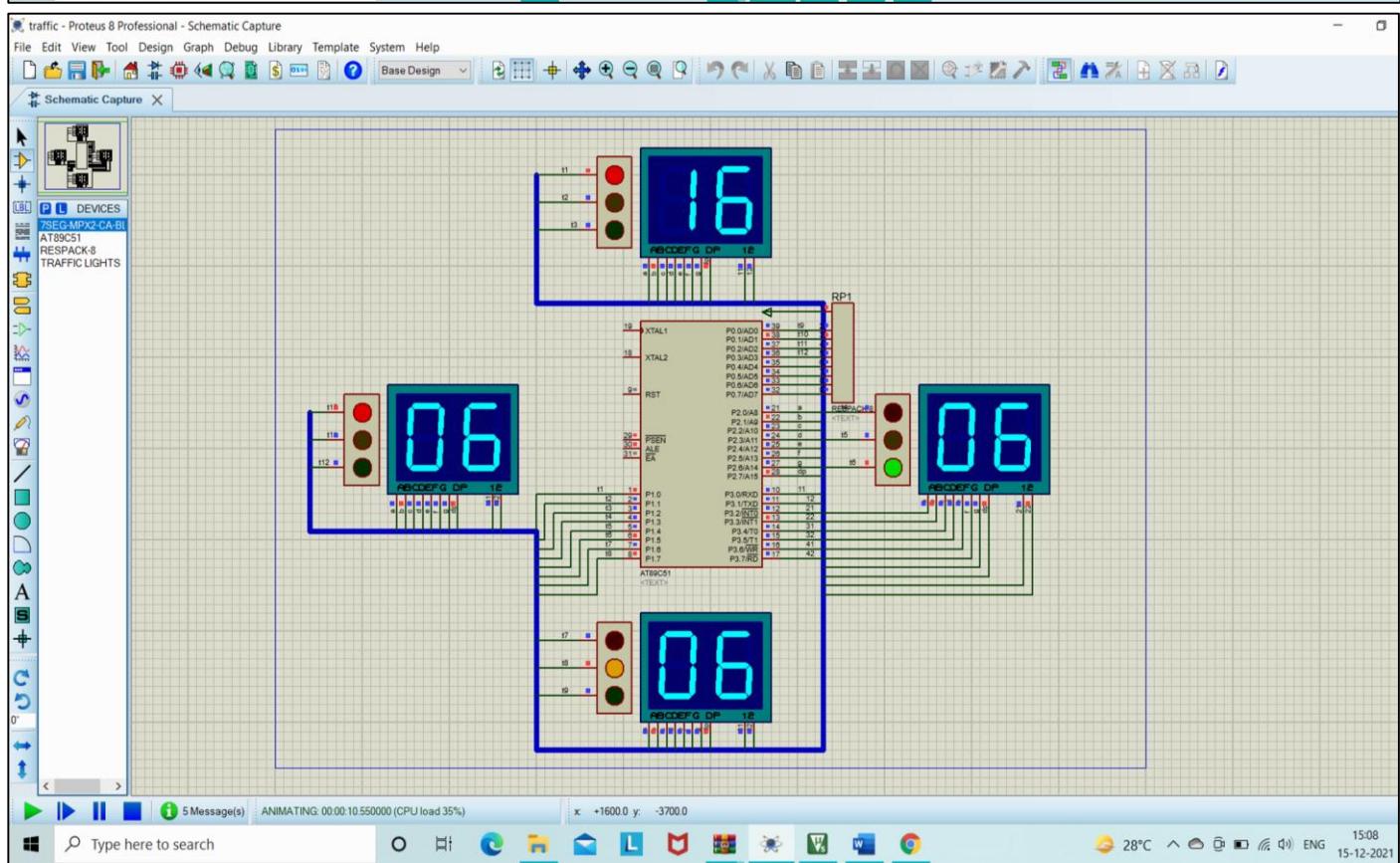
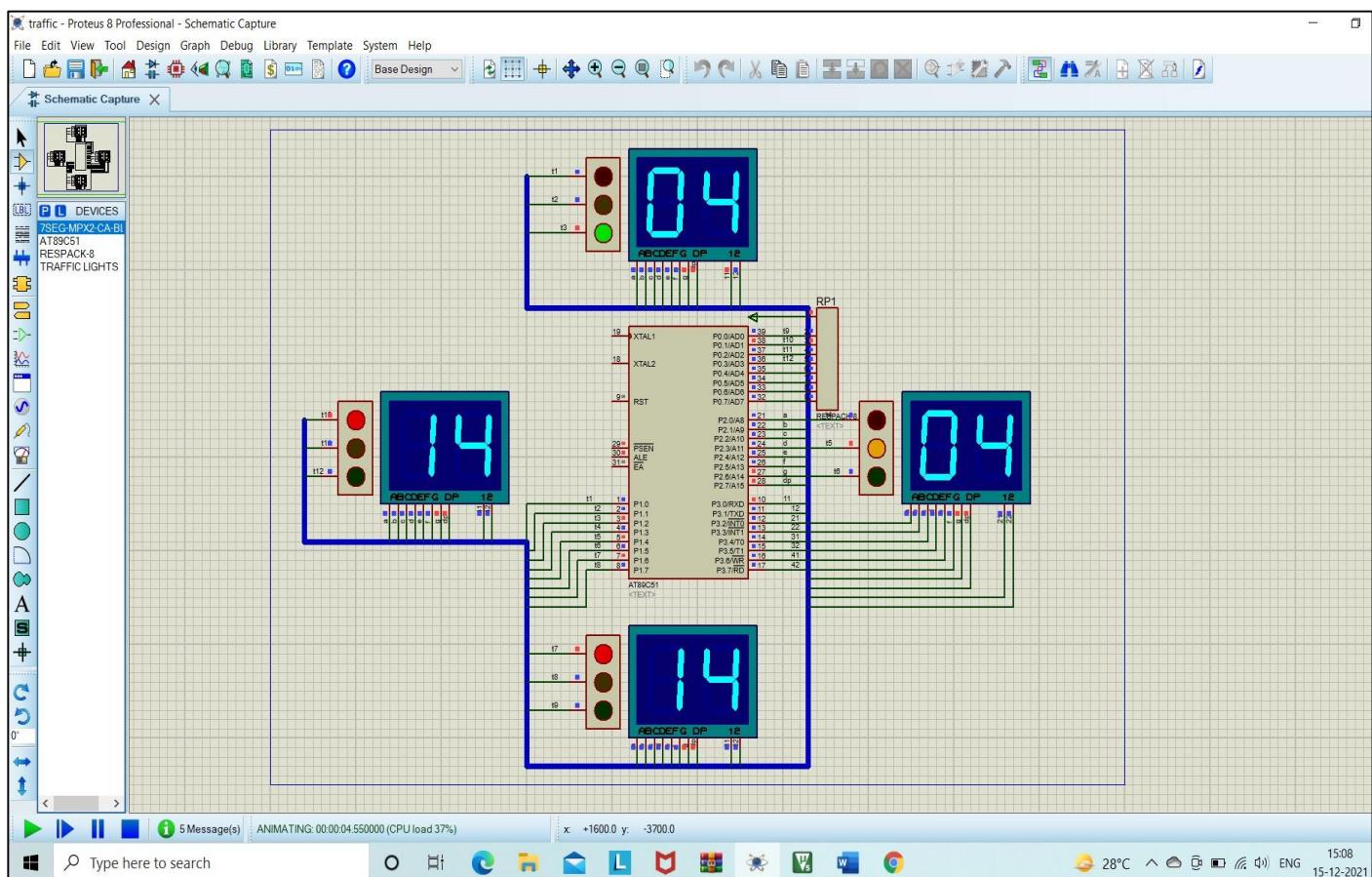
MOV P3,#00H RET

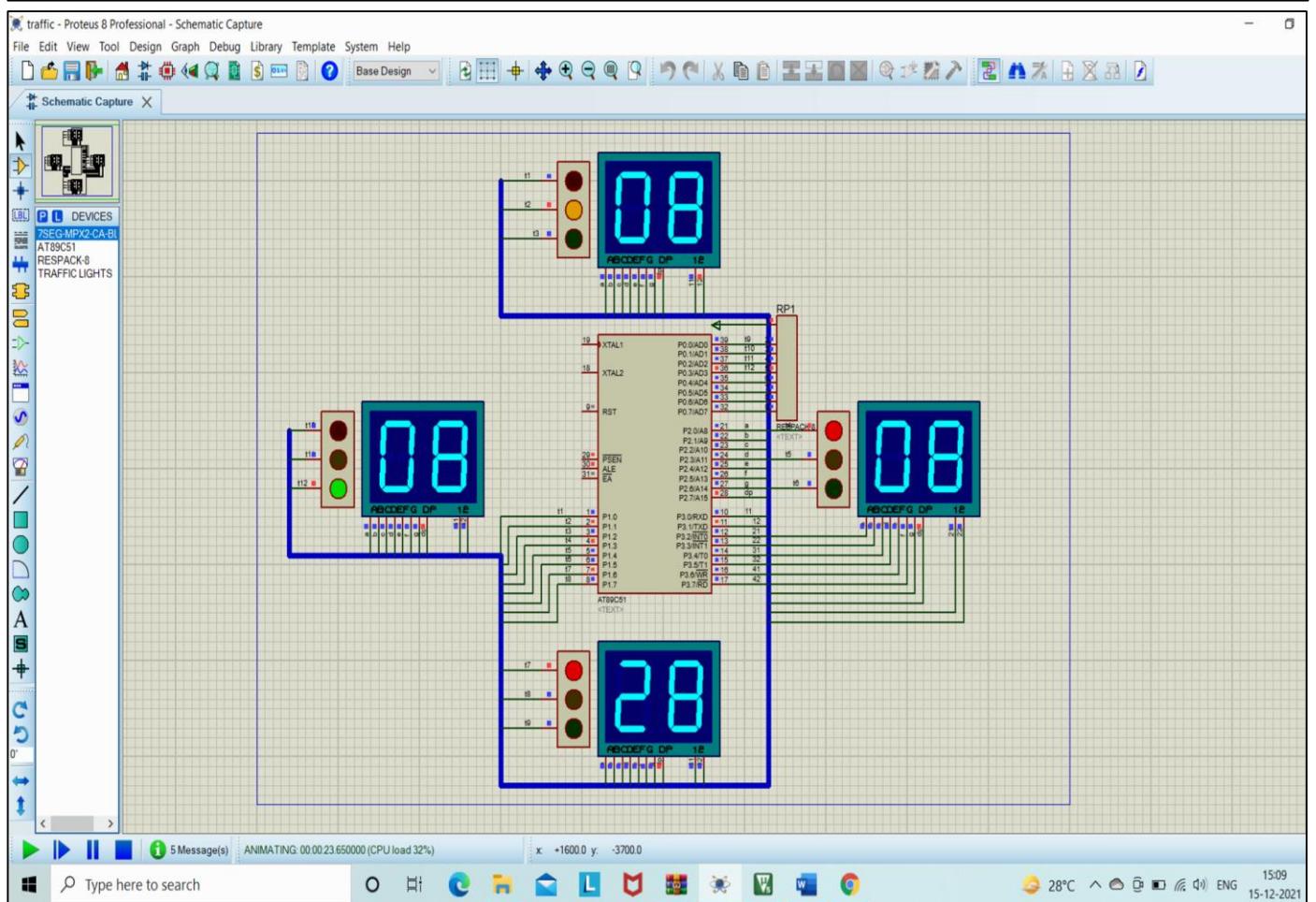
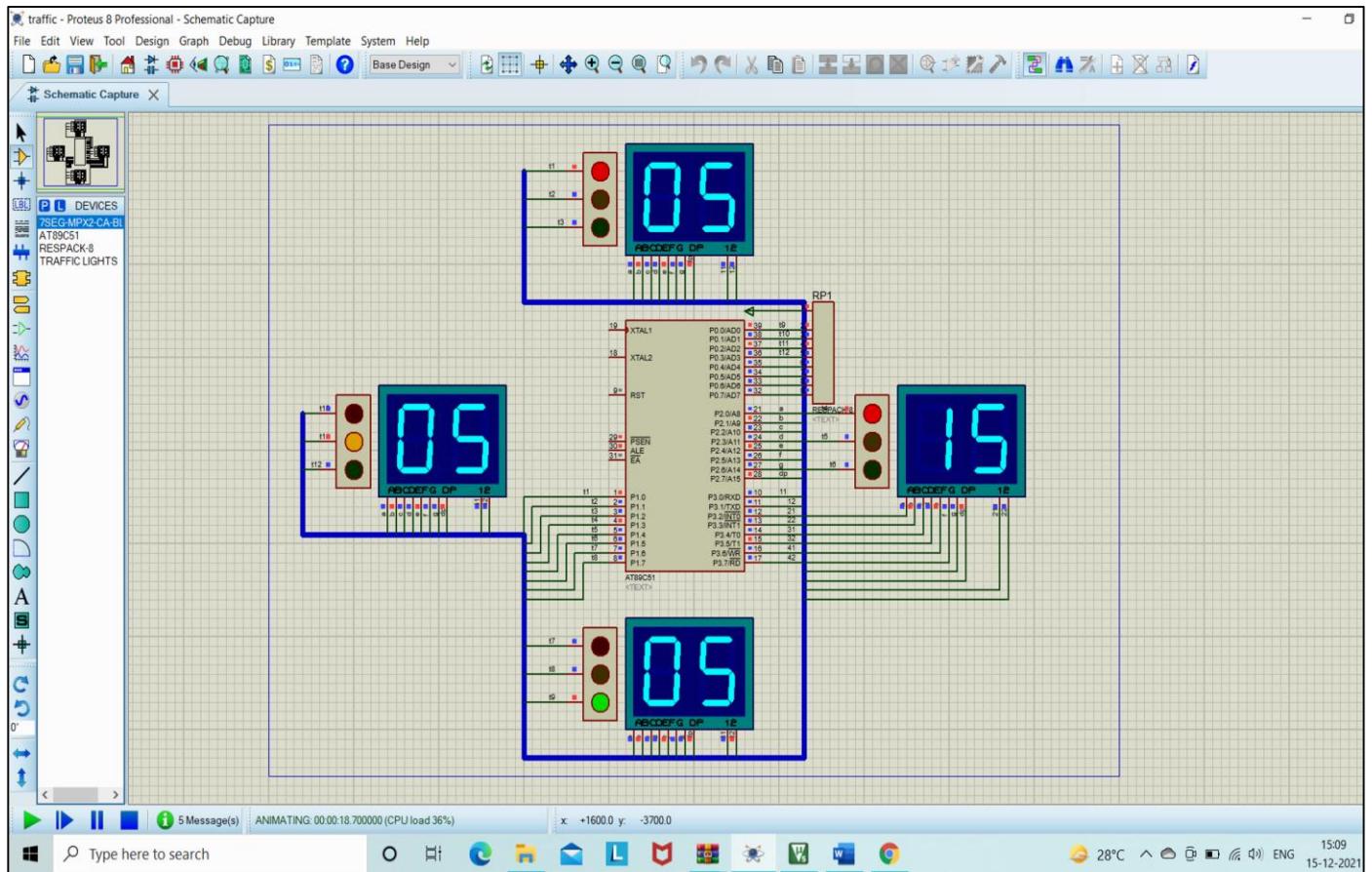
MOV 43H,#10

SETB P3.7

MOV 46H,#30

## Output:





## Conclusion:

Traffic light control system simulated successfully on Proteus software and runs with proper synchronization. It also shows time and signal properly at all the roads.