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Indian Institute of Information Technology, Lucknow

Mid Semester Examination February 2025

B.Tech 2nd Semester CS/IT/CSAI/CSB

Subject: Computer Organization & Architecture (COA2400C) Date: 24/02/2025

Duration: 2Hrs Total Marks: 40 (10 Quiz+30 Subjective Ques)

Instruction: The paper contains two sections.

Section I – Quiz Questions

(10 Questions, 1 Marks Each, All Questions are Compulsory)

1) What is the 2's complement of the binary number **1101**?
   a) 0011
   b) 0100
   c) 1111
   d) 1011
2) How many flip-flops are required to construct a **4-bit shift register**?
   a) 2
   b) 4
   c) 8
   d) 16
3) The Boolean expression for a **2-to-1 multiplexer** is:
   a) $\overline{S}A+SB$
   b) $\overline{S}\overline{A}+SB$
   c) S+A
   d) None of the above
4) **4 x 2 encoder** has:
   a) 4 Input and 2 Output lines
   b) 2 Input and 4 Output lines
   c) 4 Input, 2 Output and 2 Select lines
   d) 2 Input, 4 Output and 1 Select lines
5) A particular number is written as 132 in radix-4 representation. The same number in radix-5 representation is _____.
6) For the expression $\mathbf{Y=\overline{A}+B}$, how many minimum numbers of NAND gate is required?
   a) 2
   b) 3
   c) 4
   d) 5
7) How many **2:1 MUX** is required to implement EX-OR Gate?
   a) 2
   b) 1
   c) 3
   d) None
8) Consider the following Boolean function of four variables
   $\mathbf{F(w,x,y,z)=\Sigma\, m\,(1,3,4,6,9,11,12,14)}$. The function is:
   a) independent of 1 variable
   b) independent of 2 variables
   c) independent of 3 variables
   d) dependent on all variables
9) If **52/4=12**, then determine the base _____

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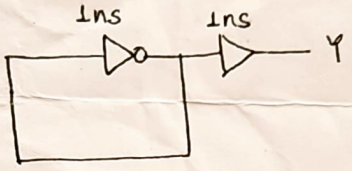
10) What is the characteristic equation of SR flip flop _____

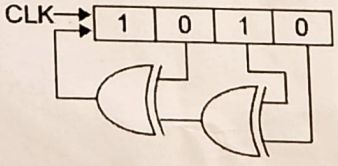
Section II – Subjective Questions

(There are 5 questions in total. Marks are indicated against each question. Questions 1 to 4 are compulsory. Attempt any one question from Question 5.)

1) In the astable multivibrator shown in the figure, propagation delay of inverter and the buffer is 1ns. What will be the fundamental time period of the circuit? (5)



2) Explain the J-K Flip-Flop, its drawback, and how the drawback can be overcome. (5)
3) Differentiate between combinational and sequential circuits. Realize the given function F (A, B, C) = Σ m (1, 3, 5, 6) using 2:1 MUX. (5)
4) Design 5 bit Parallel-in-parallel-out (PIPO) register. How many clock pulse will be required to store and get the output? (5)
5) The shift register shown in below figure, is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (i.e. MSB). After how many clock pulses will the content of the shift register become 1010 again? (10)



OR

Given: F (c, d, a, b) = Σ m (0, 1, 2, 8, 9) + Σ d (4, 10, 12). What is the minimum SOP form of given F? Design 3x8 decoder by using 2x4 decoder. (10)

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