Name: Vedant Golait Class: BE EnTC A Roll No.: 16

ALU

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 28.07.2025 09:12:37
-- Design Name:
-- Module Name: ALU - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;
use IEEE.std_logic_unsigned.all;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity ALU is
   Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
          b : in STD_LOGIC_VECTOR (3 downto 0);
          s : in STD_LOGIC_VECTOR (2 downto 0);
          y : out STD_LOGIC_VECTOR (3 downto 0));
end ALU;

architecture Behavioral of ALU is

begin
with s select
y <= a + b when "000",
a - b when "001",
a + 1 when "010",
b + 1 when "011",
```

```
a and b when "100",
a or b when "101",
a nand b when "110",
a nor b when "111",
a xor b when others;

end Behavioral;
```

ALU test bench file:

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 28.07.2025 09:12:37
-- Design Name:
-- Module Name: ALU - Behavioral
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-- Target Devices:
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--
-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
```

```
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----------------------------------------------------------------------------------



library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
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-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity ALU is
   Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
          b : in STD_LOGIC_VECTOR (3 downto 0);
          s : in STD_LOGIC_VECTOR (2 downto 0);
          y : out STD_LOGIC_VECTOR (3 downto 0));
end ALU;

architecture Behavioral of ALU is

begin
```
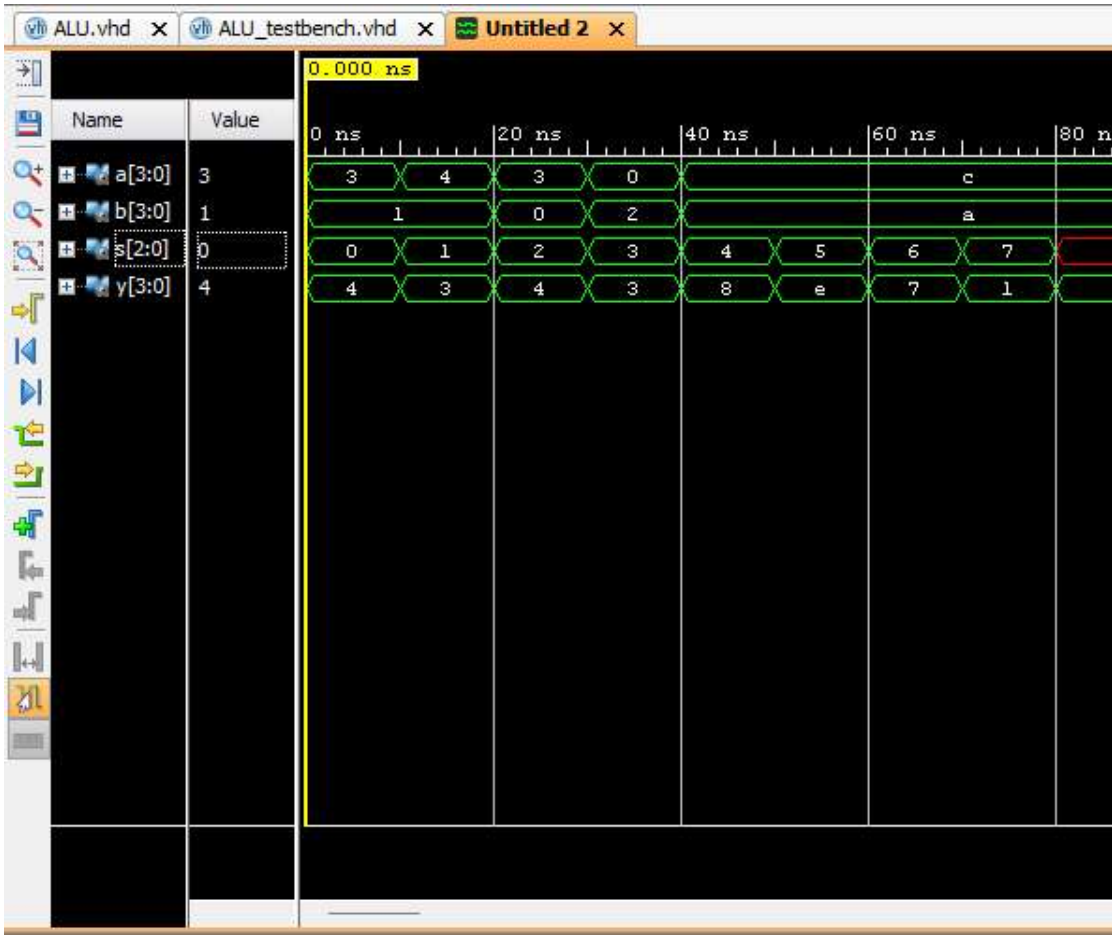

```
with s select
y <= a + b when "000",
a - b when "001",
a + 1 when "010",
b + 1 when "011",
a and b when "100",
a or b when "101",
a nand b when "110",
a nor b when "111",
a xor b when others;

end Behavioral;
```


ALU.vhd
ALU_testbench.vhd
Untitled 2
Name
Value
a[3:0]
3
b[3:0]
1
s[2:0]
0
y[3:0]
4
0.000 ns
0 ns
20 ns
40 ns
60 ns
80 n
3 4 3 0 c
1 0 2 a
0 1 2 3 4 5 6 7
4 3 4 3 8 e 7 1