Vedant Nipane

+91 9881420728 vedant.nipane@students.iiit.ac.in github.com/VedantNipane
linkedin.com/in/vedant-nipane-9759991b1/

Education

International Institute of Information Technology **2021-2025**
B.Tech. (Honours) in ECE

Experience

Head Digital Works **June 2025 – Sept 2025**
Associate Data Scientist *Hyderabad*

- Conducted comprehensive product analytics on gaming platform's redemption workflows using SQL and Python, analyzing 5.6+ lakh game instances and 23+ crore wagered amounts to identify user behavior patterns and optimize withdrawal/redeem processes
- Designed and evaluated "Discounted Game Join" feature strategy through cohort analysis on 96K+ distinct players, projecting 38K net profit by analyzing user segmentation patterns and GST optimization opportunities on winnings bucket transactions
- Developed automated fraud detection reporting system for Leave Table Alerts using Python, SQL, and MicroStrategy, streamlining anti-fraud operations and reducing manual monitoring overhead for compliance team

Remote Labs, SPCRC, IIIT Hyderabad **May 2023 – May 2025**
IoT Researcher *Hyderabad*

- Led development of "Remote Titration" project for remote access and control through a web dashboard using Raspberry Pi, Python, and Blynk.
- **Secured 1st place at Hyderabad 5G-6G Hackathon and 3rd place nationally at India Mobile Congress 2024.**

Projects

Delay and Leakage Characteristics: ML Approach | *Python,NGSpice* **March - April 2024**

- Generated datasets from simulations to train regression-based machine learning models, focusing on Process, Voltage, and Temperature (PVT) combinations.
- Conducted data analysis using 3D surface plots, dual axis plots, correlation plots, PCA, and GMM.
- Developed an ensemble-based model to predict leakage power and propagation delay, achieving an R2 score of 0.93.

Pipelined Y86-64 Processor Architecture | *Verilog, Digital Logic Design* **March 2023**

- Developed a pipelined Y86-64 processor architecture with data forwarding and control logic, capable of executing the full Y86-64 instruction set (ISA).
- Designed pipeline stages with modules for Fetch, Decode, Execute, and Memory, utilizing pipeline registers to increase throughput over a sequential model.
- Implemented hazard detection and stall mechanisms to handle control and data hazards, ensuring correct program execution flow.

Mobile Air Pollution Module | *C++, Blynk, Arduino IDE, ESP-32* **March 2023**

- Engineered portable IoT device integrating 5+ sensors for real-time environmental monitoring with GPS tracking
- Designed self-sustaining power system with dual power sources achieving 24+ hours of continuous operation

Custom Shell Implementation | *C, UNIX Commands* **January 2024**

- Implemented a UNIX-like shell supporting core commands (cd, echo, pwd) with persistent command history.
- Developed modular architecture with separate components for command parsing and directory operations.

Publications

V. Nipane et al., "Low-Cost Retrofitted IoT Based Titration Setup for Remote Labs," FiCloud Conference 2024, May 2024.

Technical Skills

Languages: Python, C, C++, Matlab, Verilog, NGSpice
Tools/Platforms: VS Code, Windows, Linux, Jupyter Notebook

Leadership & Achievements

- Led corporate sponsorship efforts as Corporate Team Head at E-Cell and Corporate Relations Executive for Felicity
- Secured 1st place at Hyderabad 5G-6G Hackathon and 3rd place nationally at India Mobile Congress 2024.
- Recipient of Research Award 2024 at IIIT Hyderabad.