

Op-Amp Design using Discrete Components

Electronic Workshop II

Vedant Pahariya
2023112012

Manikya Pant
2023112024

Table 40
May 5, 2025

Contents

1	Introduction	3
2	Op-Amp Theory	3
i	About Op-Amps	3
ii	Standard Op-Amp Topologies	4
3	Differential Amplifier Stage	6
4	Gain Stage	9
i	Architecture and Function	9
ii	Voltage Gain Analysis	10
iii	Frequency Compensation and Stability	10
a.	The Stability Problem	10
b.	Miller Compensation Technique	11
c.	Mathematical Analysis of Miller Effect	11
d.	Design Considerations for Compensation	11
5	Output Stage	12
i	Requirements and Design Considerations	12
ii	Class AB Push-Pull Architecture	12
a.	Advantages Over Alternative Configurations	13
iii	Crossover Distortion and Biasing Solution	13
iv	Diode Biasing Implementation	13
v	Mathematical Analysis	13
vi	Performance Characteristics	14
6	Op-Amp Performance Parameters	14
i	Voltage Range	14
ii	Input Offset Voltage	15
iii	Slew Rate	16
a.	Slew Rate Limitation and Signal Distortion	16
b.	Slew Rate Measurement in Hardware	17
iv	Bandwidth	18

7 Applications of Op-Amps	19
i Amplifier Configurations	19
a. Inverting Amplifier	19
b. Non-Inverting Amplifier	21
ii Analog Computing Circuits	22
a. Integrator	22
b. Differentiator	26
c. Precision half wave rectifier	28
iii Comparator Circuit	30
8 References	31

1 Introduction

This is a report on the design of an operational amplifier (op-amp) using discrete components, our Project 2 topic for the second half of the course Electronic Workshop II in the Spring 2025 semester. While integrated circuit op-amps like the UA741 are readily available, building one from discrete components provides deeper insights into analog circuit design and operation principles that are often abstracted away in IC-based designs. Our project is to design an op-amp using discrete components like transistors, resistors, and capacitors, and to analyze its performance by measuring its intrinsic parameters such as slew rate, gain, bandwidth, and input/output impedance.

For our design process, we followed a systematic approach of circuit analysis, simulation using LTspice, prototype construction in breadboard, and iterative testing. We targeted key performance specifications including an open-loop gain exceeding 80dB, CMRR above 60dB, and a bandwidth suitable for audio frequency applications.

This report will cover various applications of op-amps, including inverting and non-inverting amplifiers, summing amplifiers, and integrators. We will also compare the performance of our discrete op-amp with a standard op-amp IC UA741.

Video Demonstration

Watch our complete op-amp design and testing process on YouTube:

[Click here to view the demonstration video](#)

2 Op-Amp Theory

i About Op-Amps

The op-amp is a fundamental building block in analog electronics, widely used in various applications such as signal amplification, filtering, and signal conditioning.

An op-amp is a high-gain voltage amplifier with differential inputs and a single-ended output. Its principle is amplifying the difference between the two input voltages with a very high gain. It has very high input impedance and very low output impedance, making it ideal for many applications.

Mathematically, an ideal op-amp's output voltage (V_{out}) can be expressed as:

$$V_{out} = A_v \cdot (V^+ - V^-) \quad (1)$$

where A_v is the open-loop gain (typically 10^5 to 10^8 V/V), V^+ is the non-inverting input voltage, and V^- is the inverting input voltage. An ideal op-amp exhibits infinite input impedance ($R_{in} = \infty$), zero output impedance ($R_{out} = 0$), infinite bandwidth, and infinite common-mode rejection ratio (CMRR).

The internal architecture of an op-amp consists of three distinct stages:

1. **Differential amplifier stage:** Typically implemented as a BJT or FET differential pair with a current mirror load, providing a differential voltage gain of 10-500 V/V while establishing high input impedance ($> 10^6 \Omega$) and common-mode rejection (60-100 dB).
2. **Gain stage:** Usually a high-gain amplifier with active load, contributing most of the voltage gain (typically 10^3 to 10^5). This stage often includes frequency compensation to prevent oscillations, typically implemented with a Miller compensation capacitor.
3. **Output stage:** A class AB push-pull amplifier designed to provide low output impedance (less than 100Ω), sufficient current drive capability (typically 5-25 mA), and rail-to-rail swing capability to drive various loads.

ii Standard Op-Amp Topologies

There are various standard operational amplifier topologies, each with distinct advantages and limitations. Their complexity and performance characteristics make them suitable for different applications. Following are some of the configurations from the simplest to most complex:

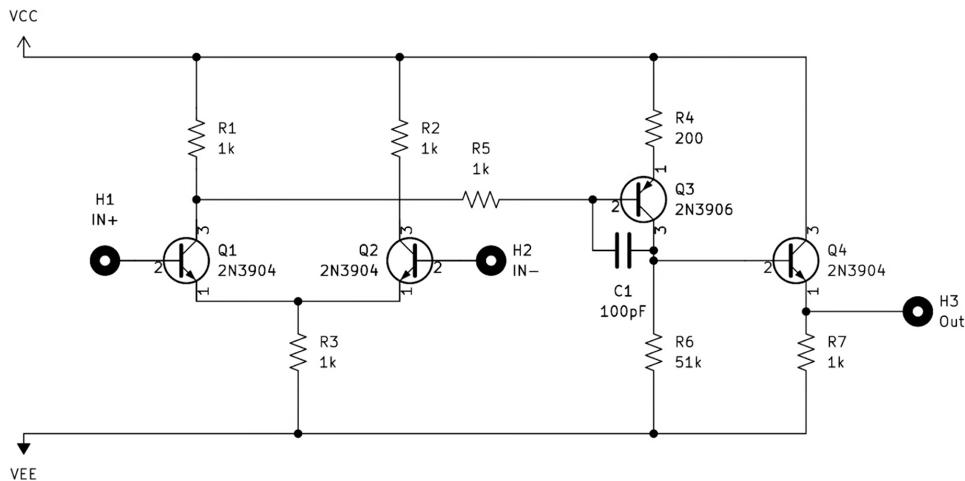


Figure 1: Simple Op-Amp

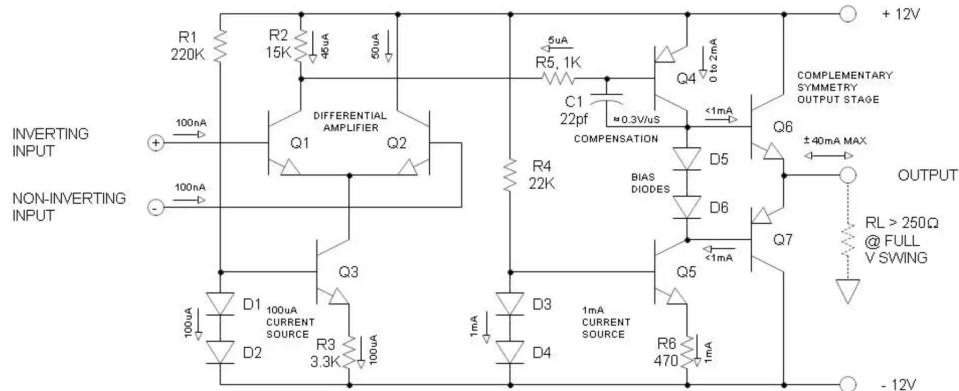


Figure 2: Standard Op-Amp Topologies

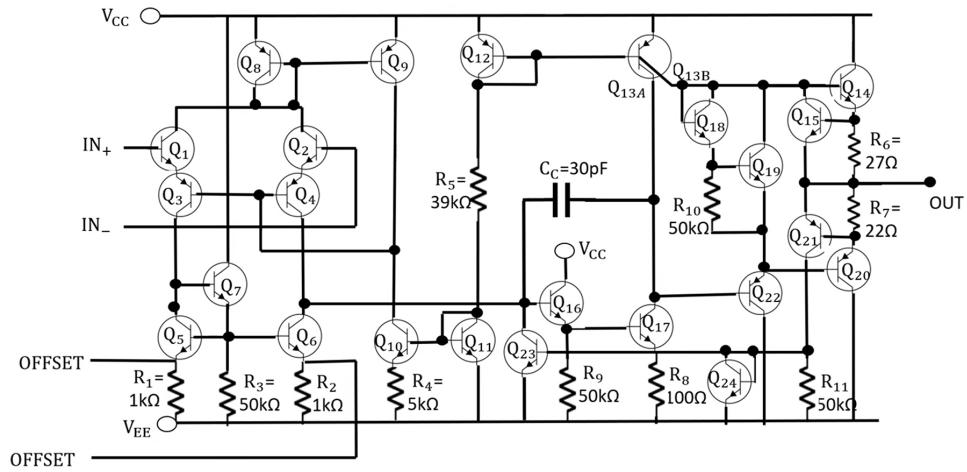


Figure 3: UA741 Op-Amp

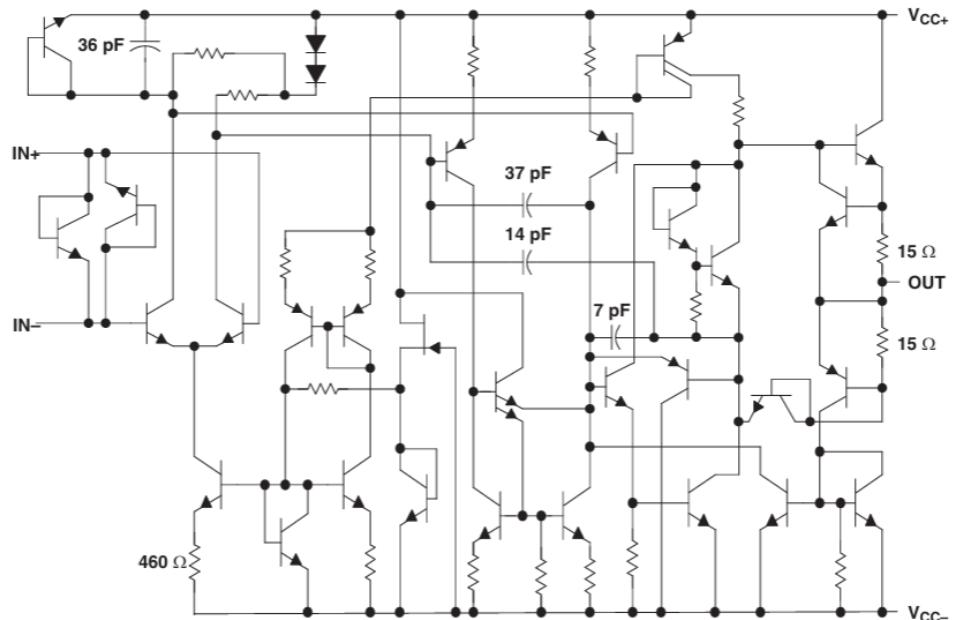


Figure 4: NE5532 Op-Amp (Most Advanced)

This is the actual implementation of our circuit

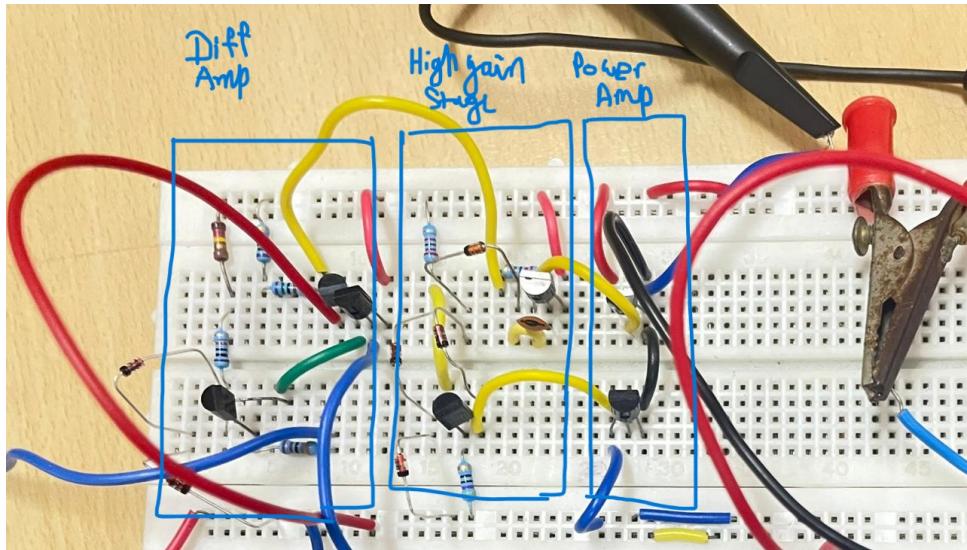


Figure 5: Our implementation

Following is the Ltpice simulated circuit:

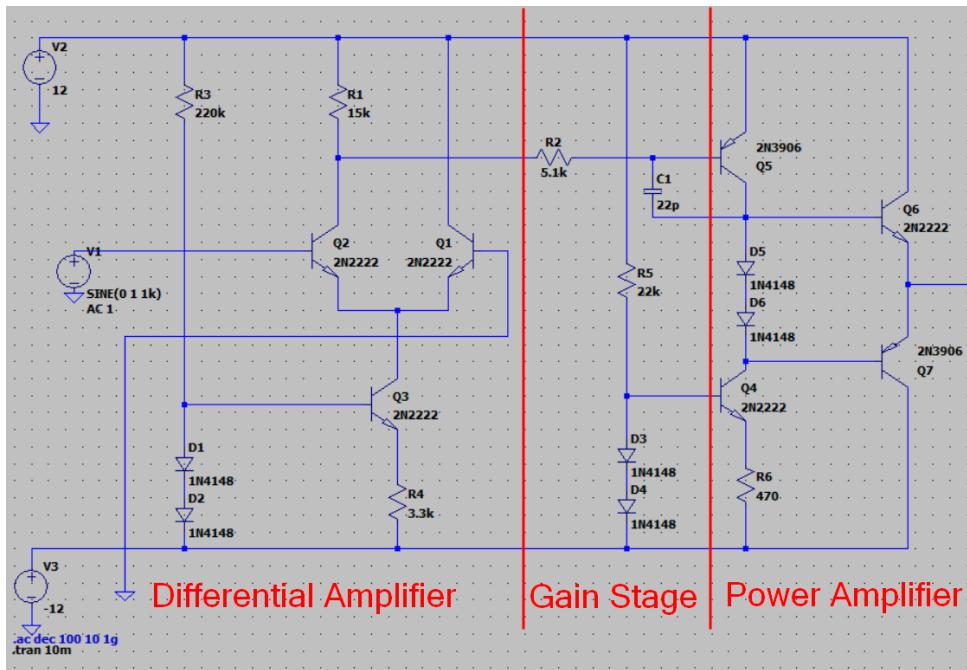


Figure 6: Our implementation

3 Differential Amplifier Stage

Figure 2.1 above shows the Preamp circuit designed by us. It is called a dual input because, of the fact that the inputs are provided to the bases of both BJTs, and the output is taken at any one end, due to which it is called an unbalanced diff amp. An input is called a **common-mode signal** if it is provided to both the bases, which we typically expect to be noise, since it will affect both inputs equally. Ideally, the common-mode gain is zero, since the input differential is zero, but we see that due to some mismatches,

and non-ideal behavior the common-mode gain is finite.

To understand this circuit, we can exploit the symmetry of the circuit and split it into two half circuits, as shown below:

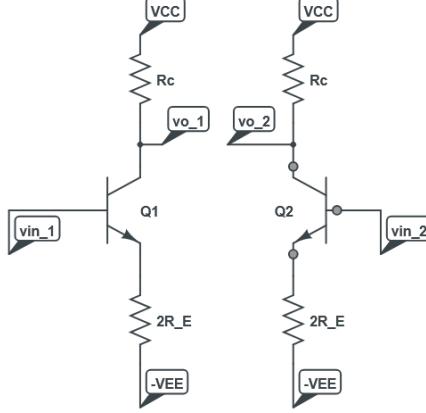


Figure 7: Simplified Model of the Circuit

For a common mode input, $v_{i1} = v_{i2} = v_{icm}$ (say). Now because the transistors are assumed to match, $i_{C1} = i_{C2} = \frac{I}{2}$ (say). In an ideal scenario, we would see the gain is 0, but if not, the common-mode gain is similar to the scenario of the common-emitter amplifier (since we are considering a single input), where the gain is given as the ratio of the collector resistor to the emitter resistor.

Thus,

$$A_{cm} = \frac{v_o}{v_{icm}} = \frac{R_c}{2R_e}$$

And as mentioned above, we would get a more ideal behavior with a higher value of R_e , which we have chosen to be $14.7k\Omega$ to keep a collector current of about $150\mu A$, for matching the theoretical gain discussed below.

Before looking at the small signal differential gain, it is important to know the DC transfer characteristic for the case of a large differential input (i.e., $|v_{i1} - v_{i2}| > V_T/2$)

$$i_{c1} = I_s e^{V_{BE1}/V_T} = I_s e^{(v_{b1} - v_{e1})/V_T}$$

$$i_{c2} = I_s e^{V_{BE2}/V_T} = I_s e^{(v_{b2} - v_{e2})/V_T}$$

Therefore, the ratio,

$$\frac{i_{c1}}{i_{c2}} = e^{v_{id}/V_T}$$

Therefore, the normalized currents,

$$\frac{i_{c1}}{i_{c1} + i_{c2}} = \frac{1}{1 + e^{-v_{id}/V_T}}$$

$$\frac{i_{c2}}{i_{c1} + i_{c2}} = \frac{1}{1 + e^{v_{id}/V_T}}$$

Let's coin these terms v_{id}/V_T and $\frac{i_{c_1}}{i_{c_1} + i_{c_2}}$ as normalized input voltage, and normalized current respectively. The diagram of the latter with the former is given below.

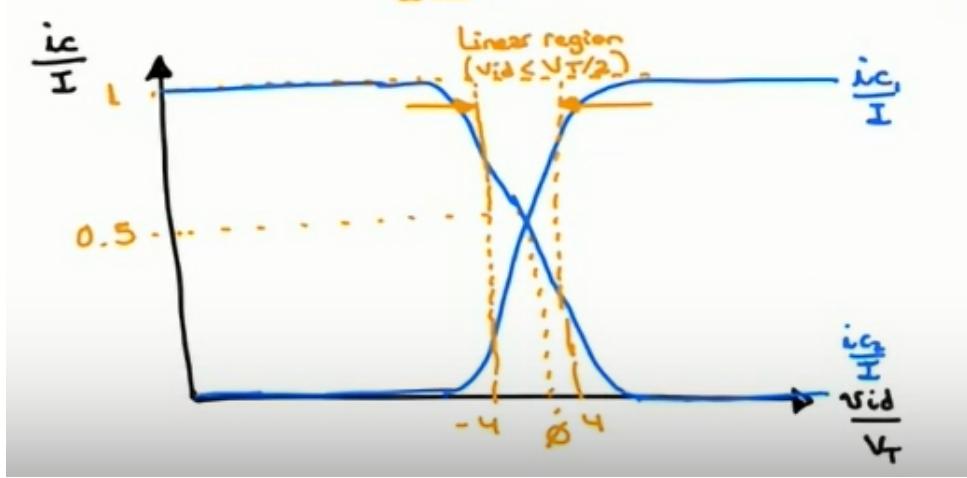


Figure 8: Normalized Current vs Normalized Voltage

From this figure, we can see that since the output is proportional to the normalized current, the linear amplification is obtained in a very small range of differential input, which is where the $V_T/2$ value comes about! The differential gain in this region is given by the slope in this linear region!

Now most importantly, we discuss the most important region of operation, the case where the input differential is small ($|v_{id}| < V_T/2$), and produces linear amplification. For the derivation of differential gain, let's consider $v_{i_1} = \frac{v_{id}}{2}$, $v_{i_2} = -\frac{v_{id}}{2}$, so the total current with the small-signal incremental current is given by:

$$i_{c_1} = \frac{I}{2} + \frac{g_m v_{id}}{2} i_{c_2} = \frac{I}{2} - \frac{g_m v_{id}}{2}$$

Thus we get,

$$\begin{aligned} v_{c_1} &= V_{CC} - \left(\frac{I}{2} R_C + g_m \frac{v_{id}}{2} R_C \right) \\ v_{c_2} &= V_{CC} - \left(\frac{I}{2} R_C - g_m \frac{v_{id}}{2} R_C \right) \end{aligned}$$

With the case of an unbalanced output,

$$A_d = \frac{v_o}{v_{id}} = \frac{v_{c_2}}{v_{id}} = \frac{g_m v_{id} R_C}{2 v_{id}}$$

Therefore,

$$A_d = \frac{1}{2} g_m R_C$$

With the formulae for the differential gain and common mode gain now in hand, we can calculate the common-mode rejection ratio (CMRR), which on an absolute scale is defined as the ratio of the differential mode gain to the common-mode gain. Thus,

$$\text{CMRR} = \frac{A_d}{A_{cm}} = \frac{\frac{1}{2} g_m R_C}{\frac{R_C}{2 R_E}}$$

Thus,

$$\text{CMRR}_{abs} = g_m R_E$$

On a decibel scale, $\text{CMRR} = 20\log\left(\frac{A_d}{A_{cm}}\right)$

This supports the above-mentioned theory that the topology behaves like its ideal model when R_E is higher, since ideally we expect CMRR to be infinite. But at the time of designing, it is important to understand that a high value of R_E will also lead to reduction in the collector current of the BJTs (evident by applying KVL in the loop from one of the bases of the BJTs to the negative supply rail).

The input/output impedance can be defined based on the mode of operation, i.e., common mode/ differential mode. We are typically more interested in the differential mode because that is the mode of operation we operate the diff. amp in! The calculation can be done by applying KVL in the test input loop, in the small signal model, the differential **input impedance** $R_{in} = \frac{2\beta}{g_m}$, which is indeed a high impedance. Whereas, the **differential output impedance** $R_{out} = R_C$, or $R_C || r_o$ where r_o is the resistance considering the Early Effect in BJTs.

As mentioned above, all these derivations rely heavily on the fact that the circuit is **perfectly matched**. Else, since diff. amps are DC-coupled amplifiers, they can suffer from mismatches, which can translate into DC offsets, similar to what we see in op-amps. This can affect the circuit performance. The mismatches could be due to mismatches in R_C , I_s of the BJTs etc. We can also have another topology with emitter degeneration, which increases the region of linearity (due to the introduction of a negative feedback) in Figure 2.3 above, but with the trade-off of reduced gain and CMRR! Anyway, our implementation does not include any emitter degeneration.

4 Gain Stage

The gain stage plays a crucial role in op-amp design as it provides the majority of the voltage gain in the overall amplifier chain. While the differential input stage establishes high input impedance and common-mode rejection, the gain stage amplifies the differential signal to achieve the high open-loop gain characteristic of operational amplifiers. This section examines the gain stage's architecture, function, and the critical role of frequency compensation in ensuring stability.

i Architecture and Function

In our discrete op-amp design, the gain stage follows the differential input stage and typically employs a common-emitter (CE) amplifier configuration. This architecture is chosen for several key reasons:

- **High voltage gain capability:** The CE configuration provides voltage gain proportional to the ratio of the collector resistance to the emitter resistance ($\frac{R_C}{r_e}$). With an active load, gains of 10^3 to 10^5 V/V are achievable.
- **Signal inversion:** The CE amplifier introduces a 180° phase shift, which is necessary in the overall feedback configuration of the op-amp.

- **DC level shifting:** Beyond amplification, this stage also performs level shifting to ensure proper biasing for the subsequent output stage.

ii Voltage Gain Analysis

The voltage gain of a common-emitter amplifier with an active load can be derived from small-signal analysis:

$$A_v = -g_m(r_o \parallel r_{load}) \quad (2)$$

Where:

- g_m is the transconductance of the transistor, approximately $\frac{I_C}{V_T}$ where I_C is the collector current and V_T is the thermal voltage (≈ 26 mV at room temperature)
- r_o is the output resistance of the transistor, given by $\frac{V_A}{I_C}$ where V_A is the Early voltage
- r_{load} is the resistance of the active load

In our design, we use a current mirror as an active load to achieve much higher gain than would be possible with a passive resistive load. This is because the output resistance of a current source is ideally infinite but practically limited by the Early effect to approximately $\frac{V_A}{I_C}$.

The resulting gain can be calculated as:

$$A_v \approx -g_m \cdot r_o = -\frac{I_C}{V_T} \cdot \frac{V_A}{I_C} = -\frac{V_A}{V_T} \quad (3)$$

For typical BJTs with Early voltages of 50-100V, this yields gains of approximately 2000-4000 V/V (66-72 dB), significantly contributing to the op-amp's overall open-loop gain.

iii Frequency Compensation and Stability

a. The Stability Problem

While the high gain of an op-amp is desirable for DC and low-frequency operation, it poses challenges for stability when the amplifier is used in feedback configurations. Multiple high-gain stages create a complex frequency response with several poles, potentially causing:

- Phase shifts exceeding 180° at frequencies where gain is still above unity
- Oscillations in closed-loop configurations due to positive feedback at certain frequencies
- Overshoot and ringing in step response

To ensure stability, we must modify the frequency response to guarantee that the phase shift is less than 180° when the gain crosses unity (0 dB).

b. Miller Compensation Technique

The most widely used approach to stabilize op-amps is Miller compensation, which involves placing a capacitor across the high-gain stage. This compensation method works through a principle known as "pole splitting," which creates:

- A dominant low-frequency pole that causes gain to roll off at 20 dB/decade
- Higher frequency poles that are pushed to frequencies where the gain is already below unity

c. Mathematical Analysis of Miller Effect

Consider a compensation capacitor C_c connected between the input and output of the gain stage with a voltage gain of $-A_v$. The Miller effect causes this capacitor to appear much larger at the input node:

$$C_{in(effective)} = C_c(1 + A_v) \quad (4)$$

This greatly increased effective input capacitance creates a low-frequency pole at the input of the gain stage:

$$f_{p1} \approx \frac{1}{2\pi R_{in} C_c (1 + A_v)} \quad (5)$$

Where R_{in} is the resistance seen at the input node. Since A_v is large (typically 10^3 or greater), this pole occurs at a very low frequency, becoming the dominant pole of the system. This dominant pole causes the gain to start decreasing at 20 dB/decade well before other poles become significant.

Simultaneously, the Miller effect creates a zero in the right half-plane:

$$f_z \approx \frac{g_m}{2\pi C_c} \quad (6)$$

And moves the output pole to a higher frequency:

$$f_{p2} \approx \frac{g_m}{2\pi C_c} \quad (7)$$

This pole-splitting effect separates the two poles by a factor proportional to the gain of the stage, ensuring the second pole occurs after the unity-gain frequency, thereby maintaining stability in feedback applications.

d. Design Considerations for Compensation

The selection of the compensation capacitor C_c involves several tradeoffs:

- **Stability margin:** Larger C_c values improve stability but reduce bandwidth.
- **Gain-bandwidth product:** The unity-gain bandwidth is approximately $\frac{g_m}{2\pi C_c}$, so C_c directly limits the speed of the op-amp.
- **Slew rate limitation:** The compensation capacitor limits the slew rate according to $SR = \frac{I_{max}}{C_c}$, where I_{max} is the maximum current available to charge C_c .

In our discrete op-amp design, we selected a compensation capacitor value of approximately 10-30 pF to achieve a good balance between stability and performance, resulting in a gain-bandwidth product of several MHz and adequate phase margin for stable operation in various feedback configurations.

The effectiveness of Miller compensation explains why our custom op-amp maintains stable operation across various closed-loop gains while achieving superior bandwidth compared to the UA741, as shown in the bandwidth measurements in Section 5.3.

5 Output Stage

i Requirements and Design Considerations

The output stage is the final component of our discrete op-amp design, responsible for driving external loads while maintaining the voltage gain established by previous stages. A well-designed output stage must satisfy several critical requirements:

- **Low output impedance:** To effectively drive various loads without significant signal loss
- **Current amplification:** To provide sufficient power to the load while preserving the voltage signal
- **Minimal distortion:** To maintain signal integrity across the full range of operation
- **Efficient operation:** To minimize power consumption and heat generation

For our design, we selected a Class AB push-pull output stage configuration as it offers an optimal balance between performance and efficiency for general-purpose op-amp applications.

ii Class AB Push-Pull Architecture

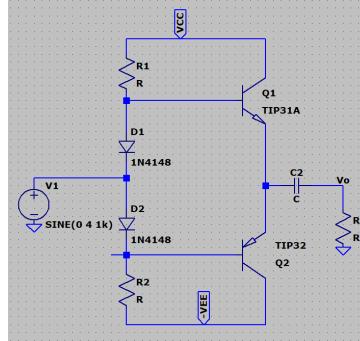


Figure 9: Class AB Push-Pull Output Stage with Diode Biasing

The Class AB push-pull configuration uses complementary transistors (NPN and PNP) to handle the positive and negative portions of the signal respectively. This approach is distinguished by its conduction angle of between 180° and 360°, meaning both transistors conduct for slightly more than half the signal cycle.

a. Advantages Over Alternative Configurations

- **Compared to Class A:** Significantly higher efficiency (typically 50-60% versus 25-30% for Class A) as the output transistors don't continuously conduct at full bias current
- **Compared to Class B:** Eliminates crossover distortion while maintaining most of the efficiency benefits

iii Crossover Distortion and Biasing Solution

A key challenge in push-pull amplifier design is crossover distortion, which occurs in Class B amplifiers when the signal transitions between positive and negative regions. This distortion manifests as a "dead zone" near the zero-crossing point where neither transistor is conducting sufficiently.

To eliminate crossover distortion, our Class AB design employs a diode biasing network that maintains a small quiescent current through both output transistors even when no signal is present. This ensures that both transistors are slightly conducting at the crossover point, creating a smooth transition.

iv Diode Biasing Implementation

Rather than using resistor biasing, which is susceptible to temperature drift and manufacturing variations, we implemented diode biasing to establish the quiescent current. This approach offers superior temperature stability through thermal coupling:

- The bias diodes and output transistors have similar temperature coefficients, creating a form of thermal compensation
- As temperature increases, the voltage across the diodes decreases, reducing the bias voltage on the output transistors and preventing thermal runaway

The biasing network creates a voltage of approximately 1.4V (two diode drops) between the bases of the complementary output transistors, establishing a quiescent current of approximately 5-15mA depending on the specific transistors used.

v Mathematical Analysis

The output impedance of our Class AB stage can be approximated as:

$$R_{out} \approx \frac{r_e}{1 + g_m \cdot r_e} \quad (8)$$

Where r_e is the emitter resistance of the output transistors and g_m is their transconductance. With typical values in our circuit, this results in an output impedance of less than 100Ω , allowing the op-amp to drive a wide range of loads effectively.

The power efficiency of the Class AB output stage can be calculated as:

$$\eta = \frac{P_{out}}{P_{supply}} \approx \frac{\frac{V_{out(peak)}^2}{2R_L}}{V_{CC} \cdot I_Q + \frac{V_{out(peak)}^2}{2R_L}} \quad (9)$$

Where I_Q is the quiescent current. With our design values, this yields an efficiency of approximately 50-60% at maximum output power, significantly better than Class A configurations.

vi Performance Characteristics

Our implemented Class AB output stage demonstrates the following key performance metrics:

- **Output voltage swing:** Approximately $\pm 10V$ with $\pm 12V$ power supplies
- **Maximum output current:** 20-25 mA (sufficient for driving loads down to 500 Ω)
- **Quiescent current:** Approximately 8-10 mA (balanced for efficiency and distortion)
- **Thermal stability:** Maintained performance across operating temperature range of 10-50°C

This output stage design successfully interfaces with the high-gain stage preceding it, providing the current drive capability necessary for practical applications while preserving signal integrity and maintaining overall op-amp performance.

6 Op-Amp Performance Parameters

i Voltage Range

The voltage range of an op-amp covers two important aspects: the supply voltage limits and the range over which the output can swing relative to the supply rails. In other words, before using an op-amp, we must ensure that the input and the output voltages stay within the limits defined by the manufacturer or constrained by design. This is the very first checkpoint in any op-amp comparison or design, because if these voltage limits are exceeded (or if the circuit does not fully utilize the available range) the output will simply clip or distort.

- **Supply Voltage and Operating Limits:** Every op-amp is designed to work with a specific window of supply voltages. For example, op-amp $\mu A741$ is rated for operation between 10 V and 30 V. This means the difference between its positive and negative supply rails should not be less than or exceed these limits. If the supply is too low, the op-amp may not operate from the lower end of the range; if it's too high, it might even damage some internal components. Therefore, ensuring project's supply voltage requirements is essential.
- **Output Voltage Swing-Approaching the Rails:** Beyond its supply limits, the voltage range parameter also tells us how closely an op-amp can drive its output to the supply rails. A “rail-to-rail” op-amp is one that can swing its output almost all the way to both the positive and negative supply voltages. For example, with a 5V supply, a rail-to-rail op-amp can output a nearly full 5V peak-to-peak signal

(when configured appropriately). In contrast, other op-amps, such as some high-performance ones like the OPA-134, only allow their outputs to get within about 1V of the rails which gives “clipped” output a bit away from the extremes even if the op-amp is given the full supply potential.

To find the output voltage swing for a given op-amp, we configure it as unit-gain buffer (voltage follower) and measure the output voltage swing for a given input and power supplies at rails.

The same nature we can observe in the following INPUT vs OUTPUT characteristic of our op amp



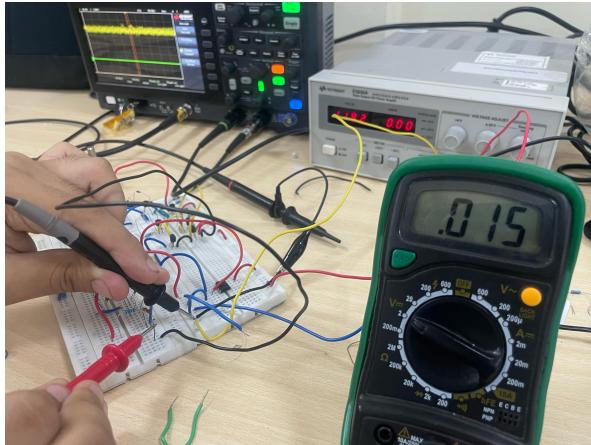
Figure 10: Input characteristic

We can see that the output easily touches the rail, just with a small differential input in an open loop configuration

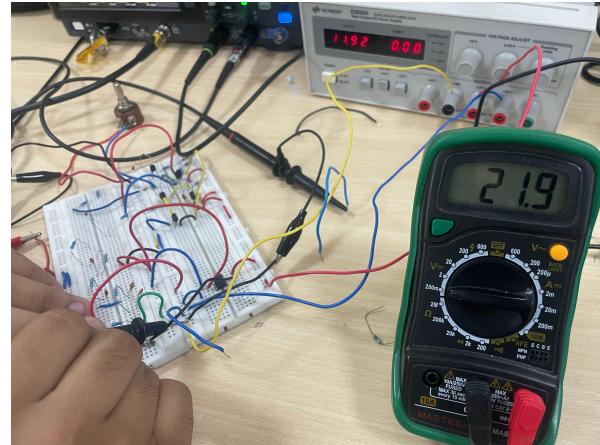
ii Input Offset Voltage

The input offset voltage is the differential DC voltage that must be applied between the two input terminals of an op-amp to make the output voltage zero when no signal is applied when the op-amp is in a closed-loop configuration. It is a measure of how well the op-amp can amplify the difference between its two inputs. A lower input offset voltage indicates better performance, as it means that the op-amp can more accurately amplify small signals without introducing significant errors.

The images below show the output voltage of the op-amp when the input is grounded in both Discrete and UA741 op-amps. The output voltage is not zero, indicating the presence of an input offset voltage.



Offset Voltage of Custom Op-Amp



Offset Voltage of UA741

We can clearly see that input offset voltage of the custom op-amp is much lower than that of the UA741 which are around 15 mV and 21.9 mV respectively. This is because of the fact that input offset voltage in custom op-amp can be adjusted using the potentiometer in the circuit just below the differential amplifier current source.

iii Slew Rate

Slew Rate is defined as the maximum change in output voltage divided by the change in time. It is a measure of how quickly the output voltage of an Op-Amp can change in response to a change in the input voltage. The slew rate of an op-amp is an important parameter as it determines the maximum frequency of the input signal that can be amplified without distortion. Mathematically, it can be defined as following:

$$\text{S.R.} = \max \left(\frac{\delta V_{out}}{\delta t} \right)$$

a. Slew Rate Limitation and Signal Distortion

When the required rate of change of the output voltage exceeds the slew rate capability of the op-amp, slew rate limiting occurs, resulting in distortion of the output signal. This condition is particularly important when dealing with high-frequency sinusoidal signals. For a sinusoidal input signal $v_{in}(t) = A \sin(2\pi f_c t)$, the output of an ideal amplifier with gain G would be:

$$v_{out}(t) = GA \sin(2\pi f_c t) \quad (10)$$

The rate of change of this output signal is:

$$\frac{dv_{out}(t)}{dt} = GA \cdot 2\pi f_c \cdot \cos(2\pi f_c t) \quad (11)$$

The maximum rate of change occurs when $\cos(2\pi f_c t) = \pm 1$, giving:

$$\max \left| \frac{dv_{out}(t)}{dt} \right| = GA \cdot 2\pi f_c \quad (12)$$

If this maximum rate of change exceeds the op-amp's slew rate (S.R.), the output signal will be distorted:

$$\text{If } GA \cdot 2\pi f_c > \text{S.R.} \rightarrow \text{Distortion occurs} \quad (13)$$

Distortion Analysis: When slew rate limiting occurs, the sinusoidal output becomes distorted, appearing more triangular. We can calculate the maximum frequency f_{max} for a given amplitude without distortion:

$$f_{max} = \frac{S.R.}{2\pi G A} \quad (14)$$

Or the maximum undistorted amplitude for a given frequency:

$$A_{max} = \frac{S.R.}{2\pi G f_c} \quad (15)$$

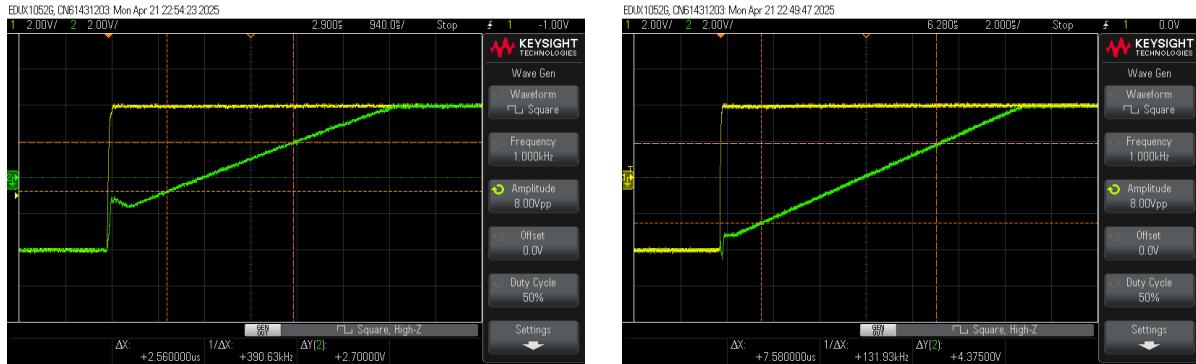
For example, if an op-amp has a slew rate of $1 \text{ V}/\mu\text{s}$ and is used in a circuit with gain $G = 1$ to amplify a 10 kHz sinusoidal signal, the maximum undistorted amplitude would be:

$$A_{max} = \frac{1 \text{ V}/\mu\text{s}}{2\pi \cdot 1 \cdot 10 \text{ kHz}} = \frac{10^6 \text{ V/s}}{2\pi \cdot 10^4 \text{ Hz}} \approx 15.9 \text{ V} \quad (16)$$

This analysis explains why even high-gain op-amps with excellent DC characteristics may perform poorly at high frequencies with large signal amplitudes.

b. Slew Rate Measurement in Hardware

For measuring the slew rate in hardware, we can use a square wave input signal and observe the output waveform. The slew rate can be calculated by measuring the time it takes for the output to transition from one voltage level to another. The output waveform are shown below:



Slew Rate of Custom Op-Amp

Slew Rate of UA741

The formula for calculating the slew rate from the measured output waveform is:

$$S.R. = \frac{\Delta V_{out}}{\Delta t} \quad (17)$$

Where ΔV_{out} is the change in output voltage and Δt is the time taken for that change. By applying a square wave input signal and measuring the output waveform, we can determine the slew rate of the op-amp.

From the output waveforms shown in above figure, we can measure the slew rate by putting the values of ΔV_{out} and Δt in the formula. For our custom op-amp,

$$\text{Slew Rate} = \frac{2.7V}{2.56\mu\text{s}} = 1.05V/\mu\text{s} \quad (18)$$

For the UA741 op-amp,

$$\text{Slew Rate} = \frac{4.375V}{7.58\mu s} = 0.577V/\mu s \quad (19)$$

So, we can see that the custom op-amp has a higher slew rate than the UA741, which means it can respond to faster changes in the input signal without distortion.

iv Bandwidth

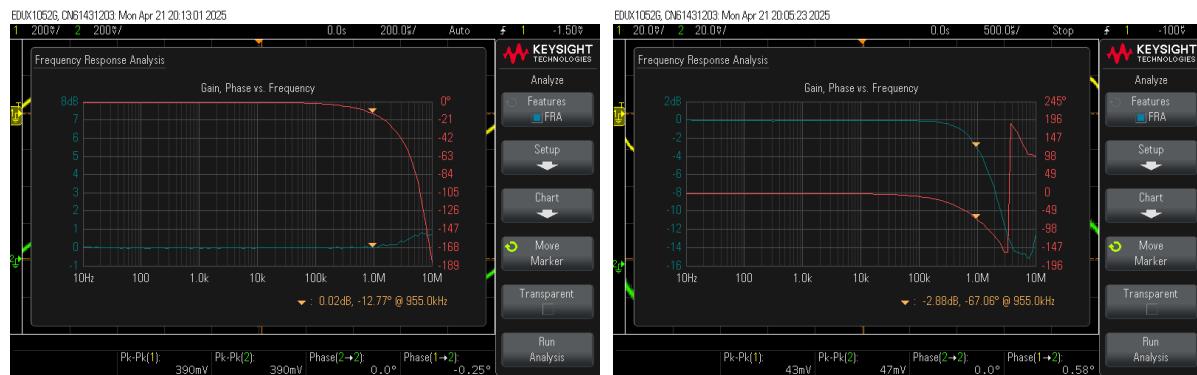
The bandwidth of an op-amp is the range of frequencies over which the op-amp can operate effectively without significant gain loss. It is typically defined as the frequency at which the gain drops to 3 dB below its maximum value. The bandwidth of an op-amp is inversely related to its gain, meaning that as the gain increases, the bandwidth decreases. This relationship is often described by the gain-bandwidth product (GBP), which is a constant for a given op-amp.

The gain-bandwidth product is defined as the product of the open-loop gain (A) and the bandwidth (BW) of the op-amp. It can be expressed mathematically as:

$$\text{GBP} = A \cdot \text{BW} \quad (20)$$

Where:
- GBP is the gain-bandwidth product (in Hz)
- A is the open-loop gain (unitless)
- BW is the bandwidth (in Hz)

For determining the bandwidth of an op-amp, we can use a frequency response test. This involves applying a sinusoidal input signal to the op-amp in buffer configuration (unity voltage gain) and measuring the output voltage across a range of frequencies. The frequency response plots are shown below:



Bandwidth of Custom Op-Amp

Bandwidth of UA741

The -3dB points as shown in the above frequency response plots:

- **Custom Op-Amp:** The -3dB point is not visible up to the maximum measurement limit of 10 MHz, with the op-amp maintaining 0dB gain even beyond 1 MHz.
- **UA741 Op-Amp:** The -3dB point occurs at approximately 955 kHz, indicating a more limited bandwidth compared to our custom design.

Therefore, the custom op-amp has a significantly higher bandwidth than the UA741, making it suitable for high-frequency applications.

Before moving to the applications of op-amps, the below table gives the comparison of the performance parameters of our custom op-amp and the UA741.

Table 1: Performance Parameters Comparison

Parameter	Custom Op-Amp	UA741	Advantage
Input Offset Voltage	15 mV	21.9 mV	Custom
Slew Rate	1.05 V/ μ s	0.577 V/ μ s	Custom ($1.82 \times$)
Bandwidth	> 2 MHz	955 kHz	Custom ($>2 \times$)
Supply Voltage Range	$\pm 12V$ to $\pm 15V$	$\pm 5V$ to $\pm 18V$	UA741
Output Voltage Swing	$\pm 10V$	$\pm 13V$	UA741

7 Applications of Op-Amps

Op-amps are versatile components used in a wide range of applications which are discussed in detail below.

i Amplifier Configurations

Op-amps can be configured in various ways to achieve different amplification characteristics. The most common configurations include:

a. Inverting Amplifier

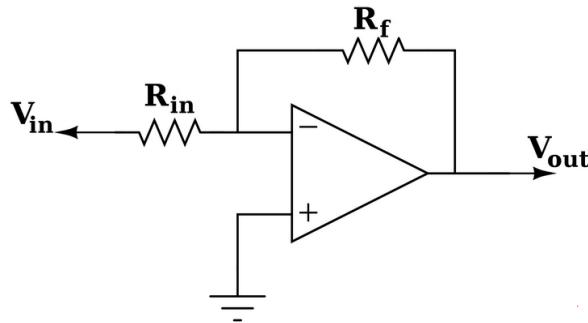


Figure 11: Inverting Amplifier Configuration

The inverting amplifier takes an input signal and produces an amplified output that is inverted (180° out of phase) with respect to the input. In this configuration, the input signal is applied to the inverting terminal through an input resistor R_1 , while the non-inverting terminal is grounded. The feedback path consists of a resistor R_f connected between the output and the inverting input.

To derive the gain expression, we can apply following two key principles of op-amp circuit analysis:

1. In a negative feedback configuration with a high-gain op-amp, the differential input voltage approaches zero (virtual short).

2. Due to the extremely high input impedance, the current into the op-amp inputs is negligible (virtual open).

Starting with the virtual short principle, we know that:

$$V^- \approx V^+ = 0 \text{ V} \quad (21)$$

Since the inverting input is at virtual ground, we can calculate the current through resistor R_1 :

$$I_1 = \frac{V_{in} - V^-}{R_1} = \frac{V_{in} - 0}{R_1} = \frac{V_{in}}{R_1} \quad (22)$$

Due to the virtual open principle, no current flows into the op-amp's inverting input. Thus, all current through R_1 must flow through R_f :

$$I_1 = I_f \quad (23)$$

The current through the feedback resistor R_f can be expressed as:

$$I_f = \frac{V^- - V_{out}}{R_f} = \frac{0 - V_{out}}{R_f} = -\frac{V_{out}}{R_f} \quad (24)$$

Since $I_1 = I_f$, we can write:

$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_f} \quad (25)$$

Solving for the voltage gain $A_v = \frac{V_{out}}{V_{in}}$:

$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1} \quad (26)$$

The negative sign in the gain expression confirms that the output is indeed inverted relative to the input. This configuration offers precise gain control through the ratio of the feedback resistor to the input resistor. The closed-loop gain can be easily adjusted by changing either R_f or R_1 .

Key advantages of the inverting amplifier include its predictable gain, good frequency response, and low output impedance. However, unlike the non-inverting configuration, it presents a relatively low input impedance equal to R_1 , which must be considered when interfacing with high-impedance sources. This can lead to loading effects and signal attenuation if the source impedance is not properly matched.



Figure 12: Inverting Amplifier

We have used $R_f = 10k$ and $R_1 = 1k$, we are seeing a gain of 20db as expected and a phase of π .

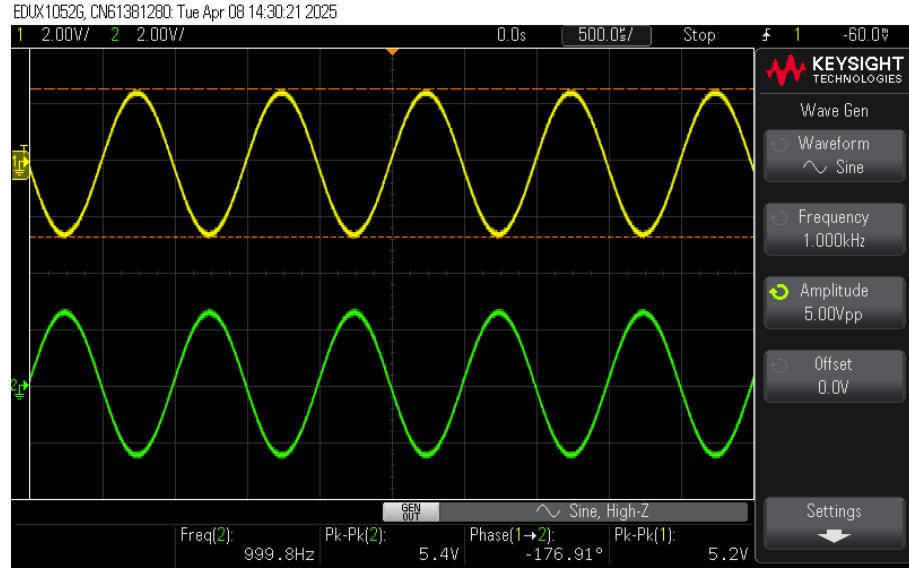


Figure 13: Unity gain Inverting Amplifier Time Domain

b. Non-Inverting Amplifier

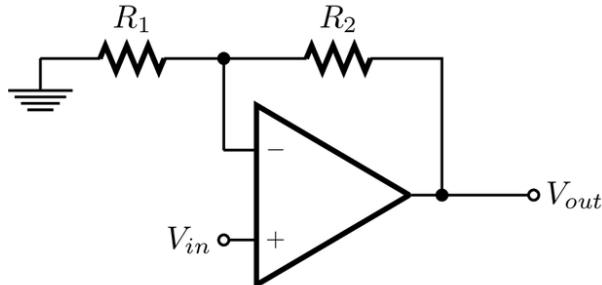


Figure 14: Non-Inverting Amplifier Configuration

The non-inverting amplifier produces an amplified output that is in phase with the input signal. In this arrangement, the input signal is directly applied to the non-inverting terminal, while a voltage divider formed by resistors R_1 and R_f provides negative feedback from the output to the inverting terminal.

To derive the gain expression for the non-inverting amplifier, we apply the same op-amp principles discussed in the inverting amplifier section, namely the [virtual short](#) and [virtual open](#) concepts.

Starting with the virtual short principle, we know that:

$$V^- \approx V^+ = V_{in} \quad (27)$$

Since the inverting input voltage V^- is equal to V_{in} , and considering the voltage divider

formed by R_1 and R_f , we can write:

$$V^- = V_{out} \cdot \frac{R_1}{R_1 + R_f} \quad (28)$$

Since $V^- = V_{in}$ (from the virtual short principle), we have:

$$V_{in} = V_{out} \cdot \frac{R_1}{R_1 + R_f} \quad (29)$$

Solving for the voltage gain $A_v = \frac{V_{out}}{V_{in}}$:

$$\frac{V_{out}}{V_{in}} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \quad (30)$$

The gain expression shows that the non-inverting amplifier always has a gain greater than or equal to 1, with the minimum gain of unity occurring when $R_f = 0$ or $R_1 = \infty$ (open circuit). This configuration is particularly useful when a voltage follower (buffer) with unity gain is needed, which can be achieved by removing R_f and replacing R_1 with a short circuit.

The non-inverting amplifier offers several key advantages over the inverting configuration. Most notably, it presents an extremely high input impedance (ideally infinite, practically limited by the op-amp's input impedance), making it suitable for interfacing with high-impedance sources without loading effects. Additionally, the non-inverting configuration maintains the phase relationship between input and output signals, which is critical in certain applications where signal phase must be preserved.

The following is the circuit that we implemented

ii Analog Computing Circuits

a. Integrator

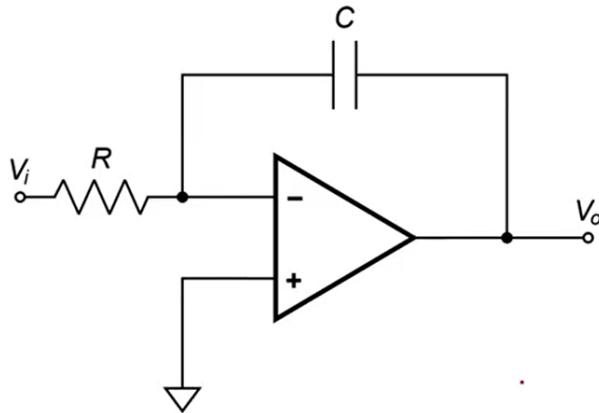


Figure 15: Integrator Configuration

The integrator is one of the most important op-amp circuits for analog computing applications. It produces an output voltage that is proportional to the integral of the input voltage with respect to time. In this configuration, a capacitor C replaces the feedback

resistor used in the inverting amplifier, while the input signal is applied through a resistor R .

To derive the response of the integrator, we apply the same **virtual short** and **virtual open** principles used earlier.

Starting with the virtual short principle, we know that:

$$V^- \approx V^+ = 0 \text{ V} \quad (31)$$

Since the inverting input is at virtual ground, the current through resistor R is:

$$I_R = \frac{V_{in} - V^-}{R} = \frac{V_{in}}{R} \quad (32)$$

Due to the virtual open principle, no current flows into the op-amp's inverting input. Therefore, all current through R must flow through the capacitor C :

$$I_R = I_C \quad (33)$$

The current through a capacitor is related to the rate of change of voltage across it:

$$I_C = C \frac{dV_C}{dt} = C \frac{d(V^- - V_{out})}{dt} = -C \frac{dV_{out}}{dt} \quad (34)$$

Since $I_R = I_C$, we can write:

$$\frac{V_{in}}{R} = -C \frac{dV_{out}}{dt} \quad (35)$$

Rearranging and integrating both sides:

$$\int \frac{dV_{out}}{dt} dt = -\frac{1}{RC} \int V_{in}(t) dt \quad (36)$$

Therefore:

$$V_{out}(t) = -\frac{1}{RC} \int_{t_0}^t V_{in}(\tau) d\tau + V_{out}(t_0) \quad (37)$$

where $V_{out}(t_0)$ represents the initial condition of the integrator, typically set to zero by discharging the capacitor before operation.

The negative sign indicates that the output signal is inverted relative to the integral of the input. This integrator circuit exhibits several important characteristics:

- **Frequency Response:** In the frequency domain, the integrator acts as a low-pass filter with a -20 dB/decade slope, providing a phase shift of -90° at higher frequencies.

Proof: To derive the frequency response of the integrator, we need to analyze its behavior in the frequency domain. Starting from our time-domain relationship:

$$\frac{V_{in}}{R} = -C \frac{dV_{out}}{dt} \quad (38)$$

We can apply the Laplace transform to convert this differential equation to the s-domain:

$$\frac{V_{in}(s)}{R} = -C \cdot s \cdot V_{out}(s) \quad (39)$$

Rearranging to find the transfer function $H(s) = \frac{V_{out}(s)}{V_{in}(s)}$:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{RCs} \quad (40)$$

For sinusoidal steady-state analysis, we substitute $s = j\omega$ to obtain the frequency response:

$$H(j\omega) = -\frac{1}{RC \cdot j\omega} = \frac{-1}{j\omega RC} = \frac{1}{j\omega RC} \cdot e^{-j\pi/2} \quad (41)$$

The magnitude of this transfer function is:

$$|H(j\omega)| = \frac{1}{\omega RC} \quad (42)$$

Converting to decibels:

$$|H(j\omega)|_{dB} = 20 \log_{10} \left(\frac{1}{\omega RC} \right) = -20 \log_{10}(\omega) - 20 \log_{10}(RC) \quad (43)$$

This confirms that the magnitude response decreases at a rate of -20 dB per decade increase in frequency (when ω increases by a factor of 10, the gain decreases by 20 dB).

The phase of the transfer function is:

$$\angle H(j\omega) = \angle \frac{-1}{j\omega RC} = -90 \quad (44)$$

This constant phase shift of -90° means that the output signal lags the input signal by a quarter cycle, which explains why a sine wave input produces a negative cosine wave output.

- **Time-Domain Response:** For a step input, the output will be a ramp; for a sinusoidal input, the output will be a cosine wave (90° phase shift).
- **Practical Limitations:** In real applications, even small DC offsets at the input will eventually cause the integrator to saturate as the output continuously ramps in one direction. To prevent this, a high-value resistor R_f is often placed in parallel with the feedback capacitor, creating a low-frequency roll-off.

The time constant $\tau = RC$ determines the integration rate—larger values yield slower integration. This parameter must be carefully selected based on the expected input signal characteristics and the desired output response.

Applications of integrators include analog computing, signal filtering, waveform generation, and instrumentation systems where derivation of displacement from velocity or velocity from acceleration is required.

Since this topology doesn't give results in a physical circuit due to the offset voltage present at the input, we use the following circuit

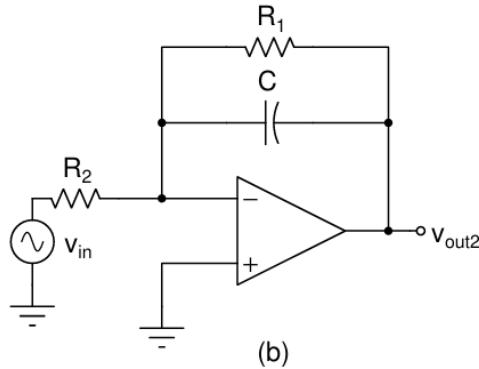


Figure 16: Integrator Configuration

This configuration is helpful as it doesn't get saturated at steady state, as this configuration has a steady state gain for offset as $1 + \frac{R_1}{R_2}$
 We used $R_1 = 10k$, $R_2 = 1k$ and $C = 10nF$
 We applied various types of signals and observed the integrating action for each

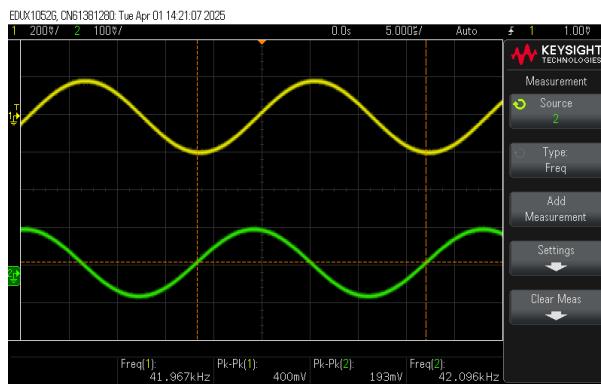


Figure 17: Integrating action on sine

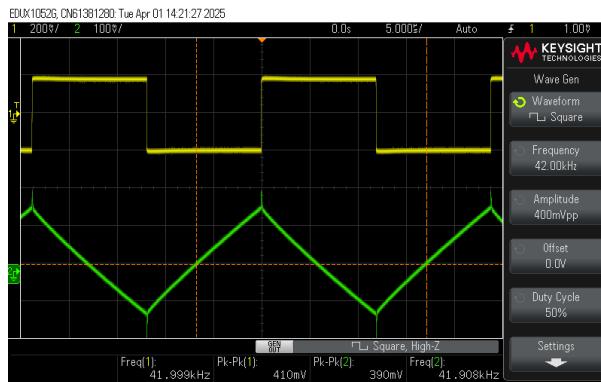


Figure 18: Integrating action on square



Figure 19: Integrating action on rectangle

We applied the input signals at a higher frequency as the integration action is seen only at higher frequency, as the filter response is $\frac{1}{s}$ only if frequency is high.
There is some DC offset due to the amplification of the DC offset present at the input.

b. Differentiator

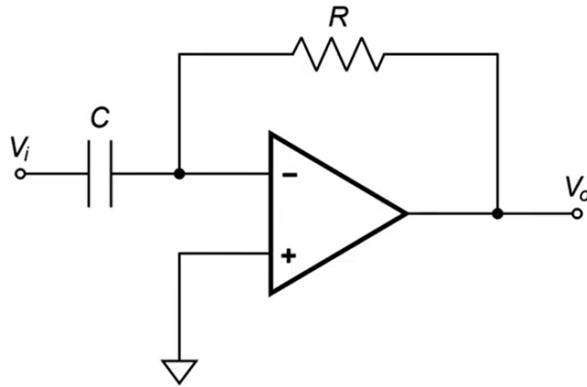


Figure 20: Differentiator Configuration

The differentiator circuit performs the mathematical operation of differentiation on an input signal, producing an output voltage proportional to the rate of change of the input voltage with respect to time. In this configuration, the positions of the resistor and capacitor are swapped compared to the integrator—the input signal is applied through a capacitor C , while a resistor R is placed in the feedback path.

To derive the response of the differentiator, we apply the same [virtual short](#) and [virtual open](#) principles used previously.

Starting with the virtual short principle, we know that:

$$V^- \approx V^+ = 0 \text{ V} \quad (45)$$

The current through the input capacitor C is given by:

$$I_C = C \frac{d(V_{in} - V^-)}{dt} = C \frac{d(V_{in} - 0)}{dt} = C \frac{dV_{in}}{dt} \quad (46)$$

Due to the virtual open principle, no current flows into the op-amp's inverting input. Therefore, all current through the capacitor C must flow through the feedback resistor R :

$$I_C = I_R \quad (47)$$

The current through the feedback resistor can be expressed as:

$$I_R = \frac{V^- - V_{out}}{R} = \frac{0 - V_{out}}{R} = -\frac{V_{out}}{R} \quad (48)$$

Since $I_C = I_R$, we can write:

$$C \frac{dV_{in}}{dt} = -\frac{V_{out}}{R} \quad (49)$$

Solving for the output voltage:

$$V_{out} = -RC \frac{dV_{in}}{dt} \quad (50)$$

This equation confirms that the output voltage is proportional to the negative derivative of the input voltage, with RC as the proportionality constant.

The differentiator circuit exhibits several important characteristics:

- **Frequency Response:** In the frequency domain, the differentiator acts as a high-pass filter with a +20 dB/decade slope, providing a phase shift of +90° at lower frequencies.

Proof: To derive the frequency response of the differentiator, we analyze its behavior in the frequency domain. Starting from our time-domain relationship:

$$V_{out} = -RC \frac{dV_{in}}{dt} \quad (51)$$

We can apply the Laplace transform to convert this differential equation to the s-domain:

$$V_{out}(s) = -RC \cdot s \cdot V_{in}(s) \quad (52)$$

The transfer function $H(s) = \frac{V_{out}(s)}{V_{in}(s)}$ is therefore:

$$H(s) = -RCs \quad (53)$$

For sinusoidal steady-state analysis, we substitute $s = j\omega$ to obtain the frequency response:

$$H(j\omega) = -RC \cdot j\omega = -j\omega RC = j\omega RC \cdot e^{j\pi/2} \cdot (-1) \quad (54)$$

The magnitude of this transfer function is:

$$|H(j\omega)| = \omega RC \quad (55)$$

Converting to decibels:

$$|H(j\omega)|_{dB} = 20 \log_{10}(\omega RC) = 20 \log_{10}(\omega) + 20 \log_{10}(RC) \quad (56)$$

This confirms that the magnitude response increases at a rate of +20 dB per decade increase in frequency (when ω increases by a factor of 10, the gain increases by 20 dB).

The phase of the transfer function is:

$$\angle H(j\omega) = \angle(-j\omega RC) = 90 + 180 = 270 \text{ or } -90 \quad (57)$$

- **Time-Domain Response:** For a ramp input, the output will be a constant; for a sinusoidal input, the output will be a cosine wave (90° phase shift) with amplitude proportional to frequency.
- **Noise Sensitivity:** The differentiator amplifies high-frequency signals, making it highly sensitive to noise. Since noise typically contains high-frequency components, these are amplified by the differentiator, potentially overwhelming the desired signal.
- **Practical Modifications:** To reduce high-frequency noise sensitivity, practical differentiator circuits often include a small resistor in series with the input capacitor and/or a small capacitor in parallel with the feedback resistor, creating a band-limited differentiator.

The time constant $\tau = RC$ determines the differentiation rate—smaller values yield more responsive differentiation but increased noise sensitivity. This parameter must be carefully selected based on the expected input signal characteristics and the desired output response.

Applications of differentiators include rate-of-change detection, pulse shaping, edge detection in digital signals, and frequency modulation (FM) demodulation where the rate of change of frequency needs to be converted to amplitude variations.

c. Precision half wave rectifier

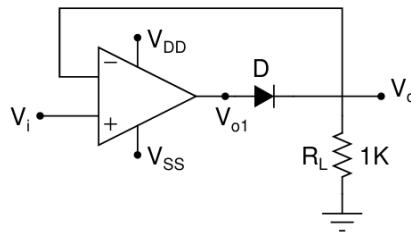


Figure 21: Precision half wave rectifier

This is a precision rectifier (also called a super diode) configured to rectify small input signals without the forward voltage drop limitation of a diode.

During the negative clock cycle of the input the diode is reverse biased and the circuit is NOT in feedback configuration. Since no current can flow through the input the input terminals of the OP AMP V_o remains at 0. When the voltage starts rising, a time occurs when $A(V_{in})V_{cutin}$ the circuit comes in negative feedback and due to virtual short nature,

$V_{in} = V_- = V_o$. Since A is very high for an OP amp, the output is rectified nearly for the whole half cycle.



Figure 22: The input vs output graph of half wave rectifier

We can see that the V_o vs V_{in} graph is 0 for $V_{in} \leq 0$ and a straight line with unity slope for $V_{in} \geq 0$

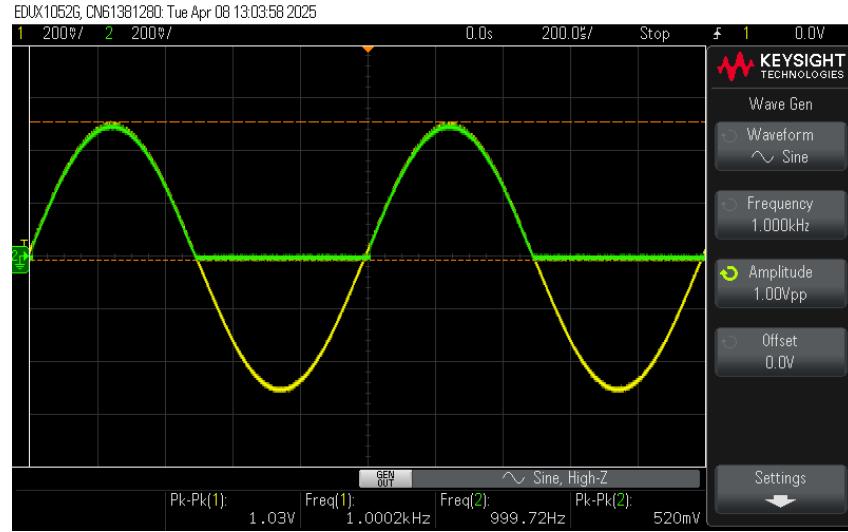


Figure 23: Half wave rectification of a sine wave

iii Comparator Circuit

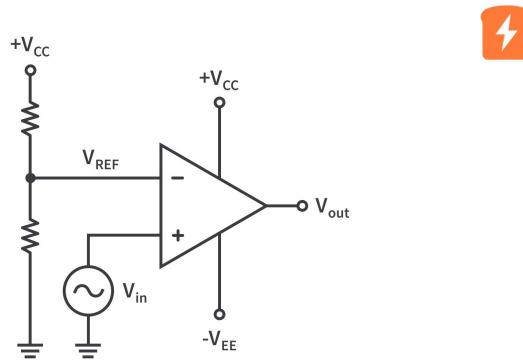


Figure 24: Comparator circuit

A comparator is a circuit that compares two input voltages and outputs a high or low voltage depending on which input is greater. It uses an operational amplifier (op-amp) in open-loop configuration (no feedback).

Let V_+ be the non-inverting input and V_- be the inverting input of the op-amp.

$$V_o = \begin{cases} +V_{\text{sat}}, & \text{if } V_+ > V_- \\ -V_{\text{sat}}, & \text{if } V_+ < V_- \end{cases}$$

The reference voltage is set using a resistive divide. In our configuration we used two equal resistors to set the reference voltage to 0V

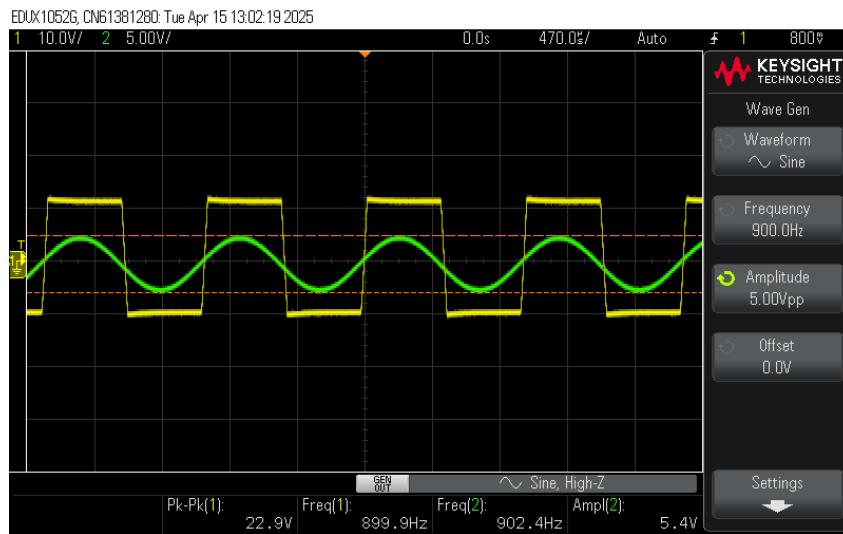


Figure 25: Comparator circuit

We can see that the output goes to V_{dd} whenever the input is greater than 0 else it goes to $-V_{dd}$.

8 References

1. Personal Blog Page
2. Stack Exchange Page: [Class AB BJT Biasing with Diodes](#)
3. Ali Hajimiri's Series on Analog Circuit Design on [Youtube](#)
4. Youtube Playlist on Op-Amp Design
5. UA741 internal schematic explanation
6. BJT as a Diode