EXPERIMENT 9 : SHIFT REGISTER

AIM: To realize and study of Shift Registers

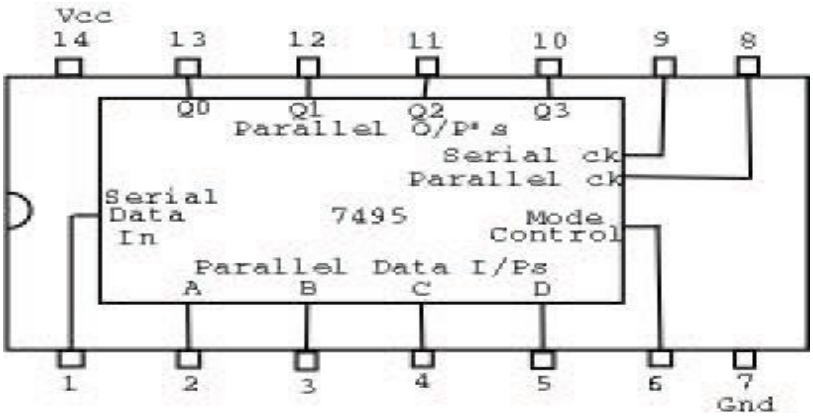
1) SISO (Serial in Serial out)
2) SIPO (Serial in Parallel out)
3) PIPO (Parallel in Parallel out)
4) PISO (Parallel in Serial out)

LEARNING OBJECTIVE:

- To identify the basic forms of data movement in shift register
- To learn different modes data transfer

COMPONENTS REQUIRED: IC 7495, LEDs, Power supply, Breadboard,

PINOUT DIAGRAM FOR IC7495:



THEORY: In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, *shifting in* the data present at its input and *shifting out* the last bit in the array, at each transition of the clock input.

More generally, a shift register may be multidimensional, such that its "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register'.

1)SERIAL IN SERIAL OUT (SISO) (Right Shift)

Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
0	t1	0	X	X	X
1	t2	1	0	X	X
0	t3	0	1	0	X
1	t4	1	0	1	0
X	t5	X	1	0	1
X	t6	X	X	1	0
X	t7	X	X	X	1
X	t8	X	X	X	X

2)SERIAL IN PARALLEL OUT (SIPO)

Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
0	t1	0	X	X	X
1	t2	1	0	X	X
0	t3	0	1	0	X
1	t4	1	0	1	0

3)PARALLEL IN PARALLEL OUT (PIPO)

Clock Input Terminal	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
CLK_2	t1	1	0	1	0

4)PARALLEL IN SERIAL OUT (PISO)

Clock Input Terminal	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
CLK_2	t1	1	0	1	0
CLK_2	t2	X	1	0	1

0	t3	X	X	1	0
1	t4	X	X	X	1
X	t5	X	X	X	X

PROCEDURE

1)Give biasing to the IC

2)Do connections for SIPO, PIPO and note down corresponding o/p.

OBSERVATIONS

I) PIPO : Parallel I/P Parallel O/P

M	**Clk2**	**A**	**B**	**C**	**D**	**Q_A**	**Q_B**	**Q_C**	**Q_D**
1									
1									

II) SIPO : Serial I/P Parallel O/P

a) Shift Right

M	**Clk1**	**Serial I / P**	**Q_A**	**Q_B**	**Q_C**	**Q_D**
0						

b) Shift Left

M	**Clk2**	**D I / P**	**Q_A**	**Q_B**	**Q_C**	**Q_D**
1						

Postlab Questions:

1. What is shift register ? Explain 4 bit bi-directional shift register
2. Design 4 bit Johnson counter.
3. Design 4 bit twisted ring counter.