EXPERIMENT : 12 VHDL : Sequential circuit Design

AIM: Simulation of sequential circuit using VHDL.

Write a code in VHDL for

1. To implement flip flop.
2. To implement 4-bit up/down synchronous counter.
3.

LEARNING OBJECTIVE:

1. Objective is to learn VHDL code and implement various sequential circuits using VHDL

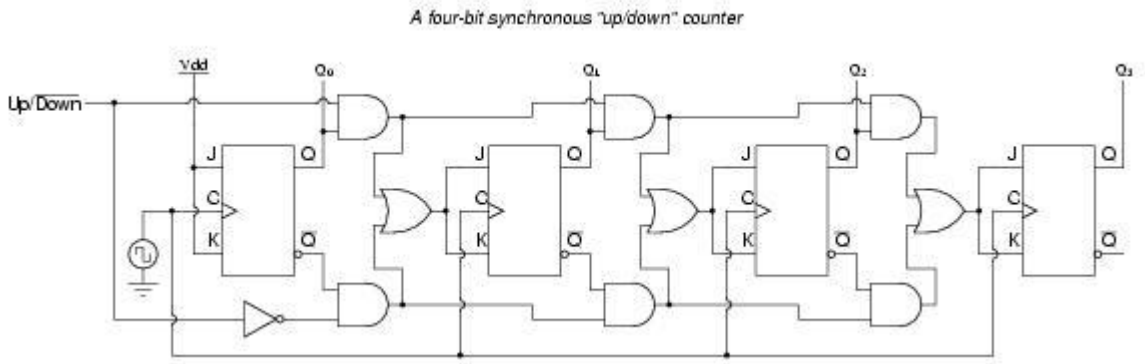
THEORY

Counter is a circuit which counts the number of clock pulses. There are two types of counters

1. Asynchronous or ripple counters.
2. Synchronous counter.

An up-down counter is a device which can count up and down. The up and down counting is controlled by an signal called as mode which decides the up and down counting of the counter.

4 –bit Synchronous up/Down counter



Operation:

When Mode =0 the circuit acts as an up counter. When Mode = 1, it acts as a down counter.

Procedure:

1. Write an appropriate VHDL code in editor for implementing Up/down synchronous counter.
2. Write Test bench code covering all the test cases for the same.
3. Compile VHDLcode and Test bench code.
4. Simulate the code using written test bench.
5. Observe the output waveforms. And compare with theoretical output.

POST LAB QUSTIONS:

1. Explain process statement in VHDL
2. Explain wait statement in VHDL