FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING
Department of Computer Engineering

Academic Term : July-Nov 2020

Class : B.E Computer Sem -VII
Subject : Mobile Communication And Computing

Practical No:	**4**
Title:	Implementation of GSM security algorithms (A3/A5/A8)
Date of Performance:	
Date of Submission:	
Roll No:	
Name of the Student:	

Evaluation:

Sr. No	Rubric	Grade
1	On time submission Or completion (2)	
2	Preparedness(2)	
3	Skill (4)	
4	Output (2)	

Signature of the Teacher :

PRACTICAL - 4

Title : Implementation of GSM security algorithms (A3/A5/A8)

Objective : To study about GSM security .

References :

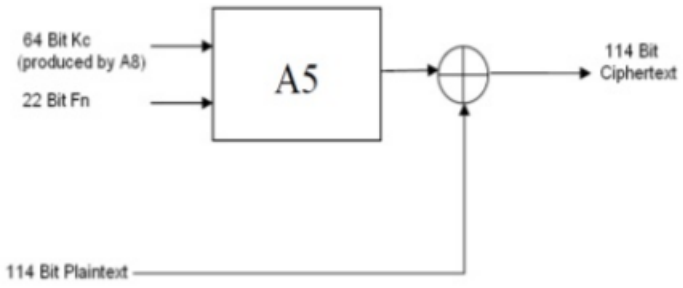
Prerequisite : knowledge of any Programming.

Theory:

A5 is a stream cipher which can be implemented very efficiently on any hardware. It is used by GSM cell phones for confidentiality.
There exist several implementations of this algorithm, the most commonly used ones are A5/0, A5/1 and A5/2 (A5/3 is used in 3G system).
As a stream cipher, A5 works on a bit by bit basis and not on blocks.

A5 Algorithm

Kc is the key which was produced by A8 algorithm. PT is the data which is transmitted. Fn is the frame bits which come from LFSR (Linear Feedback Shift Register) process.



- A5/1 employs 3 linear feedback shift registers, which will label as X,Y,Z
- Register X holds 19 bits, which we label (x0,x1,x2……..x18)
- The register Y holds 22 bits (y0,y1,y2……y21) and Z holds 23 bits (z0,z1,z2,……z22)
- So three LFSRs hold 64 bits.
- Initialize key K of size 64 bits. The key is used as the initial fill of the three registers.
- After these 3 registers are filled with the key, we are ready to generate the keystream.

Keystream Generation

- When register X steps, the following occur

  $t = x_{13}$ xor x_{16} xor x_{17} xor x_{18}

  $x_i = x_{i-1}$ for i=18,17,16,……1

  $x_0 = t$

  Similarly for registers Y and Z , each step consists of

  $t = y_{20}$ xor y_{21}

  $y_i = y_{i-1}$ for i=21,20,19,……1

  $y_0 = t$

  and

  $t = z_7$ xor z_{20} xor z_{21} xor z_{22}

  $z_i = z_{i-1}$ for i=22,21,20,……1

  $z_0 = t$

- Given three bits x,y,z , define maj(x,y,z) to be the majority vote function; that is, if the majority of x,y,z are 0, then the function returns 0, otherwise it returns 1.
- A5/1 is implemented in hardware, and at each clock pulse the value

  m= maj(x8, y10, z10) is computed.

- Then the registers X,Y and Z step according to the following rules:

  If x_8 = m then X steps

  If y_{10} = m then Y steps

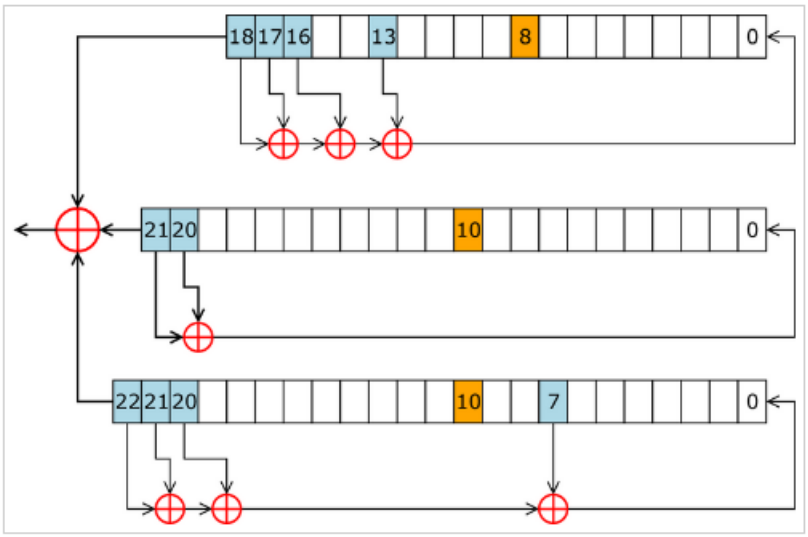
  If z_{10} = m then Z steps

- Finally , a keystream bit s is generated as

  $s = X_{18} \oplus y_{21} \oplus z_{22}$

which is then XORed with the plaintext (if encrypting) or XORed with the ciphertext (if decrypting)

Although this seem like a complicated way to generate a single keystream bit, A5/1 is easily implemented in hardware and can generate bits at a rate proportional to the clock speed .



A5/1 Keystream generator