EXPERIMENT : 11 VHDL : Design combinational circuit

AIM: Simulation of combinational circuit using VHDL.

Write a code in VHDL for

1. Implement Basic gates
2. Half adder and subtractor
3. Designing Full Adder and subtractor
4. Designing 4:1 Multiplexer.
5. Binary to gray converter
6. Gray to Binary converter

LEARNING OBJECTIVE:

1. Objective is to learn VHDL code and implement various combinational circuits using VHDL

THEORY :

VHDL stands for very high-speed integrated circuit hardware description language. It is a programming language used to model a digital system by dataflow, behavioural and structural style of modelling. This language was first introduced in 1981 for the department of Defence (DoD) under the VHSIC program.

Describing a Design:

In VHDL an entity is used to describe a hardware module. An entity can be described using,

- Entity declaration
- Architecture
- Configuration
- Package declaration
- Package body

Entity Declaration

It defines the names, input output signals and modes of a hardware module.

```
entity entity_name is
  Port declaration;
end entity_name;
```

Architecture –

Architecture can be described using structural, dataflow, behavioral or mixed style.

```
architecture architecture_name of entity_name
architecture_declarative_part;
begin
  Statements;
end architecture_name;
```

Here, we should specify the entity name for which we are writing the architecture body. The architecture statements should be inside the 'begin' and 'énd' keyword. Architecture declarative part may contain variables, constants, or component declaration.

Data Flow Modeling

In this modeling style, the flow of data through the entity is expressed using concurrent (parallel) signal. The concurrent statements in VHDL are WHEN and GENERATE.

Besides them, assignments using only operators (AND, NOT, +, *, sll, etc.) can also be used to construct code.

Finally, a special kind of assignment, called BLOCK, can also be employed in this kind of code.

In concurrent code, the following can be used −

- Operators
- The WHEN statement (WHEN/ELSE or WITH/SELECT/WHEN);
- The GENERATE statement;
- The BLOCK statement

Behavioural Modelling

In this modeling style, the behavior of an entity as set of statements is executed sequentially in the specified order. Only statements placed inside a PROCESS, FUNCTION, or PROCEDURE are sequential.

PROCESSES, FUNCTIONS, and PROCEDURES are the only sections of code that are executed sequentially.

However, as a whole, any of these blocks is still concurrent with any other statements placed outside it.

One important aspect of behavior code is that it is not limited to sequential logic. Indeed, with it, we can build sequential circuits as well as combinational circuits.

The behavior statements are IF, WAIT, CASE, and LOOP. VARIABLES are also restricted and they are supposed to be used in sequential code only. VARIABLE can never be global, so its value cannot be passed out directly.

Structural Modelling

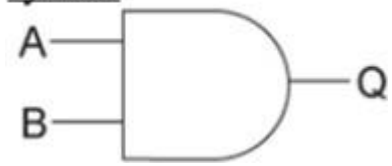
In this modeling, an entity is described as a set of interconnected components. A component instantiation statement is a concurrent statement. Therefore, the order of these statements is not important. The structural style of modeling describes only an interconnection of components (viewed as black boxes), without implying any behavior of the components themselves nor of the entity that they collectively represent.

In Structural modeling, architecture body is composed of two parts − the declarative part (before the keyword begin) and the statement part (after the keyword begin).

EXAMPLE:

Logic Operation – AND GATE

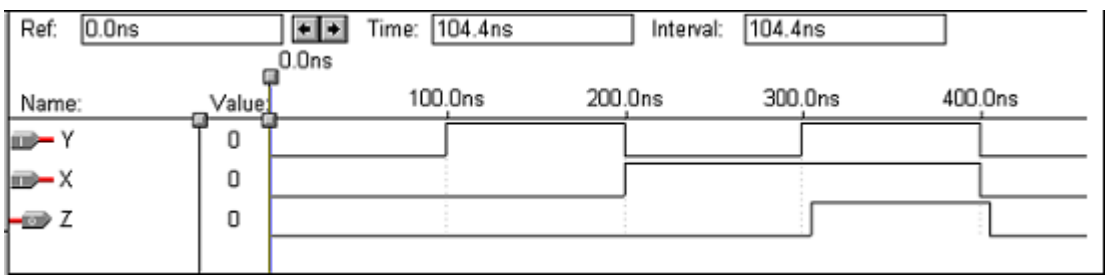
Symbol:



X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

VHDL Code:

```
Library ieee;
use ieee.std_logic_1164.all;
entity and1 is
  port(x,y:in bit ; z:out bit);
end and1;
architecture virat of and1 is
begin
  z<=x and y;
end virat;
```



Procedure:

1. Write an appropriate VHDL code in editor for implementing Full Adder circuits.
2. Write Test bench code covering all the test cases for the same.
3. Compile VHDLcode and Test bench code.
4. Simulate the code using written test bench.
5. Observe the output waveforms. And compare with theoretical output.
6. Follow similar steps for implementing 4 : 1 Multiplexer.

POST LAB QUESTIONS:

1. **Write the basic structure of VHDL File**
2. **Explain Signal statement in VHDL with example**