#### **EXPERIMENT NO 8 FLIP FLOPS**

**<u>AIM</u>**: Truth Table verification of

- 1) SR Flip Flop
- 2) JK Flip Flop.
- 3) T Flip Flop.
- 4) D Flip Flop

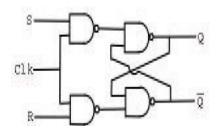
#### **LEARNING OBJECTIVE:**

- To learn about various Flip-Flops conversions
- To learn about applications of FlipFlops

**COMPONENTS:** ICs 7400, 7402, 7476, LED.

## **CIRCUIT DIAGRAM**

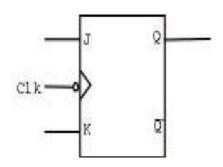
## 1.SR Flip flop using nand gate



#### TRUTH TABLE

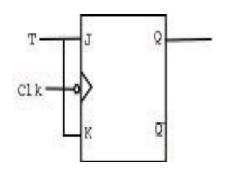
Clk	S	R	Qn
0	X	X	
$\rightarrow$	0	0	
$\rightarrow$	0	1	
$\rightarrow$	1	0	
<b>+</b>	1	1	

### 2.JK FF (IC 7476)



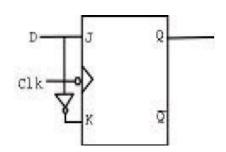
Clk	J	K	Qn
0	X	X	
$\rightarrow$	0	0	
$\downarrow$	0	1	
$\downarrow$	1	0	
$\downarrow$	1	1	

#### 3.T FF using JK



Clk	T	Qn
<b>\</b>	0	
<b>\</b>	1	

#### 4.D FF using JK



Clk	D	Qn
$\downarrow$	0	
$\downarrow$	1	

#### **THEORY:**

Logic circuits that incorporate memory cells are called sequential logic circuits; their output depends not only upon the present value of the input but also upon the previous values. Sequential logic circuits often require a timing generator (a clock) for their operation. The latch (flip-flop) is a basic bi-stable memory element widely used in sequential logic circuits. Usually there are two outputs, Q and its complementary value.

Basically, a flip flop has two inputs. The other input is the clock. The clock input is usually drawn with a triangular input. These flip-flops are *positive edge-triggered flip flops*. This means that the flip flops can only change output values when the clock is at a positive edge. There are also negative edge triggered flip flops, which change on a negative edge, and level triggered flip flops, that change only when the value is 1. We consider only positive edge triggered flip flops. When the clock is not at a positive edge, then the output value is held. That is, it does not change. A flip flop also has two outputs, **Q** and **Q'**. The output is really the bit that's stored. Thus, the flip flop is always outputting the one bit of information. There are different types of FFs . They are S-R, J-K, D & T.

#### **PROCEDURE:**

- 1) Give biasing to the IC and do necessary connections.
- 2) For various combinations of input verify the truth table.

# Post lab Questions

- 1. List the applications of flip flops
- 2. Explain Master Slave Flip flop with neat timing diagram
- 3. Convert D FF to SR FF
- 4. Convert SR to JK FF