Lab 2

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Problem

Use the following code fragment:

loop: LD R1,0(R2)

DADDI R1,R1,1

SD 0(R2),R1

DADDI R2,R2,4

DSUB R4,R3,R2

BNEZ R4,loop

Assume that the initial value of R3 is R2+396. Throughout this exercise use the classic RISC five-stage integer pipeline in H&P (branch is resolved in the second stage) and assume all memory accesses take 1 clock cycle.

a. Show the timing of this instruction sequence for the RISC pipeline without any forwarding or bypassing hardware but assuming a register read and a write in the same clock cycle "forwards" through the register file. Assume that the branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does this loop take to execute?

The five-stage pipeline includes:

i) Fetch(IF) – This is fetching the instruction from memory

ii)Decode(ID) – Decoding the instruction and reading the registers

iii)Execution(EXE) – ALU operates on operands prepared in the prior cycle

iv)Memory access (MEM) – If the instruction is a load,memory does a read and if it is a store,the memory does a write

v)Write Back Cycle(WB) – The result of the computation is written back to register

Instruction 1(loading from memory to R1) – Has no data hazard thus no stalling and all stages proceed from cycle 1 to 5

Instruction 2(DADDI) waits for the result of R1 ,leading to a data hazard but because there's no forwarding, it waits for instruction 1 to write back.

Instruction 3, (SD) stores R1 to memory and also waits for DADDI to write back,thus SD must stall until write back.

DADDI waits for SD to read R1 and not write to it.

DSUB depends on R2,thus a raw hazard,causing stalling.

BNEZ waits for R4 witten in DSUB

Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
LD	IF	ID	EXE	MEM	WB															
DADDI		IF	ID	stall	stall	EXE	MEM	WB												
SD			IF	stall	stall	ID	stall	stall	EXE	MEM	WB									
DADDI						IF	stall	stall	ID	EXE	MEM	WB								
DSUB									IF	ID	stall	stall	EXE	M	WB					
BNEZ										IF	stall	stall	ID	s	stall	EXE	MEM	WB		
LD													IF	s	s	F	D	X	M	W

- Loop runs for 99 iterations (396 / 4 = 99)
- Each iteration starts 15 cycles after the previous
  Total cycles = (98 * 15)
  = 1470 + 18
  = 1488 cycles.

b. Show the timing of this instruction sequence for the RISC pipeline with normal forwarding and bypassing hardware. Assume that the branch is handled by predicting it as not taken.

If all memory references take 1 cycle, how many cycles does this loop take to execute?

For this,data hazards are solved using forwarding.

LD has no data hazard,hence all the 5 stages(IF,ID,EXE,MEM,WB) will be smooth.

DADDI depends on LD result ,and it is forwarded after LD's write back to DADDI execution.

SD uses the result from DADDI thus waits for it to complete execution

DADDI R2,R2,4 experiences no data hazards,hence executes without stalls

DSUB uses R2 forwarded from DADDI and does not wait.

BNEZ uses results from DSUB which can be forwarded,causing a stall in ID stage.

Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14
LD	IF	ID	EXE	MEM	WB									
DADDI		IF	ID	stall	EXE	MEM	WB							
SD			IF	stall	ID	EXE	MEM	WB						
DADDI					IF	ID	EXE	MEM	WB					
DSUB						IF	ID	stall	EXE	MEM	WB			
BNEZ							IF	ID	stall	EXE	MEM	WB		
LD							IF	stall	IF	ID	stall	EXE	MEM	WB

Total cycles:

There are 98 iteration whereby each takes 9 cycles thus (98*9) = 883

Last iteration takes 12 cycles because the branch is taken. Thus total cycles:

= 882 + 12

= 894 cycles

c. Assume the RISC pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware. Schedule the instructions in the loop including the branch delay slot. You may reorder instructions and modify the individual instructions operands, but do not undertake other loop transformations that change the number or opcode of the instructions in the loops. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop.

Solution

For this,forwarding takes place.

Solution: Move the second DADDI to the load delay slot.

Inst	1	2	3	4	5	6	7	8	9	10	11
LD	IF	ID	EXE	MEM	WB						
DADDI R2,R2,4		IF	ID	EXE	MEM	WB					
DSUB			IF	ID	EXE	MEM	WB				
DADDI R1,R1,1				IF	ID	EXE	MEM	WB			
BNEZ					IF	ID	EXE	MEM	WB		
SD						IF	ID	EXE	MEM	WB	
LD							IF	IDl	EXE	MEM	WB

Number of cycles :

There are 98 iterations and each iteration takes 6 cycles and the last iteration takes 10 cycles

Thus number of cycles = ((98*6)+10)

No.of cycles = 598 cycles