Designing an effective N-bit single-layer shift register utilizing the JK Flip Flop employing QCA technology for applications in nano-communication.

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Abstract:

Quantum-dot Cellular Automata (QCA) is an exciting new technology that has a chance to transform nano communication systems because to its low power consumption and small size when compared with CMOS-enabled electronic devices. QCA is useful for digital logic architecture due to its faster operating speed, higher density, and reduced power dissipation. The task at hand is about designing circuits that are sequential with QCA. The research successfully designed an effective JK flip-flop and shown its utility in building 2-bit, 3-bit, 4-bit, and 8-bit shift registers that may be readily expanded up to N-bits using the identical flip-flop architecture. In addition, the designed JK flip-flop design's fault tolerance against single-cell addition and deletion errors is demonstrated. Through extensive evaluations of performance and energy dissipation study, it has been shown that the suggested layouts are less expensive and have lower energy dissipation. The QCA Designer program was used to validate all recommended sequential designs, verifying the designs' functionality and efficiency. In general, this research illustrates the potential of QCA in sequential circuit design, providing considerable gains in terms of speed, density, power consumption, and fault tolerance.

I. Introduction

The introduced QCA nanotechnology in 1993. Since then, it has become broadly used in the development of many digital logic circuits, such as adders and subtractors, flip-flops and related circuits, reversible logic layouts, memory, and code converters. The constraints associated with conventional semiconductor-based devices drive the use of QCA technology.

As standard semiconductor-based technique faces rising scale and complexity difficulties, the benefits of QCA technology becomes clear, particularly in the nano phase area. QCA technology outperforms CMOS technology in various ways, including lower area utilization, less excessive dissipation of energy, increased density, and small size. As a result, QCA has come to be as a promising approach for developing digital circuits at the sub-nano domain levels. QCA technology solves the needs of high concentration or small size, minimal energy dissipation, and rapid performance in the construction of nanophotonic circuits. It makes use of quantum dots to enable fast operation and other critical functions. Quantum dots, which are microscopic particles of semiconductors able to capturing electrons in quantization energy states, are essential components of computing machines. It is possible to build an automated cell capable of performing logic operations by organizing these quantum dots in a general fashion. A three-dimensional quantum isolation of electrons in the form of quantum dots confers unique foundational features, presenting them as possible essential constituents for future microelectronic and optical systems.

Fundamentals of QCA:

When contrasting with typical transistor-based systems, QCA nanotechnology functions on a distinct foundation. The underlying basis of QCA is interaction between cells rather than currentflow.A

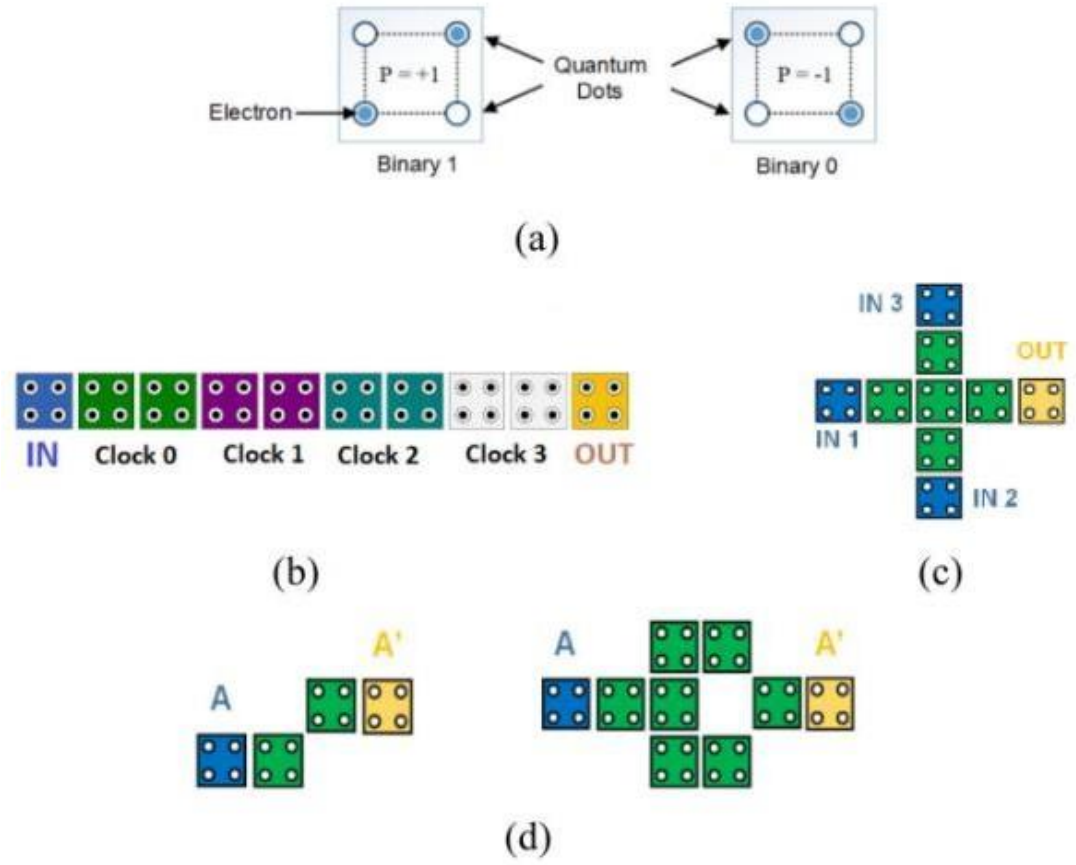

Fig 1: Schematic dig of QCA: a) Cells, b) Binary wire, c) 3 input majority vector gates, d) QCA inverter

Initially, the QCA cell, is made up of four possible holes known as quantum dots. These quantum dots enable two electrons to be arranged diagonally, reducing the attraction of electrostatics between them. As seen in Figure 1(a), this diagonally layout indicates two possible polarizations, binary 0 and binary 1.

A QCA binary cable is used to convey data. As shown in Figure 1(b), this wire is produced by joining QCA cells in an ordered arrangement. The binary wire, a three-input majority voter gate, and an inverter are the basic logic functions of QCA, as shown in Figures 1(b), 1(c), and 1(d). The 3 MV gate works on the basis of the Logical statement 3 MV (A, B, C) = AB + BC + CA, where A, B, C represent the corresponding inputs. Furthermore, an MV gate in QCA can function as both an AND an OR gate by setting one of its inputs to logic '0' and the other to logic '1'. In the creation of extremely massive circuits, complication can be minimized by adding crossovers into the building of binary wires. Interactions are classified as coplanar or multilayer in QCA. The parallel kind of interaction is widely used in design approaches because it allows the cells to live in only one direction, enabling the development procedure simpler and economical.

Clocking in QCA is the method of coordinating the processes of multiple cells inside a QCA circuit to ensure the effective functioning of QCA devices. It ensures that each cell has steady inputs and that each cell has enough time to conduct its logic function before the next cycle of the clock begins. In QCA, there are two techniques to clocking: static and dynamic.

Static clocking entails continuously sending a clock signal to the whole QCA circuit, forcing every cell to transition states in one time cycle. Although static clocking is easy to improve

Its acceleration is restricted by the propagating delay of contributes among cells. This approach works well for tiny QCA circuits but gets inefficient for bigger circuits.

In contrast, dynamic clocking applies the time signal to every cell separately, enabling every cell to change its state autonomously of all other cells within the circuit. This method allows for faster clock rates and minimizes connection latency. It entails introducing clock phases into the QCA circuit, with each of them used on a different subset of cells. Dynamic clocking produces faster clock cycles but necessitates more complicated circuit layout and operation.

A clock signal must be carefully designed in both static and dynamic clocking to ensure the best performance of the QCA circuit. The clock signal must be synced with the input data, supply enough voltage and time for changing cell states correctly, and avoid interaction with surrounding cells, which could cause to mistakes in the circuit's output.

The QCA Designer simulation tool is used for QCA circuit design and simulation. QCA Designer simulation waveform offers a graphical representation of the circuit's behavior across time. The procedures that follow are used to examine these waveforms:

• Signal recognition: Determining the input signals which control the circuit is the first stage in waveforms simulation evaluation. In the simulation waveform plots, such signals usually appear as square waves.

• Determination of output signals: The following step is to figure out the circuit's output signals. In the simulation waveform plots, such signals are often represented as another series of square waves.

• Signals comparisons among input and output: After the input and output signals have been determined, they can be examined to determine the functionality of the circuit. By contrasting the output signal to the input signal Anyone can analyze how the circuit reacts to an input signal, such as a clock signal.

• Timings and latency recognition: Detecting the timing and delays inside the circuit is another critical part of simulated waveform analysis. This involves estimating the delay in propagation between the input and output signals, in addition to detecting any setup and delay periods required for appropriate circuit operation.

• The identification of flaws and glitches: Simulated waveforms are useful to identify mistakes and glitches in a circuit. Unexpected transition or distortion in the output signal can suggest potential design flaws.

• Circuit adjustment and re-simulation: If any faults or issues are discovered throughout the analysis, changes to the circuit design can be performed. The circuit can now be used after the adjustments.

The use of flip flops in register shifts is extremely beneficial in the area of nano communication due to its versatility and adaptability in storing and moving data. These elements are crucial in digital circuits because they serve as basic components. Keeping this in mind, this work proposes JK Flip Flop, as well as 2-bit, 3-bit, 4-bit, and 8-bit Shift Registers, all of which are implemented utilizing QCA technology. These architectures can be easily scaled up to N-bits, providing an adaptable option for a variety of applications in the field.

II. Previous Work

A number of versions of JK Flip Flop circuits have been developed constructed using QCA nanotechnology. A JK-FF architecture with 90 cells and a delay of 1.50 clock cycles was built employing five 3-input majority voter gates and four inverters. Another method described in made use of six 3

Table 1: Evaluation of present JK-FF design.

Paper	Features	Drawbacks
[32]	No crossover	High Cell count Low Area utilization factor High QCA cost
[37]	Reduced cell area Reduced total area	High QCA cost High Latency
[36]	Improved Area utilization factor Reduced QCA cost	High Cell count Low speed
[35]	Improved area utilization factor Reduced cell area	High Power consumption
[36]	Reduced cell count	Low speed High power consumption
[34]	Reduced QCA cost Reduced Cell area	High latency
[33]	Reduced cell count Improved area utilization factor	High power consumption High latency Low speed
[31]	Low cell count Reduced cell and total area	Low area utilization factor High latency

Majority vector gates and two inverters, with 78 cells and a time cycle delay of 1.75 cycles. presented a JK-FF architecture with three five input majority voter gates, two inverters, 78 cells, and an average of one clock cycle. Furthermore, demonstrated a JK- FF architecture with four 3 MV gates, three inverters, 75 cells, with a delay of 1.25 clock cycles. Another JK-FF system presented in [36] used three 3 MV gates, two inverters, 57 cells, and a response time of one clock cycle. The majority voter gate-based JK-FF design was used, which included four 3 Majority Vector gates, two inverters, a cell count of 54 cells, and a delay of 1.25 clock cycles. Demonstrated two JK-FF layouts with number of cells of 45 and 30. The first design used three 3 MV gates and two inverters to achieve a response time of 1.50 clock phases, whereas the second used three 3 MV gates along with a single inverter to achieve a delay of 1.25 clock seconds. Finally, a JK-FF design with three 3 MV gates, four inverters, a cell count of 26 cells, and a latency of 1.25 clock cycles was created. Table 1 summarizes the current JK-FF designs, demonstrating that every concept has drawbacks. As a result, this research proposes a minimal latency JK-FF architecture that uses minimum majority voter gates and inverters while overcoming the drawbacks of prior systems.

III. Designing of JK Flip Flop

A JK Flip Flop is an analog circuit that determines its individual output by using both the present input and its prior output. Despite the SR Flip Flop, the JK Flip Flop solves its constraints through the addition of two further inputs: J and K, which function as the SR Flip Flop's set and reset inputs. Whenever either the J and K inputs are set to 1, the JK Flip Flop's output toggles or changes to the reverse position. Figure 2 depicts a block diagram of the JK Flip Flop.

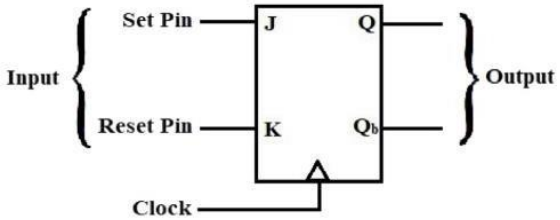

Fig 2: A block dig of JK-FF.

Table 2: JK-FF Truth Table.

J	K	Q	State
0	0	Q	Memory (no change)
0	1	0	Resest Q to 0
1	0	1	Sets Q to 1
1	1	–	Toggles

Table 3: JK-FF Excitation Table.

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

JK Flip Flop Design Based on QCA

We present an improved JK Flip Flop circuit in QCA in the present work, based on the equation:

$$Q = \bar{K}Q + J\bar{Q}$$

The mathematical representation of the proposed JK Flip Flop, that relies on a majority voter gate, is depicted in Figure 3. Three 3-input majority voter gates and two inverters are used in the layout.

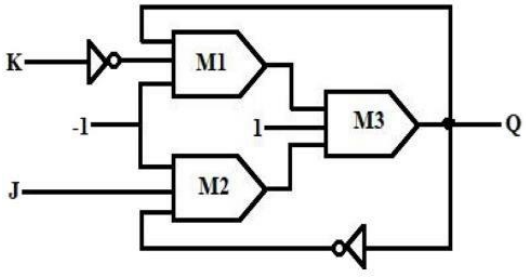

Fig 3: Demonstrated JK-FF logical structure relies on the majority vector.

The outputs of the majority voter gate M1 and M2 are sent into the M3 gate, which is an OR gate. The intended output is created by mixing both of these inputs. The output equation can be written in terms of the majority gate design as follows:

$$Q(output) = M\{M\{\bar{K}Q, -1\}, M\{J, \bar{Q} - 1\}, 1\}$$

The figures 4 and 5 demonstrate the QCA architecture and simulation waveform for the suggested JK Flip Flop device, exhibiting all feasible input pairings. The x-axis in Figure 4(b) depicts the sample's number, and the y-axis represents polarizationamplitude.

Various input, output, and clock signals are used. Additionally, the simulation outcomes were checked utilizing the truth table given in Table 2 and the QCA Designer simulation tool. The suggested JK flip-flop design according to QCA employs a total of 19 QCA cells with a cell area of 0.0061μm² and a total area of 0.0154μm². This equates to an area utilization factor (A.U.F) of 39.75%. The design has a delay of one cycle and a QCA cost of 0.0154. The QCA cost is calculated through multiplying the square of the latency by the whole area.

Fig 4: QCA design of JK-FF.

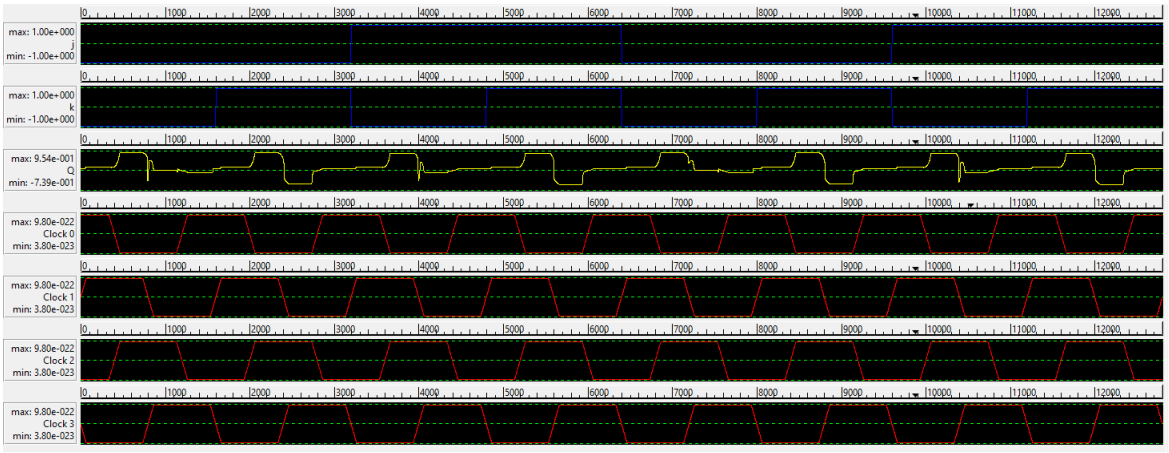

Fig 5: Outcomes of simulation.

Analysis of Fault Tolerance

Figure 6 shows a grid diagram that is utilized to define particular positions wherein cells can be inserted or removed in order to analyze the fault tolerance of the recommended JK Flip Flop design.

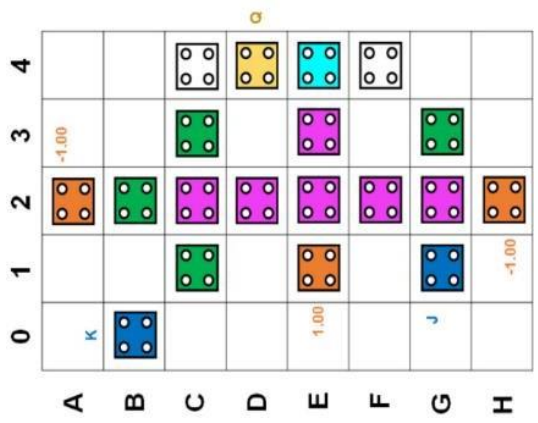

Fig 6: Grid dig explanation of proposed JK-FF

Table 4 displays the inaccurate reports and faults created for different testing vectors in single missing cell defect analysis. The fault tolerance has been calculated by computation to be (52-12) 100/52 = 76.92%. As a result, the suggested design has a fault tolerance of 76.92% for single missing cell errors.

Table 4: Fault Analysis of proposed JK-FF to single missingcell defect.

Input test vector	Total possible test	Total faults	Fault coverage
00	13	2	16.66%
01	13	1	8.33%
10	13	9	75%
11	13	0	0%
Total	**52**	**12**	**100%**

Table 5 shows the fault safeguards and faults found for various test vectors in single cell addition defect analysis. The fault tolerance is calculated to be (84- 6) 100/84 = 92.85%. As a result, the suggested design has a fault tolerance of 92.85% for single cell addition faults.

Table 5: Fault Analysis of proposed JK-FF to single cell addition defect.

Input test vector	Total possible test	Total faults	Fault coverage
00	21	2	33.33%
01	21	0	0%
10	21	4	66.66%
11	21	0	0%
Total	**84**	**6**	**100%**

IV. Proposed QCA based shift registers

A shift register is a digital circuit that stores and shifts an array of binary information. Amongst the different types of flip-flop circuits available, shift registers based on JK flip-flops offer multiple benefits over others. These advantages include:

1. Flexibility: JK flip-flops can be employed in a variety of modes, including S-R, T, and D flip-flops, enabling versatility for a wide range of operations.
2. Fast functioning: JK flip-flops operate quicker than other flip-flop kinds, which makes them suited for applications that require high speed.
3. Lower energy intake: Because JK flip-flops require less power, they are appropriate for battery-operated systems.
4. Simplicity of usage: Because JK flip-flops have a simple and easy construction, they are suited for use in simple circuits.
5. Synchronized functioning: JK flip-flops can be transmitted sequentially to produce a synchronous shift register, allowing for clock signal synchronization.
6. Bi-directional shifting capability: JK flip-flops can be built to enable data to be moved either left or right, meeting the needs of various applications.
7. Identification of errors and correcting: By integrating parity bits, JK flip-flops can be used for identifying and correcting errors in data transfer.

Overall, because of their adaptability, high-speed operation, and low power consumption, JK flip-flop-based shift registers are frequently used in digitalcircuitry.

utilization, as well as usability. They are used in the storage of data, data transfer, and sequence production. We suggest multi-bit shift registers in this research, based on the established JK Flip Flop design.

Shift Register with 2 bits

Figure 7 shows the block architecture and logic structure for the proposed 2-bit Shift Register using majority voter gates. The layout consists of two JK Flip Flops, with the first Flip Flop's output serving as the input for the second Flip Flop. Q1 is the ultimate result, while Q0 is the intermediate value. Six majority gates (M1, M2, M3, M4, M5, M6) and three inverters are used in the design.

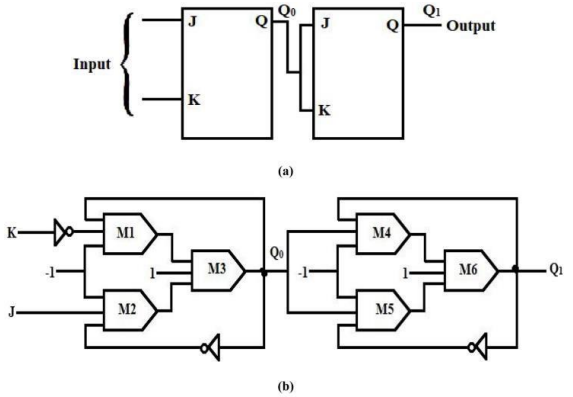

Fig 7: Shift Register with 2 bits a) Block dig and b) Majority voter-based logic utilizing JK-FF.

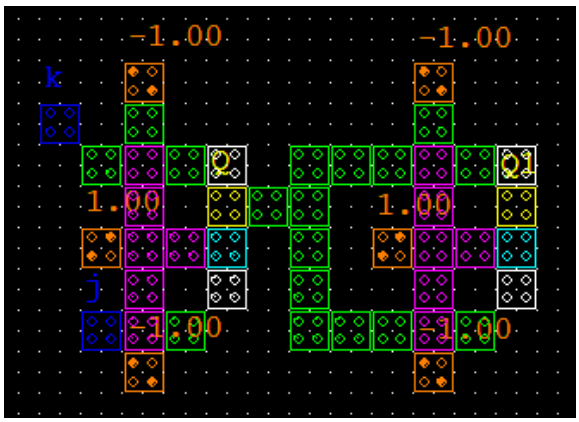

Fig 8: QCA design of shift register with 2 bits.

Figures 8 and 9 depict the design and outcomes of the simulation, respectively. A combined total of 45 QCA cells are used in the suggested 2-bit Shift Register architecture using JK Flip Flop. The cells in question cover a total area of 0.0376µm2, with each one covering 0.0145µm2. The layout obtains a 38.76% area utilization factor (A.U.F) with a delayed of 2 clock cycles, corresponding to 8 clocking zones. The cost of QCA is computed as 0.1504.

Shift Register with 3 bits

Figure 10 depicts the suggested 3-bit Shift Register's block structure and majority voter gate-based logical architecture. Three JK flip flops are used in this design.

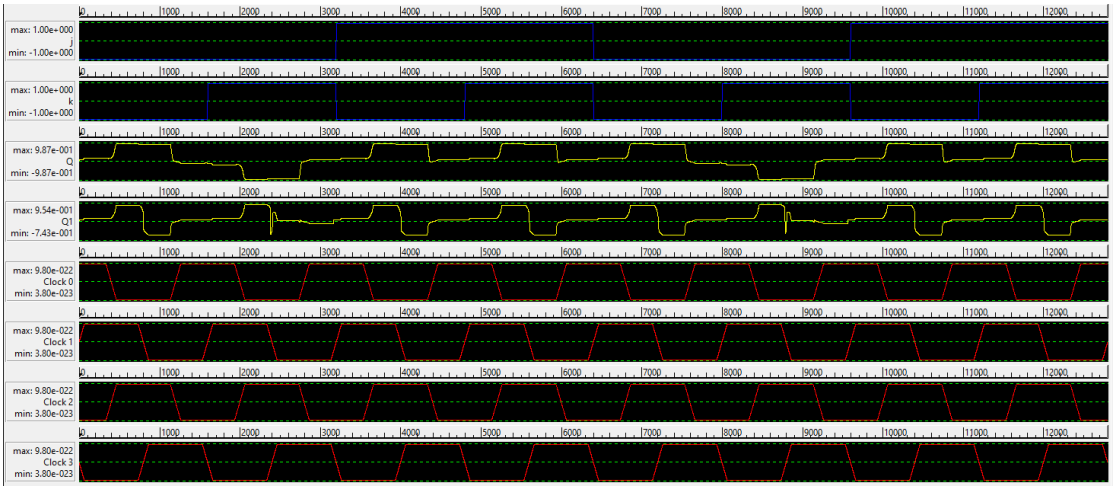

Fig 9: Outcomes of simulation.

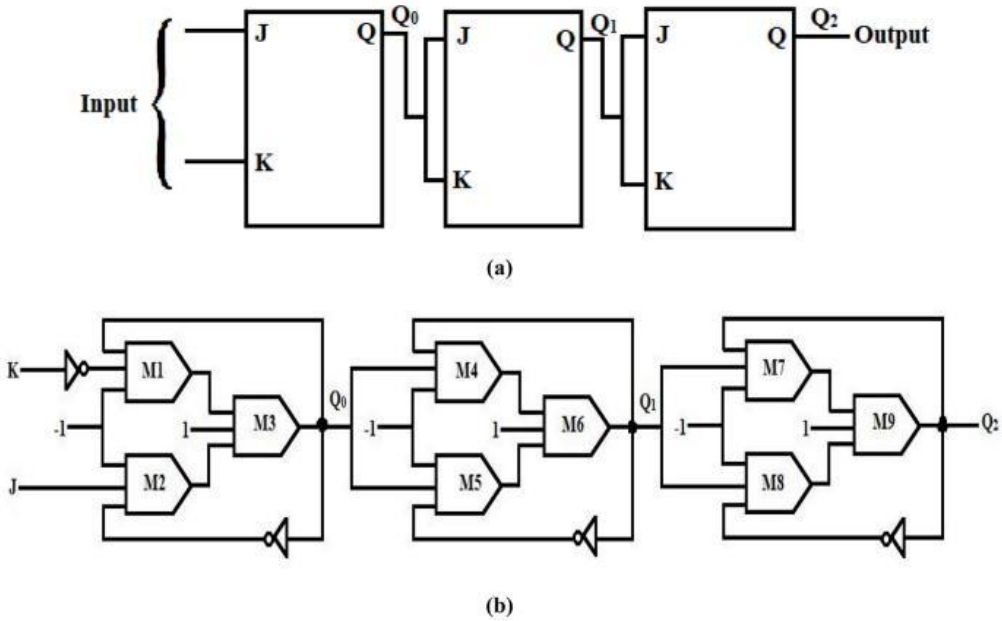

Fig 10: Shift Register with 3 bits a) Block dig and b) Majority voter-based logic utilizing JK-FF.

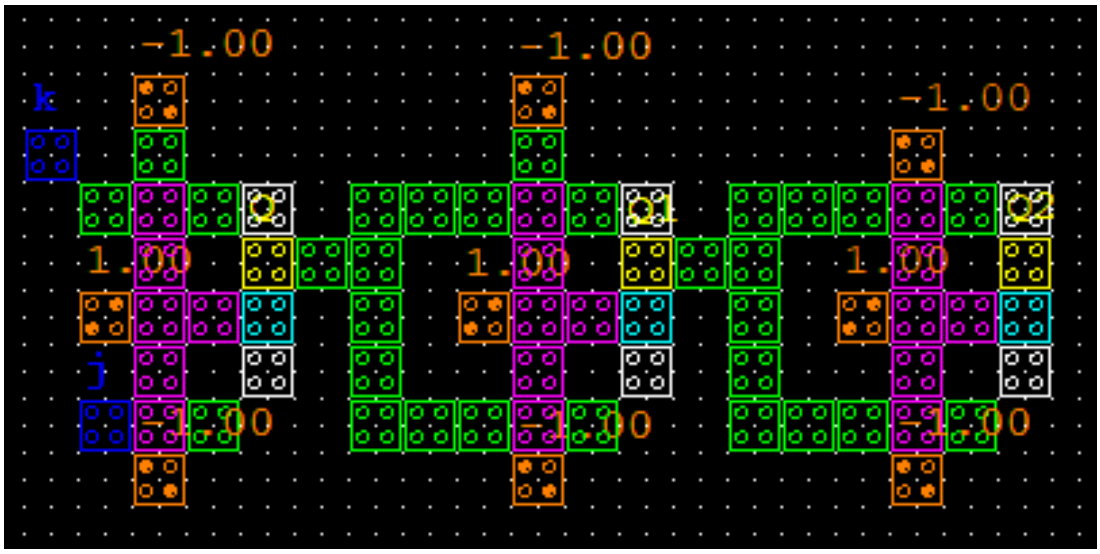

Fig 11: QCA design of shift register with 3 bits.

Figures 11 and 12 show a graphical illustration of the QCA configuration and simulated waveforms. The layout employs a total of 71 QCA cells with a total area of 0.0597μm2. Every cell has a surface area of 0.0230μm2, results in a 38.51% area utilization factor (A.U.F). The architecture has a duration of 3 clock cycles, which is the same as 12 clocking zones. This configuration's QCA cost has been determined as 0.5375.

Shift Register with 4 bits

Figure 13 depicts the suggested Shift Register with 4 bits block schematic and majority voter gate-based logical design. The layout features four JK flip flops.

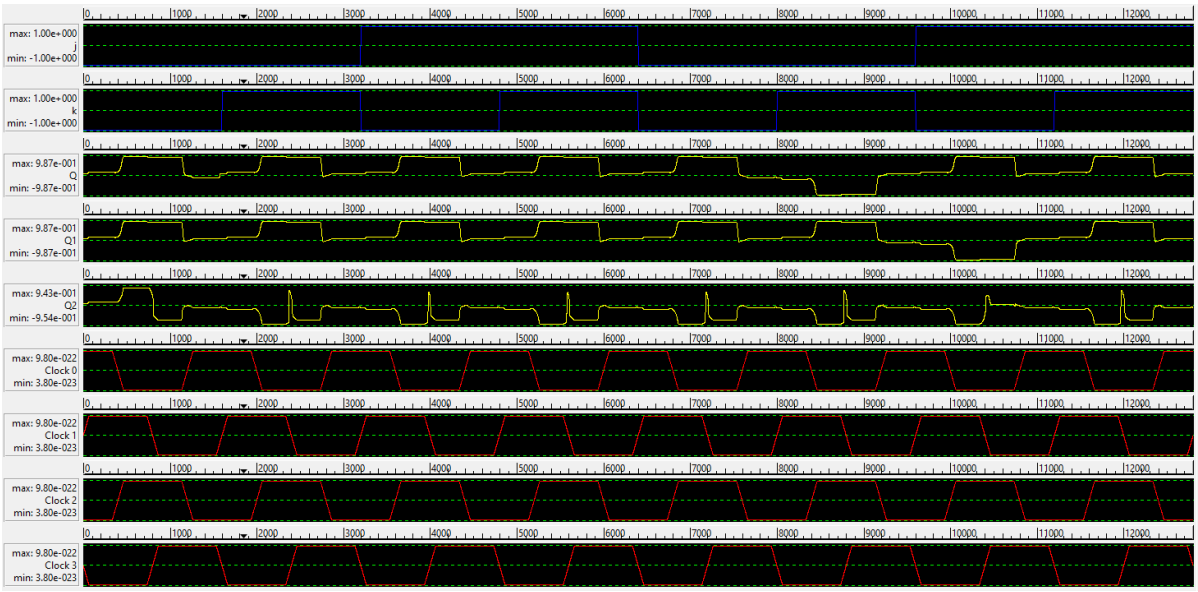

Fig 12: Outcomes of simulation.

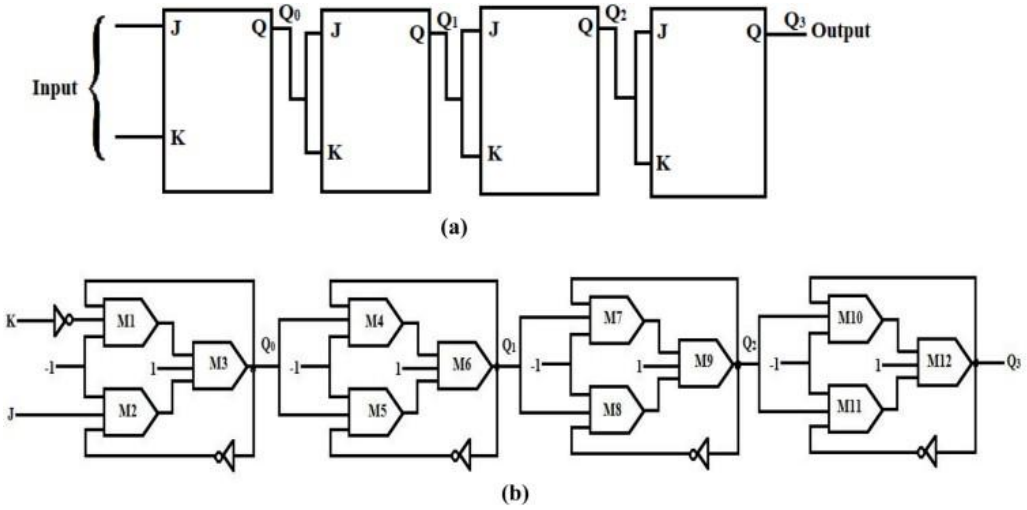

Fig 13: Shift Register with 4 bits a) Block dig and b) Majority voter-based logic utilizing JK-FF.

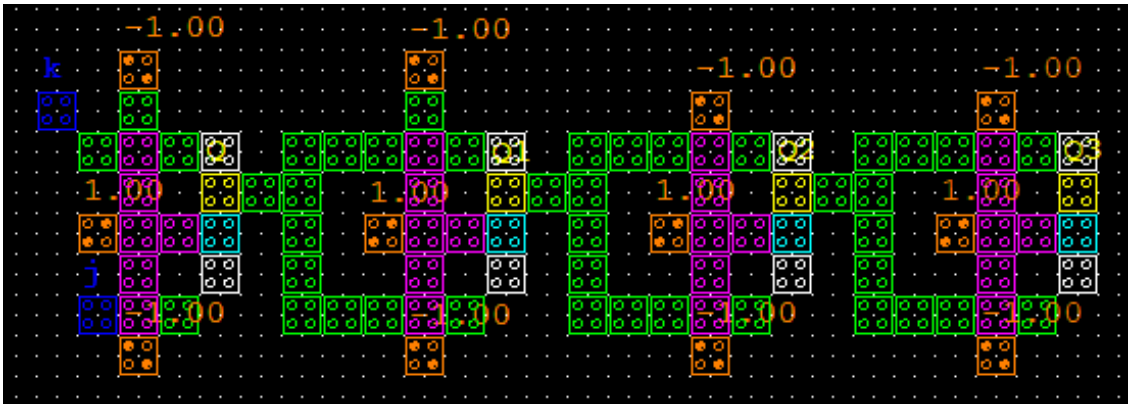

Fig14: QCA design of shift register with 4 bits.

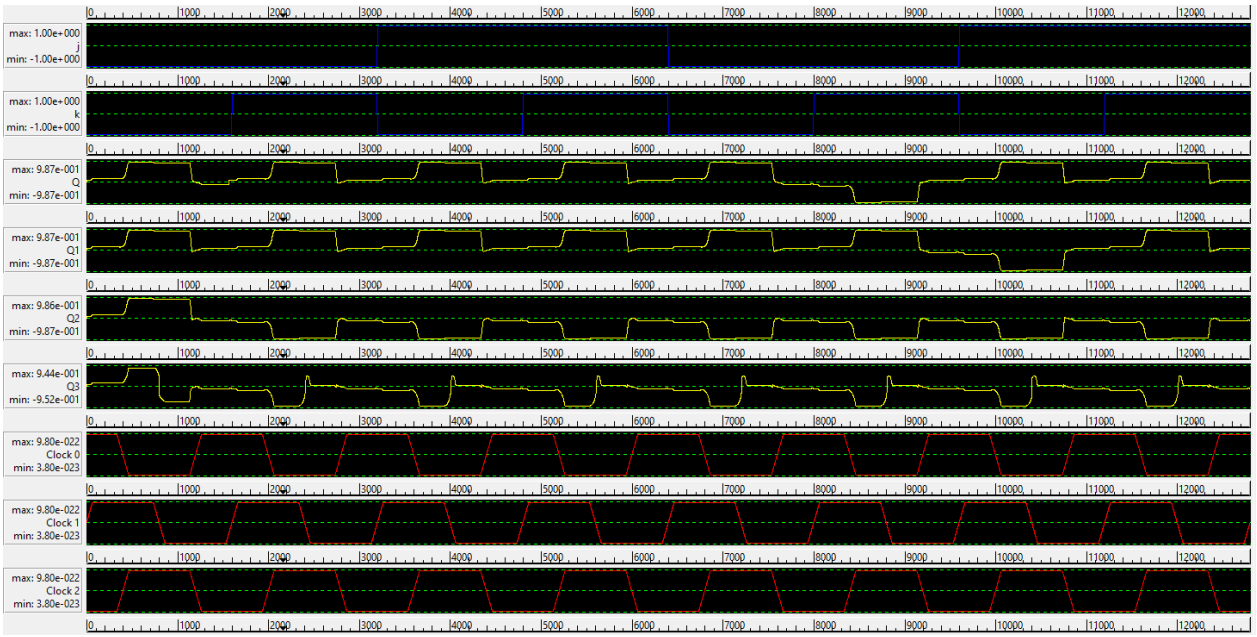

Fig 15: Outcomes of simulation.

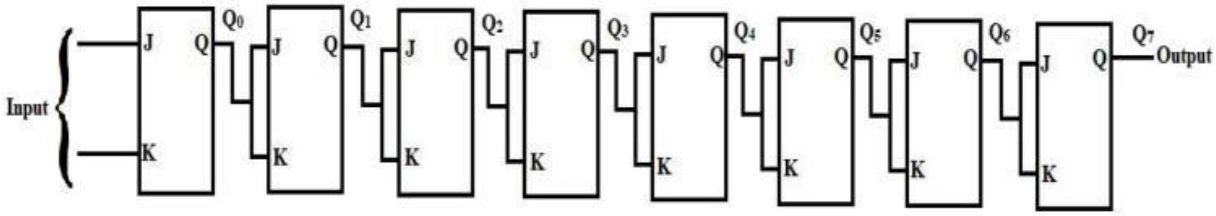

Fig 16: A block dig representation of shift register with 8 bits using JK-FF.

Shift Register with 8 bits:

The suggested 8-bit Shift Register, that consists of eight JK flip flops, is seen in Figure 16.

Figure 17 depicts the associated QCA layout. There are a total of 97 elements in this design.

QCA cells were used, covering a total surface of 0.1703 µm2. Each of the cells has a surface area of 0.0651 µm2, leading to an area utilization factor (A.U.F.) of 38.23%. The architecture has an 8-clock cycle lag, which corresponds to 32 clocking zones. This configuration's QCA cost has been determined as 10.9007.

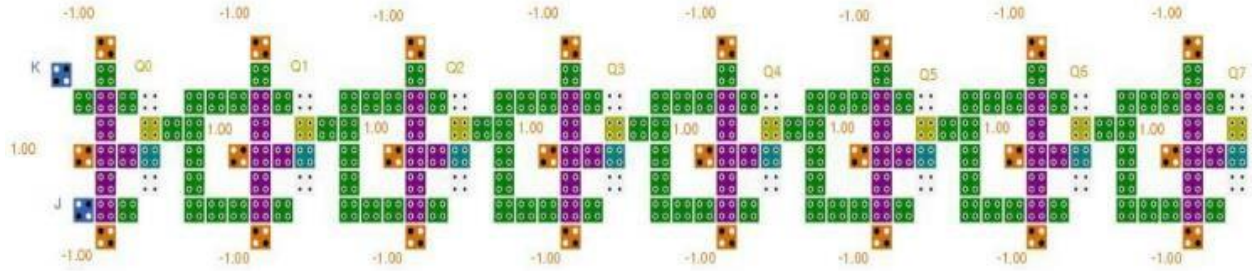

Fig 17: shift register with 8 bits QCA layout.

Table 6: JK-FF operating parameters for the suggested shift registers.

Proposed shift register	Cell count	Cell area (μm^2)	Total area (μm^2)	Latency	A.U.F. (%)	QCA cost
2-bit	45	0.0145	0.0376	2	38.76%	0.1504
3-bit	71	0.0230	0.0597	3	38.51%	0.5375
4-bit	97	0.0314	0.0818	4	38.39%	1.3095
8-bit	201	0.0651	0.1703	8	38.23%	10.9007
N-bit	(N*26)-7	C.A. = [(N*26)-7]*324	T.A. = [140N-42]*158	N	C.A/T.A	[140N-42]*158*N^2

It's important to note that these structures can be expanded to support N bits. The suggested formulas in Table 6 can be used to calculate the performance metrics of an N-bit shift register.

V. Discussions:

Shift Registers have previously been accomplished via D Flip Flops. However, the primary objective of this effort has been on creating Shift Registers based on JK Flip Flops. We examined the JK Flip Flop and the 4-bit Shift Register in order to contrast their performance, and the findings are shown in Tables 7 and 8, accordingly. Particularly, the JK Flip Flop design suggested in this work has a smaller number of cells in the layout and a significantly reduced cell count in the layout. QCA price was lowered in comparison to other designs identified in the research.

We used the QCA Pro tool to evaluate the suggested designs' dissipation of energy. The approximation method is used in this probabilistic simulation tool to detect cells with irregular power flow. On the diagram, a darker cell implies greater power dissipation, whereas a white cell denotes an input cell.

The power consumption performance of the suggested QCA architectures for the JK Flip Flop and Shift Registers are shown in Tables 9 and 10, respectively. The findings show that every single one of these QCA-based systems use a smaller amount of energy than conventional designs.

Table 7: A evaluation of present and future JK-FF designs.

JK Flip-flop designs	Total cells	Total area (μm^2)	Cell area (μm^2)	Area utilization factor (A.U.F.)	Latency	QCA cost
[45]	329	0.39	0.1066	27.33%	1.25	0.6094
[46]	274	0.29	0.0887	30.58%	1	0.29
[47]	234	0.347	0.0758	21.85%	3.5	4.25
[48]	132	0.1584	0.04277	27%	1.25	0.2475
[49]	120	0.146	0.0388	26.57%	2	0.584
[32]	90	0.0975	0.0291	29.84%	1.50	0.2193
[50]	80	0.12	0.0259	21.58%	1.25	0.1875
[37]	78	0.0717	0.0252	35.23%	1.75	0.2196
[36]	78	0.0665	0.0252	37.89%	1	0.0665
[35]	75	0.0768	0.0243	31.64%	1.25	0.1201
[36]	57	0.0518	0.0184	35.59%	1	0.0518
[34]	54	0.0518	0.0174	33.72%	1.25	0.0810
[33]	45	0.0388	0.0145	37.57%	1.50	0.0873
[51]	39	0.0416	0.0126	30.28%	0.5	0.0104
[33]	30	0.0300	0.0097	32.52%	1.25	0.0470
[31]	26	0.0312	0.0084	26.93%	1.25	0.0487
Proposed Design	19	0.0154	0.0061	39.75%	1	0.0154

Table 8: Examination of shift register with 4 bits layout using JK-FF.

4-Bit shift register	Total cells	Total area (μm^2)	Cell area (μm^2)	Area Utilization Factor (AUF)	Latency	Cost
[52]	234	0.4755	0.0758	15.94%	4	7.6083
[53]	173	0.1851	0.0560	30.27%	4.25	3.3444
Proposed	97	0.0850	0.0314	36.95%	4	1.3608

Table 9: Examination of low power energy between current and future JK-FF systems

JK Flip Flop	Avg. leakage (meV)			Avg. switching (meV)			Total (meV)		
	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek
[51]	20.57	23.89	45.79	28.86	28.98	34.89	49.43	52.87	80.68
[45]	95.07	298.91	543.04	554.39	480.30	407.70	649.46	779.21	950.74
[46]	89.34	261.64	460.76	420.48	367.99	318.64	509.82	629.63	779.40
[48]	43.21	127.39	226.58	62.07	53.83	45.85	105.28	181.22	272.43
[49]	35.48	109.72	197.39	182.55	158.05	134.4	218.03	267.77	331.79
[50]	32.68	103.77	189.04	203.73	177.7	152.21	236.41	281.47	341.25
Proposed	6.8	18.56	31.47	16.48	13.69	11.39	23.28	32.25	42.86

Table 10: Analysis of low power energy of the proposed JK-FF based registers

Shift registers	Average leakage (meV)			Average switching (meV)			Total (meV)		
	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek
4-bit [51]	130.98	140.91	184.69	145.87	132.89	120.67	276.85	273.8	305.36
Proposed 2-bit	16.05	44.63	76.82	44.91	38.38	32.54	60.96	83.01	109.36
Proposed 3-bit	25.8	71.44	122.97	53.12	45.02	37.94	78.92	116.46	160.91
Proposed 4-bit	35.39	97.92	168.73	53.13	45.05	37.99	88.52	142.97	206.71

previous designs, implying that they may be suitable for ultra-low power applications.

VI. Conclusion

This study provides an extremely effective QCA-based JK Flip Flop architecture and suggests its use in Shift Registers. The recommended architectures' scalability enables for easy integration of bigger N-bits. The efficiency of these designs was tested by simulations utilizing the QCA Designer simulated tool, and their layouts and functions were determined to be successful. Our suggested logic structures in QCA reveal considerable savings in cell count, area, latency, and cost, owing mostly to their compactness.

Additionally, despite single-cell missing and addition defects, the Flip Flop design proposed in this study has fault tolerance rates of 76.92% and 92.85%, respectively. Furthermore, the proposed designs have low energy dissipation, which renders them suitable for fast speeds and low-power usage. As a result, these

The proposed designs bring up new avenues for building more complex and more sophisticated sequenced circuits.

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