G Veerasakthi

Coimbatore,India
+91-9597498418 ganesan.veerasakthi@gmail.com G Veerasakthi

EDUCATION

Amrita Vishwa Vidaypeetham **2021 – 2025**
B.Tech Electronics and communication Engineering - ***6.2 / 10*** *Coimbatore, India*

Maharishi Vidya Mandir **2007 – 2019**
Class 10 - PCM - ***Percentage*** - ***74.8%*** *Chennai, India*

Kola Saraswathi Vaishnav **2019 – 2021**
Class 12 - PCM - ***Percentage*** - ***80.4%*** *Chennai, India*

EXPERIENCE

GFR Robots – Power Electronics Design Intern **11 2024 – Present**

- Design and Integration: Assist in designing and integrating circuits for power distribution, motor control, buck converters, motor drivers and LIDAR.
- Circuit Testing: Perform testing to ensure the proper functioning of electrical components and systems.
- Power Management: Work on optimizing power efficiency and management across various circuits and systems.
- Hands-on Work: Gain experience with hardware tools, circuit design, and system integration.
- Collaboration: Work closely with senior engineers to solve technical challenges and improve circuit designs.
- Troubleshooting: Identify and address issues related to circuit functionality and performance.

PROJECTS

Role: Power Electronics Designer: – **11 2024 – Present**

- **Farm Robotics Challenge (Autonomous Agricultural Drone Development):** Designed and integrated the power distribution system for motors, sensors, and flight control.
- Developed a battery management system (BMS) to monitor performance and ensure efficient power use.
- Power Management: Work on optimizing power efficiency and management across various circuits and systems.
- Implemented power-saving algorithms and thermal management to ensure reliable operation in field conditions.
- Worked with DC-DC converters for efficient power regulation.
- Troubleshooting: Identify and address issues related to circuit functionality and performance.

ISRO Robotics Challenge 2024: **11 2023 - 07 2024**

- Developed an autonomous rover with a robotic arm designed for sample retrieval missions, capable of climbing and navigating through obstacles. The rover utilizes an RGBD camera and a 360° camera for obstacle avoidance and object detection.
- Defined rover architecture by identifying key components and their roles in the system.
- Collaborated with the team to select appropriate components and determine their specifications to meet the rover's performance goals.
- Conducted power and current consumption analysis for each component to ensure efficient energy use.
- Ensured compatibility between components and optimized power distribution to maintain system stability.
- Troubleshooting: Identify and address issues related to circuit functionality and performance.

Optimized Viterbi decoder architecture: A precomputed table approach for BMU **07 2024 - Present**

- Designed conventional and modified Viterbi decoder architectures to enhance error correction performance.
- Proposed an advanced optimization technique to further reduce power consumption beyond the capabilities of recent architectures.
- Integrated the new optimization technique into the modified Viterbi decoder to evaluate its effectiveness.
- Performed power analysis using suitable simulation software to validate the improvements in energy efficiency.

Electronic Harmonium: **01 2024 - 07 2024**

- Recreated the sound of a traditional harmonium using a 555 timer IC to generate specific audio frequencies for each musical note.
- Implemented a keyboard interface to trigger the 555 timer IC for generating desired frequencies when a key is pressed.
- Amplified the output signal to produce audible sound through a speaker.
- Eliminated the need for manual air pumping, making the instrument portable and stable.
- Maintained the characteristic tones of a traditional harmonium while ensuring ease of use.

4 BIT Arithmetic Logic unit: **01 2024 - 07 2024**

- Designed and implemented a 4-bit Arithmetic Logic Unit (ALU) using VHDL, capable of performing various operations based on a 4-bit opcode.
- Developed modules for key arithmetic functions including addition, subtraction, multiplication, and division.
- Incorporated bitwise logic operations such as AND, OR, NAND, NOR, and XNOR.
- Implemented shift and rotation operations, including left and right shifts.
- Deployed the ALU design on a Basys FPGA board for real-time performance.
- Verified functionality through extensive simulation and real-world testing to ensure accuracy and reliability.

Security System with 4-Bit BCD Adder Access Control: **01 2022 - 07 2022**

- Developed a 3-bit binary login code and a 2-bit password input for user authentication.
- Implemented access control to allow only four authorized users based on correct login credentials.
- Designed a 4-bit Binary Coded Decimal (BCD) adder accessible upon successful authentication.
- Ensured unauthorized users received a default output of zero from the BCD adder.
- Integrated a seven-segment display to visually output the results of the BCD adder.
- Included an LED indicator to signal a carry output from the adder, providing clear feedback to users.

TECHNICAL SKILLS

Languages: Python, C
Tools: LT Spice, Proteus, Vivado, Synopsys, Spyder IDLE, Ansys HFSS, Yolo V4
Hardware Experience: Power Electronics, Battery, Analog Electronics, Linear Integrated circuits, Digital Circuits, VLSI Boards(Basys), Embedded Boards(LPC2148)

CERTIFICATIONS

- Electronics Cars–Workshop Amrita
- Robotics–Teachnook
- Bio-Medical Signal processing–Workshop Amrita