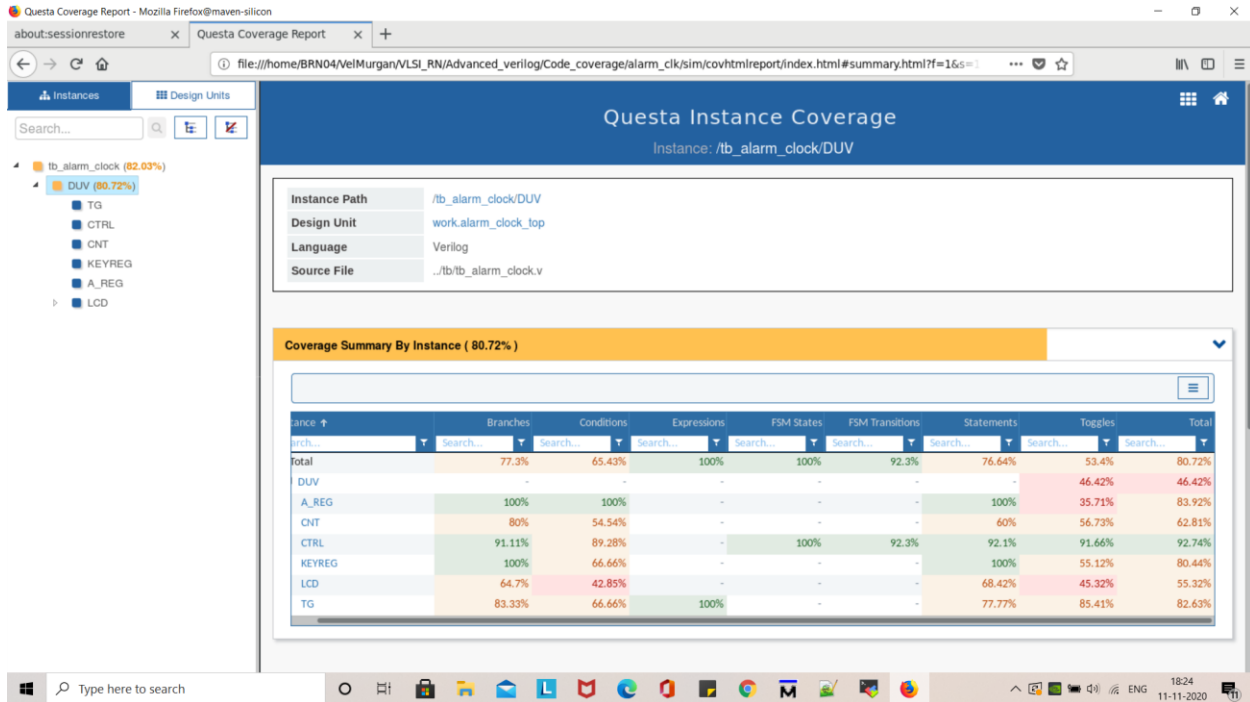
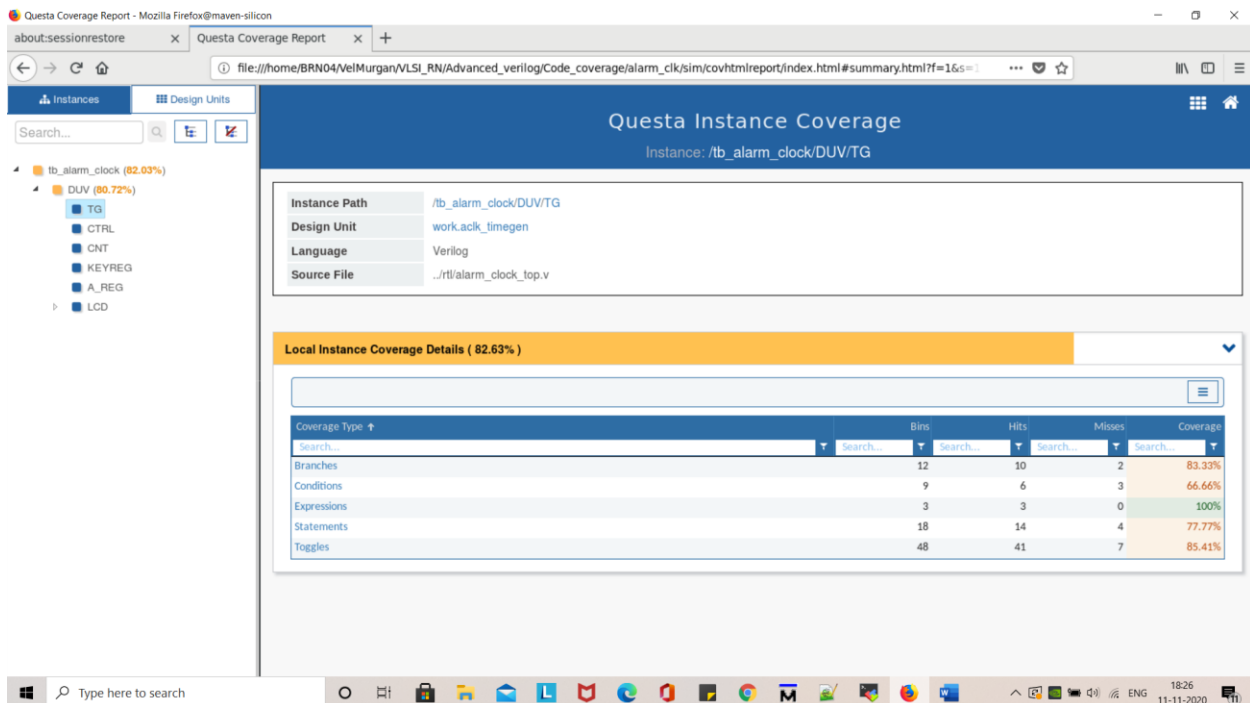


# Alarm Clock Coverage

## DUV Total:



## Timing Generator:



## Aclk\_Controller:

Questa Coverage Report - Mozilla Firefox@maven-silicon

about:sessionrestore x Questa Coverage Report x +

file:///home/BRN04/VelMurgan/VLSI\_RN/Advanced\_verilog/Code\_coverage/alarm\_clk/sim/covhtmlreport/index.html#summary.html?f=16&s=

Instances Design Units

Search...

- tb\_alarm\_clock (82.03%)
  - DUV (80.72%)
    - TG
    - CTRL
    - CNT
    - KEYREG
    - A\_REG
    - LCD

### Questa Instance Coverage

Instance: /tb\_alarm\_clock/DUV/CTRL

Instance Path: /tb\_alarm\_clock/DUV/CTRL  
Design Unit: work.aclk\_controller  
Language: Verilog  
Source File: ../rtl/alarm\_clock\_top.v

#### Local Instance Coverage Details ( 92.74% )

Coverage Type	Bins	Hits	Misses	Coverage
Branches	45	41	4	91.11%
Conditions	28	25	3	89.28%
FSM States	7	7	0	100%
FSM Transitions	13	12	1	92.3%
Statements	38	35	3	92.1%
Toggles	60	55	5	91.66%

## Aclk\_Counter:

Questa Coverage Report - Mozilla Firefox@maven-silicon

File Edit View History Bookmarks Tools Help

about:sessionrestore x Questa Coverage Report x +

file:///home/BRN04/VelMurgan/VLSI\_RN/Advanced\_verilog/Code\_coverage/alarm\_clk/sim/covhtmlreport/index.html#summary.html?f=16&s=

Instances Design Units

Search...

- tb\_alarm\_clock (82.03%)
  - DUV (80.72%)
    - TG
    - CTRL
    - CNT
    - KEYREG
    - A\_REG
    - LCD

### Questa Instance Coverage

Instance: /tb\_alarm\_clock/DUV/CNT

Instance Path: /tb\_alarm\_clock/DUV/CNT  
Design Unit: work.counter  
Language: Verilog  
Source File: ../rtl/alarm\_clock\_top.v

#### Local Instance Coverage Details ( 62.81% )

Coverage Type	Bins	Hits	Misses	Coverage
Branches	10	8	2	80%
Conditions	11	6	5	54.54%
Statements	20	12	8	60%
Toggles	104	59	45	56.73%

## Aclk\_KeyReg:

Questa Coverage Report - Mozilla Firefox@maven-silicon

File Edit View History Bookmarks Tools Help

about:sessionrestore x Questa Coverage Report x +

file:///home/BRN04/VelMurgan/VLSI\_RN/Advanced\_verilog/Code\_coverage/alarm\_clk/sim/covhtmlreport/index.html#summary.html?f=16s=1

Instances Design Units

Search...

tb\_alarm\_clock (82.03%)

DUV (80.72%)

- TG
- CTRL
- CNT
- KEYREG
- A\_REG
- LCD

Questa Instance Coverage

Instance: /tb\_alarm\_clock/DUV/KEYREG

Instance Path: /tb\_alarm\_clock/DUV/KEYREG

Design Unit: work.keyreg

Language: Verilog

Source File: ../rtl/alarm\_clock\_top.v

Local Instance Coverage Details ( 80.44% )

Coverage Type	Bins	Hits	Misses	Coverage
Branches	3	3	0	100%
Conditions	3	2	1	66.66%
Statements	9	9	0	100%
Toggles	78	43	35	55.12%

## Aclk\_Alarm\_Reg:

Questa Coverage Report - Mozilla Firefox@maven-silicon

about:sessionrestore x Questa Coverage Report x +

file:///home/BRN04/VelMurgan/VLSI\_RN/Advanced\_verilog/Code\_coverage/alarm\_clk/sim/covhtmlreport/index.html#summary.html?f=16s=1

Instances Design Units

Search...

tb\_alarm\_clock (82.03%)

DUV (80.72%)

- TG
- CTRL
- CNT
- KEYREG
- A\_REG
- LCD

Questa Instance Coverage

Instance: /tb\_alarm\_clock/DUV/A\_REG

Instance Path: /tb\_alarm\_clock/DUV/A\_REG

Design Unit: work.alarm\_reg

Language: Verilog

Source File: ../rtl/alarm\_clock\_top.v

Local Instance Coverage Details ( 83.92% )

Coverage Type	Bins	Hits	Misses	Coverage
Branches	3	3	0	100%
Conditions	2	2	0	100%
Statements	6	6	0	100%
Toggles	70	25	45	35.71%

## Aclk\_Alarm\_LCD:

Questa Coverage Report - Mozilla Firefox@maven-silicon

File Edit View History Bookmarks Tools Help

about:sessionrestore x Questa Coverage Report x +

file:///home/BRN04/VelMurgan/VLSI\_RN/Advanced\_verilog/Code\_coverage/alarm\_clk/sim/covhtmlreport/index.html#summary.html?f=16s=1

Instances Design Units

Search...

tb\_alarm\_clock (82.03%)

DUV (80.72%)

- TG
- CTRL
- CNT
- KEYREG
- A\_REG
- LCD

### Questa Instance Coverage

Instance: /tb\_alarm\_clock/DUV/LCD

Instance Path: /tb\_alarm\_clock/DUV/LCD  
Design Unit: work\_lcd\_driver\_4  
Language: Verilog  
Source File: ../rtl/alarm\_clock\_top.v

#### Coverage Summary By Instance ( 55.32% )

Instance	Branches	Conditions	Statements	Toggles	Total
Total	64.7%	42.85%	68.42%	45.32%	55.32%
LCD	-	-	-	42.52%	42.52%
LS_HR	52.94%	42.85%	57.89%	40.74%	48.6%
LS_MIN	88.23%	42.85%	89.47%	62.96%	70.88%
MS_HR	52.94%	42.85%	57.89%	37.03%	47.68%
MS_MIN	64.7%	42.85%	68.42%	55.55%	57.88%

#### Local Instance Coverage Details ( 42.52% )

#### Recursive Hierarchical Coverage Details ( 55.32% )

Type here to search

18:31 11-11-2020