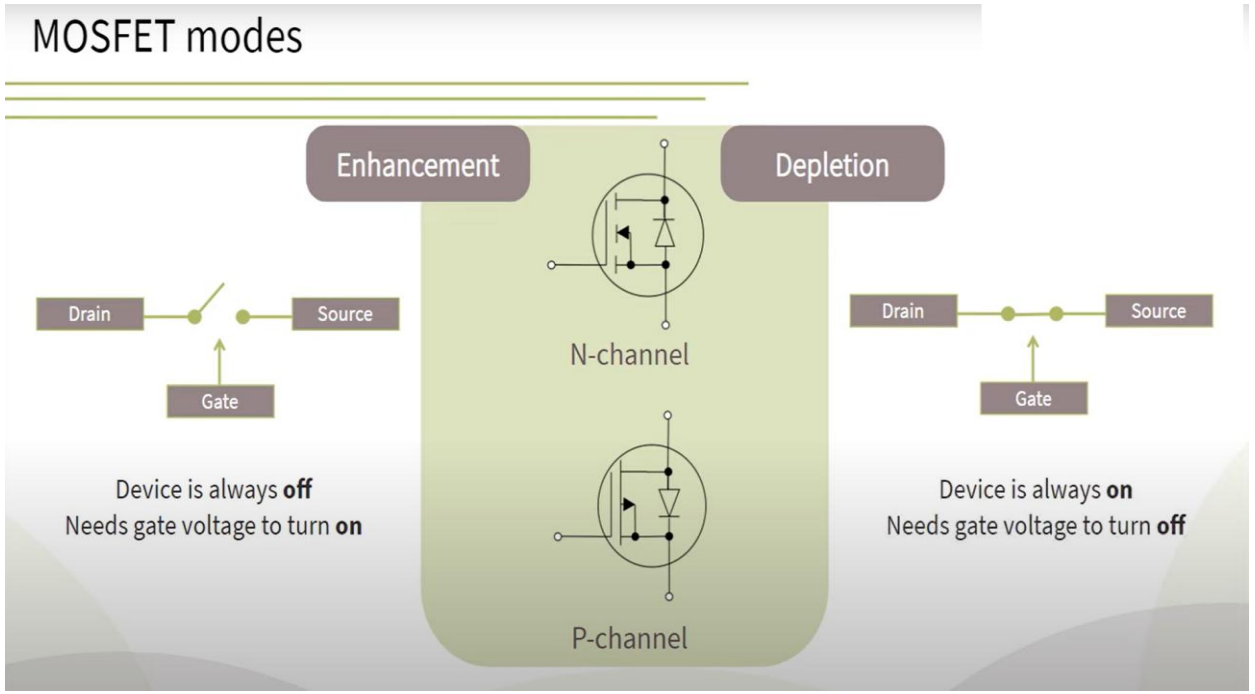
MOSFET

Jishnu Sankar VC
Assistant Professor
EEE Dept.
ASE Amritapuri

MOSFET: metal-oxide semiconductor FET

- The metal-oxide semiconductor FET, or MOSFET, has a source, gate, and drain.
- The MOSFET differs from the JFET, however, in that the gate is insulated from the channel.
- Because of this, the gate current is even smaller than it is in a JFET.
- There are two kinds of MOSFETs, the depletion-mode type and the enhancement-mode type.
- The enhancement-mode MOSFET is widely used in both discrete and integrated circuits.
  - In discrete circuits, the main use is in power switching, which means turning large currents on and off .
- In integrated circuits, the main use is in digital switching, the basic process behind modern computers.
  - Although their use has declined, depletion mode MOSFETs are still found in high-frequency front-end communications circuits as RF amplifiers.

Enhancement MOSFET	Depletion MOSFET
It is Normally OFF device at zero Gate to Source voltage	It is Normally ON device at zero Gate to Source voltage
At OFF condition it cannot conduct electrical current.	At OFF condition it can conduct electrical current.
Positive gate voltage (more than source voltage) is required to turn on this type of MOSFET	Negative gate voltage(less than threshold voltage) is required to turn off this type of MOSFET
In this type of MOSFET, the gate voltage directly proportional to the Drain Current.	In this type of MOSFET, the gate voltage Inversely proportional to the Drain Current.
There is no permanent channel; a temporary channel is produced when a voltage applied across it.	There is a permanent fabricated channel available. Generally, the N-Type channel
Enhancement MOSFET has leakage current and diffusion current concept.	Depletion MOSFET does not have any leakage current and diffusion current concept.
The advantage of Enhancement MOSFET is ultra-fast switching capability with high current conduction.	The advantage of Depletion MOSFET is, it can be used as a variable resistive load.



Power MOSFET

A power MOSFET is a voltage-controlled device and requires only a small input current. The switching speed is very high and the switching times are of the order of nanoseconds. Power MOSFETs find increasing applications in low-power high-frequency converters. MOSFETs do not have the problems of second breakdown phenomena as do BJTs. However, MOSFETs have the problems of electrostatic discharge and require special care in handling. In addition, it is relatively difficult to protect them under short-circuited fault conditions.

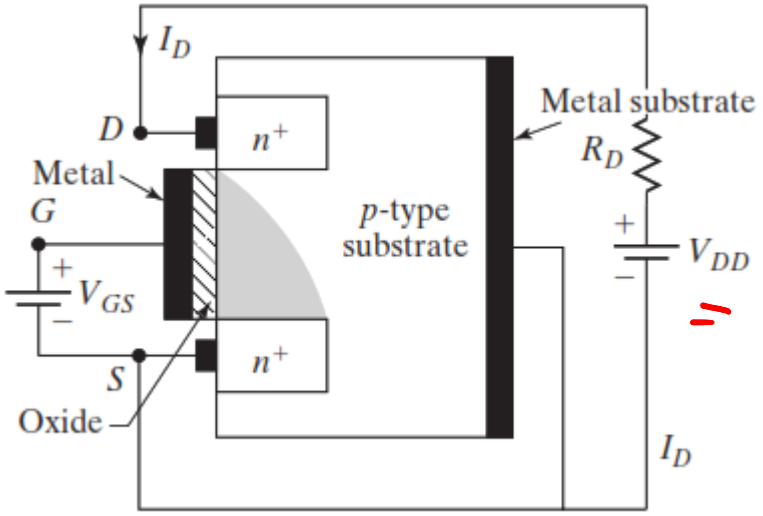
The two types of MOSFETs are (1) depletion MOSFETs and (2) enhancement MOSFETs

Second Breakdown in BJT

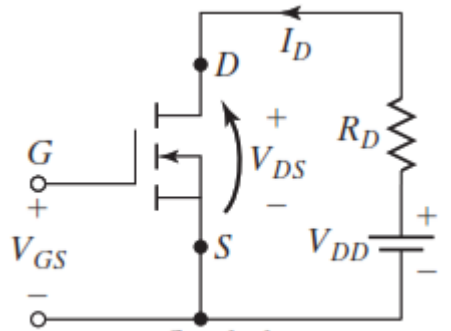
Second breakdown is a destructive failure mode in **Bipolar Junction Transistors (BJTs)** that occurs when the device is operating under **high voltage and high current conditions**. It is a type of **thermal runaway** but is distinct from regular junction overheating.

n-Channel enhancement-type MOSFET

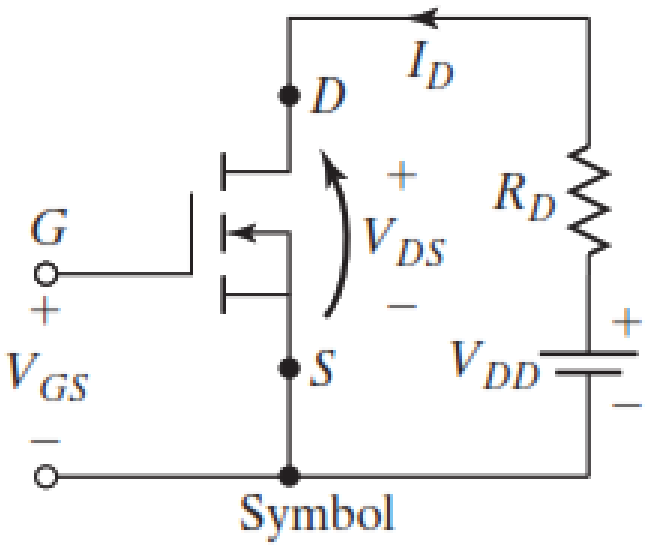
An *n*-channel enhancement-type MOSFET has no physical channel, as shown in Figure 4.2a. If V_{GS} is positive, an induced voltage attracts the electrons from the *p*-substrate and accumulates them at the surface beneath the oxide layer. If V_{GS} is greater than or equal to a value known as *threshold voltage* V_T, a sufficient number of electrons are accumulated to form a virtual *n*-channel, as shown by shaded lines in Figure 4.2a, and the current flows from the drain to source.

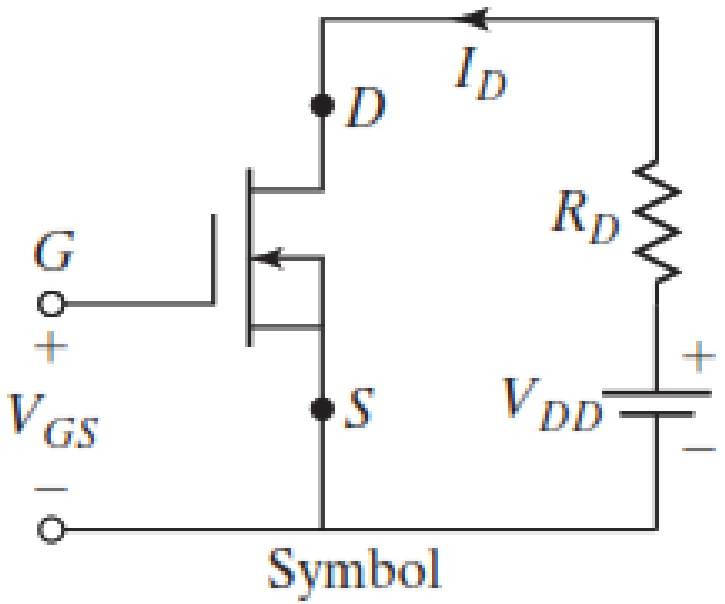


Basic structure

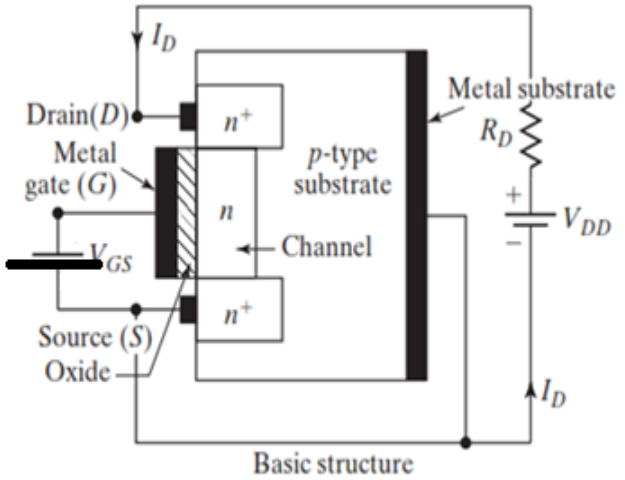


Symbol


I_D
D
+
V_{DS}
−
R_D
G
+
V_{GS}
−
S
V_{DD}
+
−
Symbol

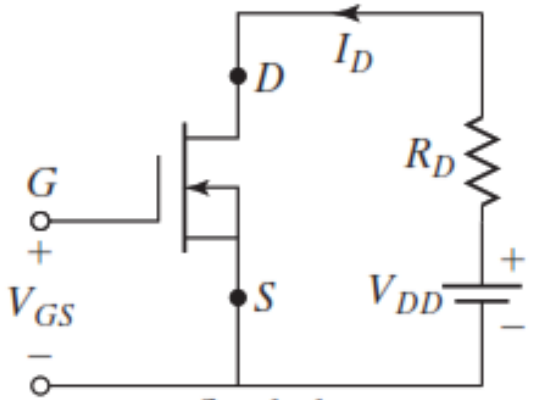

I_D
D
R_D
G
+
V_{GS}
−
S
V_{DD}
+
−
Symbol

n-Channel depletion-type MOSFET

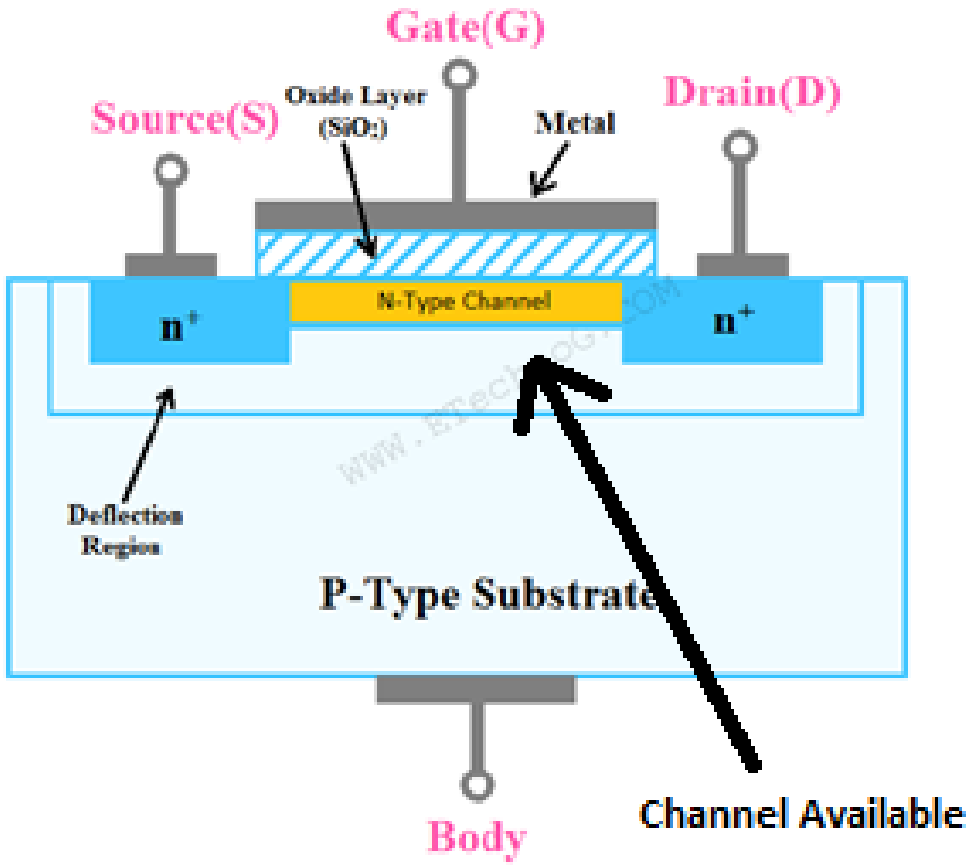


Basic structure

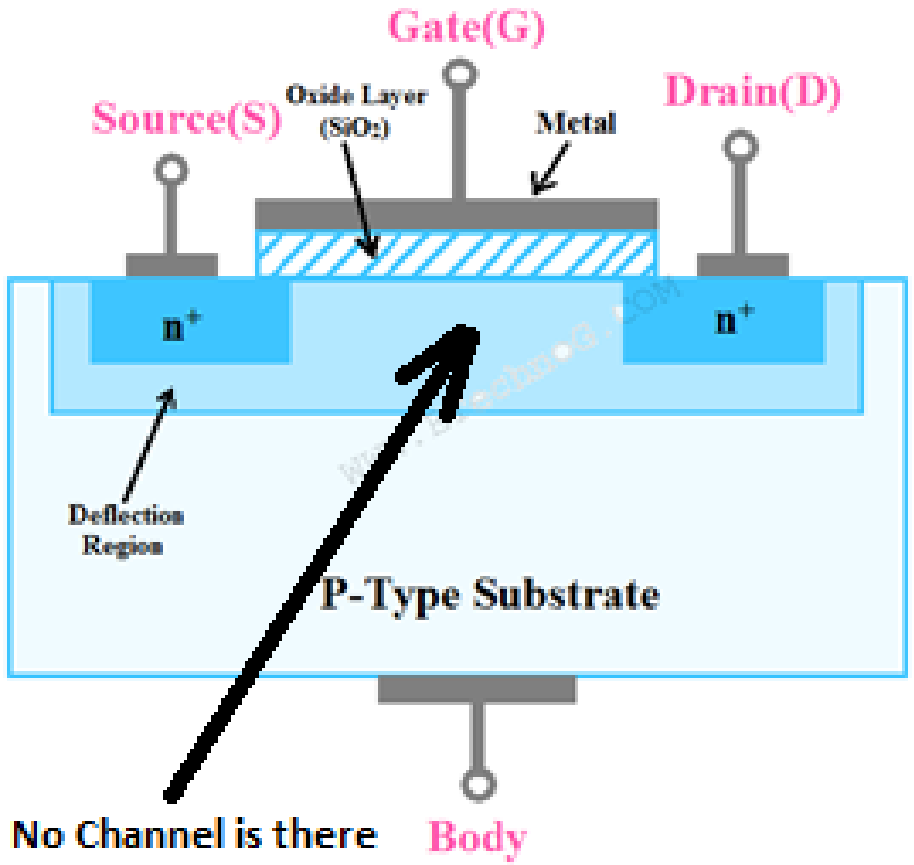
|. An n-channel depletion-type MOSFET is formed on a p-type silicon substrate as shown in Figure 4.1a, with two heavily doped n^+ silicon sections for low-resistance connections. The gate is isolated from the channel by a thin oxide layer. The three terminals are called *gate, drain*, and *source*. The substrate is normally connected to the source. The gate-to-source voltage V_{GS} could be either positive or negative. If V_{GS} is negative, some of the electrons in the n-channel area are repelled and a depletion region is created below the oxide layer, resulting in a narrower effective channel and a high resistance from the drain to source R_{DS}. If V_{GS} is made negative enough, the channel becomes completely depleted, offering a high value of R_{DS}, and no current flows from the drain to source, $I_{DS} = 0$. The value of V_{GS} when this happens is called *pinch-off voltage* V_P. On the other hand, if V_{GS} is made positive, the channel becomes wider, and I_{DS} increases due to reduction in R_{DS}. With a p-channel depletion-type MOSFET, the polarities of V_{DS}, I_{DS}, and V_{GS} are reversed, as shown in Figure 4.1b.



Symbol



Depletion Type MOSFET

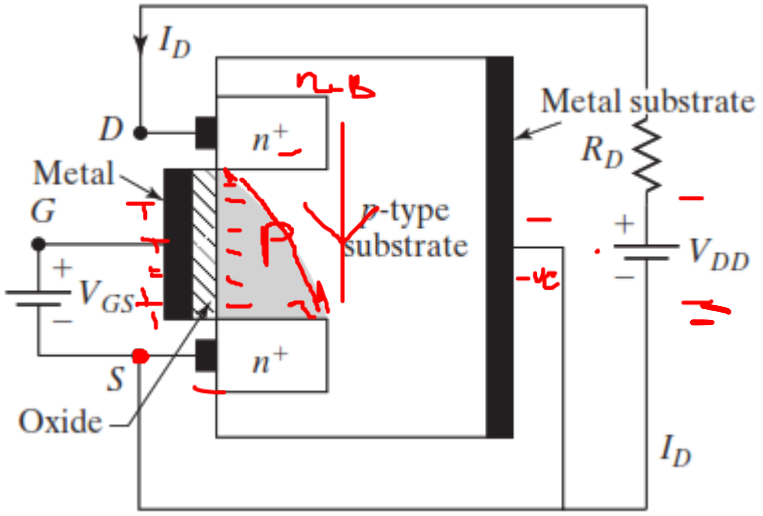


Enhancement Type MOSFET

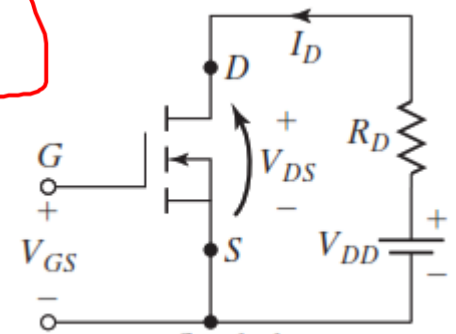
Source: source of majority charge carriers through the channel

n-Channel enhancement-type MOSFET

An *n*-channel enhancement-type MOSFET has no physical channel, as shown in Figure 4.2a. If V_{GS} is positive, an induced voltage attracts the electrons from the *p*-substrate and accumulates them at the surface beneath the oxide layer. If V_{GS} is greater than or equal to a value known as *threshold voltage* V_T, a sufficient number of electrons are accumulated to form a virtual *n*-channel, as shown by shaded lines in Figure 4.2a, and the current flows from the drain to source.



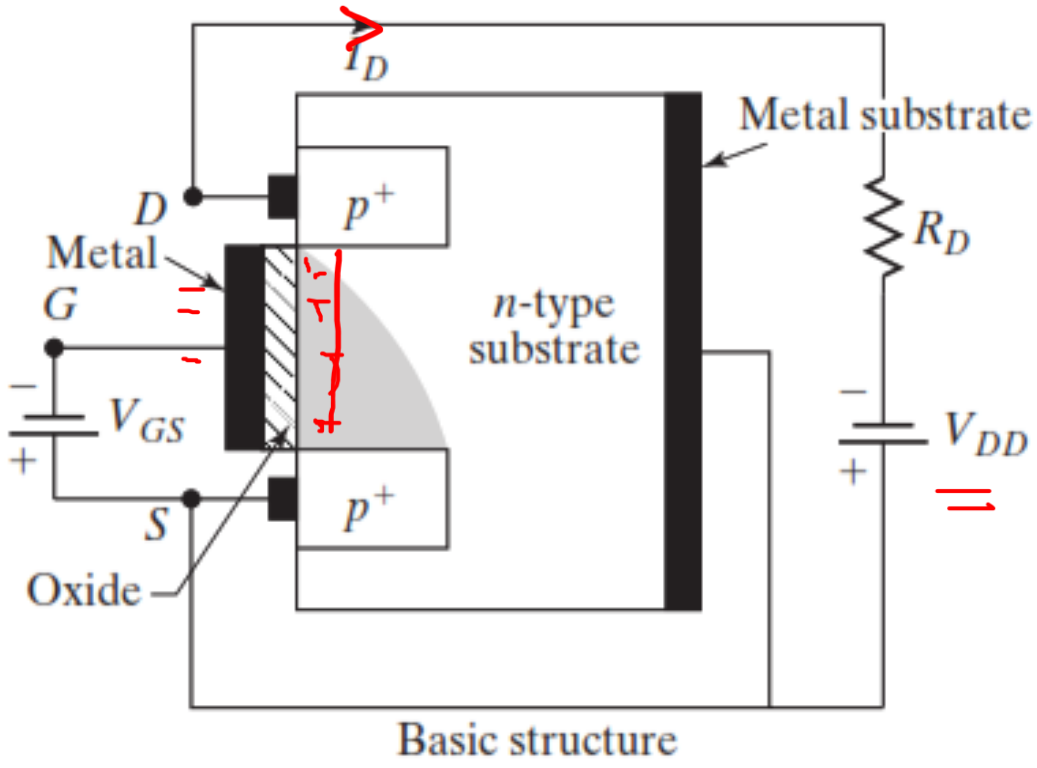
Basic structure

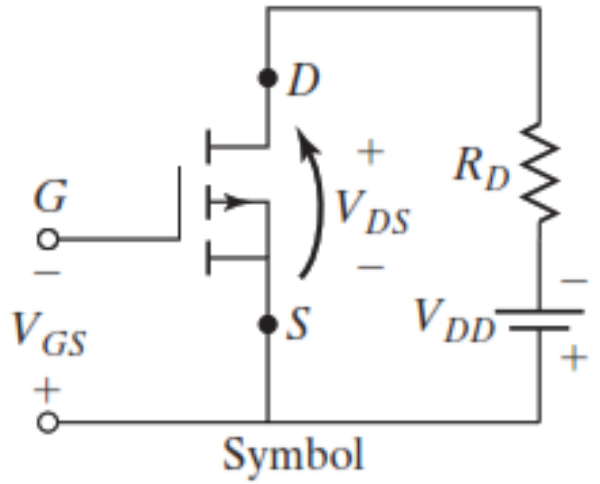


Symbol

p-Channel enhancement-type MOSFET

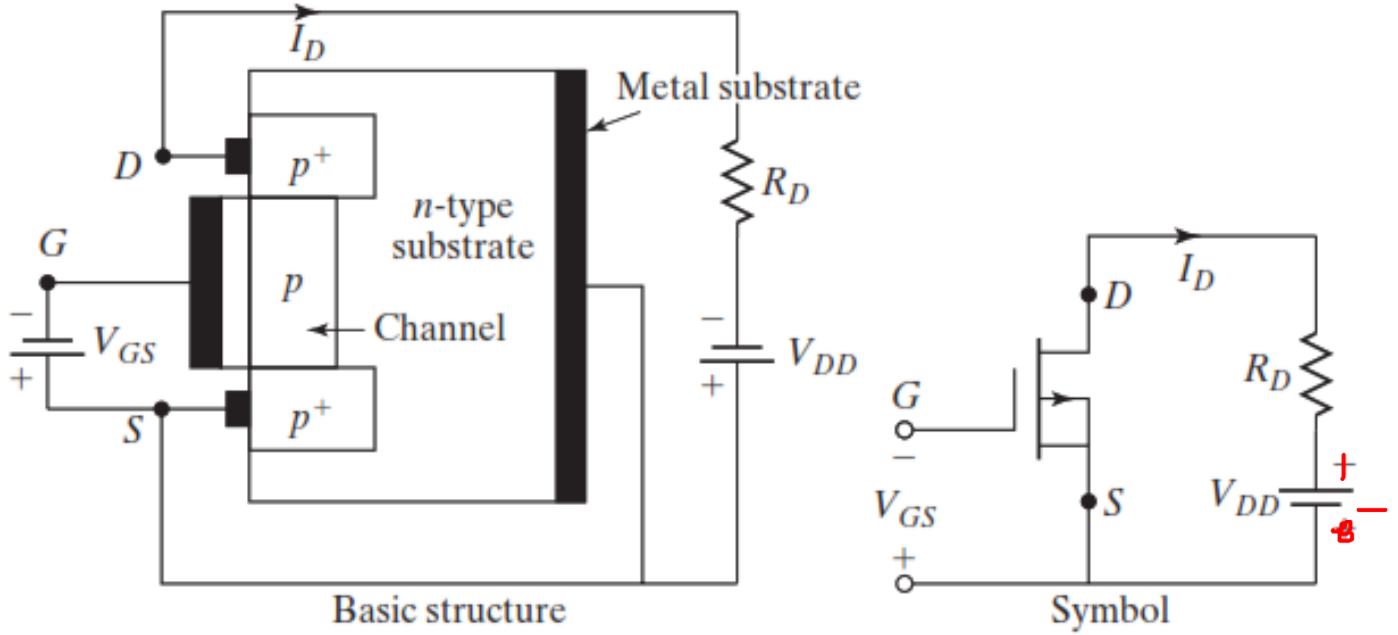
The polarities of V_{DS}, I_{DS}, and V_{GS} are reversed for a p-channel enhancement-type MOSFET,





p-Channel depletion-type MOSFET

. With a *p*-channel depletion-type MOSFET,
the polarities of V_{DS}, I_{DS}, and V_{GS} are reversed, as shown in Figure 4.1b.



(b) *p*-Channel depletion-type MOSFET

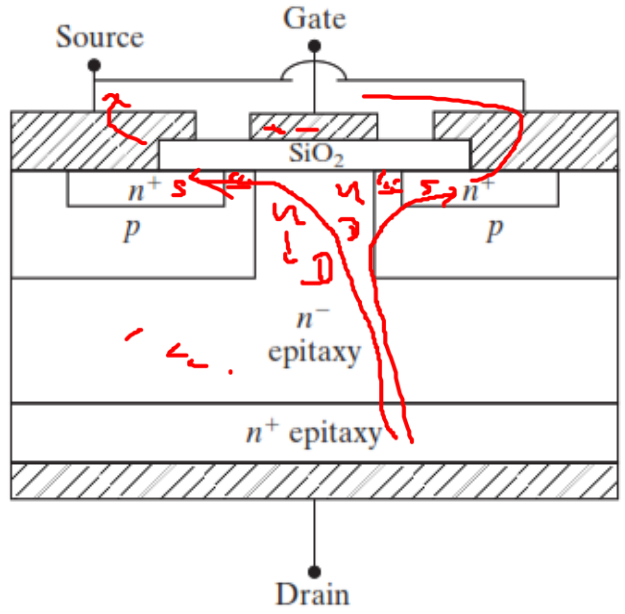
Because a depletion MOSFET remains on at zero gate voltage, whereas an enhancement-type MOSFET remains off at zero gate voltage, the enhancement-type MOSFETS are generally used as switching devices in power electronics.

Structure of Power MOSFET

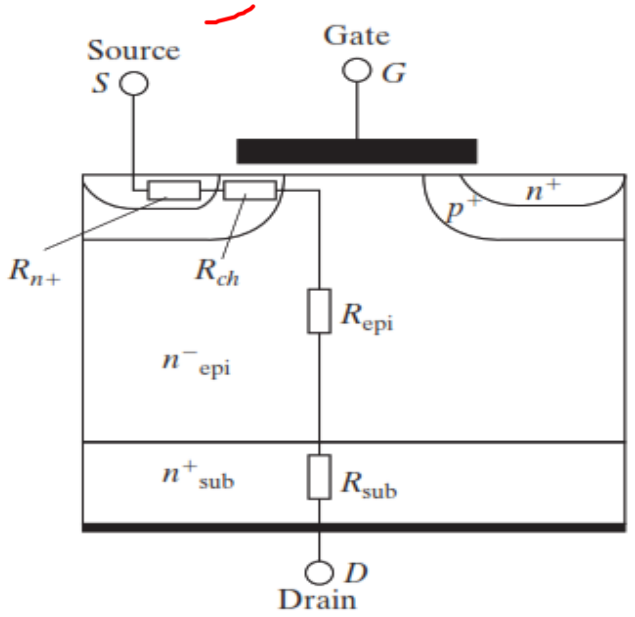
In order to reduce the on-state resistance by having a larger current conducting area, the V-type structure is commonly used for power MOSFETs. The cross section of a power MOSFET known as a vertical (V) MOSFET is shown in Figure 4.4a.

When the gate has a sufficiently positive voltage with respect to the source, the effect of its electric field pulls electrons from the $n+$ layer into the p layer. This opens a channel closest to the gate, which in turn allows the current to flow from the drain to the source. There is a silicon oxide (SiO_2) dielectric layer between the gate metal and the $n+$ and p junction. MOSFET is heavily doped on the drain side to create an $n+$ buffer below the n-drift layer. This buffer prevents the depletion layer from reaching the metal, evens out the voltage stress across the n layer, and also reduces the forward voltage drop during conduction. The buffer layer also makes it an asymmetric device with rather low reverse voltage capability.

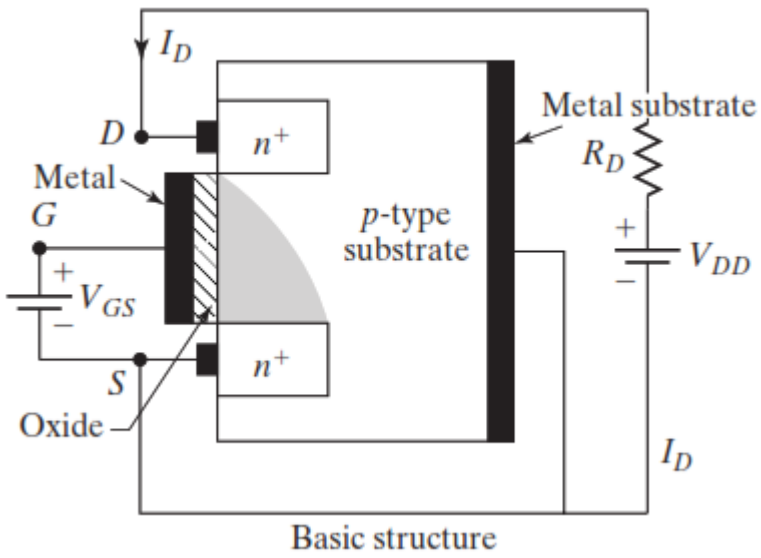
MOSFETs require low gate energy, and have a very fast switching speed and low switching losses. The input resistance is very high, 10^9 to 10^{11} Ω. MOSFETs, however, suffer from the disadvantage of high forward on-state resistance as shown in Figure 4.4b, and hence high on-state losses, which makes them less attractive as power devices,



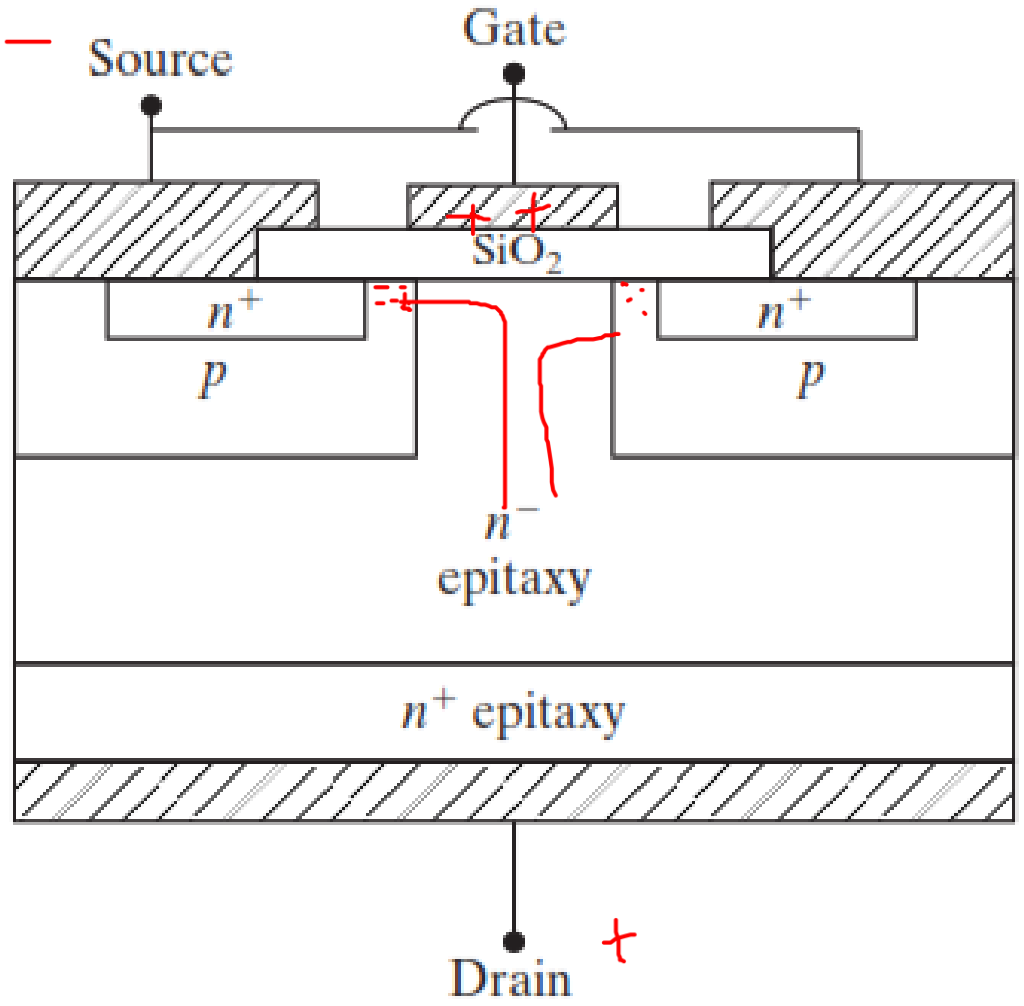
(a) Cross section of V-MOSFET



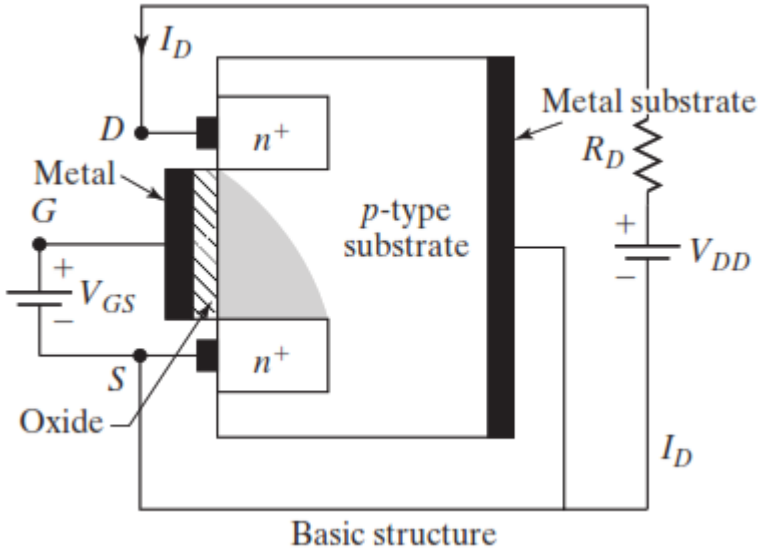
(b) On-state series resistances of V-MOSFET



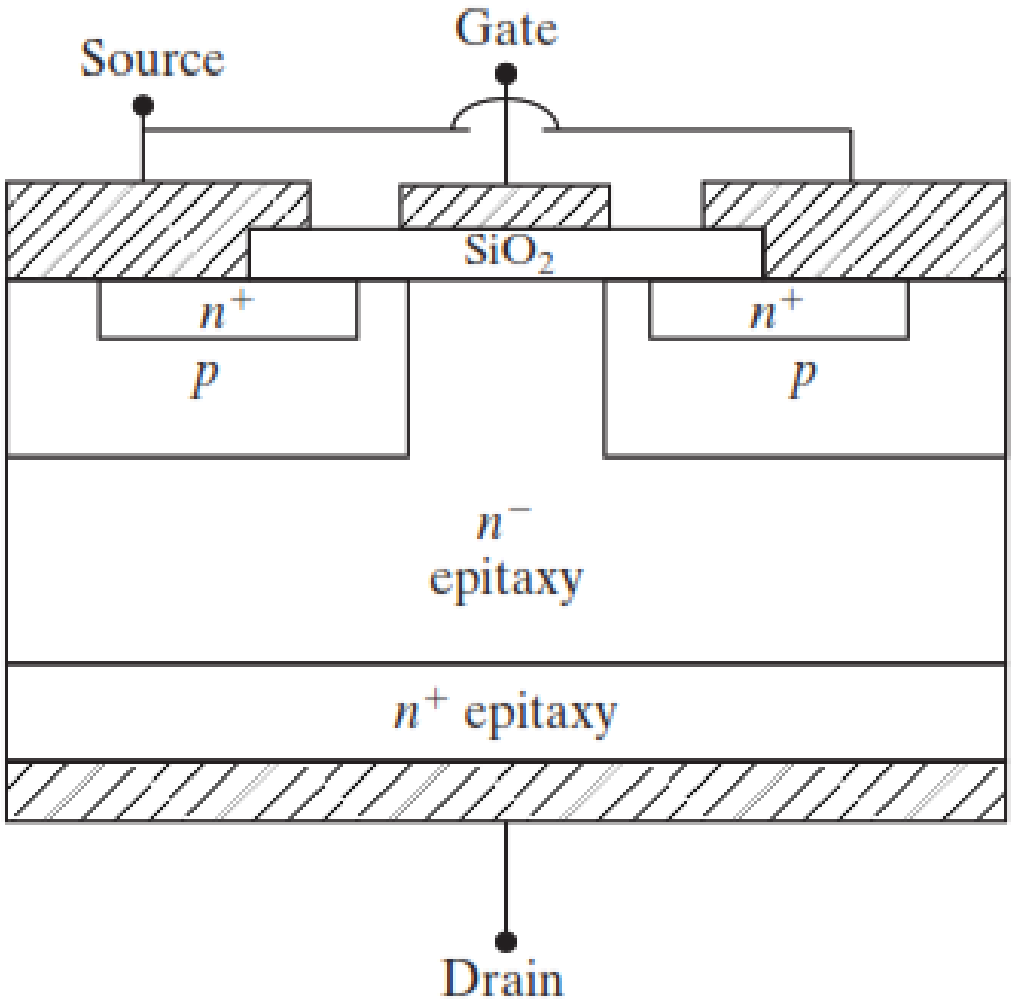
Basic structure



(a) Cross section of V-MOSFET



Basic structure



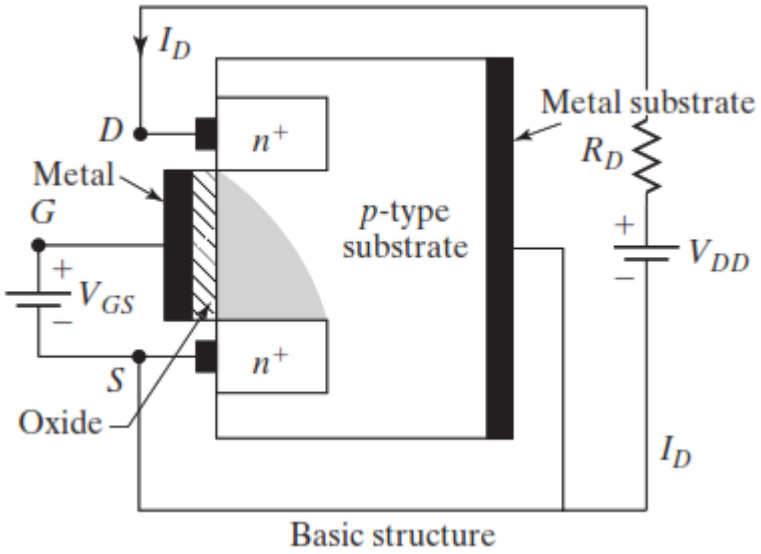
(a) Cross section of V-MOSFET

Steady-State Characteristics

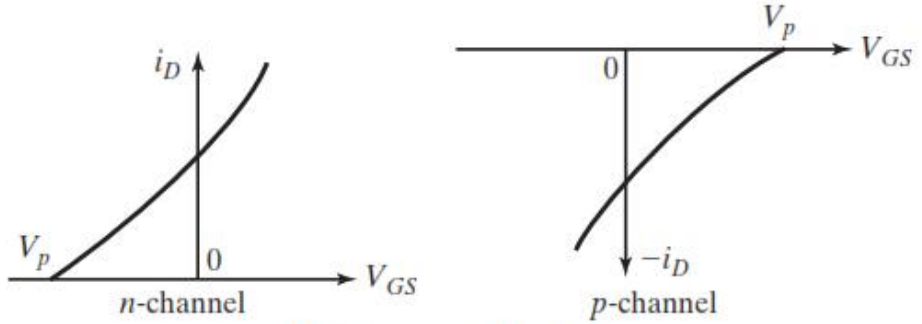
Transfer characteristics of MOSFETs

The MOSFETs are voltage-controlled devices and have a very high input impedance. The gate draws a very small leakage current, on the order of nanoamperes. The current gain, which is the ratio of drain current I_D to input gate current I_G, is typically on the order of 10^9. However, the current gain is not an important parameter. The *transconductance*, which is the ratio of drain current to gate voltage, defines the transfer characteristics and is a very important parameter.

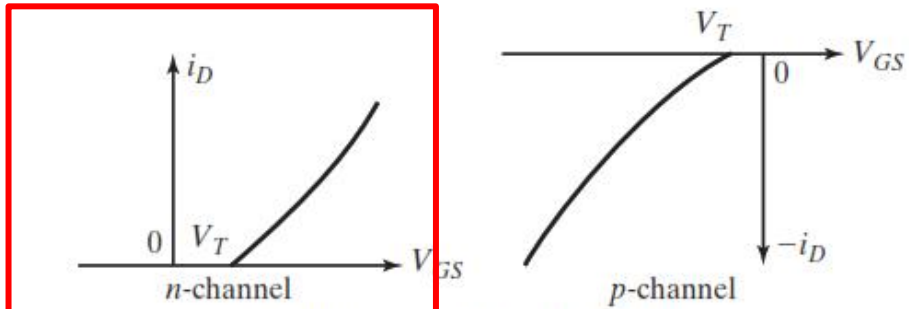
The transfer characteristics of *n*-channel and *p*-channel MOSFETs are shown in Figure



Basic structure



(a) Depletion-type MOSFET



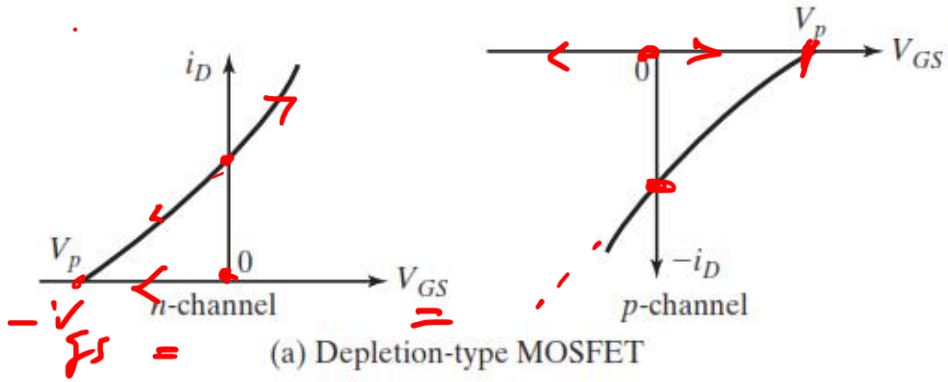
(b) Enhancement-type MOSFET

Steady-State Characteristics

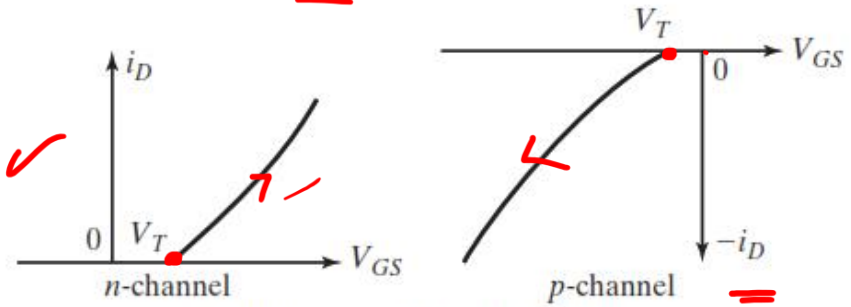
Transfer characteristics of MOSFETs

The MOSFETs are voltage-controlled devices and have a very high input impedance. The gate draws a very small leakage current, on the order of nanoamperes. The current gain, which is the ratio of drain current I_D to input gate current I_G, is typically on the order of 10^9. However, the current gain is not an important parameter. The *transconductance*, which is the ratio of drain current to gate voltage, defines the transfer characteristics and is a very important parameter.

The transfer characteristics of *n*-channel and *p*-channel MOSFETs are shown in Figure



(a) Depletion-type MOSFET



(b) Enhancement-type MOSFET

output characteristics of an n-channel enhancement MOSFET

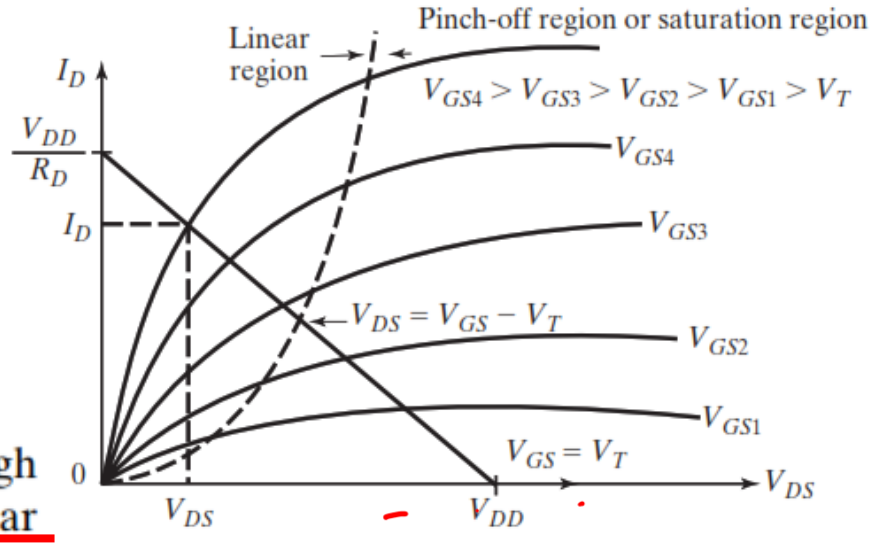
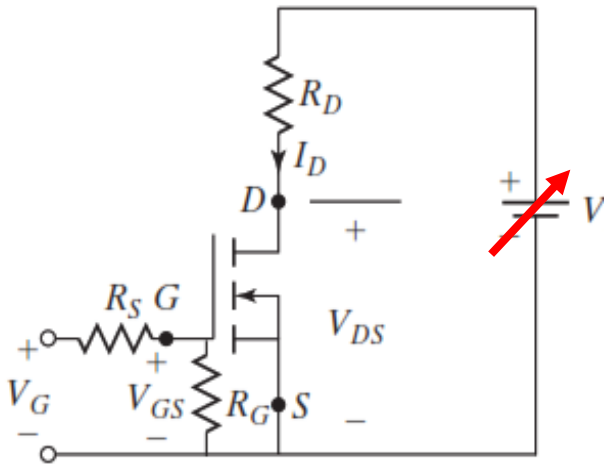
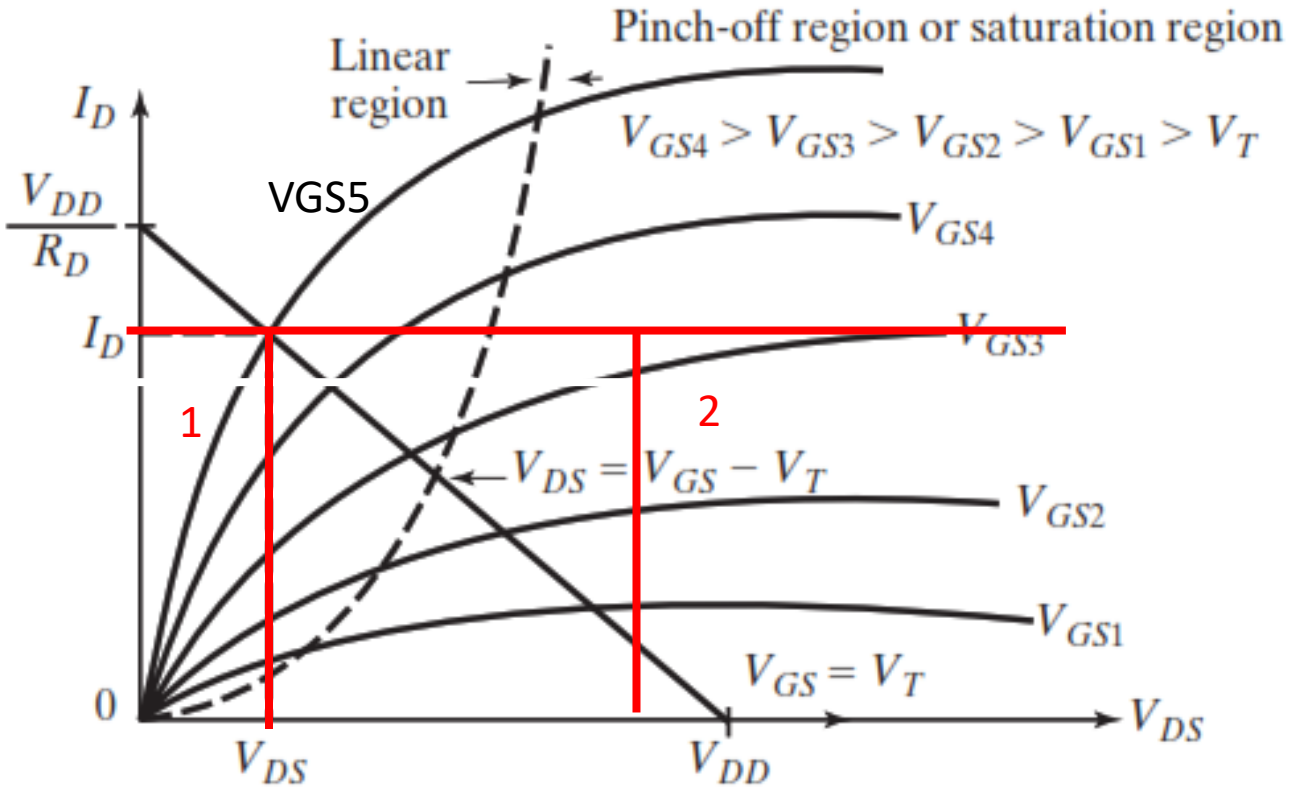


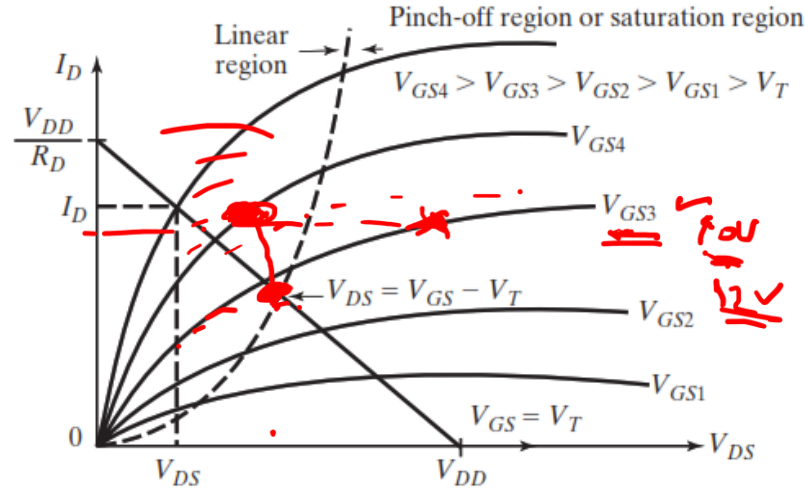
Figure 4.6 shows the output characteristics of an *n*-channel enhancement MOSFET. There are three regions of operation: (1) cutoff region, where $V_{GS} \leq V_T$; (2) pinch-off or saturation region, where $V_{DS} \geq V_{GS} - V_T$; and (3) linear region, where $V_{DS} \leq V_{GS} - V_T$. The pinch-off occurs at $V_{DS} = V_{GS} - V_T$. In the linear region, the drain current I_D varies in proportion to the drain–source voltage V_{DS}. Due to high drain current and low drain voltage, the power MOSFETs are operated in the linear region for switching actions. In the saturation region, the drain current remains almost constant for any increase in the value of V_{DS} and the transistors are used in this region for voltage amplification. It should be noted that saturation has the opposite meaning to that for bipolar transistors. In the linear or ohmic region, the drain–source v_{DS} is low



(a) Circuit diagram

a given ID can be obtained with VGS5 or VGS 3 where VGS5>VGS3. With high VGS (VGS3)the MOSFET can be driven to linear region where the resistance and drop are low





The load line of a MOSFET with a load resistance R_D as shown in Figure 4.7a can be described by

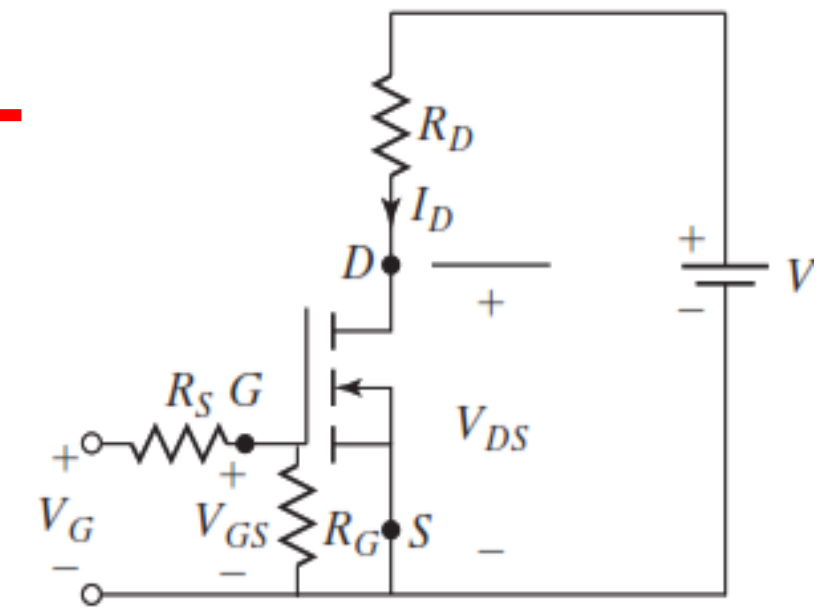
$$i_D = \frac{V_{DD} - v_{DS}}{R_D} \tag{4.4}$$

where $i_D = V_{DD}/R_D$ at $v_{DS} = 0$ and $v_{DS} = V_{DD}$ at $i_D = 0$

In order to keep the value of V_{DS} low, the gate–source voltage V_{GS} must be higher so that the transistor operates in the linear region.

The steady-state switching model, which is the same for both depletion-type and enhancement-type MOSFETs, is shown in Figure 4.7. R_D is the load resistance. A large resistance R_G in the order of megohms is connected between the gate and source to establish the gate voltage to a defined level. R_S ($\ll R_G$) limits the charging currents through the internal capacitances of the MOSFET. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{constant}} \tag{4.5}$$



(a) Circuit diagram

Important points to remember

The output resistance, $r_o = R_{DS}$, which is defined as

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D}$$

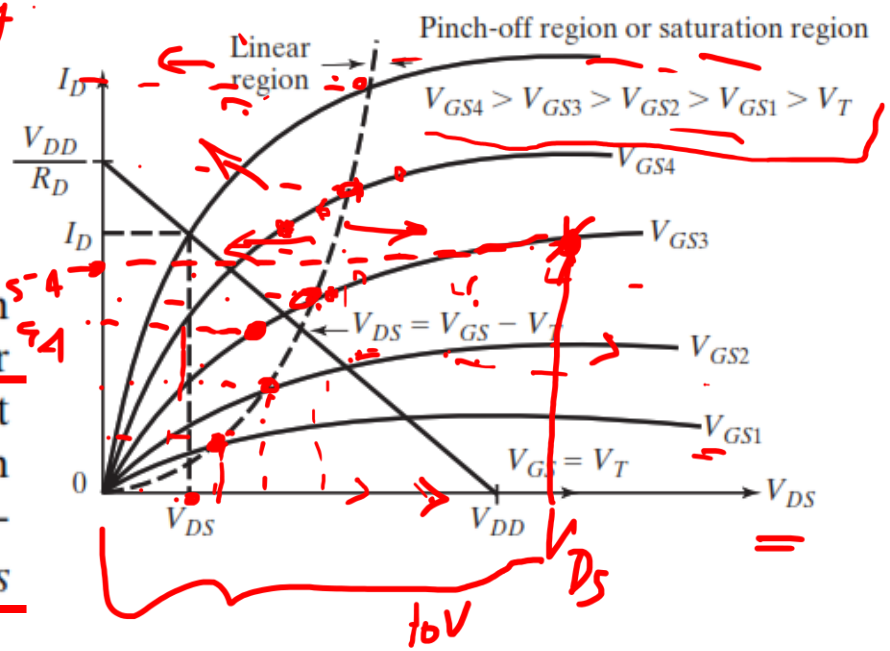
is normally very high in the pinch-off region, typically on the order of megohms and is very small in the linear region, typically on the order of milliohms.

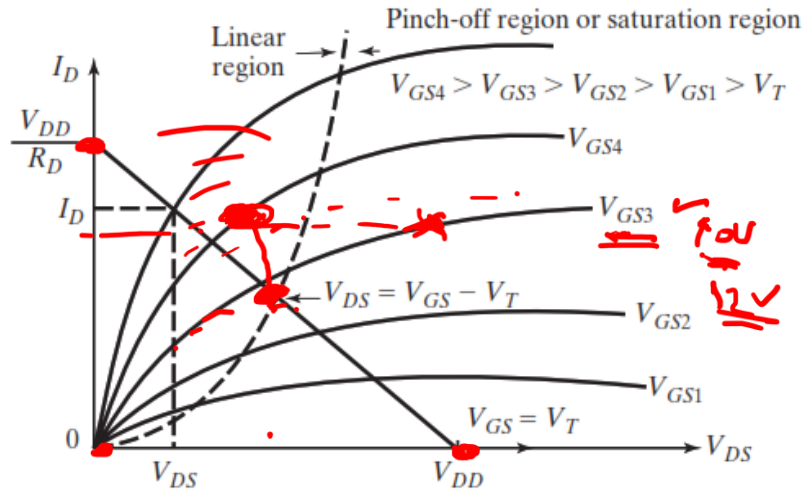
the on-state resistance R_{DS} of the MOSFET switch can be decreased by increasing the gate–source drive voltage, v_{GS}.

The power MOSFETs are generally of the enhancement type.

output characteristics of an n-channel enhancement MOSFET

Figure 4.6 shows the output characteristics of an *n*-channel enhancement MOSFET. There are three regions of operation: (1) cutoff region, where $V_{GS} \leq V_T$; (2) pinch-off or saturation region, where $V_{DS} \geq V_{GS} - V_T$; and (3) linear region, where $V_{DS} \leq V_{GS} - V_T$. The pinch-off occurs at $V_{DS} = V_{GS} - V_T$. In the linear region, the drain current I_D varies in proportion to the drain–source voltage V_{DS}. Due to high drain current and low drain voltage, the power MOSFETs are operated in the linear region for switching actions. In the saturation region, the drain current remains almost constant for any increase in the value of V_{DS} and the transistors are used in this region for voltage amplification. It should be noted that saturation has the opposite meaning to that for bipolar transistors. In the linear or ohmic region, the drain–source v_{DS} is low





The load line of a MOSFET with a load resistance R_D as shown in Figure 4.7a can be described by

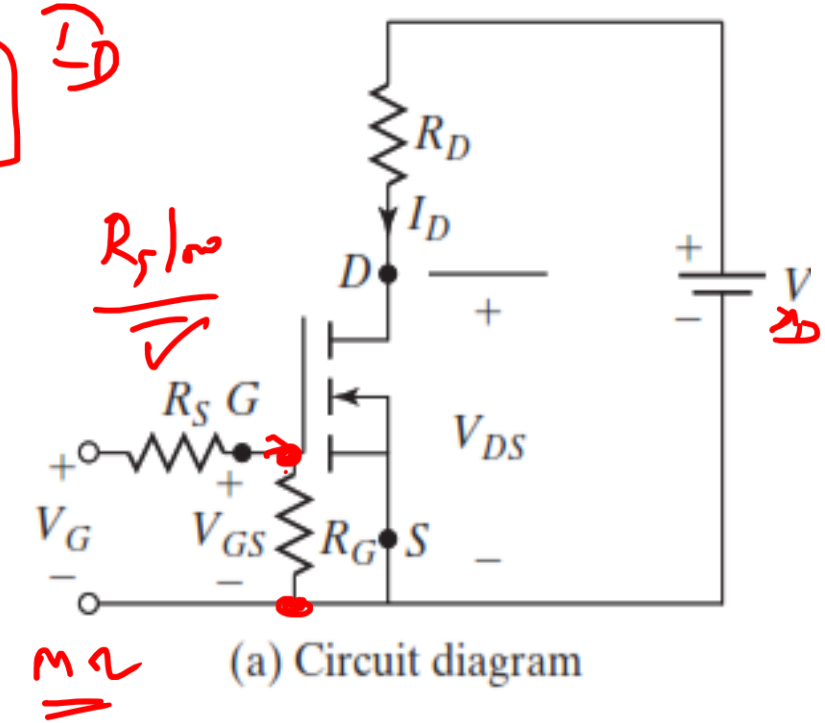
$$i_D = \frac{V_{DD} - v_{DS}}{R_D} \tag{4.4}$$

where $i_D = V_{DD}/R_D$ at $v_{DS} = 0$ and $v_{DS} = V_{DD}$ at $i_D = 0$

In order to keep the value of V_{DS} low, the gate–source voltage V_{GS} must be higher so that the transistor operates in the linear region.

The steady-state switching model, which is the same for both depletion-type and enhancement-type MOSFETs, is shown in Figure 4.7. R_D is the load resistance. A large resistance R_G in the order of megohms is connected between the gate and source to establish the gate voltage to a defined level. R_S ($\ll R_G$) limits the charging currents through the internal capacitances of the MOSFET. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{constant}} \tag{4.5}$$



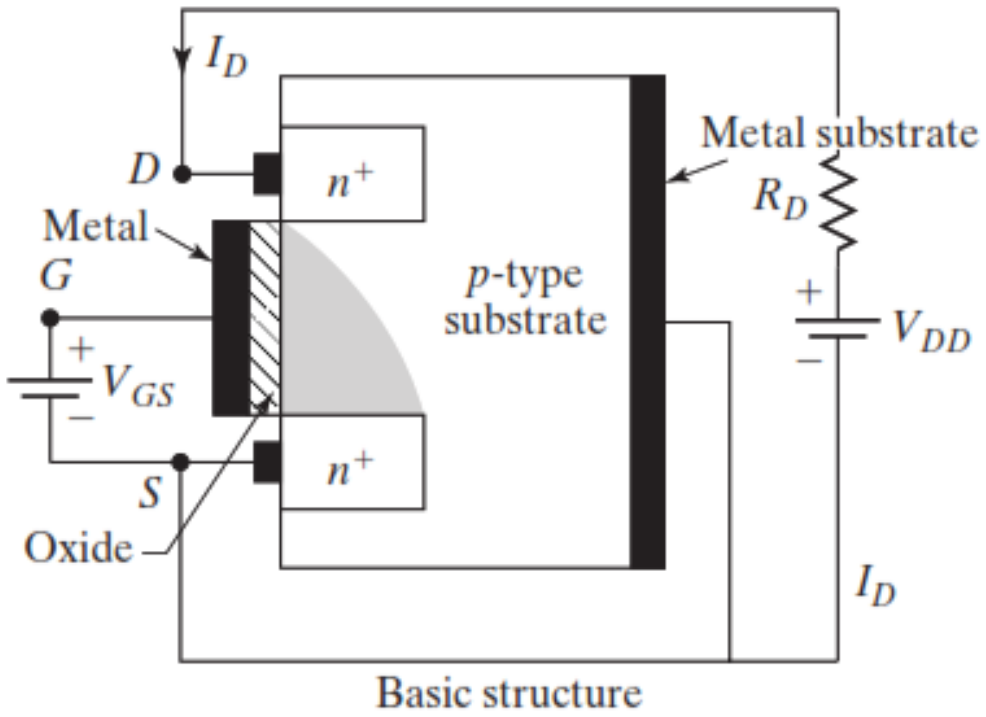
The output resistance, $r_o = R_{DS}$, which is defined as

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D}$$

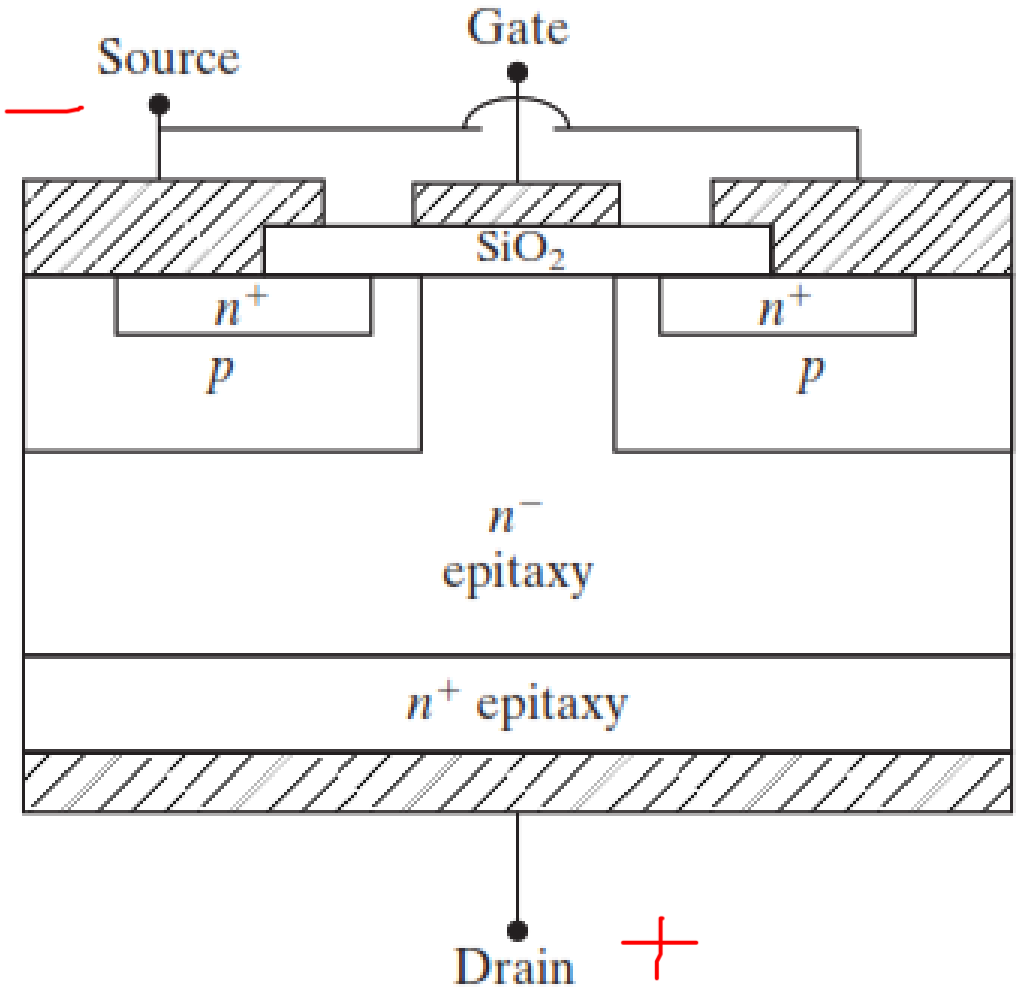
is normally very high in the pinch-off region, typically on the order of megohms and is very small in the linear region, typically on the order of milliohms.

the on-state resistance R_{DS} of the MOSFET switch can be decreased by increasing the gate–source drive voltage, v_{GS}.

The power MOSFETs are generally of the enhancement type.

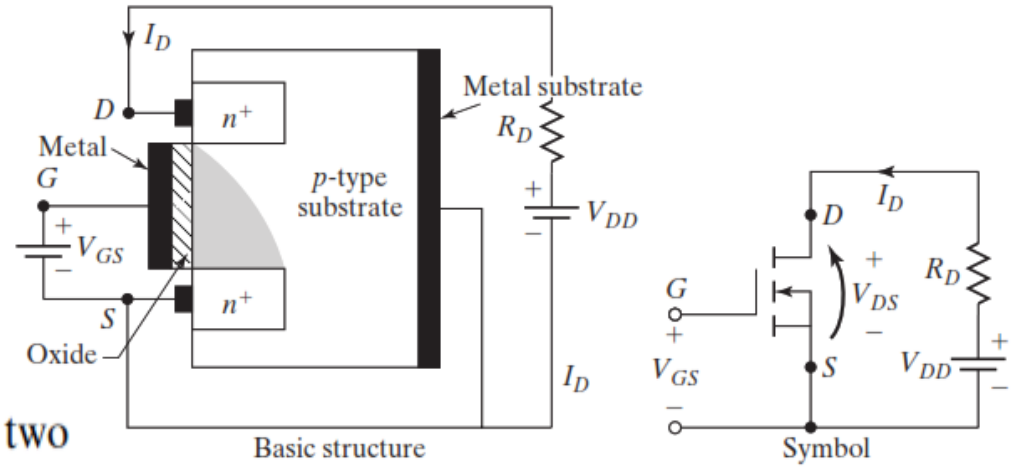


Basic structure



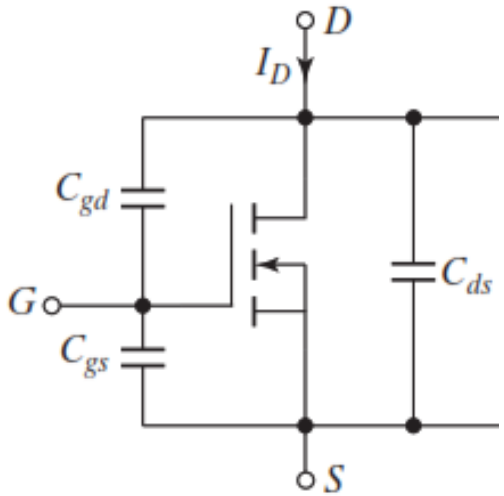
(a) Cross section of V-MOSFET

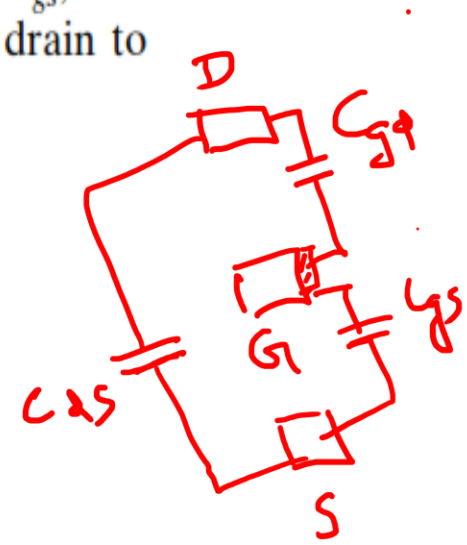
Switching Characteristics

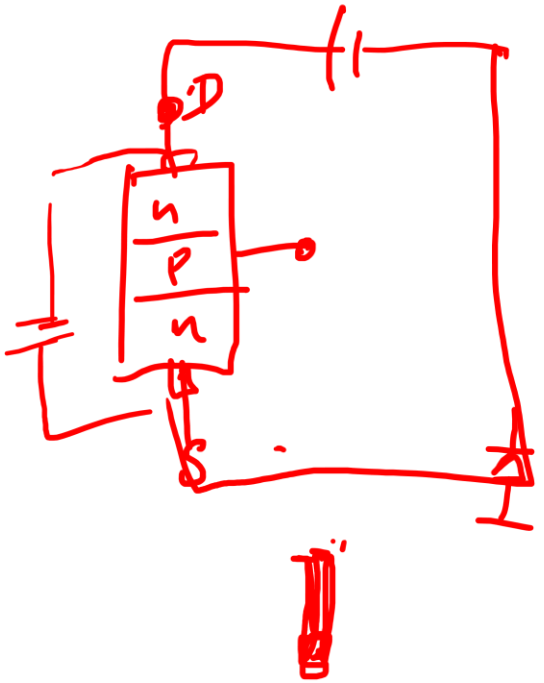


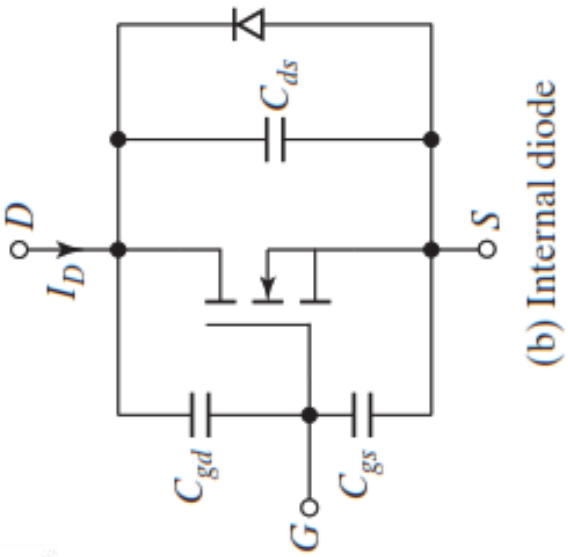
(a) *n*-Channel enhancement-type MOSFET

Without any gate signal, the enhancement-type MOSFET may be considered as two diodes connected back to back (*np* and *pn* diodes as shown in Figure) or as an *NPN*-transistor. The gate structure has parasitic capacitances to the source, C_{gs}, and to the drain, C_{gd}. The *NPN*-transistor has a reverse-bias junction from the drain to the source and offers a capacitance, C_{ds}.

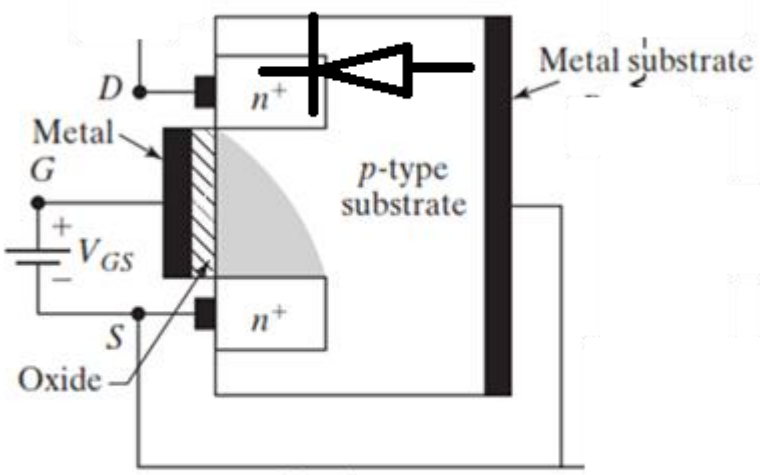


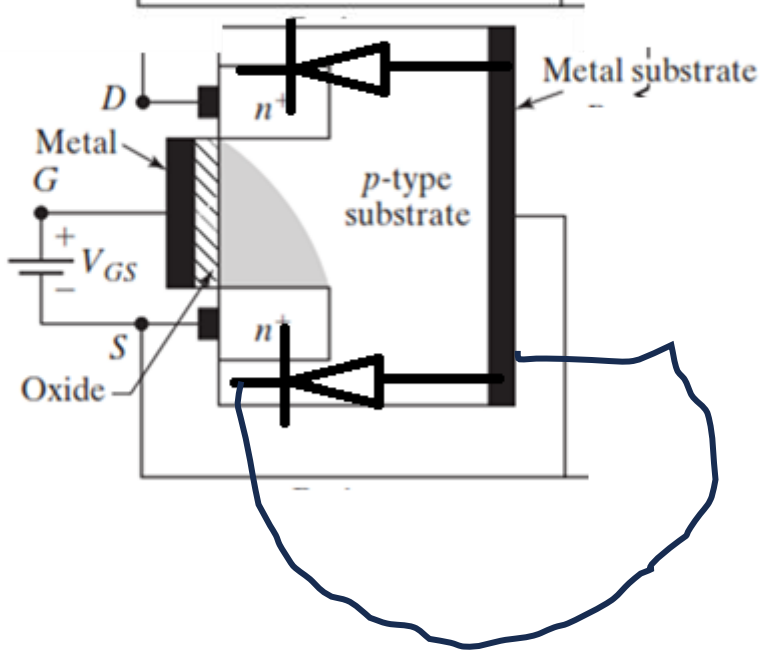


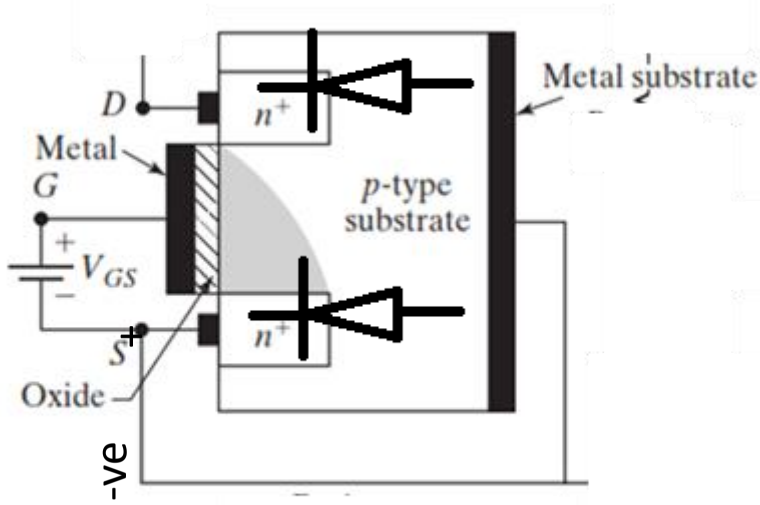


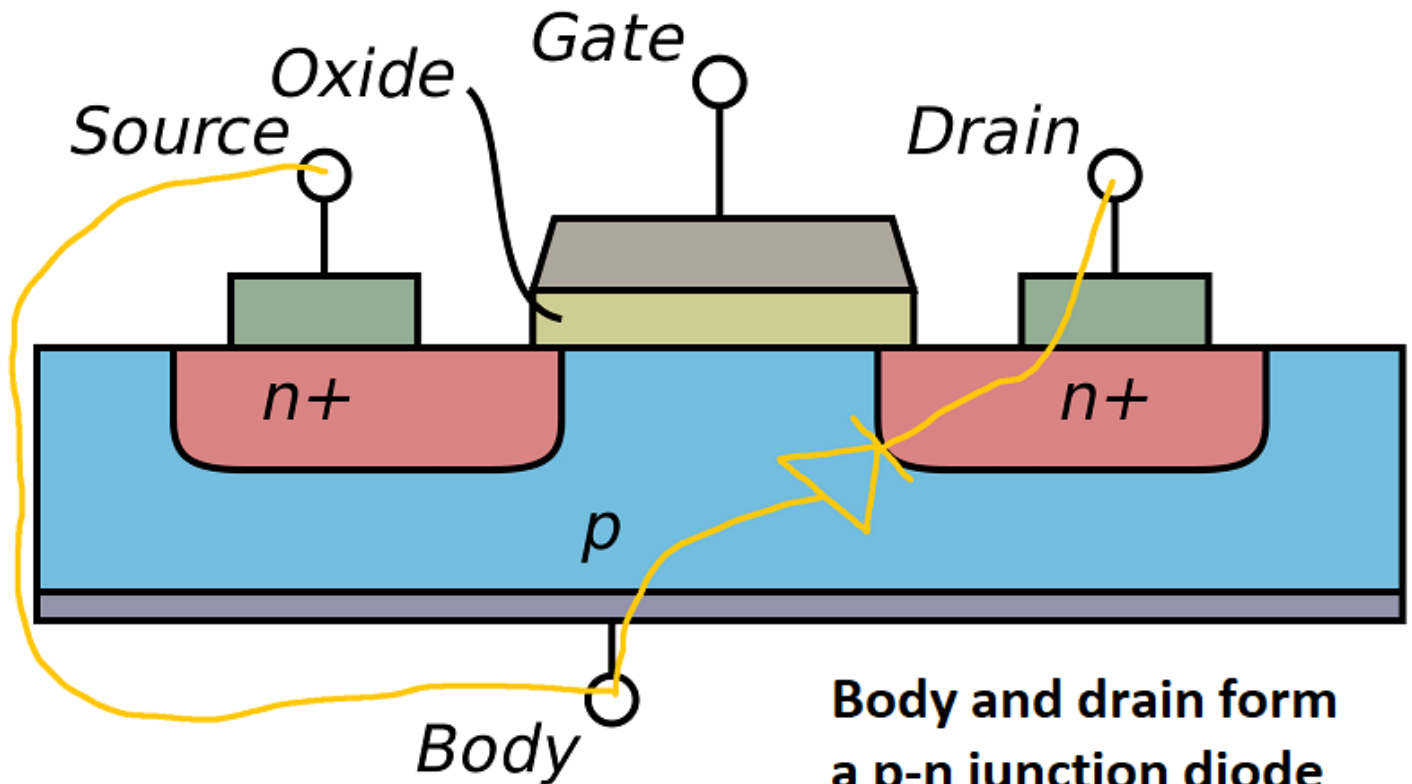


(b) Internal diode





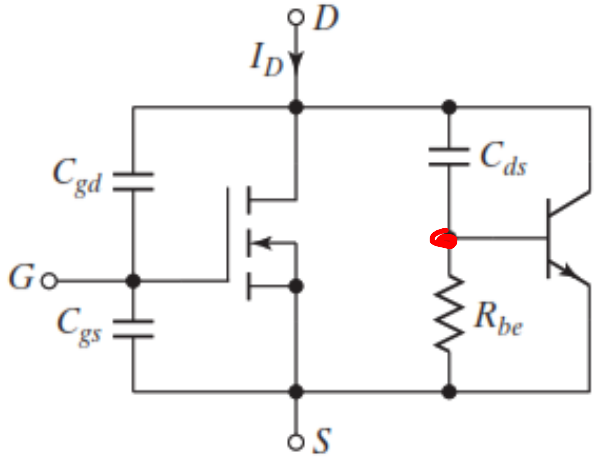




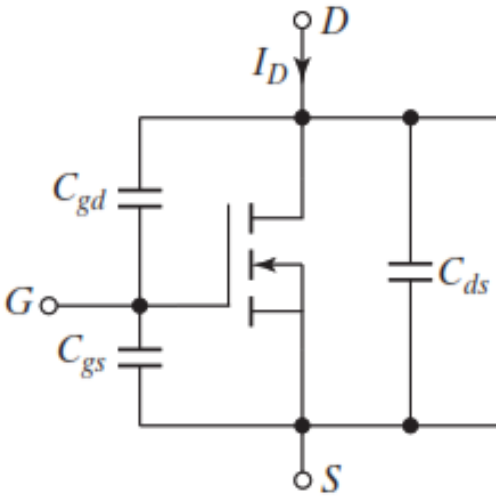
Source and body tied together in the package

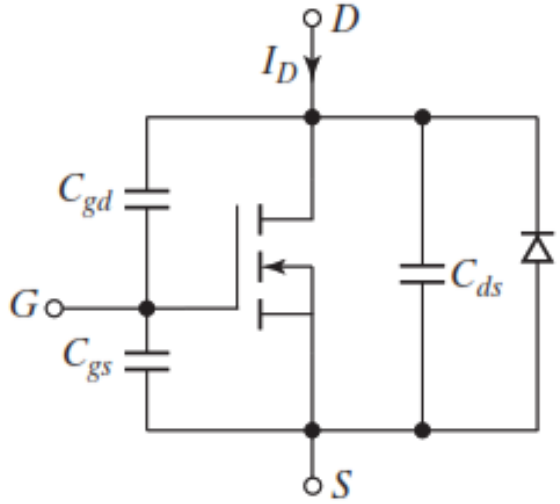
Body and drain form a p-n junction diode

Figure 4.8a shows the equivalent circuit of a parasitic bipolar transistor in parallel with a MOSFET. The base-to-emitter region of an *NPN*-transistor is shorted at the chip by metalizing the source terminal and the resistance from the base to emitter due to bulk resistance of *n*- and *p*-regions, R_{be}, is small. Hence, a MOSFET may be considered as having an internal diode and the equivalent circuit is shown in Figure 4.8b. The parasitic capacitances are dependent on their respective voltages.



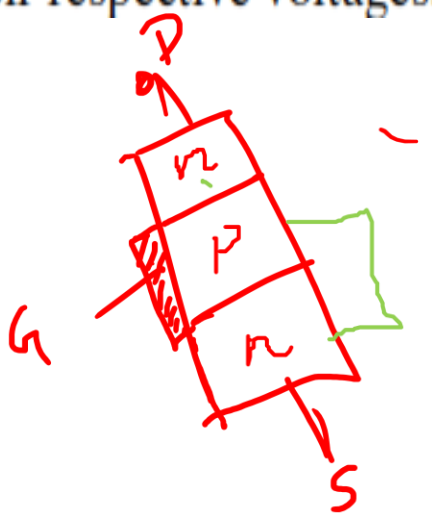
(a) Parasitic biploar

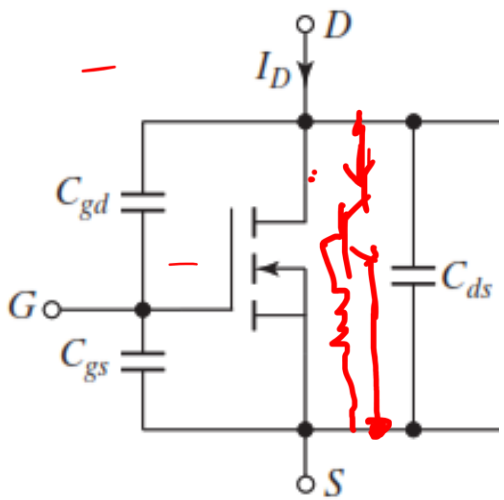


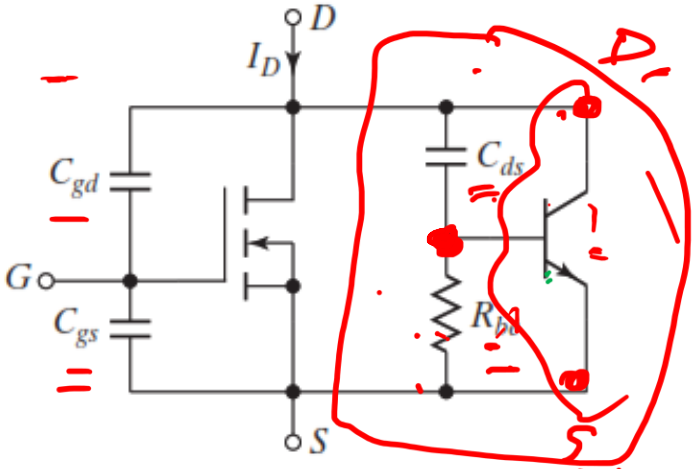


(b) Internal diode

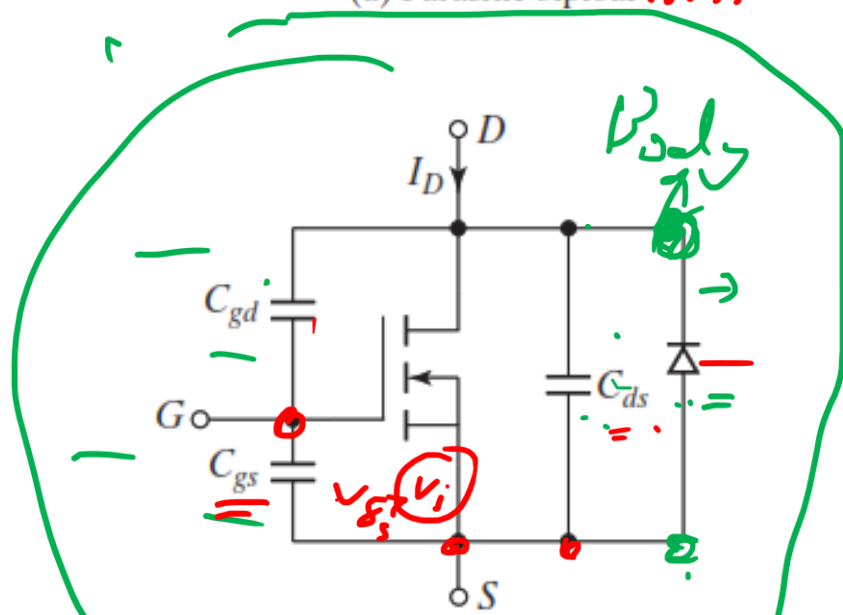
Figure 4.8a shows the equivalent circuit of a parasitic bipolar transistor in parallel with a MOSFET. The base-to-emitter region of an *NPN*-transistor is shorted at the chip by metalizing the source terminal and the resistance from the base to emitter due to bulk resistance of *n*- and *p*-regions, R_{be}, is small. Hence, a MOSFET may be considered as having an internal diode and the equivalent circuit is shown in Figure 4.8b. The parasitic capacitances are dependent on their respective voltages.





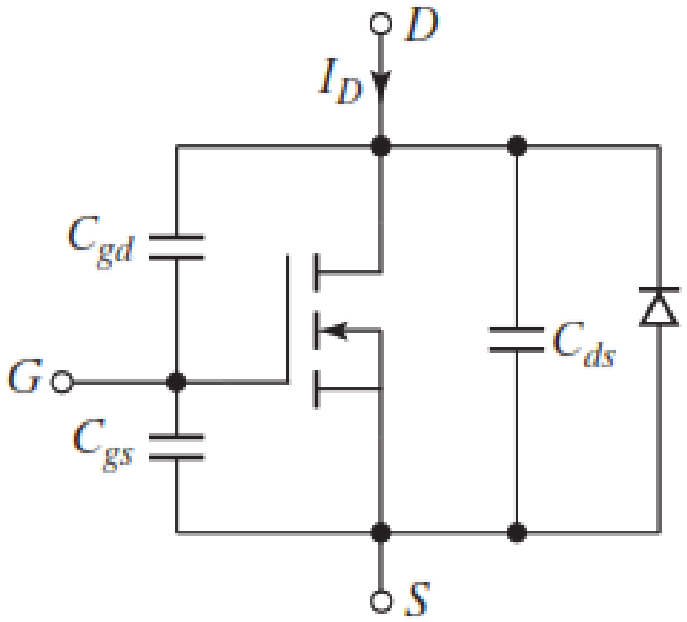


(a) Parasitic bipolar transistor



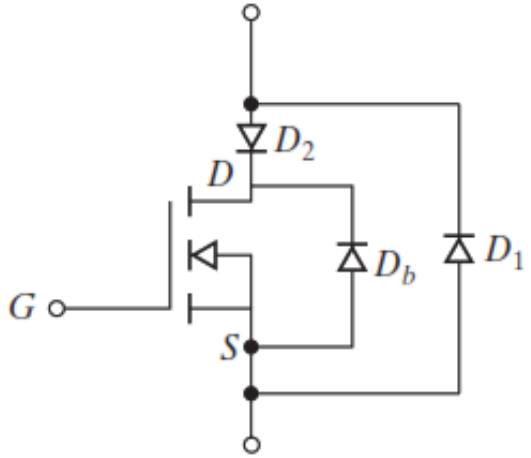
(b) Internal diode

The internal built-in diode is often called the *body diode*. The switching speed of the body diode is much slower than that of the MOSFET. Thus, an NMOS (*n*-channel metal oxide semiconductor) will behave as an uncontrolled device. As a result, a current can flow from the source to the drain if the circuit conditions prevail for a negative current. This is true if the NMOS is switching power to an inductive load and the NMOS will act as a freewheeling diode and provide a path for current flow from the source to the drain. The NMOS will behave as an uncontrolled device in the reverse direction. The NMOS data sheet would normally specify the current rating of the parasitic diode.



(b) Internal diode

If body diode D_b is allowed to conduct, then a high peak current can occur during the diode turn-off transition. Most MOSFETs are not rated to handle these currents, and device failure can occur. To avoid this situation, external series D_2 and antiparallel diodes D_1 can be added as in Figure 4.8c. Power MOSFETs can be designed to have a built-in fast-recovery body diode and to operate reliably when the body diode is allowed to conduct at the rated MOSFET current. However, the switching speed of such body diodes is still somewhat slow, and significant switching loss due to diode stored charge can occur. The designer should check the ratings and the speed of the body diode to handle the operating requirements.



(c) MOSFET with external diodes

Switching Characteristics of MOSFET

(1) $t_{d\ (on)}$: Turn-on delay time

The time from when the gate-source voltage rises over 10% of V_{GS} until the drain-source voltage reaches 90% of V_{DS}

(2) t_r: Rise time

The time taken for the drain-source voltage to fall from 90% to 10% of V_{DS}

(3) t_{on}: Turn-on time

The turn-on time is equal to $t_{d\ (on)} + t_r$.

(4) $t_{d\ (off)}$: Turn-off delay time

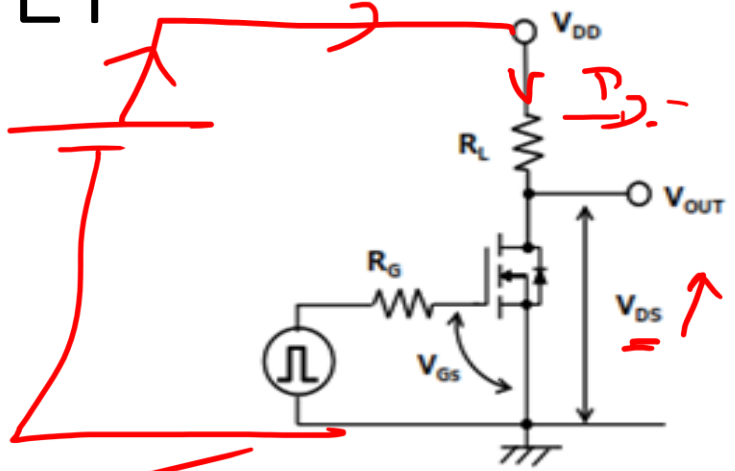
The time from when the gate-source voltage drops below 90% of V_{GS} until the drain-source voltage reaches 10% of V_{DS}

(5) t_f: Fall time

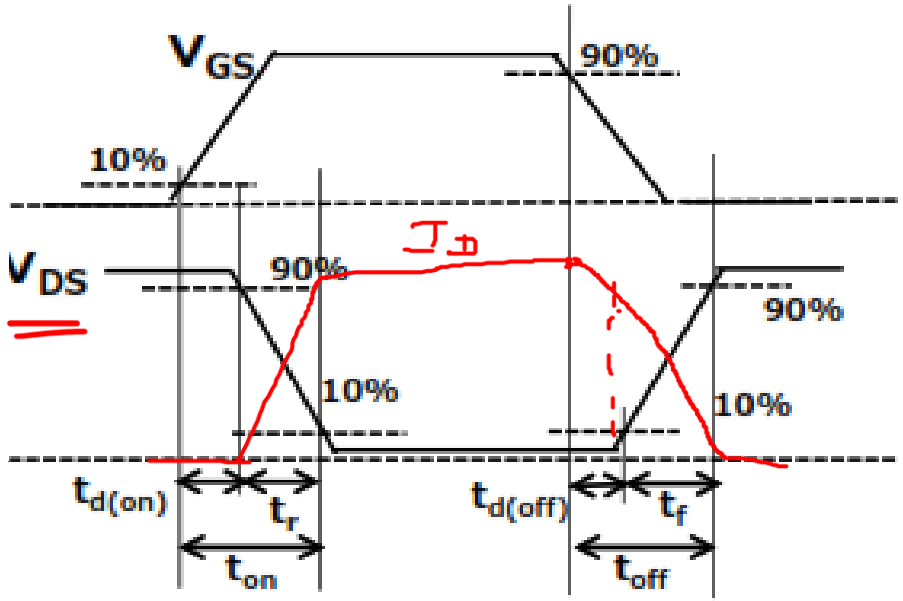
The time taken for the drain-source voltage to rise from 10% to 90% of V_{DS}

(6) t_{off}: Turn-off time

The turn-off time is equal to $t_{d\ (off)} + t_f$.



(a) Test Circuit



(b) Input and Output Waveforms

Switching Characteristics

The switching model of MOSFETs with parasitic capacitances is shown in Figure 4.9. The typical switching waveforms and times are shown in Figure 4.10. The *turn-on delay* $t_{d(on)}$ is the time that is required to charge the input capacitance to threshold voltage level. The *rise time* t_r is the gate-charging time from the threshold level to the full-gate voltage V_{GSP}, which is required to drive the transistor into the linear region. The *turn-off delay time* $t_{d(off)}$ is the time required for the input capacitance to discharge from the overdrive gate voltage V_1 to the pinch-off region. V_{GS} must decrease significantly before V_{DS} begins to rise. The *fall time* t_f is the time that is required for the input capacitance to discharge from the pinch-off region to threshold voltage. If $V_{GS} \leq V_T$, the transistor turns off.

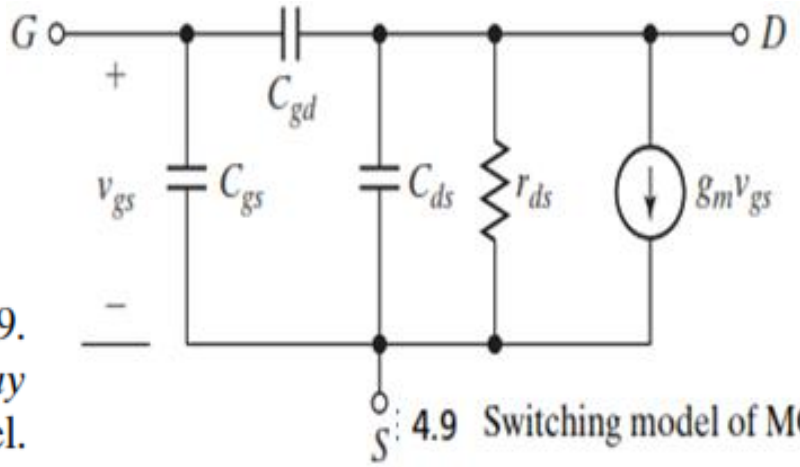


FIGURE 4.9 Switching model of MOSFETs.

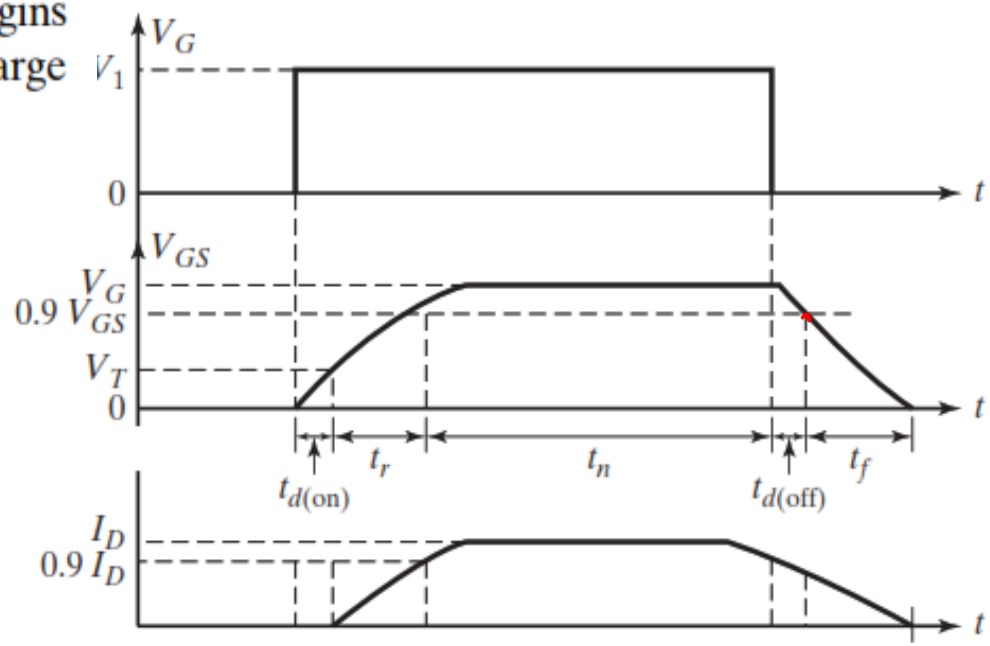
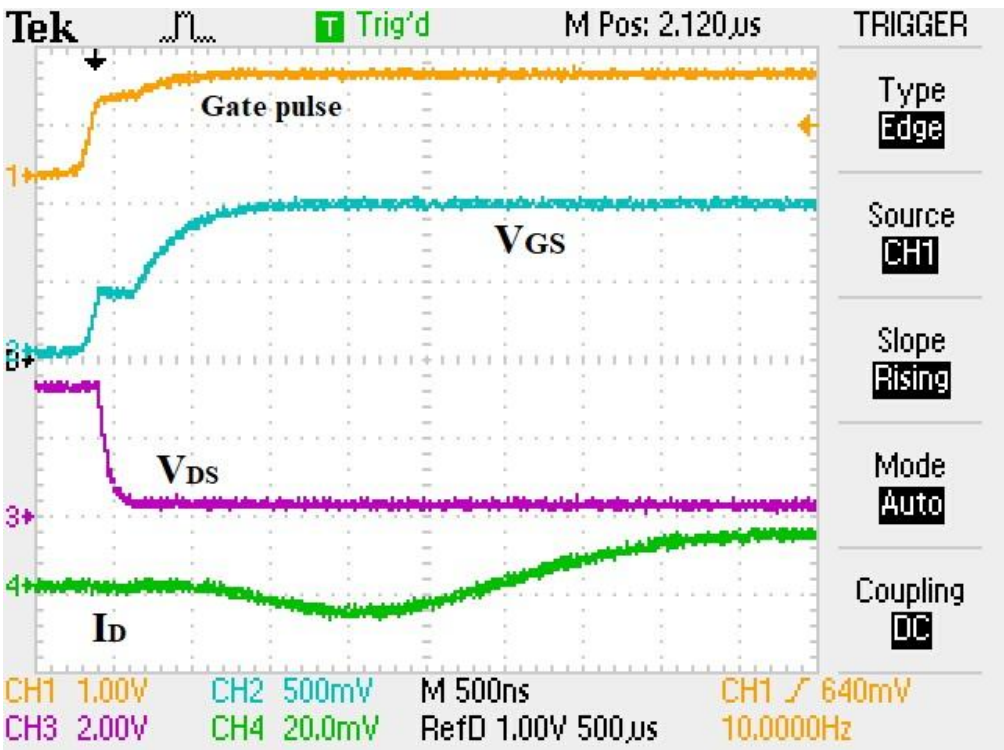
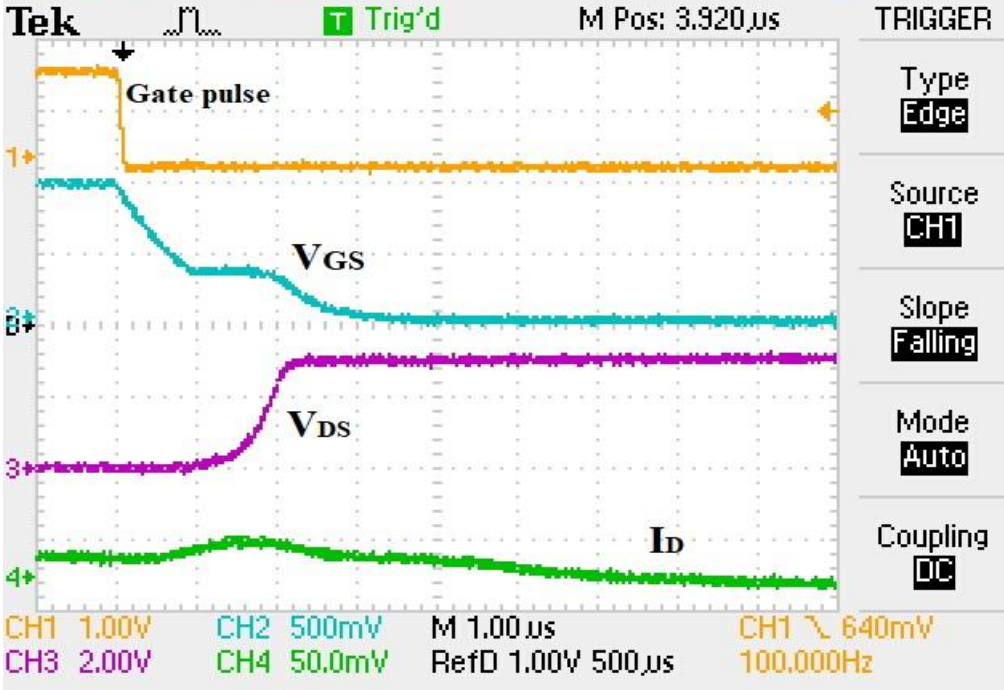


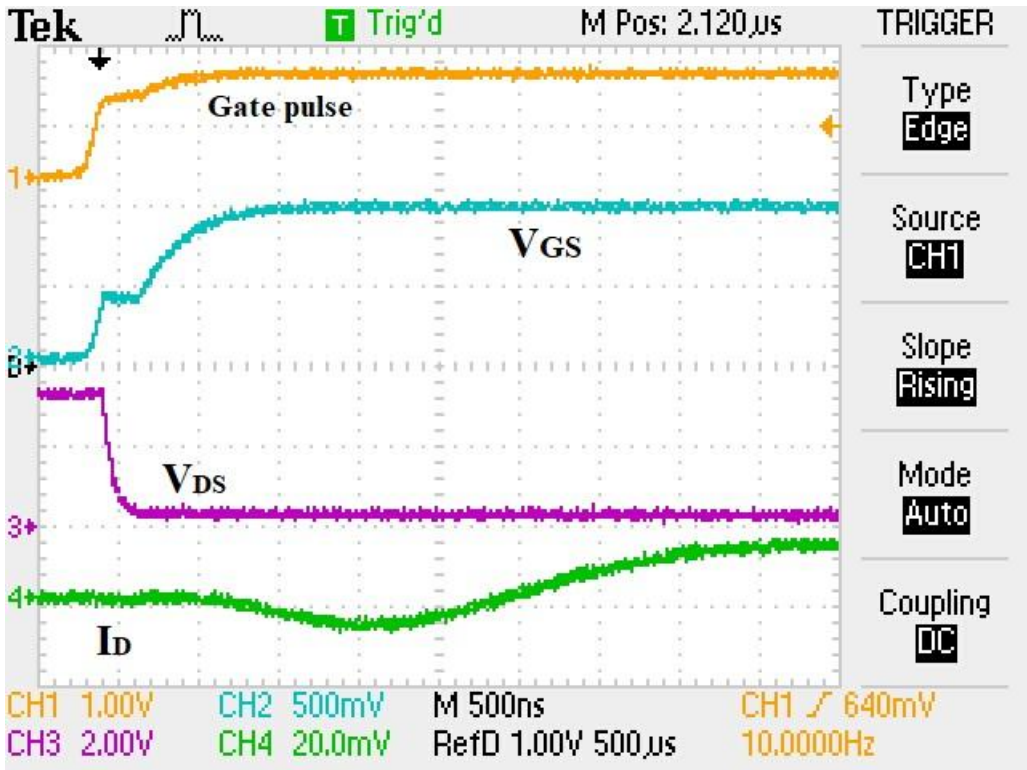
FIGURE 4.10 Switching waveforms and times.

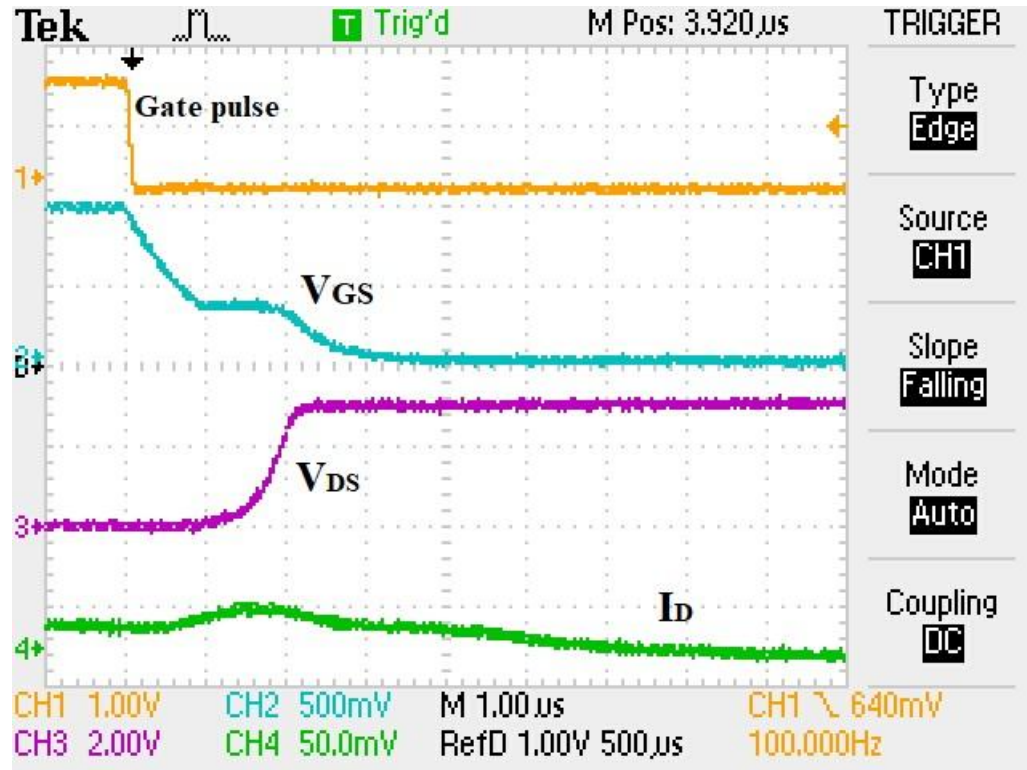
Switching Characteristics

- The **turn-on delay** $t_a(on)$ is the time that is required to charge the input capacitance to threshold voltage level.
- The **rise time** t_r is the gate-charging time from the threshold level to the full-gate voltage *V_GSP*, which is required to drive the transistor into the linear region.
- The **turn-off delay time** $t_a(off)$ is the time required for the input capacitance to discharge from the overdrive gate voltage V_1 to the pinch-off region.
- *V_GS* must decrease significantly before *V_DS* begins to rise.
- The **fall time** *t_f* is the time that is required for the input capacitance to discharge from the pinch-off region to threshold voltage.
- If $V\_GS \leq V\_T$, the transistor turns off.






Tek
Trig'd
M Pos: 2.120µs
TRIGGER
Gate pulse
VGS
VDS
ID
Type
Edge
Source
CH1
Slope
Rising
Mode
Auto
Coupling
DC
CH1 1.00V
CH2 500mV
M 500ns
CH1 640mV
CH3 2.00V
CH4 20.0mV
RefD 1.00V 500µs
10.0000Hz


Tek
Trig'd
M Pos: 3.920µs
TRIGGER
Gate pulse
VGS
VDS
ID
Type
Edge
Source
CH1
Slope
Falling
Mode
Auto
Coupling
DC
CH1 1.00V
CH2 500mV
M 1.00µs
CH1 640mV
CH3 2.00V
CH4 50.0mV
RefD 1.00V 500µs
100.000Hz

Switching Characteristics

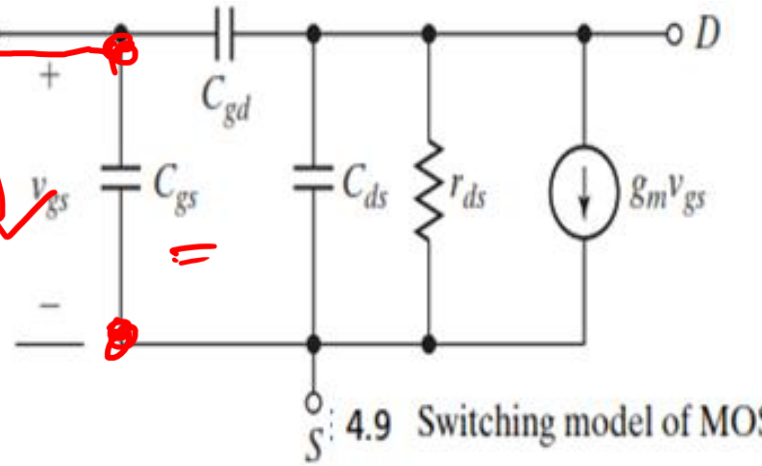


FIGURE 4.9 Switching model of MOSFETs.

The switching model of MOSFETs with parasitic capacitances is shown in Figure 4.9. The typical switching waveforms and times are shown in Figure 4.10. The *turn-on delay* $t_{d(on)}$ is the time that is required to charge the input capacitance to threshold voltage level. The *rise time* t_r is the gate-charging time from the threshold level to the full-gate voltage V_{GSP}, which is required to drive the transistor into the linear region. The *turn-off delay time* $t_{d(off)}$ is the time required for the input capacitance to discharge from the overdrive gate voltage V_1 to the pinch-off region. V_{GS} must decrease significantly before V_{DS} begins to rise. The *fall time* t_f is the time that is required for the input capacitance to discharge from the pinch-off region to threshold voltage. If $V_{GS} \leq V_T$, the transistor turns off.

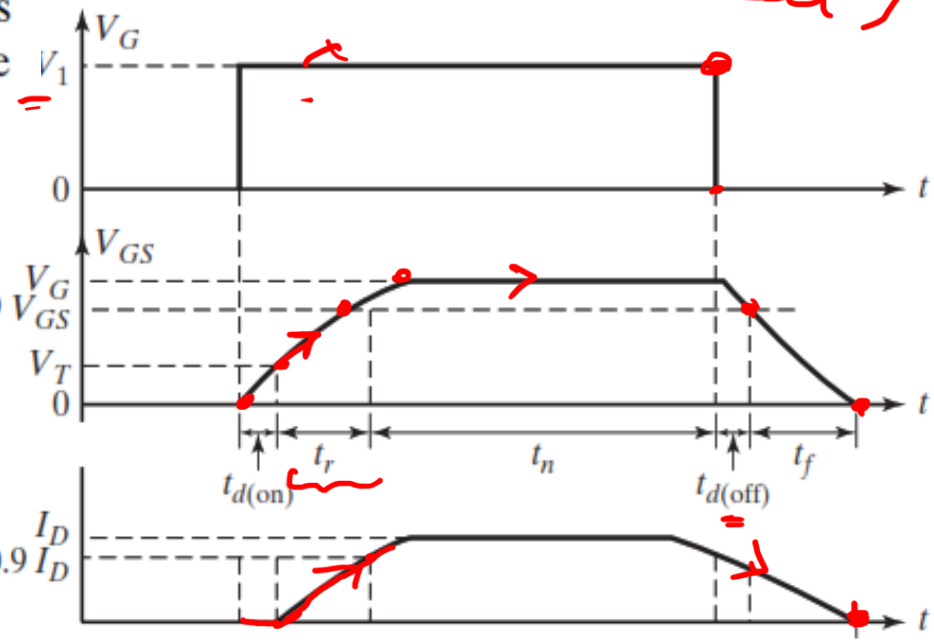
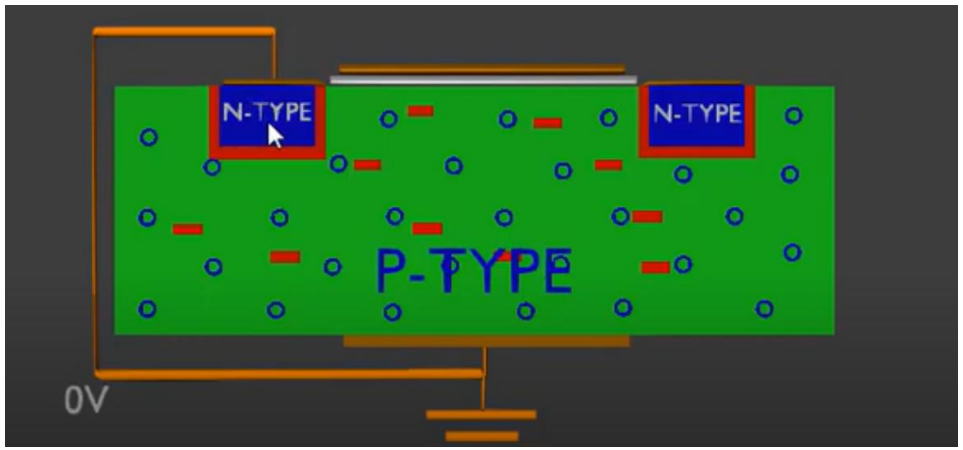
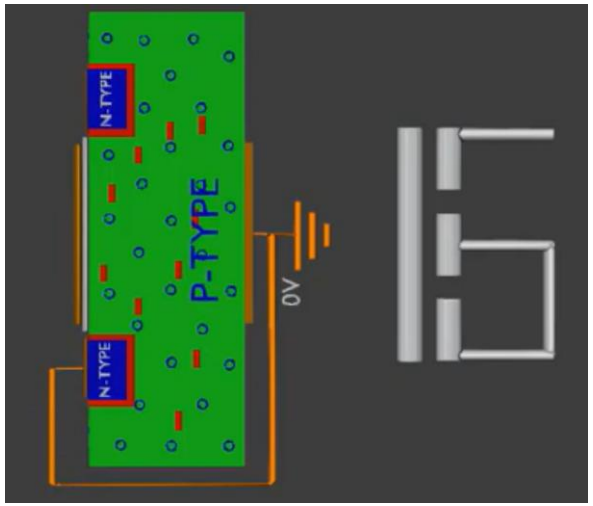
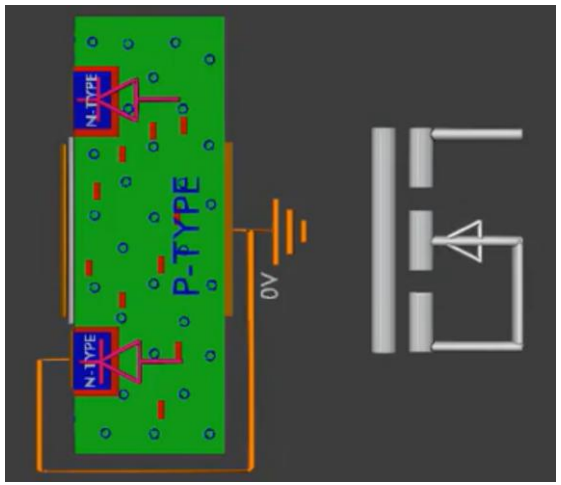


FIGURE 4.10 Switching waveforms and times.

- https://www.youtube.com/watch?v=tz62t-q_KEc
- https://www.youtube.com/watch?v=rkbjHNEKcRw
- https://www.youtube.com/watch?v=p34w6ISouZY&t=163s
- https://www.youtube.com/watch?v=NqnWcv3KXSA


N-TYPE
N-TYPE
P-TYPE
0V


N-TYPE
P-TYPE
0V
N-TYPE


N-TYPE
P-TYPE
0V
N-TYPE