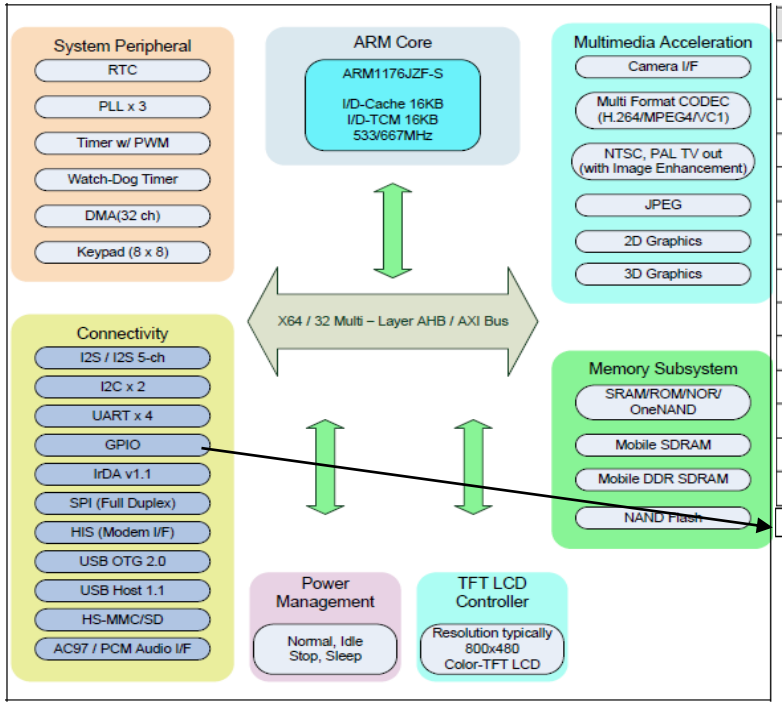
CMPE242 EMBEDDED HARDWARE SYSTEMS LAB1 A

CPU ARCHITECTURE BLOCK DIAGRAM



REGISTER MEMORY MAP

Address		Size(MB)	Description
0x0000_0000	0x07FF_FFFF	128MB	Booting Device Region by XOM Setting
0x0800_0000	0x0BFF_FFFF	64MB	Internal ROM
0x0C00_0000	0x0FFF_FFFF	64MB	Stepping Stone (Boot Loader)
0x1000_0000	0x17FF_FFFF	128MB	SROMC Bank0
0x1800_0000	0x1FFF_FFFF	128MB	SROMC Bank 1
0x2000_0000	0x27FF_FFFF	128MB	SROMC Bank 2
0x2800_0000	0x2FFF_FFFF	128MB	SROMC Bank 3
0x3000_0000	0x37FF_FFFF	128MB	SROMC Bank 4
0x3800_0000	0x3FFF_FFFF	128MB	SROMC Bank 5
0x4000_0000	0x47FF_FFFF	128MB	Reserved
0x4800_0000	0x4FFF_FFFF	128MB	
0x5000_0000	0x5FFF_FFFF	256MB	DRAM Controller of the Memory Port1
0x6000_0000	0x6FFF_FFFF	256MB	
0x7000_0000	0x7F00_FFFF	64KB	AHB, APB BUS

0x7F00_0000	0x7F00_0FFF	TZPC
0x7F00_1000	0x7F00_1FFF	AC97
0x7F00_2000	0x7F00_2FFF	I2S Ch0
0x7F00_3000	0x7F00_3FFF	I2S Ch1
0x7F00_4000	0x7F00_4FFF	I2C
0x7F00_5000	0x7F00_5FFF	UART
0x7F00_6000	0x7F00_6FFF	PWM Timer
0x7F00_7000	0x7F00_7FFF	IrDA
0x7F00_8000	0x7F00_8FFF	GPIO
0x7F00_9000	0x7F00_9FFF	PCM Ch0
0x7F00_A000	0x7F00_AFFF	PCM Ch1
0x7F00_B000	0x7F00_BFFF	SPI0
0x7F00_C000	0x7F00_CFFF	SPI1
0x7F00_D000	0x7F00_DFFF	I2S V40
0x7F00_F000	0x7F00_FFFF	I2C1

GPECON	0x7F008080	R/W	Port E Configuration Register
GPEDAT	0x7F008084	R/W	Port E Data Register
GPEPUD	0x7F008088	R/W	Port E Pull-up/down Register
GPECONSLP	0x7F00808C	R/W	Port E Sleep mode Configuration Register
GPEPUDSLP	0x7F008090	R/W	Port E Sleep mode Pull-up/down Register

REGISTER CONFIGURATION

GPDCON	Bit	Description		Initial State
GPE0	[3:0]	0000 = Input 0010 = PCM SCLK[1] 0100 = AC97 BITCLK 0110 = Reserved	0001 = Output 0011 = I2S CLK[1] 0101 = Reserved 0111 = Reserved	0000
GPE1	[7:4]	0000 = Input 0010 = PCM EXTCLK[1] 0100 = AC97 RESETn 0110 = Reserved	0001 = Output 0011 = I2S CDCLK[1] 0101 = Reserved 0111 = Reserved	0000
GPE2	[11:8]	0000 = Input 0010 = PCM FSYNC[1] 0100 = AC97 SYNC 0110 = Reserved	0001 = Output 0011 = I2S LRCLK[1] 0101 = Reserved 0111 = Reserved	0000
GPE3	[15:12]	0000 = Input 0010 = PCM SIN[1] 0100 = AC97 SDI 0110 = Reserved	0001 = Output 0011 = I2S DI[1] 0101 = Reserved 0111 = Reserved	0000
GPE4	[19:16]	0000 = Input 0010 = PCM SOUT[1] 0100 = AC97 SDO 0110 = Reserved	0001 = Output 0011 = I2S DO[1] 0101 = Reserved 0111 = Reserved	0000

GPEDAT	Bit	Description
GPE[4:0]	[4:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPECON = 0x00000010

GPECON (SPECIAL PURPOSE REGISTER)	BITS	VALUES
GPE0 (INPUT)	[0:3]	0000
GPE1 (OUTPUT)	[7:4]	0001

GPEDAT (SPECIAL PURPOSE REGISTER)
GPE[0] (INPUT BIT)
GPE[1] (OUTPUT BIT)

DEVICE DRIVER CODE (IMPORTED LIBRARIES NOT SHOWN)

```
static long sbc2440_leds_ioctl(struct file *filp, unsigned int cmd, unsigned long arg)
{

    unsigned tmp;
    tmp = readl(S3C64XX_GPEDAT);
    if((tmp & (1<<0))) // If the input bit is logic 1 (Input bit is bit 0)
    {
        tmp |= (1<<1);
        printk("The LED should glow\n");
    }
       else
    {
        tmp &= ~(1<<1);
        printk("The LED should not glow\n");
    }
    writel(tmp,S3C64XX_GPEDAT);
    return 0;

}

static struct file_operations dev_fops = {
    .owner            = THIS_MODULE,
    .unlocked_ioctl    = sbc2440_leds_ioctl,
};

static struct miscdevice misc = {
    .minor = MISC_DYNAMIC_MINOR,
    .name = DEVICE_NAME,
    .fops = &dev_fops,
};
```

```
static int __init dev_init(void)
{
    int ret;

    {
        unsigned tmp;
        writel(0x10, S3C64XX_GPECON);
        printk("GPECON value is %x", tmp);
    }

    ret = misc_register(&misc);

    printk (DEVICE_NAME"\tinitialized\n");

    return ret;
}

static void __exit dev_exit(void)
{
    misc_deregister(&misc);
}

module_init(dev_init);
module_exit(dev_exit);
MODULE_LICENSE("GPL");
MODULE_AUTHOR("Venkat Raja Iyer.");
```