

**Division of Electronics and Communication Engineering  
2024-2025 (ODD SEM)**

**REPORT**  
*for*  
**FPGA BASED SYSTEM DESIGN-PROJECT BASED COURSE**

*Title of the Report: FPGA implementation of Digital circuits*

*A report submitted by*

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**Total marks: \_\_\_\_\_ / 10 Marks**

**Signature of Faculty with date:**

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# CHAPTER 1

## INTRODUCTION

### Introduction to Binary-to-Gray Code Conversion

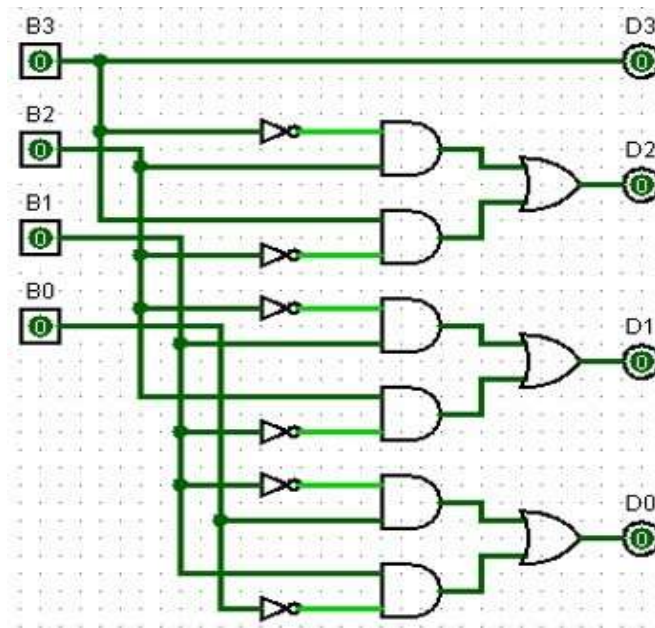
**Binary-to-Gray code conversion** is a fundamental operation in digital systems that transforms binary numbers into their corresponding Gray code representation. Gray code, where only one bit changes between consecutive numbers, is ideal for applications requiring smooth transitions.

#### Key benefits:

- Glitch-free operation
- Error detection
- Simplified hardware implementation

This report will cover the algorithm, Verilog implementation, hardware components, and real-world applications of binary-to-Gray code conversion.

### Structure of Binary-to-Gray Code Conversion



The above circuit converts a 4-bit Gray code input to a 4-bit BCD output using XOR and AND gates. It's useful in systems where Gray code is used and BCD output is required.

### Truth Table of Binary-to-Gray Code Conversion

Natural-binary code				Gray code			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

### Applications of Binary to Gray code conversions

- **Analog-to-digital converters (ADCs):** To reduce glitches and improve accuracy during the conversion process.
- **Rotary encoders:** To provide a smooth and glitch-free output signal.
- **Digital control systems:** To ensure accurate and reliable control signals.
- **Data transmission:** To minimize errors and improve data integrity.

# CHAPTER 2

## IMPLEMENTATION

### CODE:

#### WITH OPTIMIZATION

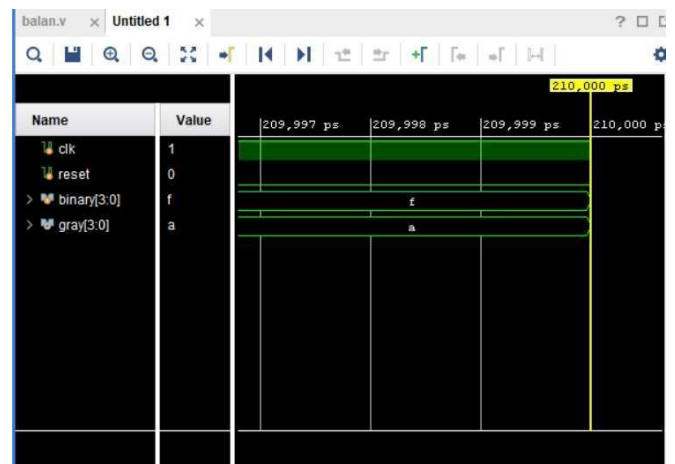
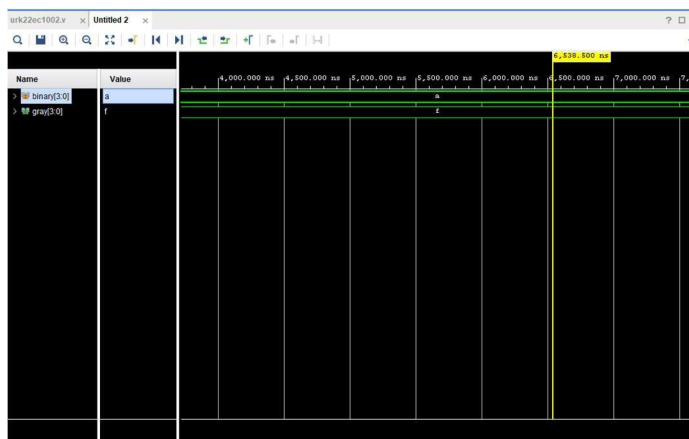
```
binarylogray.v x Zybo-LF-Master.xdc x
D:\lineproject_1\binarylogray.v

1 module binary_to_gray{
2     input wire [3:0] binary,
3     output wire [3:0] gray
4 }
5
6 assign gray[3] = binary[3];
7 assign gray[2] = binary[3] ^ binary[2];
8 assign gray[1] = binary[2] ^ binary[1];
9 assign gray[0] = binary[1] ^ binary[0];
10
11 endmodule
```

#### WITHOUT OPTIMIZATION

```
C:\Users\ACER\bin\balan\src\resources_1\threewban.v

1 module binary_to_gray_pipeline {
2     input wire clk,
3     input wire reset, // Active-high reset
4     input wire [3:0] binary,
5     output reg [3:0] gray
6 }
7
8 // Intermediate registers for pipeline
9 reg [3:0] stage1;
10 reg [3:0] stage2;
11 reg [3:0] stage3;
12
13 always @(posedge clk or posedge reset) begin
14     if (reset) begin
15         stage1 <= 4'b0;
16         stage2 <= 4'b0;
17         stage3 <= 4'b0;
18     end else begin
19         // Stage 1: Pass binary input
20         stage1[3] <= binary[3];
21         stage1[2] <= binary[2];
22         stage1[1] <= binary[1];
23         stage1[0] <= binary[0];
24     end
25 end
```



## SIMULATION:

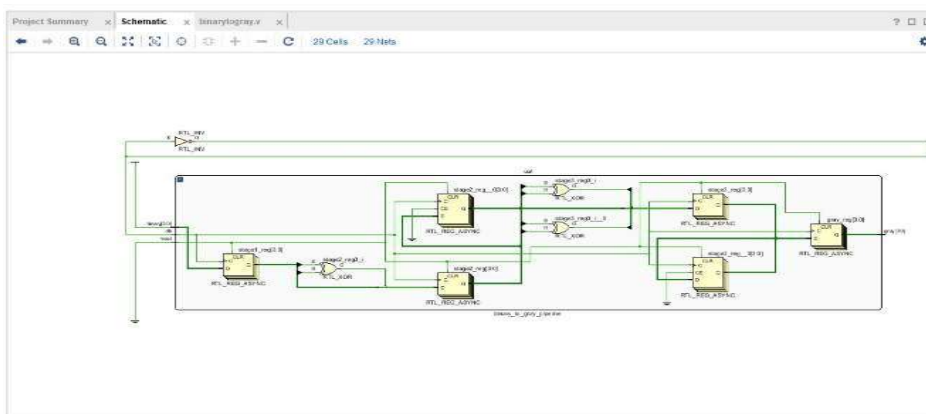
## SYNTHESIZE THE DESIGN:

- After writing the code, click **Run Synthesis** in the **Flow Navigator**.
- If there are any errors in your code, resolve them and rerun the synthesis.

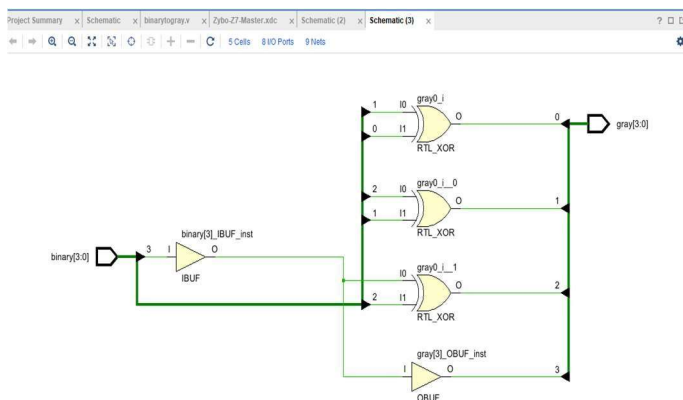
## IMPLEMENT THE DESIGN:

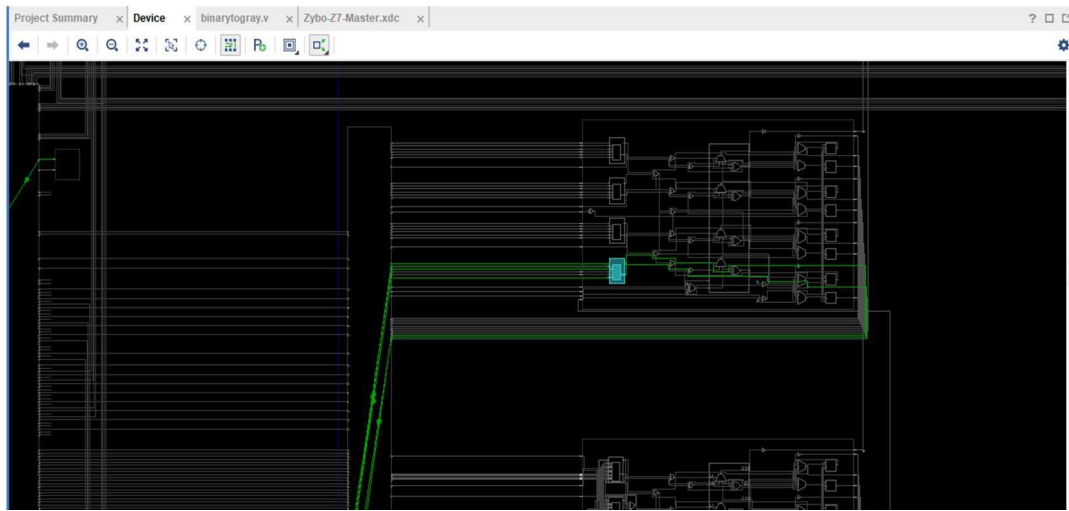
Once synthesis is complete, click **Run Implementation** in the **Flow Navigator**.

- This step maps your design to the actual FPGA resources.



## After





### GENERATE BITSTREAM:

- After the implementation is completed, click **Generate Bitstream**. This generates the .bit file, which is required to program your FPGA.
- If prompted to save the design, click **Yes**.

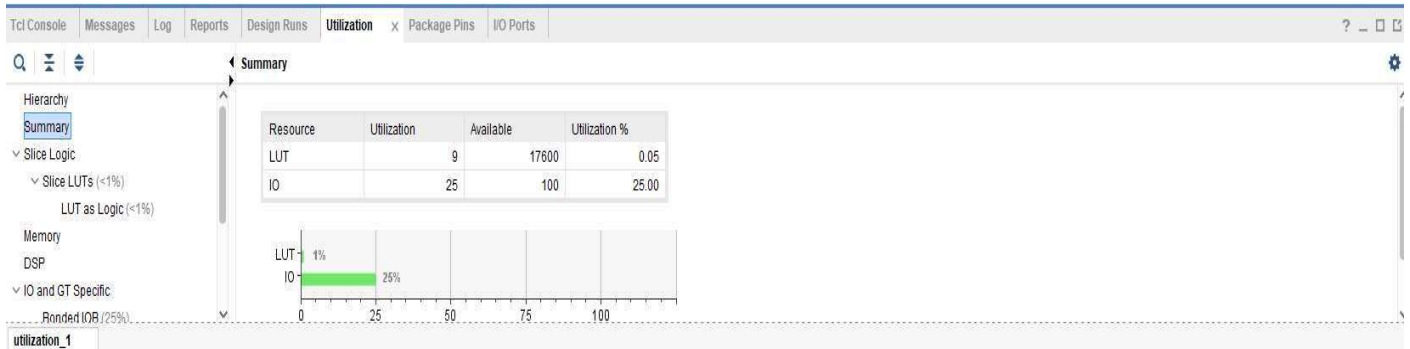
### CONFIGURE THE FPGA (DOWNLOAD BITSTREAM):

- Once the bitstream file is generated, open the **Hardware Manager** by clicking **Open Hardware Manager** in the Flow Navigator.
- Click **Open Target** > **Auto Connect** to connect to your FPGA board.
- After the board is connected, click **Program Device** and select the generated bitstream file (.bit).

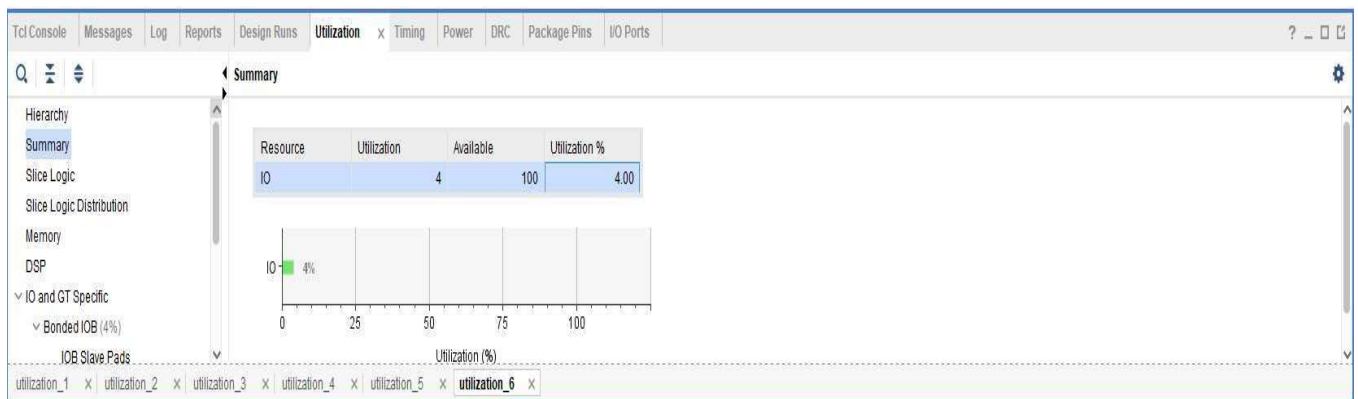
# CHAPTER 4

## CONCLUSION

### BEFORE OPTIMIZATION



### AFTER OPTIMIZATION





**CHATPER 4**  
**CONCLUSION**

**TABULATION**

CODE	IUT USED	IOB USED
ORIGINAL CODE	9	25
MODIFIED	1	4

## **CHAPTER 4**

### **CONCLUSION**

This report has explored the concept of binary-to-Gray code conversion, a fundamental operation in digital systems. We have discussed the algorithm, Verilog implementation, hardware components, and real-world applications of this conversion.

Gray code offers several advantages, including glitch-free operation, error detection, and simplified hardware implementation. By understanding the principles and techniques involved in binary-to-Gray code conversion, you can design and implement digital systems that require precise and reliable operation