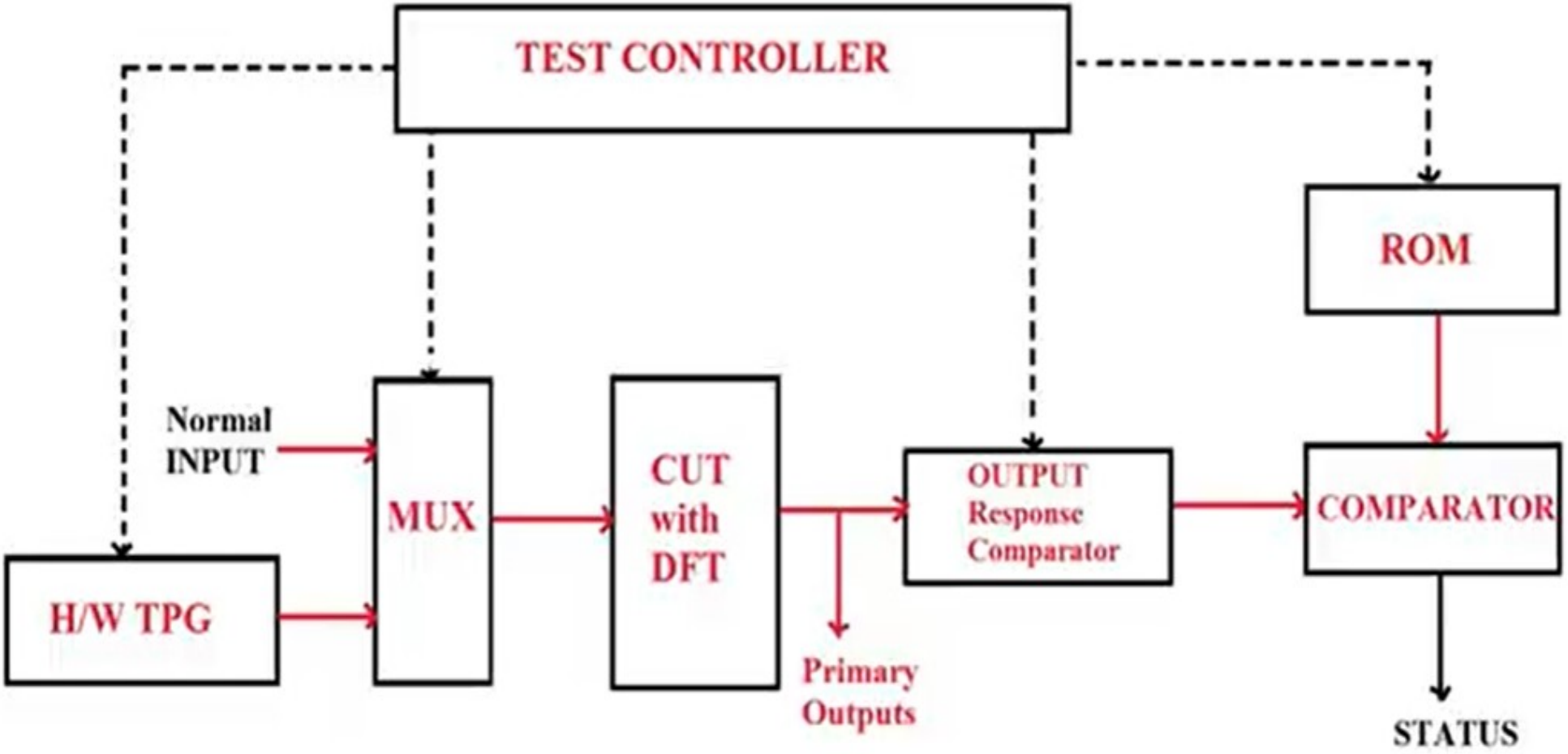
Built in Self Test(BIST)

Introduction:

- It is technique of designing additional hardware and software into integrated circuit to allow them to perform self testing.
- Aim of BIST technique is to avoid costly use of ATE(Automated test Equipment)testing.
- As IC's are getting complex ,many blocks are interfaced in IC with analog and Digital ports, in that ATE testing is difficult and costly service.
- BIST is also useful to those blocks of IC which has no direct connection with external pins .
- As IC's are upgrading ,in future conventional testers will no longer be adequate for the latest and fastest chip.

BIST Architecture:



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- The essential circuit models required for BIST

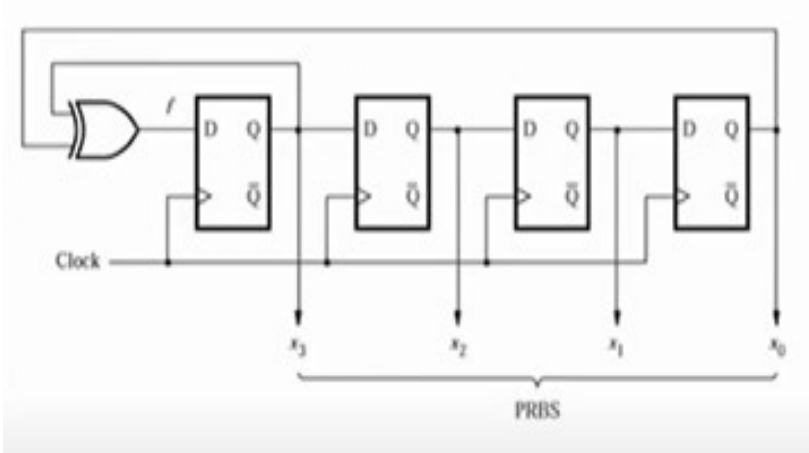
  (1).Pseudo Random pattern generator(PRPG)

  (2).Signature analyser

These two modules can be implemented with a linear Feedback shift Register.

❖ Pseudo Random pattern generator(PRPG):

- A practical approach for generating the test vector on-chip is to use pseudorandom tests.
- The generator for pseudorandom tests is easily constructed using a feed back shift register.
- The circuit is representative of a class of circuit known as linear feedback shift register



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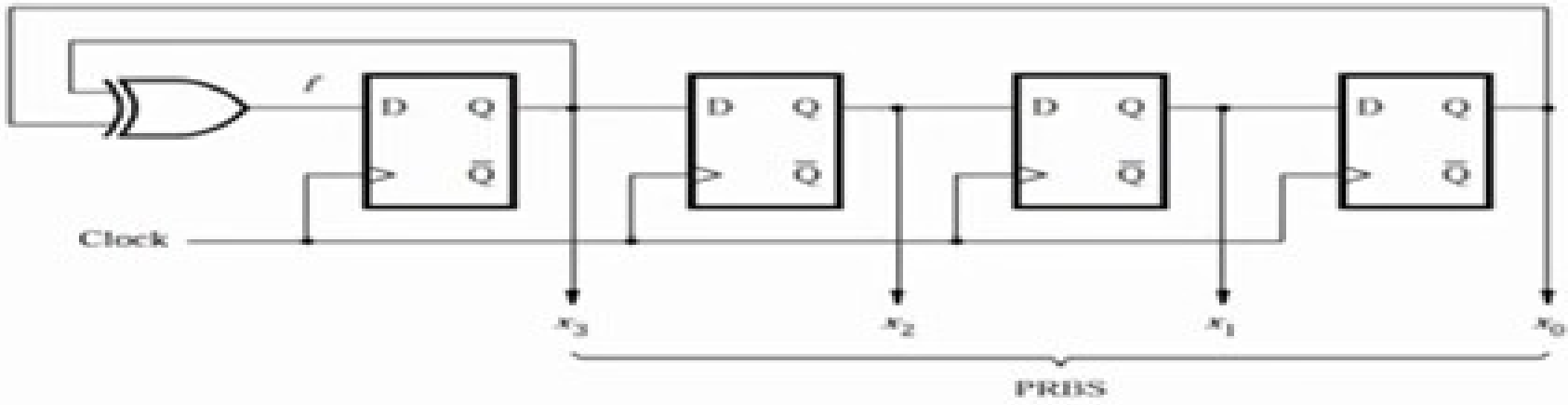

x3	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0	1
x2	0	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0
x1	0	0	1	1	1	1	0	1	0	1	1	0	0	1	0	0
x0	0	0	0	1	1	1	1	0	1	0	1	1	0	0	1	0
f	1	1	1	0	1	0	1	1	0	0	1	0	0	0	1	1

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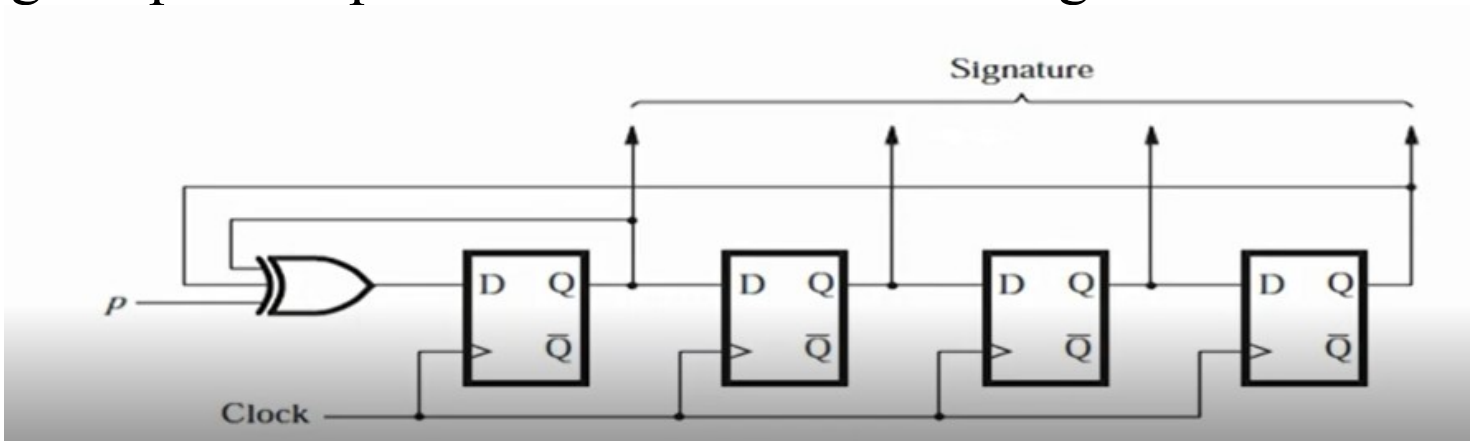
❖Signature analyser:

- To reduce the chip area data compression schemes are used.one of the popular data compression schemes is signature analysis, which is based on the concept of cyclic redundancy checking.
- The single input compressor circuit as shown in figure



- Not attractive to store a large number of responses to the tests on a chip.
- Practical solution is to compress the results of the tests.
- Can be done using an LFSR circuit.

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- After applying a number of test vectors, the resulting values of p drive the SIC and coupled with the LFSR functionality, produce a four-bit pattern.
- The pattern generated by the SIC is signature of the tested circuit for the given sequence of tests.
- The signature can be compared against a predetermined pattern to see if the tested circuit is working properly.

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❖Advantages:

- It lower testing cost.
- Testing is independent on future technology
- Better fault coverage
- Shorter test time

❖Disadvantages:

- Additional circuit (silicon area)for BIST testing in IC
- Additional pin required for BIST testing in IC
- On chip testing may get failed then how to test it.