10T Hybrid XOR-XNOR Full Adder Logic Style Performance Comparison

R. Advaith[#1], J. Venkatesh[#2], Nukilan J.[#3], Bharath Vaaishnav T. B.[#4]

[#]*Vellore Institute of Technology, Chennai Campus*

Under the Guidance of Dr. S Umadevi

[1] advaith.r2023@vitstudent.ac.in; 23BEC1205

[2] venkatesh.j2023@vitstudent.ac.in; 23BEC1231

[3] nukilan.j2023@vitstudent.ac.in; 23BEC1072

[4] bharath.vaaishnav2023@vitstudent.ac.in; 23BEC1022

Abstract— **This paper investigates the timing and power characteristics of full adder circuits through comprehensive transient simulations. The study focuses on propagation delays in critical paths (sum and carry chains) and analyses dynamic power dissipation under varying operational patterns. Delay measurements reveal both nominal and anomalous behaviours, with the latter suggesting potential metastability or measurement edge cases. Power analyses are done based on pattern-dependent stimulus and power spectrums. The results provide insights into design trade-offs between performance and power efficiency, with implications for clock network optimization and power management in nanoscale integrated circuits. The 10T XNOR and XOR full adder cells have been compared using the mentioned metrics. The software tools used for this analysis are Linux operated computing system, Cadence® Virtuoso, gpdk 180nm technology and analogLib libraries.**

Keywords— **Digital circuits, propagation delay, dynamic power, metastability, transient analysis, VLSI design, Cadence Virtuoso, 180nm technology**

I. Introduction

The full adder (FA), being a foundational component of arithmetic circuits like multipliers and ALUs, plays a pivotal role in determining overall system performance. Among the various FA implementations, hybrid logic styles have emerged as a preferred approach due to their ability to balance power, speed, and area.

This report investigates the performance characteristics—specifically delay and power—of full adder designs based on a novel 10-transistor (10T) XOR–XNOR logic cell. The 10T design aims to provide simultaneous full-swing XOR and XNOR outputs with minimal power-delay product (PDP), making it a promising candidate for low-power and high-speed applications. Two hybrid full adder configurations, referred to as Design 3 (FA3) and Design 4 (FA4) from the reference study, are analysed. These designs utilize the 10T XOR–XNOR cell combined with distinct SUM and CARRY generation modules, enabling a meaningful comparative evaluation. With the literature review, one of the research serves as the basis for this project report while others were used for reference to narrow down the analysis to meaningful comparison parameters.

The simulations and analyses presented in this report were conducted using the Cadence Virtuoso tool suite, employing the GPDK 180nm CMOS technology node. Delay patterns and average power consumption are the principal metrics used to assess the performance of each adder design. Delays are calculated based on the Elmore concept of worst-case scenario path for toggling outputs. Further, we calculated the average delay for the functionality of the whole circuit and compared the derived results to determine which circuit would be a better choice for any application. Through this comparative study, we aim to identify which configuration offers superior trade-offs for scalable VLSI applications, particularly in cascaded and low-voltage environments. The two designs are illustrated below [1].

FIGURE I
DESIGN 1 CIRCUIT DIAGRAM

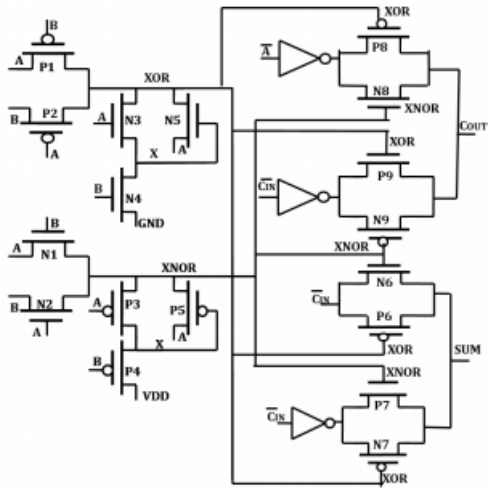
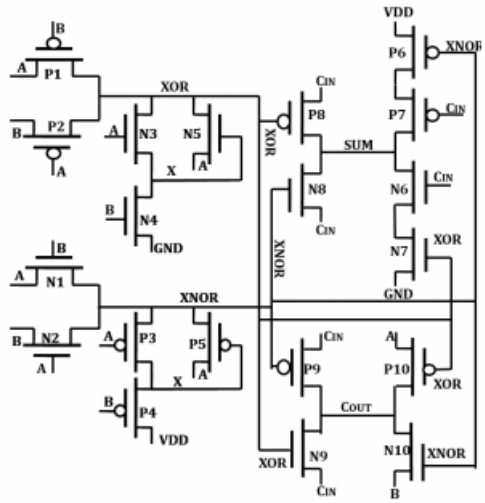


FIGURE II
DESIGN 2 CIRCUIT DIAGRAM



II. Literature Review

Jyoti Kandpal, Abhishek Tomar, Member, IEEE, Mayur Agarwal, Member, IEEE, and K. K. Sharma[1] presented us four designs for the implementation of high-speed 10T driven XOR-XNOR logic for a full adder cell. Their research forms the basis for this report.

A comprehensive study by Khatun et al. (2023)[2] compared multiple hybrid full adder cells across different technology nodes including 180nm, using Cadence Virtuoso. Their analysis provided critical insights into delay, power, and power-delay product (PDP), establishing a baseline for performance across technology scales.

Annarose et al. (2022)[3] presented a comparative analysis between MOSFET and FINFET based hybrid adders implemented in 180nm and 32nm nodes using Cadence Virtuoso. They highlighted that Transmission Gate Adders offered better performance in terms of delay compared to other hybrid designs.

Another significant contribution came from Maryan et al. (2021)[4] who introduced a technique using input-controlled leakage restrainer transistors to reduce leakage and short-circuit power in 1-bit hybrid full adders. Their work, simulated in a deep submicron CMOS process, showed substantial reductions in power and PDP.

Kishore and Krishna (2023)[5] focused on designing a Voltage Difference Transconductance Amplifier using both GPDK 180nm and FINFET technologies within Cadence Virtuoso. Their comparison offered insights into the power efficiencies achievable with different technological adaptations.

Lastly, S and Monica (2022)[6] proposed an energy-efficient row bypassing scheme for binary multipliers implemented in gpdk 180nm. Their design showed notable improvements in power and delay metrics, validating the efficacy of targeted circuit modifications in this technology node.

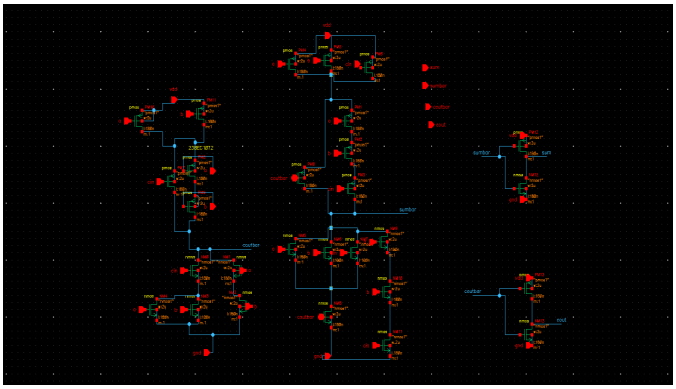
III. Circuit Simulations and Methodology

The three circuits taken into consideration are the static-CMOS designed 28 transistor full adder, design 1 which contains one variant of the 10T XOR-XNOR driven full adder cell and design 2 which is also another variant of a similarly driven full adder cell. First, the circuits were designed by generating the Cadence schematics and the outputs were verified by input stimulus.

A. 28T Full Adder

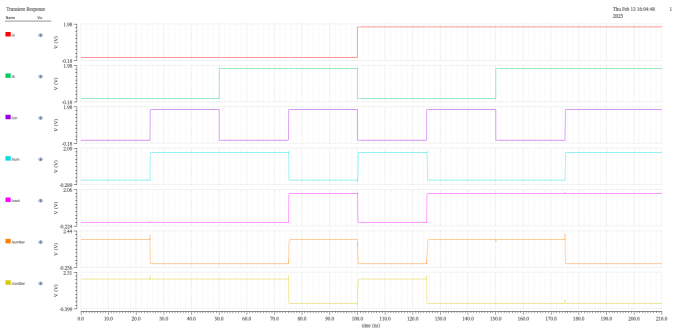
The simplified full adder using 28T logic has been implemented using static CMOS logic using the Cadence tools. The schematic is as follows:

FIGURE III
28T Static CMOS Full Adder Schematic



This circuit has been simulated to verify its functionality. The simulation graph generated is pasted as follows:

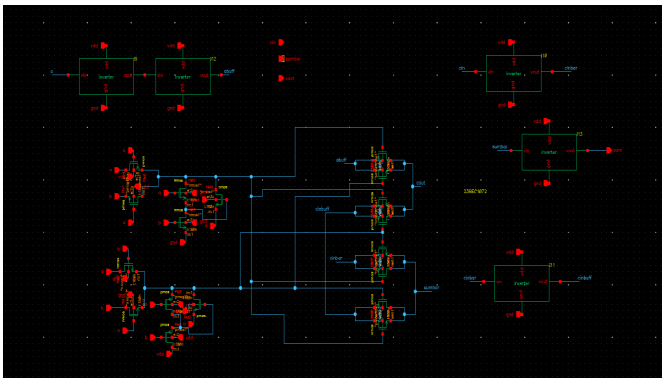
FIGURE IV
28T Static CMOS Simulation



B. Design 1 Full Adder

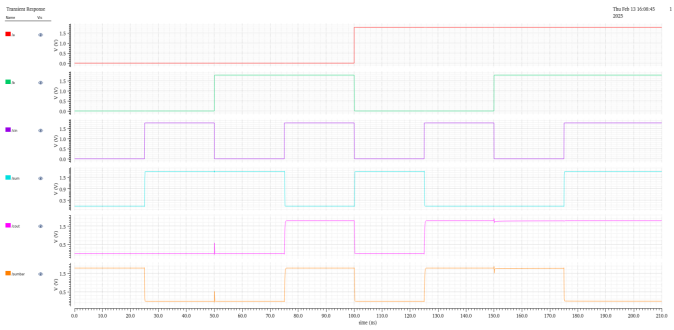
The first design that is taken into consideration is as follows:

FIGURE V
DESIGN 1 SCHEMATIC



The functionality of the circuit has been verified by input stimuli. The results are plotted in a graph as follows:

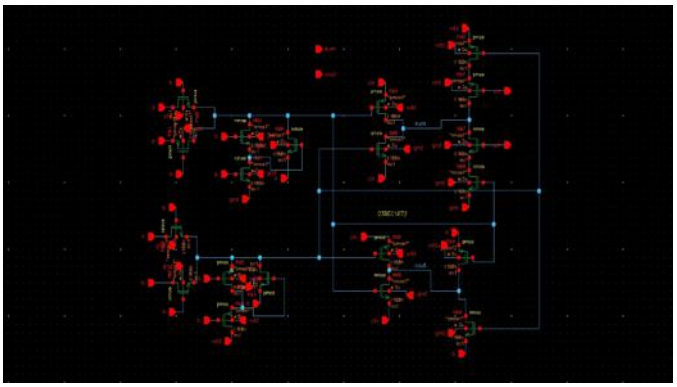
FIGURE VI
DESIGN 1 SIMULATION



C. Design 2 Full Adder

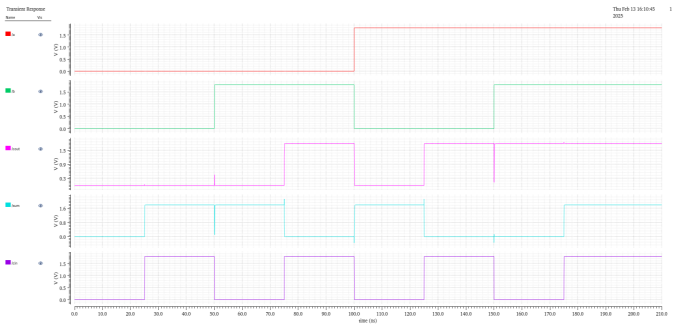
The second design taken for comparison is as follows:

FIGURE VII
DESIGN 2 SCHEMATIC



Again, by stimulating inputs, the functionality of the full adder was verified as follows:

FIGURE VIII
DESIGN 2 SIMULATION



The circuits were compared based on these performance metrics:

- Delays for alternating inputs
- Overall average power consumed for computation

The power spectrums have also been generated, and the waveform was used to find out the average power of the respective full adder circuits. All the power spectrums are as follows:

FIGURE IX
28T FULL ADDER POWER SPECTRUM

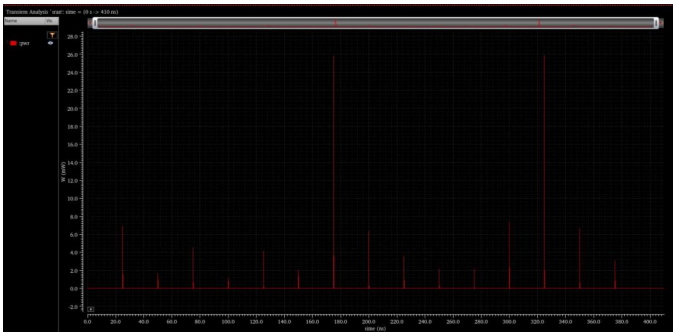


FIGURE X
DESIGN 1 POWER SPECTRUM

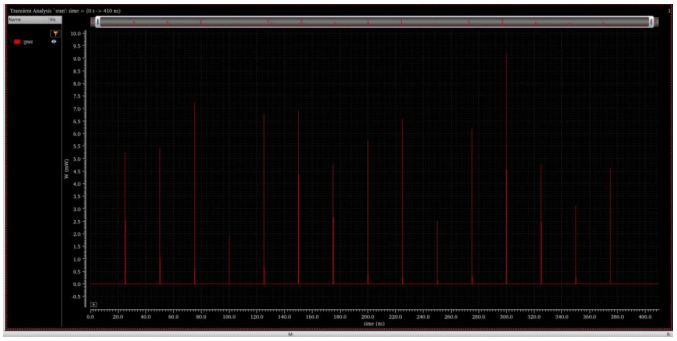
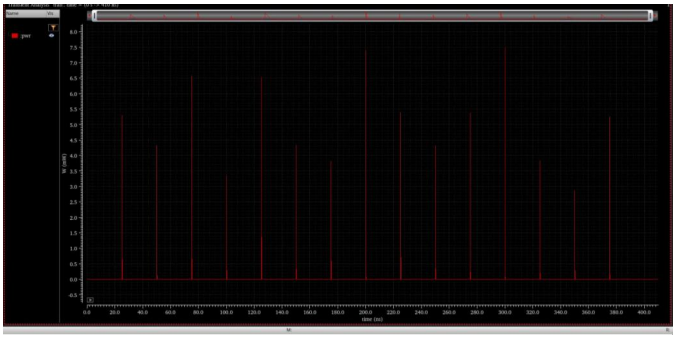


FIGURE XI
DESIGN 2 POWER SPECTRUM



IV. COMPARISON RESULTS AND DISCUSSION

The comparison metrics are evaluated using Cadence calculator formulae. The input patterns for the sum and carry are same for all the three full adder cells. The input patterns are stimulated in such a way that the outputs toggle to get the rising and falling edges. The delays are calculated with the respective edges between input and output waveforms.

A. 28T Full Adder

The 28-transistor full adder cell is already implemented, and the outputs are verified. The delays are calculated for toggling outputs. All the results have been tabulated in Table V and Table VI.

B. Design 1 Full Adder Cell

The circuit schematic given in Figure I is implemented on Cadence by designing the schematic and then with the same input stimulus as 28T full adder, the delays are compared, and the powers were evaluated as well. The delays are tabulated in Table I and Table II.

TABLE I
DESIGN 1 SUM DELAYS

Input Patterns			**Output**	**Delays (in pico-seconds)**
A	**B**	**C**		
0	0	1	1	103.9
1	1	0	0	134.7
0	1	0	1	161.5
1	0	1	0	161.1
1	0	0	1	161.6
0	1	1	0	125.7
1	1	1	1	129.3
0	0	0	0	

TABLE III
DESIGN 1 CARRY DELAYS

Input Patterns			**Output**	**Delays (in pico-seconds)**
A	**B**	**C**		
0	1	1	1	112.3
1	0	0	0	118.2
1	0	1	1	145.0
0	1	0	0	118.0
1	1	1	1	114.1
0	0	0	0	80.38
1	1	0	1	80.02
0	0	1	0	78.27

TABLE IIIII
DESIGN 2 SUM DELAYS

Input Patterns			**Output**	**Delays (in pico-seconds)**
A	**B**	**C**		
0	0	1	1	103.9
1	1	0	0	75.60
0	1	0	1	161.5
1	0	1	0	161.1
1	0	0	1	161.6
0	1	1	0	125.7
1	1	1	1	129.3
0	0	0	0	

TABLE IVV
DESIGN 2 CARRY DELAYS

Input Patterns			**Output**	**Delays (in pico-seconds)**
A	**B**	**C**		
0	1	1	1	112.3
1	0	0	0	118.2
1	0	1	1	145.0
0	1	0	0	118.0
1	1	1	1	114.1
0	0	0	0	80.38
1	1	0	1	80.02
0	0	1	0	78.27

TABLE V
28T F.A. SUM DELAYS

Input Patterns			**Output**	**Delays (in pico-seconds)**
A	**B**	**C**		
0	1	1	1	191.6
1	0	0	0	235.0
1	0	1	1	170.7
0	1	0	0	230.3
1	1	1	1	166.7
0	0	0	0	107.7
1	1	0	1	181.0
0	0	1	0	

TABLE VI
28T F.A. CARRY DELAYS

Input Patterns			**Output**	**Delays (in pico-seconds)**
A	**B**	**C**		
0	1	1	1	67.2
1	0	0	0	103.7
1	0	1	1	70.23
0	1	0	0	128.4
1	1	1	1	41.04
0	0	0	0	88.84
1	1	0	1	84.03
0	0	1	0	186.3

TABLE VII
AVERAGE POWERS

Design	Average Power (µW)
28T Full Adder	3.292
Design 1	8.598
Design 2	4.626

C. Design 2 Full Adder Cell

The circuit schematic given in Figure I is implemented on Cadence by designing the schematic and then with the same input stimulus as 28T full adder, the delays are compared, and the powers were evaluated as well. The delays are tabulated in Table III and Table IV.

D. Delay Comparison and Discussions

1) *28T Full Adder:* With the delays tabulated, the average delay of sum is evaluated to be 183.28. Similarly, the average delay for carry is 109.96.

2) *Design 1 Full Adder Cell*: With the delays tabulated, the average delay of sum is evaluated to be 139.68. Similarly, the average delay evaluated for carry is 131.24.

3) *Design 2 Full Adder Cell:* With the delays tabulated, the average delay of sum is evaluated to be 131.24. Similarly, the average delay evaluated for carry is 120.89.

E. Powers

From Table VII, it can be inferred that the 28T Full Adder gives the least power. The 10T XOR-XNOR logic designs produce lesser delays but generates more power. This power is evaluated using the average function on the power spectrum graphs. The power spectrums for all the three circuits are given in Figure IX, X and XI, respectively.

F. Results

From the average powers, the following inferences can be made:

- 28T full adder consumes the least power among the three designs.
- Design 1 takes up the most power, taking close to 8.6 µW (average power consumption).

From the delays calculated, the following inferences can be made:

- The average delays in sum of design 1 and 2 are significantly lesser than the 28T full adder, proving its high-speed characteristics.
- There is a minor increase in the delay in carry production in design 1 and 2 as compared to the 28T CMOS logic. However, the lesser time in producing sum significantly outweighs the slight delay in carry production.

Thus, depending on the requirement of the project, an appropriate choice can be made between these full adder designs.

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We would also like to acknowledge the VIT Chennai Laboratory facilities, particularly for the provision and access to Cadence Design Tools, which were essential for the design, simulation, and analysis phases of this VLSI project. We would also like to sincerely thank all the authors of this project report for their dedication.

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[2] Khatun et al., 2023, "Comparative analysis of Hybrid adders with different Technology node using cadence virtuoso", *IEEE ICECCT*

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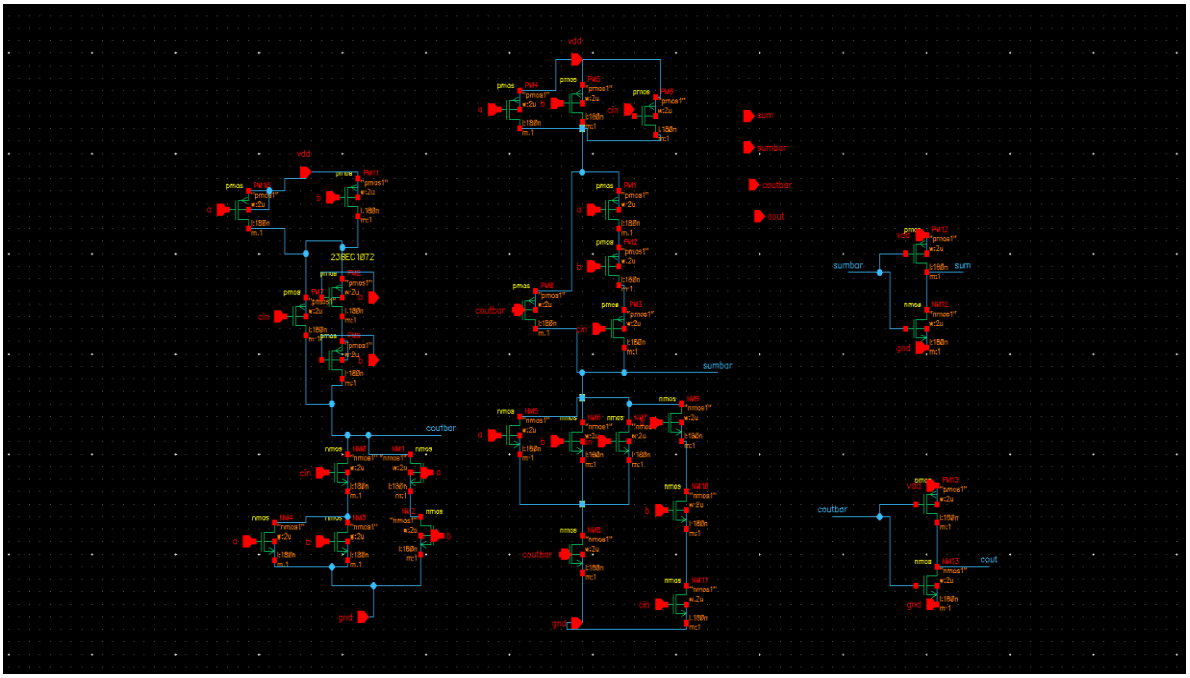
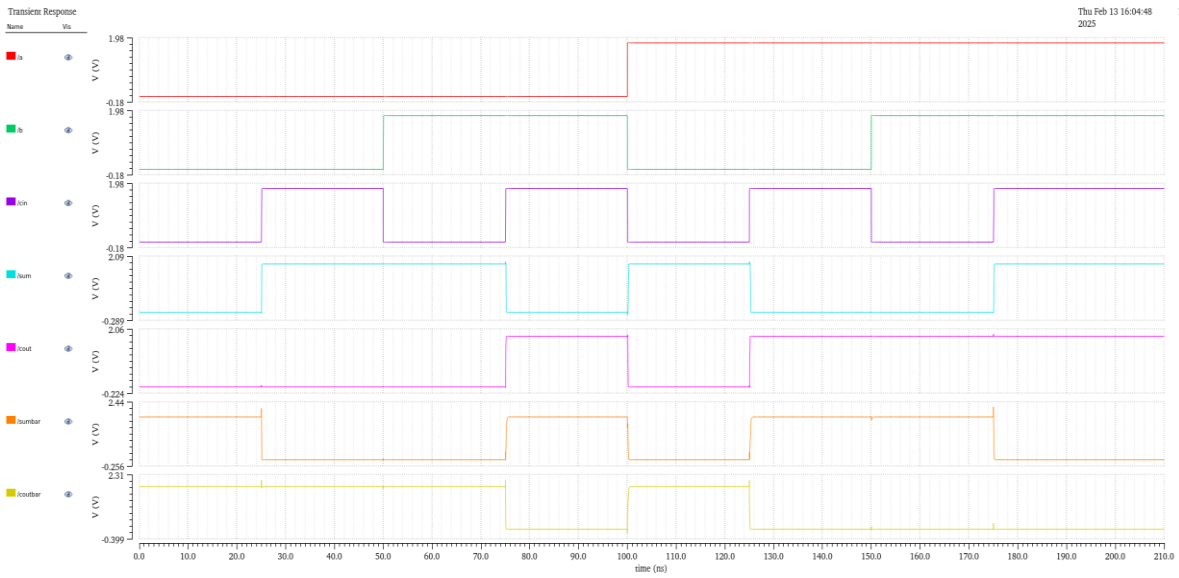
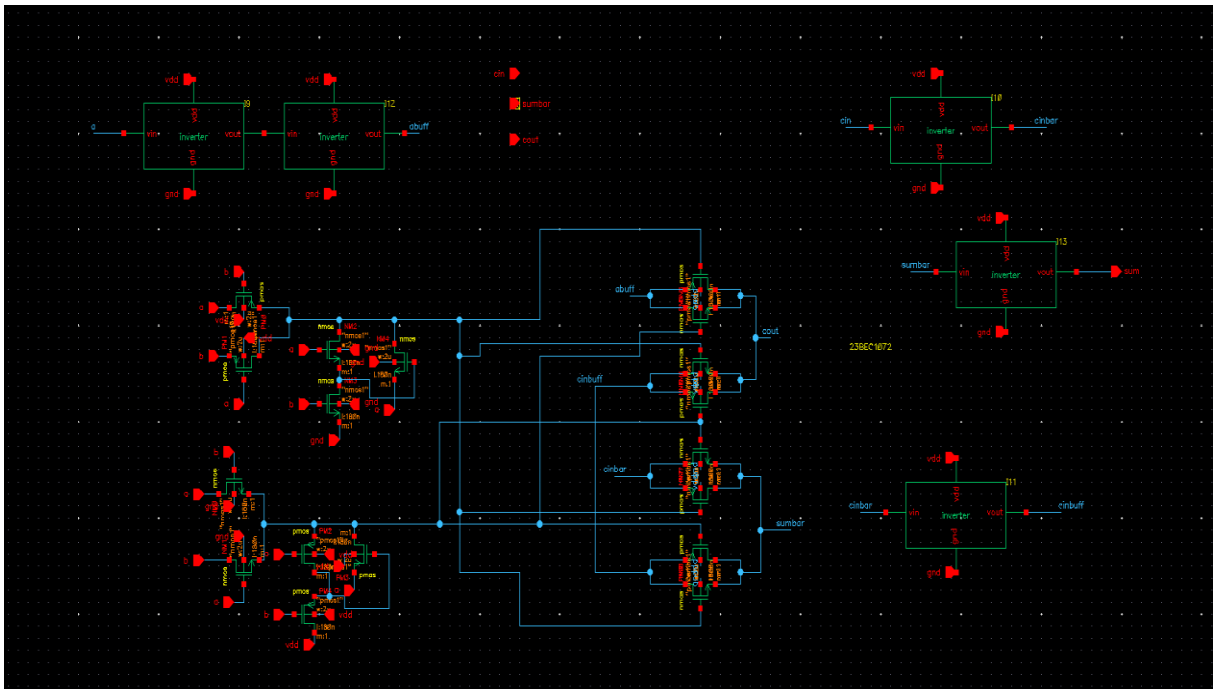
[5] Kishore & Krishna, 2023, "Design and analysis of Voltage Difference Transconductance Amplifier (VDTA) at FINFET CMOS technology", *i-manager's Journal on Circuits and Systems.*

[6] S & Monica, 2022, "Energy Efficient Row Bypassing Scheme for Low Power Binary Multipliers", *IEEE iSES.*

ENLARGED GRAPHS AND SCHEMATICS (IN CHRONOLOGICAL ORDER)



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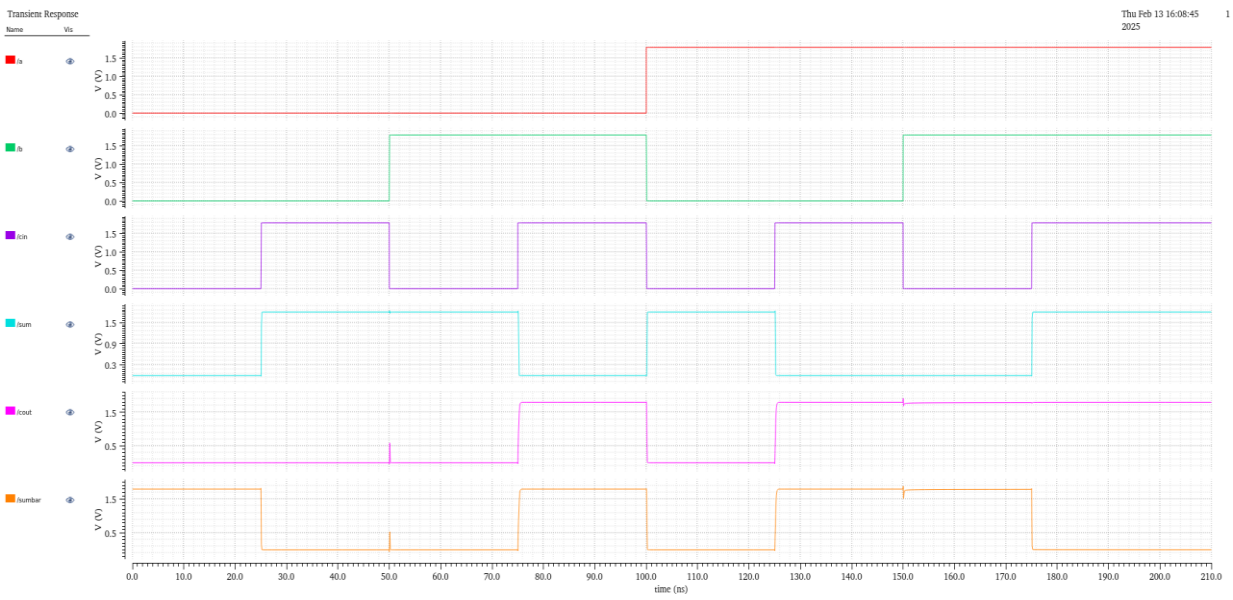
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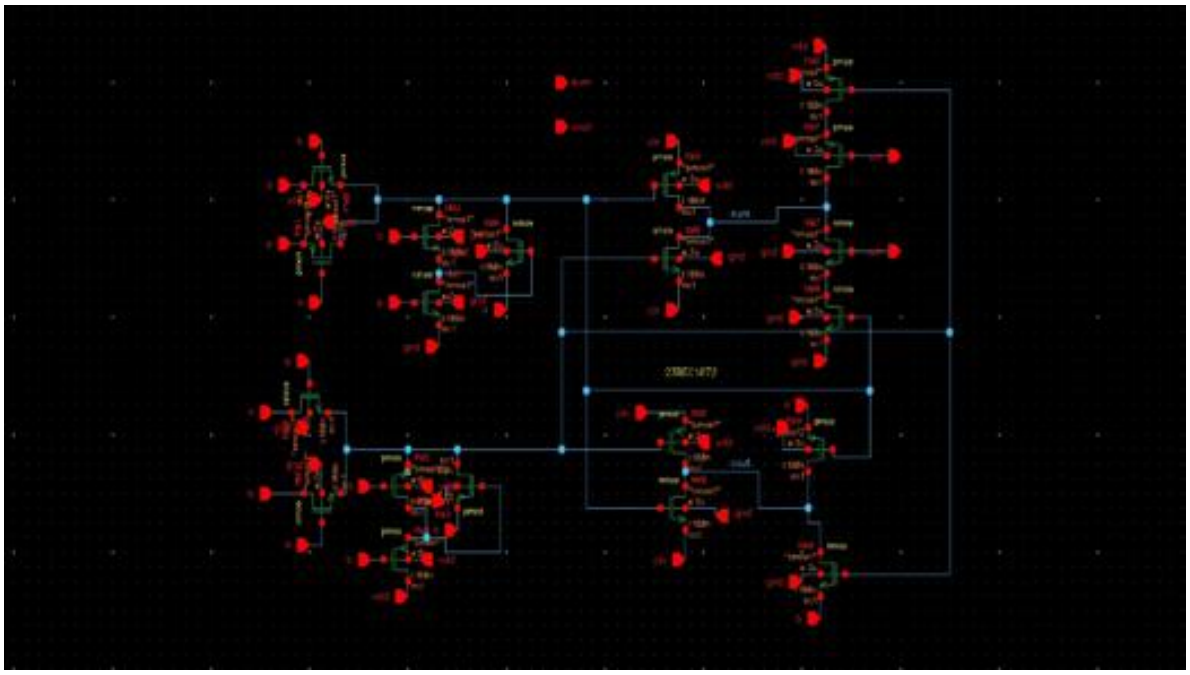

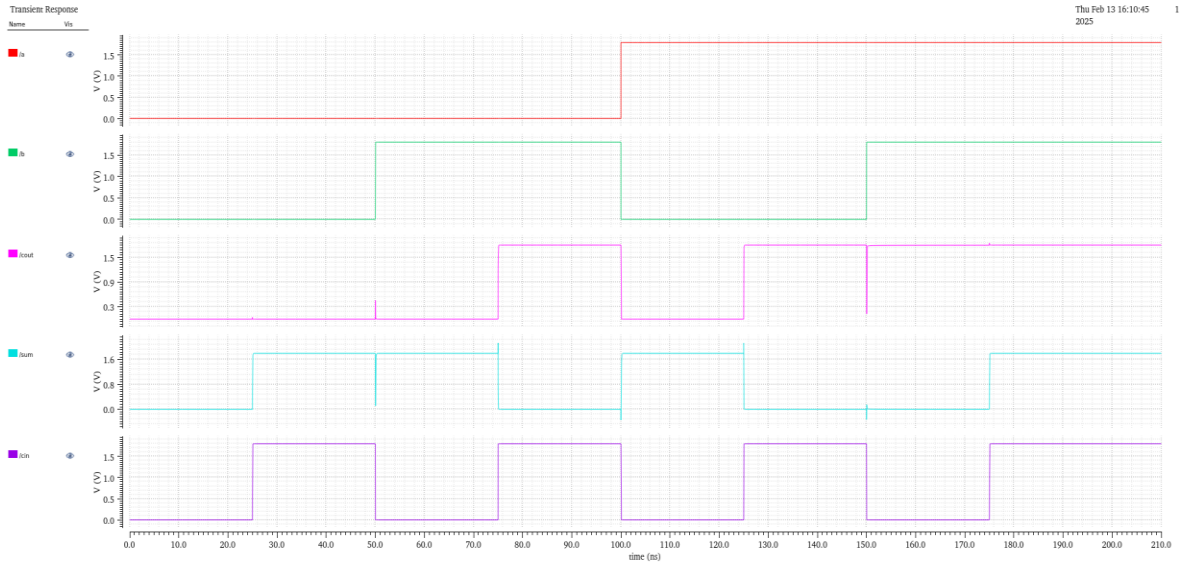
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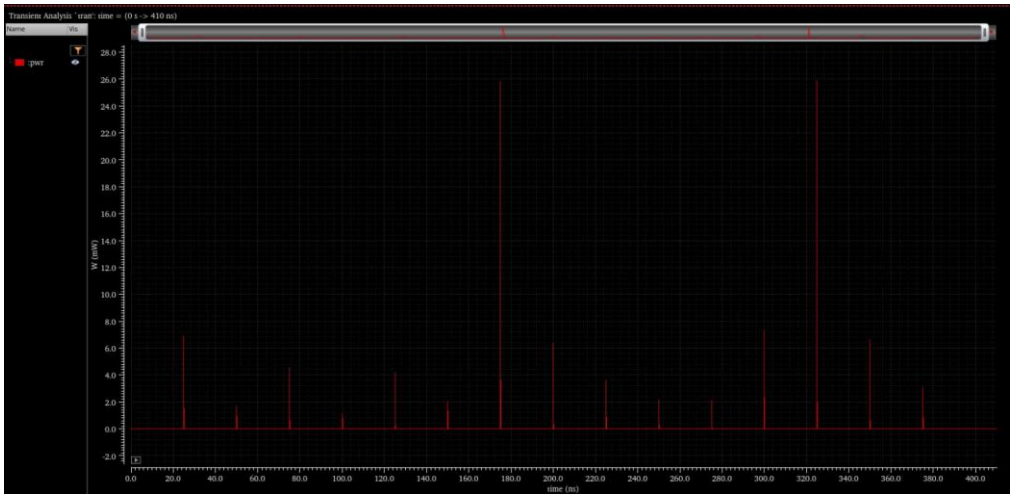
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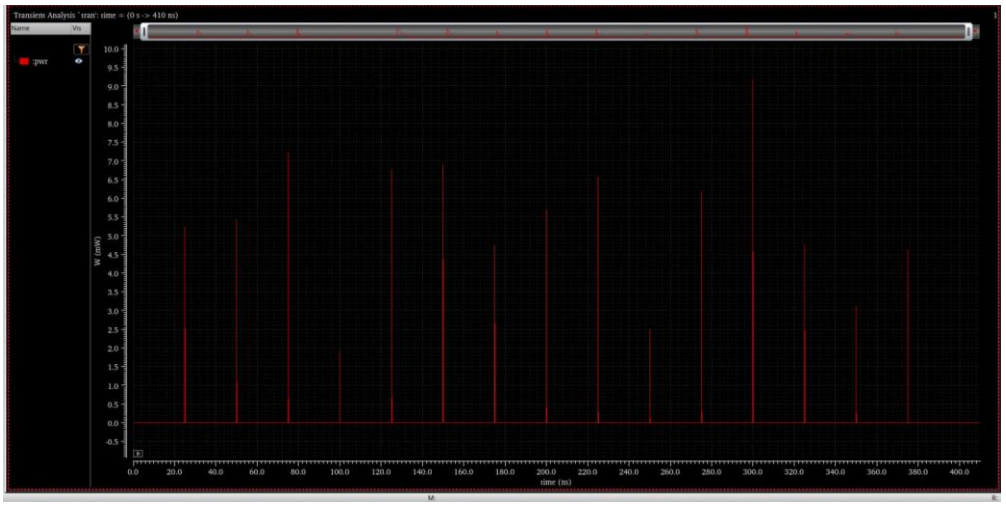
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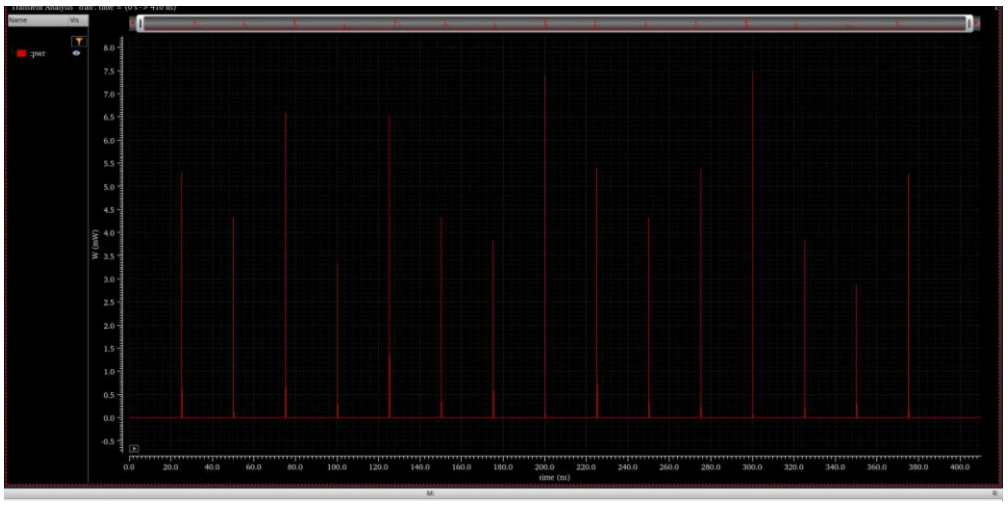
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