EE5803 - FPGA LAB
Assignment-1

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EE22RESCH01005

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Q. Reduce the following boolean expression to its simplest form using K-Map.

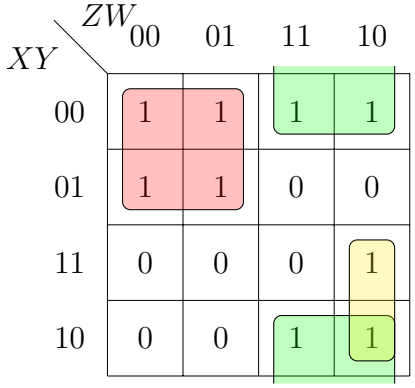
$$F(X, Y, Z, W) = \sum(0, 1, 2, 3, 4, 5, 10, 11, 14) \tag{1}$$

Sol. First we will build a Truth Table for the given expression as below,

X	Y	Z	W	**F**
0	0	0	0	**1**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**1**
0	1	0	0	**1**
0	1	0	1	**1**
0	1	1	0	**0**
0	1	1	1	**0**
1	0	0	0	**0**
1	0	0	1	**0**
1	0	1	0	**1**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**0**
1	1	1	0	**1**
1	1	1	1	**0**

Table 1: Truth Table

We can express the same boolean expression in K-Map as follows



The implicants in 0,1,4,5 gives us $\bar{X}\bar{Z}$
The implicatns in 2,3,10,11 gives us $\bar{Y}Z$
The implicants in 10,14 gives us $XZ\bar{W}$

Combining all the above terms will give us

$$F(X,Y,Z,W) = \bar{X}\bar{Z} + \bar{Y}Z + XZ\bar{W} \tag{2}$$

In order to implement it using NAND gates, we will write the above SOP form as below

$$F(X,Y,Z,W) = \overline{(\bar{X}\bar{Z} + \bar{Y}Z + XZ\bar{W})} \tag{3}$$

$$F(X,Y,Z,W) = \overline{(\bar{X}\bar{Z}.\overline{\bar{Y}Z}.\overline{XZ\bar{W}})} \tag{4}$$

The corresponding circuit diagram with only NAND gates can be drawn as follows.

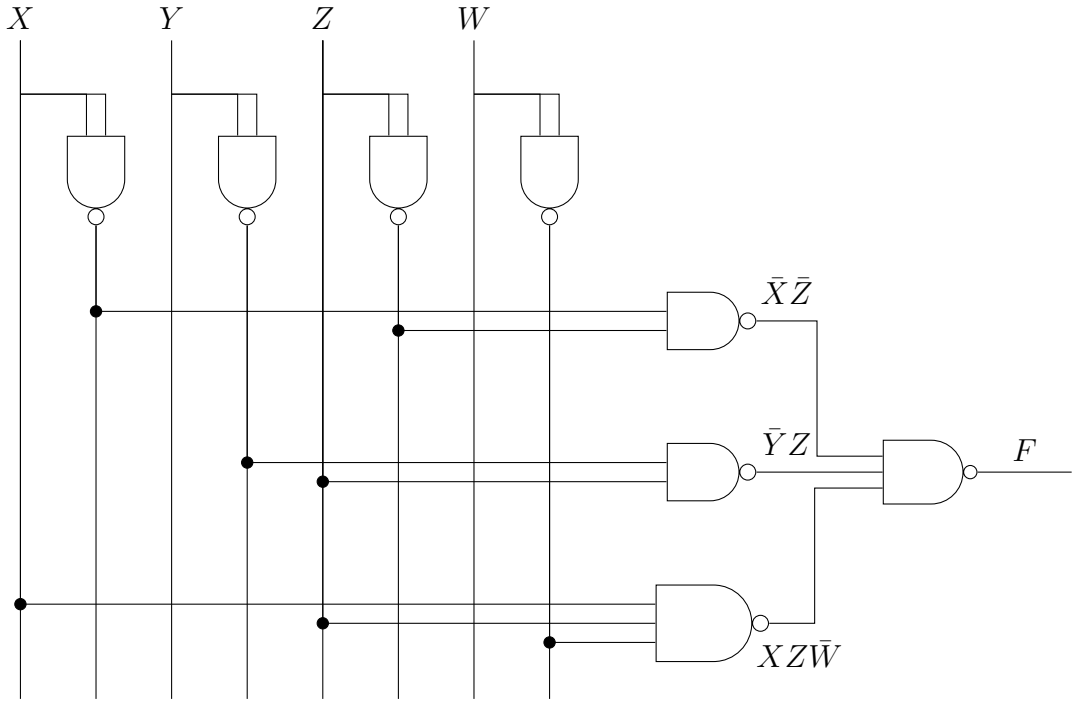


Figure 1: Circuit Diagram using NAND gates

The above logic circuit is realized using a C-program and the corresponding code is available at *./assignment_1.c*