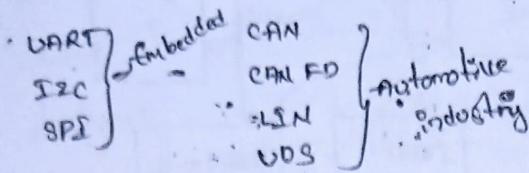


I<sub>2</sub>C

I<sub>2</sub>C → Inter-Integrate circuit

→ widely used in these protocols  
in the companies



\* Protocol: - It is not a hardware & software

\* It is a set of Ad rules.

→ I<sub>2</sub>C protocol: - Means the set of Ad rules to the circuit writing the programming.

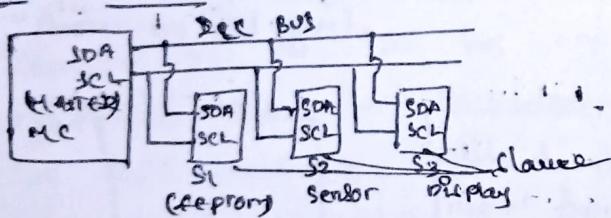
→ I<sub>2</sub>C devices: sensors, LCD display

\* Multi slave communication is not possible in the VART protocol.

\* To over-come that I<sub>2</sub>C is designed

\* It is a two-wire communication (SDA, SCL).

\* we can communicate multiple device through the multiple slave in the I<sub>2</sub>C protocol.



→ Master can communicate with slaves  
at at a same time, it communicate with one by one

→ Advantage of I<sub>2</sub>C:

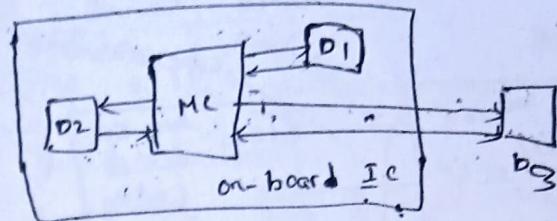
→ By these two wires we can communicate many devices one by one.

→ Power consumption is more while connecting parallel (more devices)

→ we need pull-up register in I<sub>2</sub>C protocol to match input vfg of the devices

Introduction of I<sub>2</sub>C

→ It was designed by Philips  
(NXP) level for on-board IC communication (or) short distance communication.



→ while MC is communicating with D1 & D2, it is called on-board IC communication.

→ in case MC is communicating with D3, it is called off-board IC communication.

→ off-board IC communication.

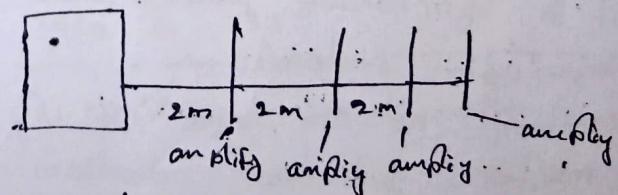
It is also possible using I<sub>2</sub>C protocol with a small distance (less meters).

→ I<sub>2</sub>C RS 232 cable is used for longer distance.

\*\*\* How to send data for a longer distance using I<sub>2</sub>C protocol?

→ I<sub>2</sub>C protocol is designed only for short communication,  
by using repeaters we can communication for longer distance.

Repeater is a amplifier



(amplify = Repeater)

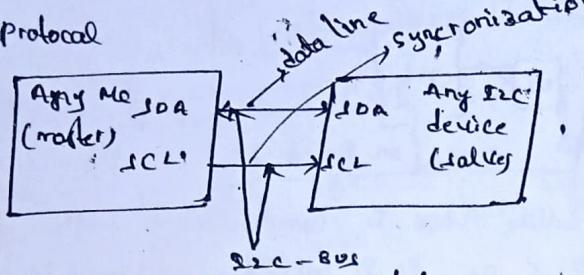
\* for longer distance communication we can use VART, CAN, CAN FD

- Features of I2C Protocol
- Hardware Setup → I2C-fields

- Data frames of I2C

### FEATURES

- It is two-wired Comm. Protocol



- Master is modulator,
- It will control the device

\* only master can generate the clk pulse pulses

\* I2C is also called as data line  
we can read & write the data  
from the slave.

\* CLK line is used for synchronization  
then, when we send the data,  
when we get the data it will  
control.

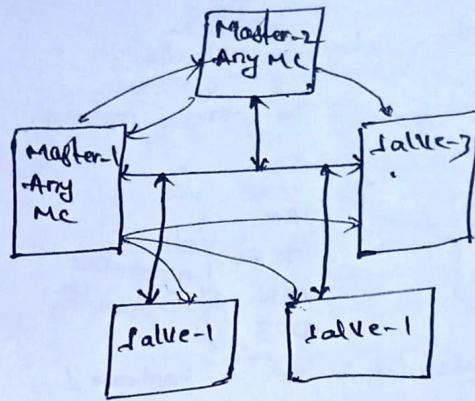
→ CLK pulse speed set by the  
master

→ synchronization is controlled by  
the CLK pulse.

### I2C is half-duplex

3. I2C is differential protocol serial  
communication protocol  
(common CLK line used in  
master & slaves)

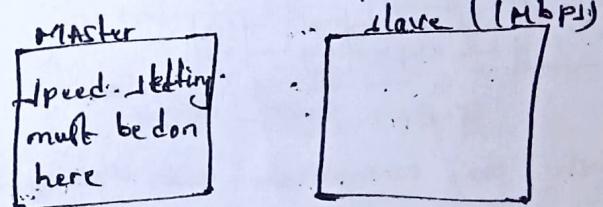
4. I2C is multi-master &  
master communication protocol;



→ One Master can communicate  
with all slaves &  
one master can communicate  
with another master also it  
is called multi-slave & multi  
master communication

Note:- Slave communicate at  
a time, one by one  
communicate.

5. Speed of I2C is upto 5Mbps  
(Mega bits per second)



→ we can set communication  
speed = 1Mbps

upto 100Kbps :- standard speed mode

upto 400Kbps :- fast speed mode (FMS)

upto 1Mbps :- FMT

upto 3.4Mbps :- high speed mode (HS)

upto 5Mbps :- ultra, high speed mode  
(UHS)

\* later only master can do  
these settings

to every slot

⑥ Every slave of I<sub>2</sub>C protocol carries with predefined address which is given by the designer.

size of address is 7 bits (01)

10 bits ( $2^7 + 2^1$ )

\* Every I<sub>2</sub>C devices comes with its own address (0x53)

### → IPv6 Versions

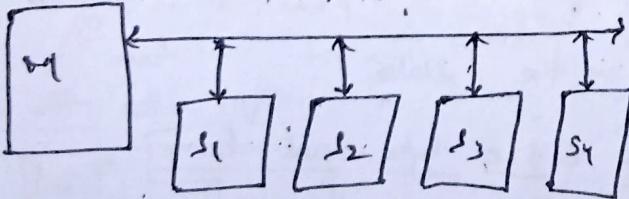
→ We can give every elements on earth including human, they gives IP addresses

→ IoT → Internet of things

→ Now Companies are using IoT Internet of Everything

⑦ The Max no. of slaves that are connected on the I<sub>2</sub>C bus are restricted by the slave address (or device address).

Note: Slave address is also called device address



\* We can connect multiple slaves but restricted.

\* We can't connect same type of slave to slave bus, it will be corrupted the data

→ How to connect two slaves with the same address?

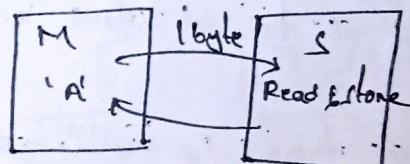
\* We can connect two same slaves with the same address through the I<sub>2</sub>C multiplexer.

⑧ It is an acknowledgement based protocol

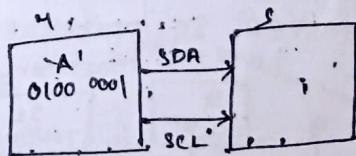
\* In the I<sub>2</sub>C protocol, master will get acknowledgement after every 8 bits written into slave.

\* Acknowledgment represents the data has been received successfully (reply)

\* After writing 1 byte of data slave will give acknowledgement to master.



⑨ Data transfer direction is from MSB to LSB.



→ Byte by byte transmitted from MSB to LSB.

⑩ It supports multi-master arbitration mechanism.

→ What is arbitration?

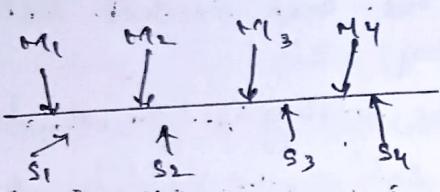
\* When 2 or more than two masters are sending a data at a same time on the bus.

10. It supports multi-master arbitration mechanism.

### What is arbitration?

When two or more than two masters are sending a data at the same time on the bus, it will clash the data & data gets corrupted.

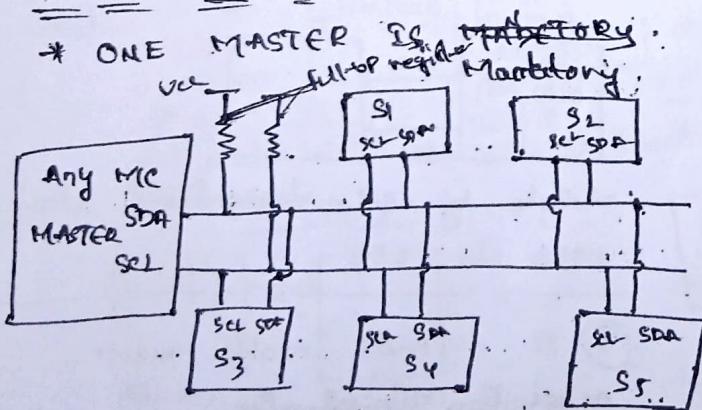
To avoid this data corruption the mechanism used in the multi-master communication protocol is called as arbitration.



→ winner will decide by the parity of the sel. slave address.

Note:- where there is multi-master communication there is arbitration

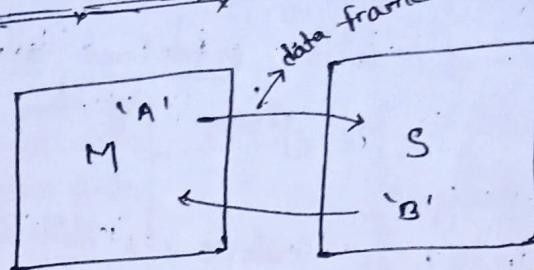
### I2C - Hardware Setup



→ full-up registers are used to adjust address & utg's of the slaves.

→ Master utg's are different & slave utg's also diff.

### I2C Data frames



→ Master wants to write data into slave, in I2C-protocol master can not write data into the frame.

→ for writing a data, master creates the write data frame, if we read the data, master creates the read data frame.

→ stop & start conditions are available not stop & start point.

→ I2C-protocol data frame, P.

bigger as compare to UART

they are two types of frames

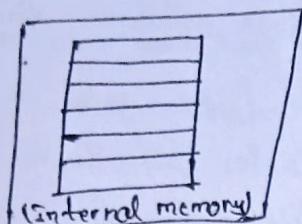
#### 1. I2C byte write frame:

This frame is used by the master to write 1 byte of data into a particular address of the slave.

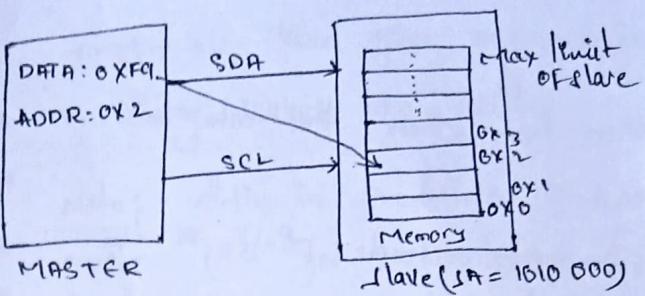
#### 2. I2C byte read frame:

This frame is used by the master to read 1 byte of data from the particular address of the slave.

## understanding slave address & Memory addresses of the slave/I<sub>2</sub>C device

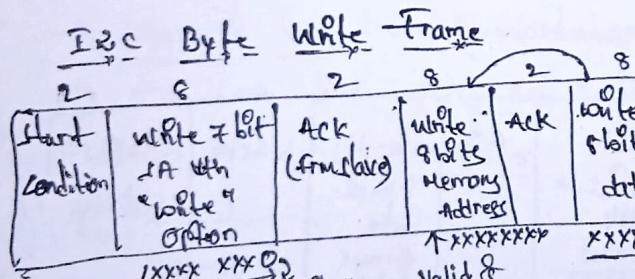
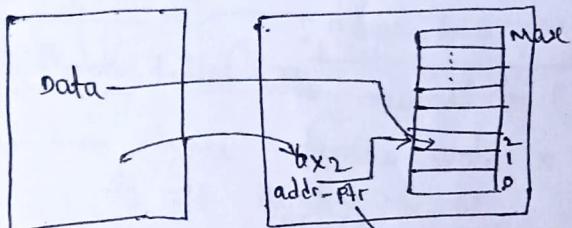


Any I<sub>2</sub>C device (I<sub>2</sub>C slave)



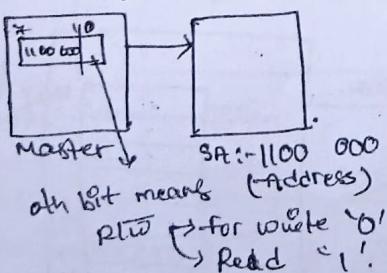
start	0xA0	ACK	0x2	ACK	0xF9	ACK	stop
-------	------	-----	-----	-----	------	-----	------

- \* Every I<sub>2</sub>C device has unique slave address → slave address is the name of the slave.
- Memory Address is true where data to be stored at a particular location
- \* Every I<sub>2</sub>C device comes with internal memory (volatile/non-volatile)
- Volatile means changes.
- \* Every I<sub>2</sub>C has
- \* size of the internal memory changes from devices to devices



start  $\rightarrow 1010\ 000\ 0 \rightarrow A \rightarrow Mr.\ Add \rightarrow A \rightarrow$  stop  $\leftarrow A \leftarrow$  data

- \* SA with write option:-



→ size of the frame is 34

Notes:- If the master is generating start condition: master should slave address with read/write option

- \* If master is given write operation then master after ACK, MR-address
- \* If master is read operation then after ACK, they can't write MR-address

hard → 1010 0001 → A → read\_data  
↑  
Read

I<sub>2</sub>C Fields in the I<sub>2</sub>C Data Frames

where from where the data to  
read ?

ans - where addrlr pointing at the  
location. now.

we want read-data from the  
particular location how?

\* 89c stand

\* D2c stop

# 22c white

at 120 read

\* DLC Aek.

8 Dec. NOOK.

The diagram illustrates the memory access sequence:

- Address:**  $1010\ 0000 \rightarrow A \rightarrow MA \rightarrow A \rightarrow \text{START} \rightarrow 1010\ 0001$
- Pointer:**  $\omega$  (with an arrow pointing to the first  $A$ )
- Data:**  $0x6$  (with an arrow pointing to the second  $A$ )
- Read Data:**  $\text{read\_data}$  (with an arrow pointing to the third  $A$ )
- Stop:**  $\leftarrow NA \leftarrow \text{read\_data} \leftarrow A \leftarrow R$  (with an arrow pointing to the fourth  $A$ )

→ why start again?

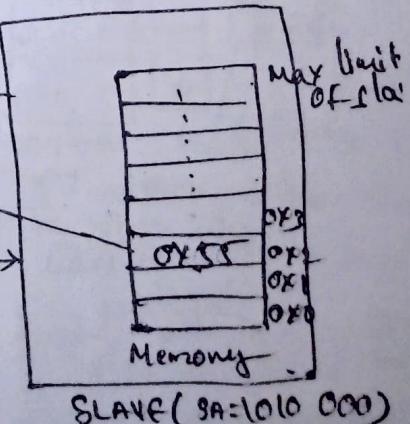
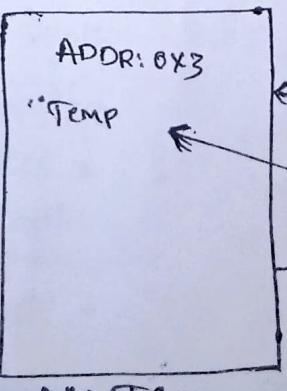
$\Rightarrow$  Because after start there will  
a slave address.

I2C      Byte Read Frame (Random read frame)

The diagram illustrates the timing sequence for a memory write operation. It shows two bus cycles: S → M and M → S.

- S → M Cycle:**
  - Phase 1: Address and control signals (Write, Write strobe, Write enable) are sent from Slave to Master.
  - Phase 2: Data is written to the Slave's memory.
  - Phase 3: An ACK signal is sent from Slave to Master.
- M → S Cycle:**
  - Phase 1: Address and control signals (Read, Read strobe, Read enable) are sent from Master to Slave.
  - Phase 2: The Slave performs a read operation.
  - Phase 3: Data is read from the Slave's memory.
  - Phase 4: An ACK signal is sent from Slave to Master.

to capture from  
which master wants  
to read data



\* Understanding I<sup>2</sup>C Fields

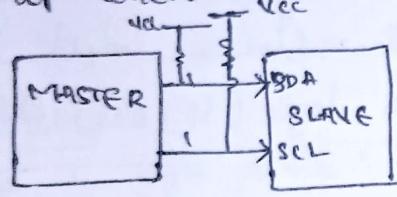
\* Implementation of I<sup>2</sup>C protocol using Bit Banging Method

\* Idle condition of the I<sup>2</sup>C bus

\* When Master & slave not communicating what should be the level of SDA & SCL?

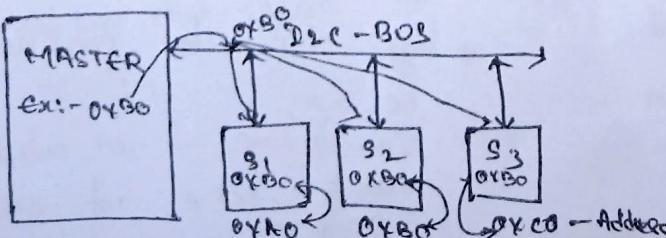
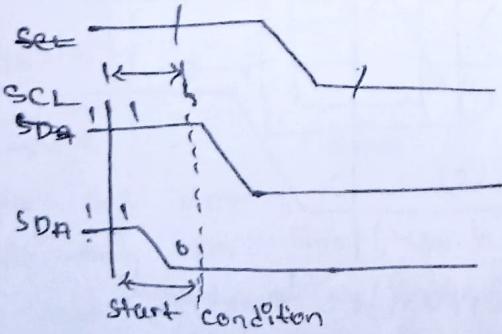
→ Idle Condition of the I<sup>2</sup>C bus representing with '1' (high volt)

→ A bus considered idle if both SDA & scl lines are high after a stop condition.



I<sup>2</sup>C start Condition

A high to low transition (change) on the SDA line while scl is high defines a start condition.



Q1 :- Suppose if slave is not present what would happen?  
Ans :- No slave give acknowledgement remaining slaves are waiting

Notes - Within predefined time master will get acknowledgement from slave (3.4ms)  $\rightarrow$  100kbpss

For 3.4ms master understand no such a slave is not present.

\* When stop condition occurs the became to the Idle-condition (I<sup>2</sup>C-bus).

\* It can't possible to send two to a slave address at a time

Protocol implementation methods

→ Two types

- i) Bit Banging method
- ii) Peripheral method

(i) Bit Banging method

Software method of protocol implementation. Here master has to generate clock pulses using software & it has to send and receive each bit using software only.

(ii) Peripheral method

Hardware method of implementing protocol. In the master of I<sup>2</sup>C controller is available then the peripheral method can be used to implement protocol.

I<sup>2</sup>C controller :- dedicated hardware used for I<sup>2</sup>C communication

→ This I<sub>2</sub>C Controller will take care of generating clock pulses & sending & receiving of data bits serially.

Program for start condition

1. I<sub>2</sub>C-fields.c + /

#include <reg51.h>

#include <header.h>

sbit SDA = P2^0; } up-on reset  
sbit SCL = P2^1; } pull pins are high

void i<sub>2</sub>c\_start(void)

{

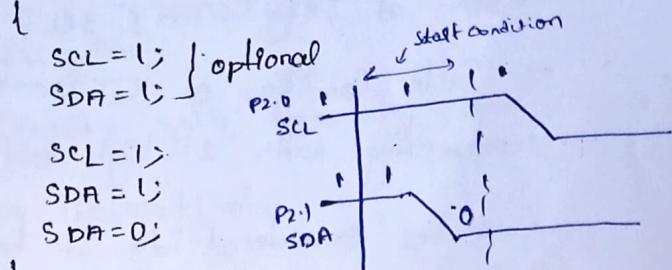
SCL = 1; } optional

SDA = 1;

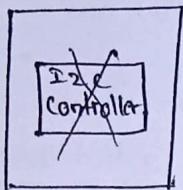
SCL = 1;

SDA = 1;

SDA = 0;

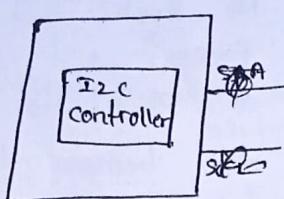


e.g.-any version of 8051



Bit-Banging method

e.g.: LPC2148/LPC2129



Peripheral method/  
bit-banging method

Note:- In bit-banging method

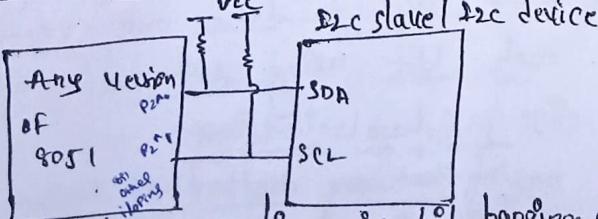
for multi-master we must  
written a logic (if (SCL=1 & SDA=1))

Note:- suppose in peripheral method  
in-built I<sub>2</sub>C controller they  
fixed pin numbers available for  
SDA & SCL.



e.g.: -LPC2148/LPC2129

Bit Banging Method

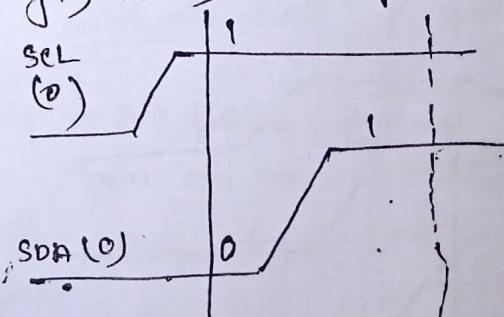


H/W connections in bit-banging Method

Note:- In the bit-banging method

to interface I<sub>2</sub>C device we can  
use any two IO pins

I<sub>2</sub>C Stop Condition (change)  
\* A low to high transition  
on the SDA line while set to  
high, defines a stop condition.



(Opposite to start)

\* logic for stop condition

SCL = 0;

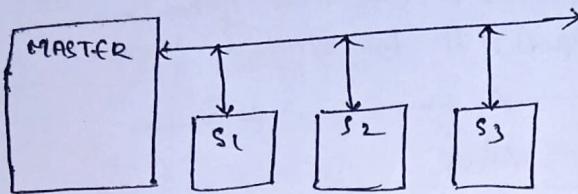
SDA = 0;

SCL = 1;

SDA = 1;

```
void i2c_stop(void)
```

```
{  
    SCL = 0;  
    SDA = 0;  
    SCL = 1;  
    SDA = 1;  
}
```



$S / SDA + W / A / M7\_add / A / natal / A / P \rightarrow$  stop condition

Start condition

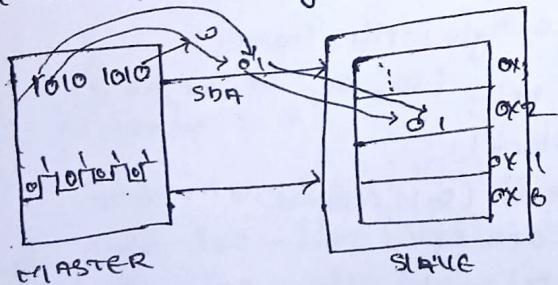
→ Bus becomes free while bus becomes  
Idle condition i.e., stop condition

————— x ————— x —————

I2C - write  
\* How to write 8-bits into Slave?

It may be 8 address, memory address  
8 bits data.

Note:- Master can write 1bit using  
1 clock pulse only.



→ When SCL becomes '1' then read  
1 bit from SDA line (MSB to LSB)

For next bit read we must clear  
SCL '0' and read again thru through

the SCL '1'.

→ Master has to generate '8' clock  
pulses for 8 bit data.

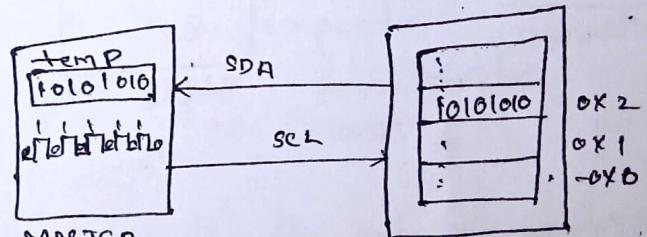
```
void i2c_write(ug d)  
{  
    S8,  $\frac{d}{8}$  → signed variable  
    for ( $i = 7; i >= 0; i--$ )  
    {  
        SCL = 0;  
        SDA =  $(d \gg i) \& 1$ ; // result '0' or '1'  
        SCL = 1;  
    }  
}
```

} (BPL by 8bit writing in slave)  
————— x ————— x —————  
I2C - Read  
(Reading 8bits from the slave)

```
ug i2c_read(ug)
```

```
{  
    ug temp = 0x0;  
    S8,  $\frac{d}{8}$   
    for ( $i = 7; i >= 0; i--$ )  
    {
```

```
        SCL = 1;  
        if (SDA == 1)  
            temp |=  $1 \ll i$ ;  
        SCL = 0;  
    }  
    return temp;  
}
```



(7bit to 8th position in slave)

Note:- Master can read 1 data bit

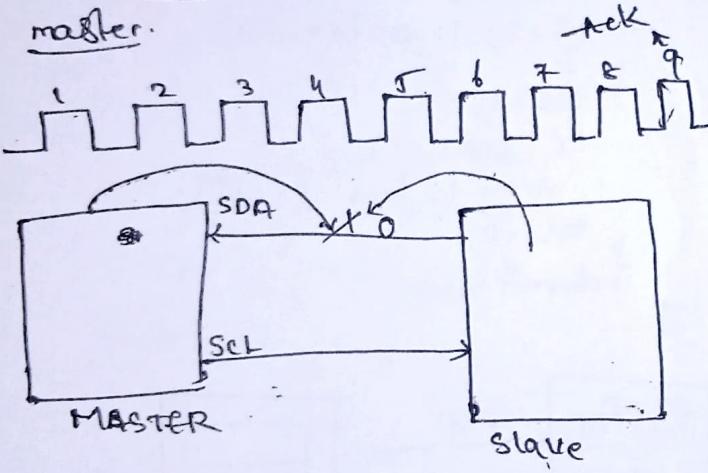
from slave using 1 clock pulse  
only

\* for setting 7th bit at the msb  
location we want to check  
SDA line status ( $SDA == 0$ )

Note :- Peripheral method is mostly preferred because  
it less burden to CPU also

## I2C-Ack

- Suppose slave have not given Ack, then set automatically master generator stop condition.  
(Display the error message)
- \* In the I2C protocol, master gets acknowledgement after every 8 bits written onto the slave.
- \* Every 9th clock pulse is reserved for acknowledgement.
- \* By writing 0(zero) on the SDA line slave will acknowledge to master.



bit i2c\_ack(void)

```
{
    SCL=0;
    SDA=1; // master write 1 to SDA line
    SCL=1; // 9th clock pulse
    SCL=0; // 3.4ms delay function
    if (SDA==0) // master needs get
    { SCL=0; // ack from the slave
        return 0; // got the ack
    }
    else { SCL=0; // error to stop
        return 1; // error to stop condition
    }
}
```

#include <iostream.h>  
Pre defined func -nop-( )  
Macro

It gives 1ms delay.

-nop-( ); // 1ms time }  
-nop-( ); // 1ms time } 3.4ms delay  
-nop-( ); // 1ms time } Approx  
-nop-( ); // 1ms time } 4ms

## I2C-NACK

- NACK gives master to slave.
- At it is only read mode.

void i2c\_nack(void){

```
{
    SCL=0;
    SDA=1;
    SCL=1;
```

## i2c\_frame.c

/\* i2c\_frame.c \*/

#include "header.h"

void i2c\_byte\_write\_frame

(us, sa, us mr, us d)

```
{
    bit ret;
    i2c_start();
    i2c_write(sa); //SA+10
    ret=i2c_ack();
    if (ret==1)
        goto out;
    i2c_write(sr);
    ret=i2c_ack();
    if (ret==1)
        goto out;
    i2c_write(d);
    ret=i2c_ack();
    if (ret==1)
        goto out;
    out: i2c_stop();
}
```

```

u8 i2c_byte_read_frame(u8 sa, u8 mr)
{
    u8 temp; bit ret;
    i2c_start();
    i2c_write(sa); //SA+R
    ret = i2c_ack();
    if (ret == 1)
        goto out;
}

```

```

i2c_write(mr)
ret = i2c_ack(); }
if (ret == 1) } for ACK decking
    goto out;
}

```

```

i2c_start(); //retransmit condition
i2c_write(~sa | 1); //SA+R
ret = i2c_ack();
if (ret == 1)
    goto out;
}

```

```

temp = i2c_temp,
temp = i2c_read();
i2c_nack(); //
}

```

```

out: i2c_stop();
return temp;
}

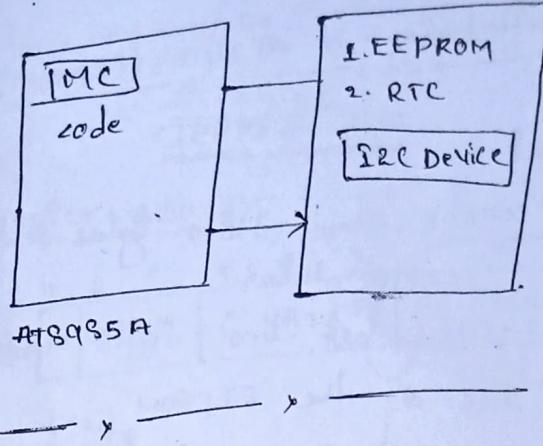
```

```
#include <i2c.h>
```

```

void i2c_start(void);
void i2c_stop(void);
void i2c_write(u8 d);
u8 i2c_read(u8 id);
bit i2c_ack(void);
void i2c_nack(void);
void i2c_byte_write_frame(u8 sa,
                         u8 mr, u8 d);
u8 i2c_byte_read_frame(u8 sa, u8 mr);
}

```



Interfacing of EEPROM with AT89S51 / W78E052D (Nuvoton 8051)

List of I2C Devices

- \* EEPROM (AT24C08 / AT24C04)
- \* RTC (DS1307 / DS3231)
- \* Digital thermometer (DS1621)
- \* OLED display
- \* Accelerometer
- \* Pressure sensor
- \* Temperature Sensor
- \* Paul expander
- \* Digital potentiometer
- \* ADC (ADS1115)
- etc.

→ for testing the code we must connect to the I2C device

## Interfacing of AT24C08 (EEPROM)

Atmel With AT89S52

AT24C08: Atmel 1Kilo Bytes of EEPROM  
→ EEPROM device

- AT24C08: - last two digits represent the size of the EEPROM
- 8 represents 8k bits ( $8 \times 1024$  bits)
- 8 means that  $\frac{8192}{8}$  (1Kilo Bytes)
- 8KB → Kilo bytes
- 8kb → Kilo bytes

AT24C04: - 4Kilo Bits (4096 bits)

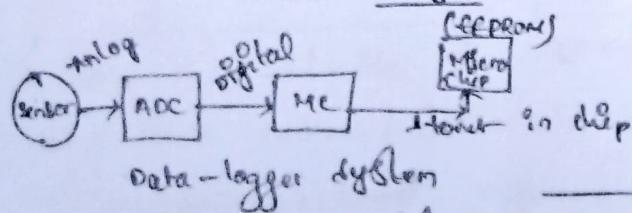
$\frac{4096}{8} \rightarrow 512$  Bytes  
→ What is EEPROM?  
Ans: - EEPROM is permanent R/W data memory.

(Electrically erasable programmable ROM)

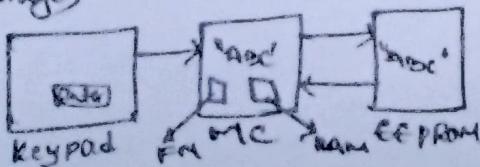
Volatile → RAM (Temporary memory)

Non-volatile → Hard Disk (Permanent Memory)

- Why EEPROM? ⇒ used in the
- 1. \* Data logger system (DLS)  
Ex: Black box system in planes
- It will stores all the informations of heading of sensors that is called logger



2. \* Security based system (password storage)



3. \* Electric Meters also to store little bit to inform

## Introduction to AT24C08

Supply =  $-5.0$  ( $V_{CC} = 4.5$  to  $5.5$  V)

=  $-2.7$  ( $V_{CC} = 2.7$  to  $5.5$  V)

→ Two-wire interface

- \* Schmitt trigger, filtered inputs for noise suppression.
- \* Bi-directional data transfer protocol

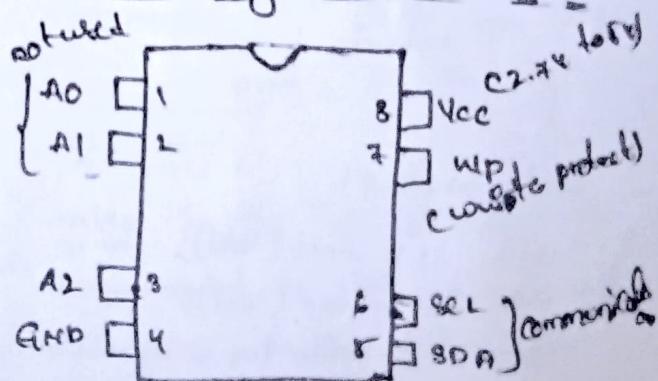
\* 100kHz (2.7V and)  
400kHz (5V compatibility)

\* High-reliability

Endurance: 1M  $\times 10^9$  a write cycles.

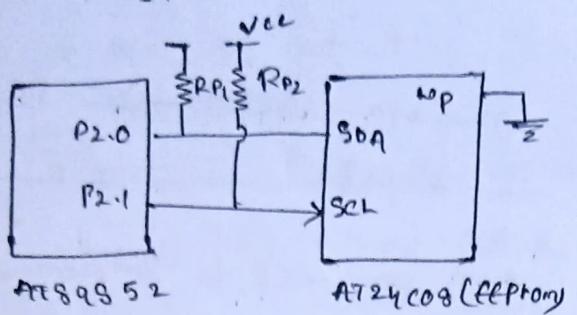
data Retention: 100 years

## Pin-diagram of EEPROM



\* MC reads from the EEPROM & compare with Scanner if scanned password be match password which is stored in the EEPROM.

## Interfacing of EEPROM to MC

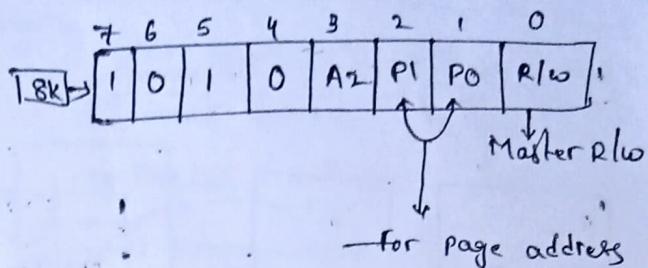


\* Pull-up registers are required

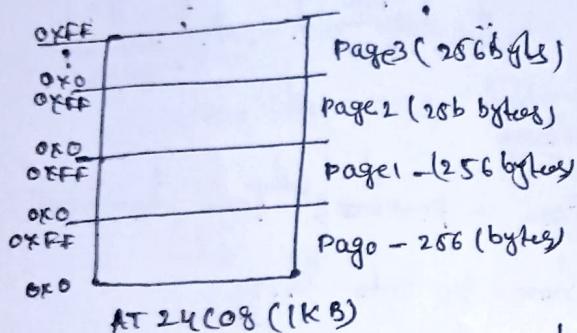
Slave Address / Device Address of

AT&T CO8

\* \*  
Device address:



## Memory Mapping of EEPROM



\* There are four pages in the

\* Every page starts with 0x0  
\* ends with 0xFF

- \* Page Section can be done using program.

$S \rightarrow SA + U \rightarrow A \xrightarrow{mr} \downarrow$   
 $8\text{ bits} - 1\text{ byte}$

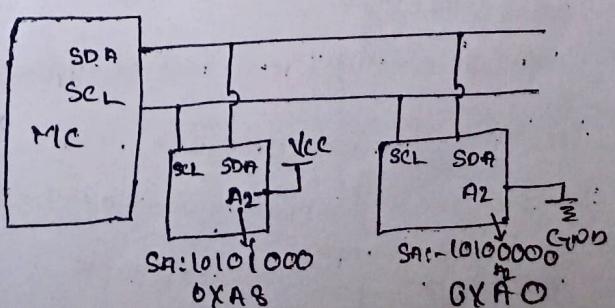
\* How to read / write from EEPROM?

~~one~~ slave address / device address

of  $MgCO_3$  must be refined.

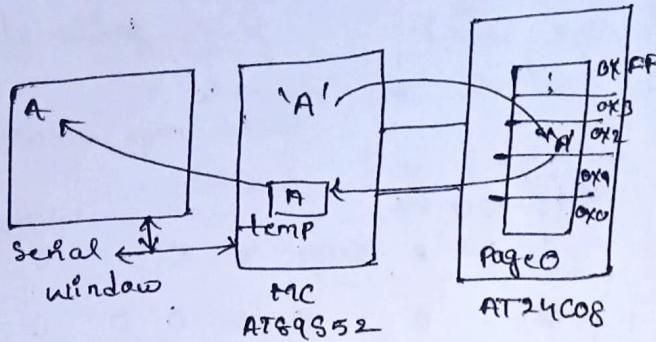
This pin is used to change device address of EEPROM (AT 24C08), so that one can connect two EEPROM's on the same I<sup>2</sup>C bus.

Note:- In the IEEE protocol, it is recommended to not connect same addressable device on the same bus.



\* Through the AT24C04 we can use 4 EEPROMs, there is A1 & A2 pins available.

### AT24C08 EEPROM Programming



- \* Taking 1 byte of data writing into EEPROM (one of the address locations)
- \* And read back data in a temp and display on Serial window

### loop back test

It is used for checking the device status i.e. it is working properly.

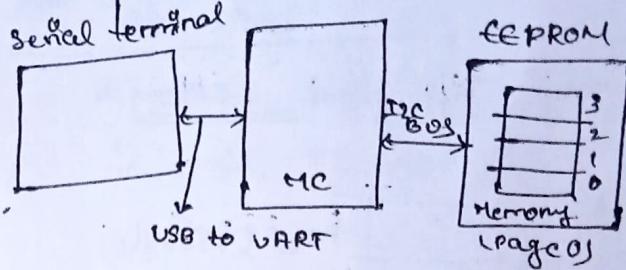
### MP4C08

```
/* main-ecrom.c */
#include "header.h"

main() {
    us temp;
    vart - Init(9600);
    vart - tx - string("printing EEPROM");
    * I2C - byte - write - frame(0xA0, 0x8, 'A');
    temp = I2C - byte - read - frame(0xA0, 0x8);
    vart - tx (temp);
    while (1); // lookback.
}
```

PC → MC → EEPROM → NC - PC

\* \* \*  
\* w/ an ECP, to implement password authentication program using UART & EEPROM.



### Procedure

1. Scan a password from terminal & store in into array.
2. Read password from EEPROM & compare it with scanned password.
3. Display result on Serial terminal & repeat.

### I2C Multiplexer

Allow you to connect same type of I2C devices (same addressable devices) on the same bus.

extension & program to read data in runtime

while (1)

{ vart - tx - string("In character to write in EEPROM: ");

ch = vart - rx();

vart - tx(ch); // loop back

↓ i.e. vart - tx (frame(0xA0, 0x3, ch));

## RTC - Real-time Clock

\* RTC will not sleep (or) not shutdown

\* RTC will continuously running

- through the CMOS Battery (Cmos Battery)

→ Why RTC?

\* through the RTC we get Current time & Current date.

\* It takes less V<sub>cc</sub> & Current.

\* Note:- RTC takes will not take the cmos battery v<sub>cc</sub> all the time, only when the system to shutdown the PC.

→ Power-failure detect & switch circuitry is available in the RTC

Eg:- Wheeler monitoring system

### Introduction to

### DS1307 OF RTC

Delta Semiconductor

→ It is migrated maxpm integrated

→ It is dedicated hardware.

→ 64 Bytes memory in the RTC.

### Benefits & Features

\* Completely manages All time keeping functions (Real-time clock counter, days, minutes, hours, weekdays, months, years)

(i) 56-Byte, Battery-Backed, general purpose ram with unlimited writes

(ii) programmable square-wave output signal

\* Simple serial port interface to most Microcontrollers

(i) I<sup>2</sup>C Serial Interface

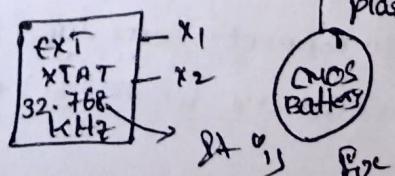
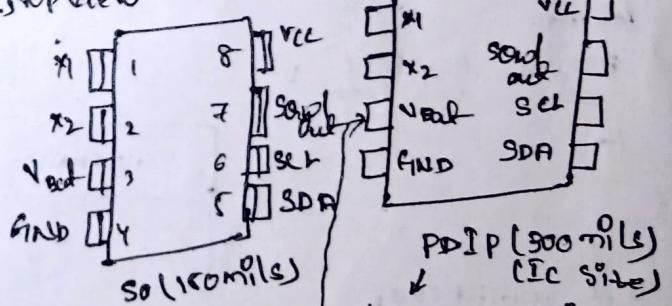
\* Low power Operation Extended Battery Backup Run time.

(ii) less than 500nA (Consumes) & backup mode

(iii) Automatic power-fail detect and switch

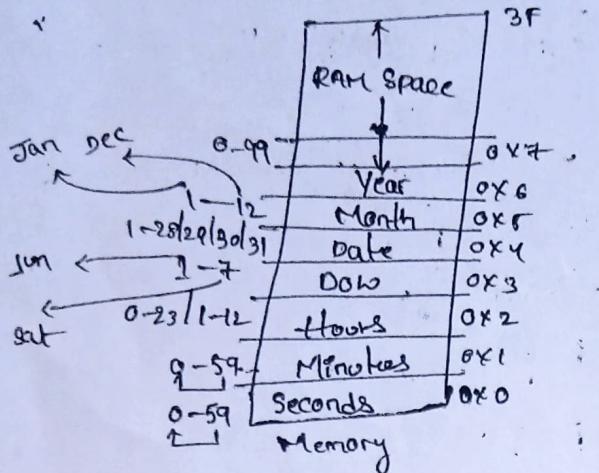
### PIN Configuration

TOP view



\* memory size inside the RTC is 64 Bytes (0-63) memory locations (all) address are available.

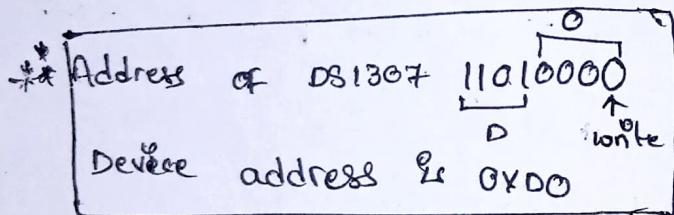
## Memory Mapping of DS1307



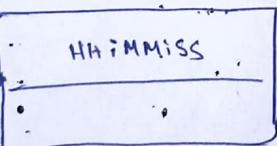
\* Data is safe in the RAM space

\* Will when Memory is dead the data will lose.

\* Only once to set the setting.



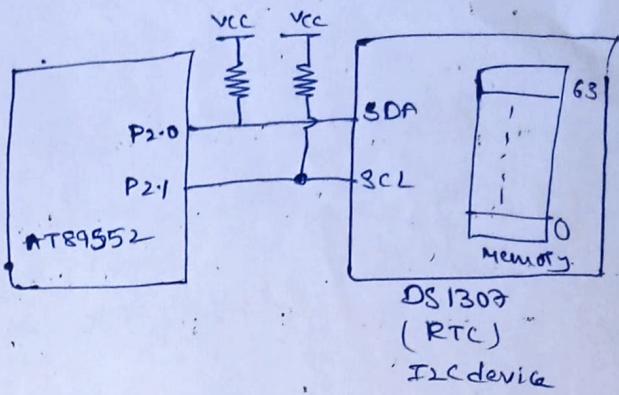
## Program on RTC



## I2C multiplexer

→ allow you to connect same type of I2C devices (same addressable I2C devices) on the same bus.

## Interfacing of RTC with AT89S52 / W78E052D



/\* main - rtc.c \*/

#include "header.h"

main()

{ us, hms;

Lcd\_init();

→ // setting RTC time to 11:59:0PM //

i2c\_byte\_write\_frame(0x00, 0x23);  
// setting hour

i2c\_byte\_write\_frame(0x00, 0x1, 0x59);  
// setting min

i2c\_byte\_write\_frame(0x00, 0x0, 0x50);  
Lcd\_Cmd(0x80); // disable cursor // setting second

→ // Read RTC time & Print it on a LCD //

while(1)

{ h=i2c\_byte\_read\_frame(0x00, 0x8); // read m=i2c\_byte\_read\_frame(0x00, 0x1); // read s=i2c\_byte\_read\_frame(0x00, 0x0); // read

Lcd\_Cmd(0x80);

Lcd\_Data(h/16+48);

Lcd\_Data(h%16+48);

Lcd\_Data(':'');

Lcd\_Data(m/16+48);

Lcd\_Data(m%16+48);

Lcd\_Data(':');

Lcd\_Data(s/16+48);

Lcd\_Data(s%16+48);