# ABSTRACT

This project presents the design of the SPI master core. It is a commonly used communication protocol that allows serial data transfer between a master and multi-slave device over a short distance. In this project, we will focus on block-level architecture and develop RTL code for the same. This controller is developed using Verilog HDL based on the IEEE standards and also verified using Verilog HDL code. The main part of the SPI master core is to generate the serial clock which will be derived from the wishbone master clock. The SPI protocol works with Master-Slave configuration, in full duplex mode. This is a 4-wire transmission that includes “SCLK, MOSI, MISO, SS”. MOSI will transfer the bit serially from the SPI master core to the SPI slave and MISO will receive the serial bit from the SPI slave to the SPI master.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| SPI | Serial Peripheral Interface |
| RTL | Register Transfer Level |
| HDL | Hardware Description Language |
| MOSI | Master Out Slave In |
| MISO | Master In Slave Out |
| SS | Slave Select |
| SCLK | Serial Clock |